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MLX71122

300 to 930MHz FSK/FM/ASK Receiver

Datasheet

Features

- Programmable PLL synthesizer
- 8-channel preconfigured or fully programmable SPI mode
- Double super-heterodyne receiver architecture with 2nd mixer as image rejection mixer
- Reception of FSK, FM and ASK modulated signals
- Low shut-down and operating currents
- AGC – automatic gain control
- On-chip IF filter
- Fully integrated FSK/FM demodulator
- RSSI for level indication and ASK detection
- 2nd order low-pass data filter
- Positive and negative peak detectors
- Data slicer (with averaging or peak-detector adaptive threshold)
- 32-pin Quad Flat No-Lead Package (QFN)
- EVB programming software is available on Melexis web site

Ordering Information

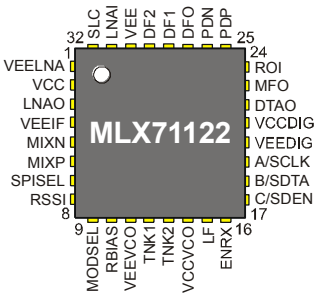
Part Number	Temperature Code	Package Code	Delivery Form
MLX71122	R (-40 °C to 105 °C)	LQ (32 L QFN 5x5 Quad)	73 pc/tube 5000 pc/T&R

Application Examples

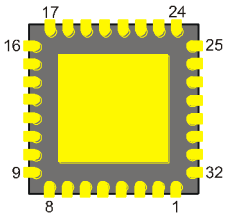
- General digital and analog RF receivers at 300 to 930MHz
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Low power telemetry systems
- Alarm and security systems
- Active RFID tags
- Remote controls
- Garage door openers
- Home and building automation

Pin Description

top



bottom



General Description

The MLX71122 is a multi-channel RF receiver IC based on a double-conversion super-heterodyne architecture. It is designed to receive FSK and ASK modulated RF signals either in 8 predefined frequency channels or frequency programmable via a 3-wire serial programming interface (SPI).
The IC is designed for a variety of applications, for example in the European bands at 433MHz and 868MHz or for the use in North America or Asia, e.g. at 315MHz, 447MHz or 915MHz.

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1. Theory of Operation

1.1. General

The MLX71122 receiver architecture is based on a double-conversion super-heterodyne approach. The two LO signals are derived from an on-chip integer-N PLL frequency synthesizer. The PLL reference frequency is derived from a crystal (XTAL). The PLL synthesizer consists of an integrated voltage-controlled oscillator with external inductor, a programmable feedback divider chain, a programmable reference divider, a phase-frequency detector with a charge pump and an external loop filter.

In the receiver's down-conversion chain, two mixers MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. The second mixer MIX2 is an image-reject mixer. As the first intermediate frequency (IF1) is very high (typically above 100 MHz), a reasonably high degree of image rejection is provided even without using an RF front-end filter. At applications asking for very high image rejections, cost-efficient RF front-end filtering can be realized by using a SAW filter in front of the LNA.

The receiver signal chain is set up by a low noise amplifier (LNA), two down-conversion mixers (MIX1 and MIX2), an on-chip IF filter (IFF) as well as an IF amplifier (IFA). By choosing the required modulation via an FSK/ASK switch (at pin MODSEL), either the on-chip FSK demodulator (FSK DEMOD) or the RSSI-based ASK detector is selected. A second order data filter (OA1) and a data slicer (OA2) follow the demodulator. The data slicer threshold can be generated from the mean-value of the data stream or by means of the positive and negative peak detectors (PKDET+/-).

In general the MLX71122 can be set to shut-down mode, where all receiver functions are completely turned off, and to several other operating modes. There are two global operating modes that are selectable via the logic level at pin SPISEL:

- 8-channel pre-configured mode (**ABC mode**)
- fully programmable mode (**SPI mode**).

In ABC mode the number of frequency channels is limited to eight but no microcontroller programming is required. In this case the three lines of the serial programming interface (SPI) are used to select one of the eight predefined frequency channels via simple 3-bit parallel programming. Pins ENRX and MODSEL are used to enable/disable the receiver and to select FSK or ASK demodulation, respectively.

SPI mode is recommended for full programming flexibility. In this case the three lines of the SPI are configured as a standard 3-wire bus (SDEN, SDTA and SCLK). This allows changing many parameters of the receiver, for example more operating modes, channels, frequency resolutions, gains, demodulation types, data slicer settings and more. The pin MODSEL has no effect in this mode.

1.2. Technical Data Overview

- Input frequency ranges: 300 to 930MHz
- Power supply range: 3.0 to 5.5V
- Temperature range: -40 to +110°C
- Shutdown current: 50nA
- Operating current: 12mA (typ.)
- FSK input sensitivity: -107dBm (typ.)
- ASK input sensitivity: -112dBm (typ.)
- Internal IF2: 2MHz with 230kHz 3dB bandwidth
- Maximum data rate: 100kbps NRZ code, 50kbps bi-phase code
- Minimum frequency resolution: 10kHz
- Total image rejection: > 65dB (with external RF front-end filter)
- FSK/FM deviation range: ±10 to ±50kHz
- Spurious emission: < -70dBm
- Linear RSSI range: > 50dB
- FSK input frequency acceptance range:
- 180kHz (3dB sensitivity loss)
- Crystal reference frequency: 10MHz

1.3. Block Diagram

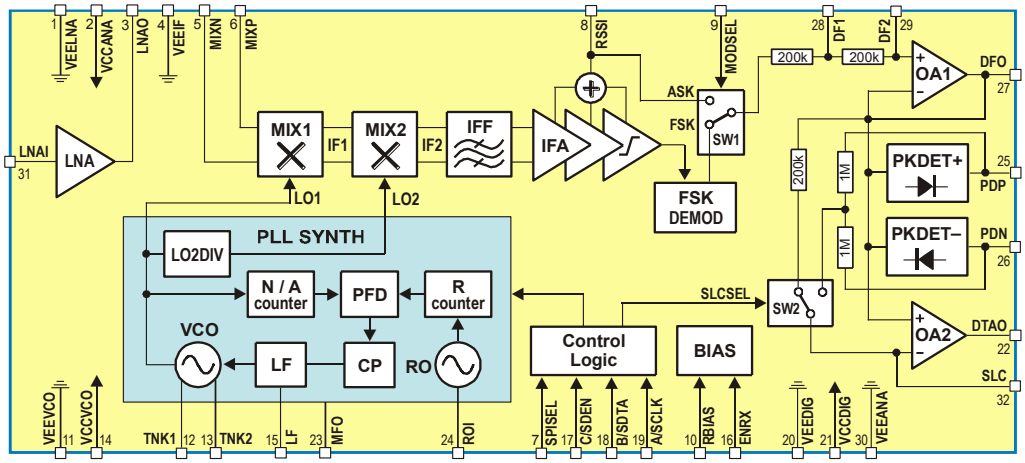


Fig. 1: MLX71122 block diagram

The MLX71122 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) to generate the first and second local oscillator signals LO1 and LO2, parts of the PLL SYNTH are the voltage-controlled oscillator (VCO), the feedback dividers N/A and R, the phase-frequency detector (PFD), the charge pump (CP) and the crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (intermediate frequency)
- Second mixer (MIX2) with image rejection for down-conversion from the first to the second IF
- IF Filter (IFF) with a 2MHz center frequency and a 230kHz 3dB bandwidth
- IF amplifier (IFA) to provide a large amount of voltage gain and an RSSI signal output
- FSK demodulator (FSK DEMOD)
- Operational amplifiers OA1 and OA2 for low-pass filtering and data slicing, respectively
- Positive (PKDET+) and negative (PKDET-) peak detectors
- Switches SW1 to select between FSK and ASK as well as SW2 to chose between averaging or peak detector data slicer
- Control logic with 3-wire bus serial programming interface (SPI)
- Biasing circuit with modes control

1.4. Enable/Disable in ABC Mode

ENRX	Description
0	Shutdown mode
1	Receive mode

Pin ENRX is pulled down internally. Device is in shutdown by default, after power supply on.
If ENRX = 0 and SPISEL = 1 then operating modes according to OPMODE bit (refer to control word R0).
If ENRX = 1 then OPMODE bit has no effect (hardwired receive mode).

1.5. Demodulation Selection in ABC Mode

MODSEL	Description
0	FSK demodulation
1	ASK demodulation

Pin MODSEL has no effect in SPI mode (SPISEL = 1). We recommend connecting it to ground to avoid a floating CMOS gate.

1.6. Programming Modes

SPISEL	Description
0	ABC mode (8 channels preconfigured)
1	SPI mode (programming via 3-wire bus)

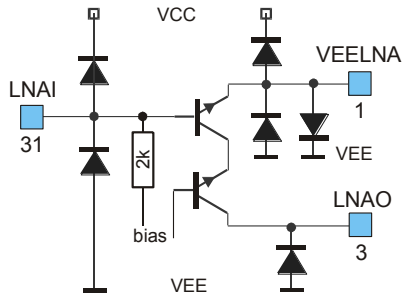
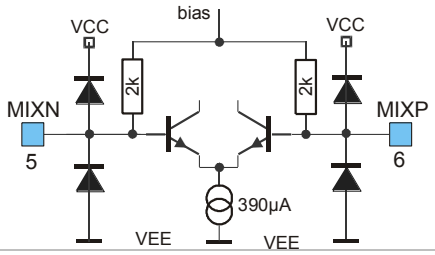
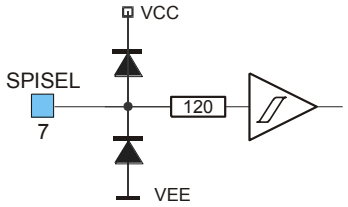
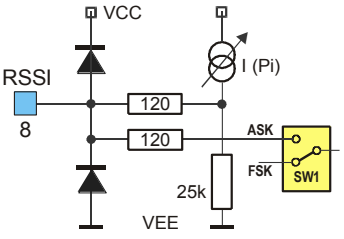
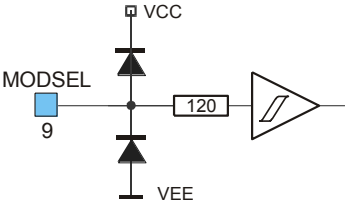
1.7. Preconfigured Frequencies in ABC Mode

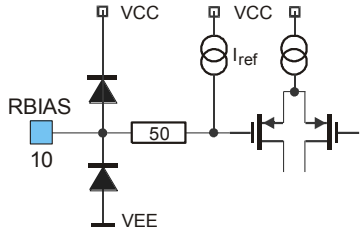
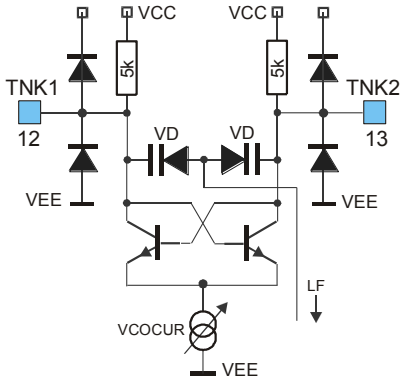
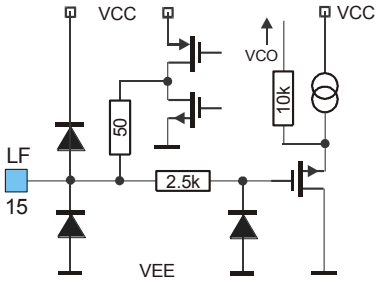
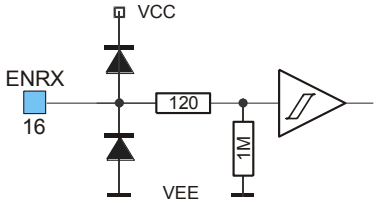
A	B	C	Receive Frequency
0	0	0	FSK1: 369.5 MHz
0	1	0	FSK5: 388.3 MHz
1	0	0	FSK2: 371.1 MHz
1	1	0	FSK4: 376.9 MHz
0	0	1	FSK3: 375.3 MHz
0	1	1	FSK7: 394.3 MHz
1	0	1	FSK6: 391.5 MHz
1	1	1	FSK8: 395.9 MHz

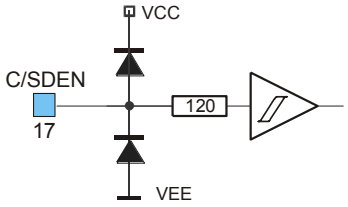
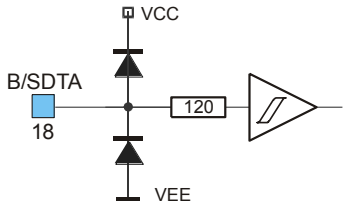
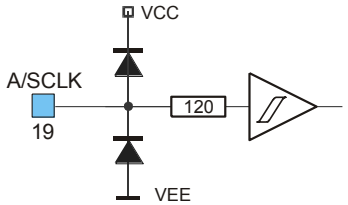
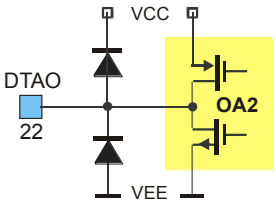
As all pins, pins A, B, and C are equipped with ESD protection diodes that are tied to VCC and to VEE. Therefore these pins should not be directly connected to positive supply (a logic “1”) before the supply voltage is applied to the IC. Otherwise the IC will be supplied through these control lines and it may enter into an unpredictable mode. In case the user wants to apply a positive supply voltage to these pins before the supply voltage is applied to the IC, a protection resistor should be inserted in each control line.

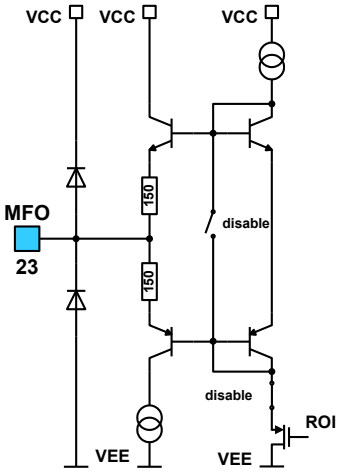
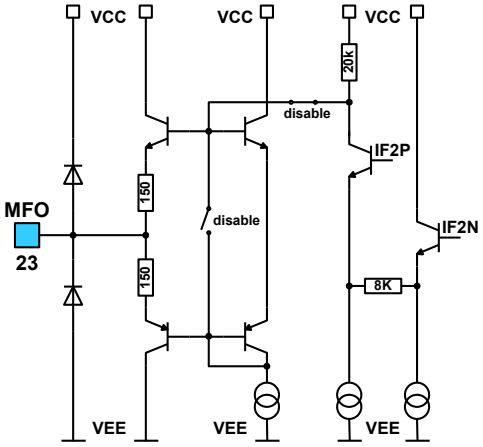
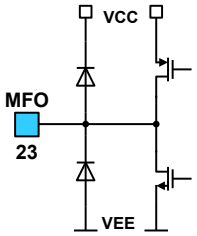
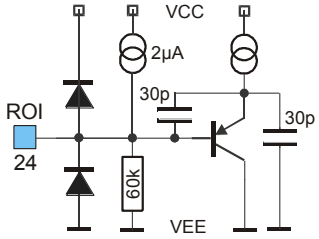
2. Pin Definitions and Descriptions

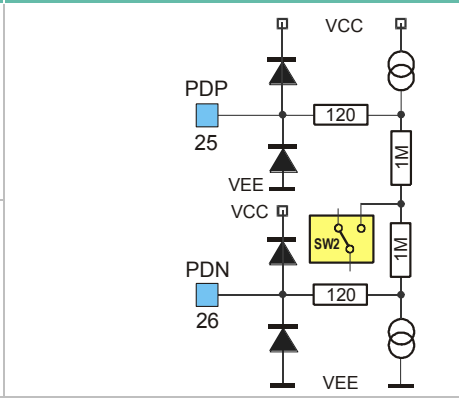
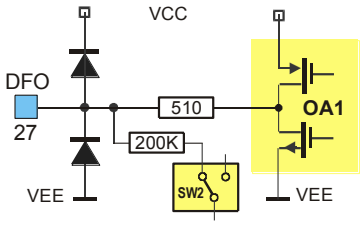
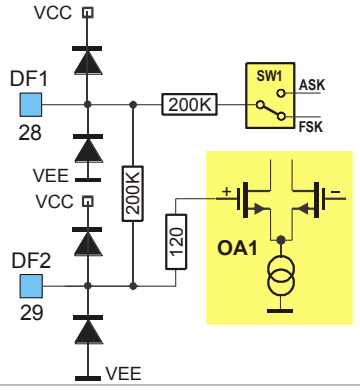
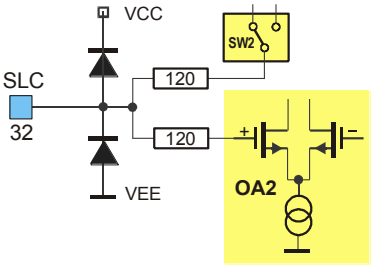
2.1. Pin Schematics

Pin No.	Name	I/O Type	Functional Schematic	Description
1	VEELNA	ground		ground of LNA core
31	LNAI	analog input		LNA input, approx. 27Ω single-ended
3	LNAO	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
2	VCCANA	supply		positive supply of LNA, MIX1 MIX2, IFF, IFA, FSK DEMOD, OA1, OA2, PKDET+, PKDET- and BIAS
4	VEEIF	ground		negative supply of LNA, MIX1 MIX2, IFF, IFA, and FSK DEMOD
5	MIXN	analog input		mixer 1 negative input
6	MIXP	analog input		mixer 1 positive input
7	SPISEL	CMOS input		SPI select input
8	RSSI	analog output		RSSI output, approx. 25kΩ
9	MODSEL	CMOS input		demodulation select input (FSK or ASK demodulation)

Pin No.	Name	I/O Type	Functional Schematic	Description
10	RBIAS	analog I/O		external resistor for voltage and current biasing, 30kΩ by default, to provide stable parameters over temperature and supply variations
11	VEEVCO	ground		ground of VCO
12	TNK1	analog I/O		VCO collector output, connection 1 to external LC tank
13	TNK2	analog I/O		VCO collector output, connection 2 to external LC tank
15	LF	analog I/O		charge pump output, connection to external loop filter
14	VCCVCO	supply		positive supply of VCO
16	ENRX	CMOS input		enable/disable control input (with internal pull-down)

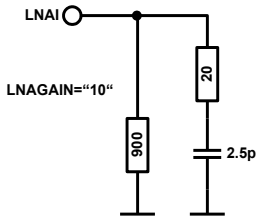
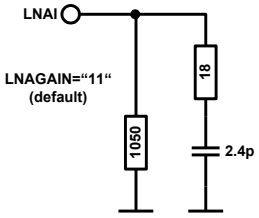
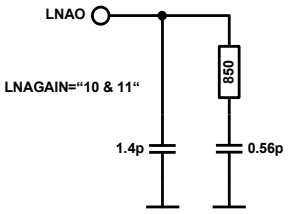
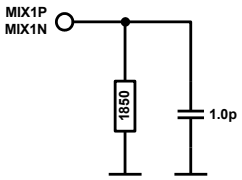
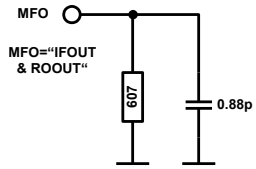
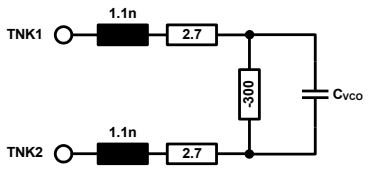
Pin No.	Name	I/O Type	Functional Schematic	Description
17	C/SDEN	CMOS input		frequency control line C or SPI control line SDEN
18	B/SDTA	CMOS input		frequency control line B or SPI control line SDTA
19	A/SCLK	CMOS input		frequency control line A or SPI control line SCLK
20	VEEDIG	ground		ground of PLL SYNT (except of VCO), Control Logic, and OA2 out stage
21	VCCDIG	supply		positive supply of PLL SYNT (except of VCO), Control Logic, RO and OA2 out stage
22	DTAO	CMOS output		data output, 2mA sink or source capability

Pin No.	Name	I/O Type	Functional Schematic	Description
23	MFO	analog output (option 1)		multifunctional output: reference oscillator output selected (default setting) (see 4.1.4)
23	MFO	analog output (option 2)		multifunctional output: IF2 signal output selected (see 4.1.4)
23	MFO	digital output tristate (option 3)		multifunctional output: digital output signal selected (see 4.1.4)
24	ROI	analog input		reference oscillator input for connecting an external crystal, Colpitts type oscillator with internal feedback capacitors

Pin No.	Name	I/O Type	Functional Schematic	Description
25	PDP	analog I/O		peak detector positive output for connecting an external capacitor
26	PDN	analog I/O		peak detector positive output for connecting an external capacitor
27	DFO	analog output		data filter output
28	DF1	analog I/O		data filter connection 1 for connecting an external capacitor
29	DF2	analog I/O		data filter connection 2 for connecting an external capacitor
30	VEEANA	ground		ground of RO, OA1, OA2, PKD+, PKD- and BIAS
32	SLC	analog I/O		slicer reference input for connecting an external capacitor

2.2. RF Pin Impedance Models

The following table gives the typical equivalent circuits modelling the impedance of the RF-pins including the package but without the PCB parasitics.
The LNA, MIX1 and TNK1/2 models are valid from 300 to 930MHz, the MFO model is valid from 1 to 10MHz.

LNAI (GAIN=”10”)	LNAI (GAIN="11”)
	
LNAO (GAIN=”10”´& “11”)	**MIX1P & MIX1N**
	
MFO	**TNK1/2**
	

V_{LF} / V	VCORANGE=0 VCC=3V C_{VCO} / pF	VCORANGE=1 VCC=5V C_{VCO} / pF
0.0	6.50	6.20
0.5	6.40	6.10
1.0	6.10	6.05
1.5	4.80	5.75
2.0	3.60	5.10
2.5	3.05	4.40
3.0	2.80	3.75
3.5	-	3.20
4.0	-	2.65
4.5	-	2.45
5.5	-	2.35

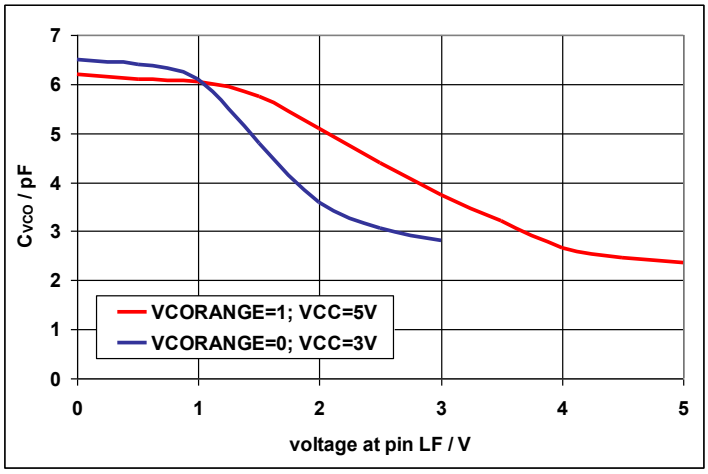


Fig. 2: C-V tuning characteristic of the VCO

The C-V-characteristics for other supply voltages than given above can be derived by shifting the right end of the curves to the desired supply voltage, since the VCO frequency depends on V_{CC}-V_{LF}.

3. Functional Description

3.1. Frequency Planning

Because of the double conversion architecture that employs two mixers and two IF signals, there are four different combinations for injecting the LO1 and LO2 signals:

LO1 high side and LO2 high side: receiving at $f_{RF\ High\text{-}High}$
LO1 high side and LO2 low side: receiving at $f_{RF\ High\text{-}Low}$
LO1 low side and LO2 high side: receiving at $f_{RF\ Low\text{-}High}$
LO1 low side and LO2 low side: receiving at $f_{RF\ Low\text{-}Low}$

As a result, four different input frequencies could produce the same second IF (IF2). This may seem like a problem, but being able to select high or low side injection makes it possible to avoid interference from undesired signals. This can not be done with the more common receivers which are single conversion with a low IF frequency. It is also often possible with the MLX71122 to use a simple RF filter to get better image rejection than low IF receivers which have an image reject mixer.

Referring to the block diagram in fig.1, the following equations apply:

$f_{IF2} = 2.0MHz$, N_{LO2} = LO2DIV = 4 or 8 $\qquad$ f_{IN} = desired RF signal frequency

LO1 on high side: $f_{VCO} - f_{IN} = f_{IF1}$ $\qquad$ LO2 on high side: $\frac{f_{VCO}}{N_{LO2}} - f_{IF1} = 2.0MHz$

LO1 on low side: $f_{IN} - f_{VCO} = f_{IF1}$ $\qquad$ LO2 on low side: $f_{IF1} - \frac{f_{VCO}}{N_{LO2}} = 2.0MHz$

From these seven equations, we get:

LO1 high side and LO2 high side: $$f_{VCO} = (f_{IN} - 2MHz)\frac{N_{LO2}}{N_{LO2} - 1} \quad (1)$$

LO1 high side and LO2 low side: $$f_{VCO} = (f_{IN} + 2MHz)\frac{N_{LO2}}{N_{LO2} - 1} \quad (2)$$

LO1 low side and LO2 high side: $$f_{VCO} = (f_{IN} + 2MHz)\frac{N_{LO2}}{N_{LO2} + 1} \quad (3)$$

LO1 low side and LO2 low side: $$f_{VCO} = (f_{IN} - 2MHz)\frac{N_{LO2}}{N_{LO2} + 1} \quad (4)$$

Fig. 3 on the next page shows the 4 possible RF frequencies when receiving at $f_{RF\ High\text{-}High}$ is desired.

Example:

Let $f_{IN} = 315MHz$ and $N_{LO2} = 4$. From (1) we get $f_{VCO} = (315MHz - 2MHz)\frac{4}{4-1} = 417.33MHz$ and further $f_{IF1} = 102.33MHz$, $f_{LO2} = 104.33MHz$ and the 2nd IF frequency is 2.0MHz.

The image frequencies of the two mixers are now:
$f_{MIX1IMAGE} = 417.33 + 102.33 = 519.66MHz$, RF response, suppressed by the RF bandpass filter,
$f_{MIX2IMAGE} = 104.33 + 2.0 = 106.33MHz$, suppressed by the image rejection of mixer 2.

$f_{MIX2IMAGE}$ leads to two further RF response frequencies:

$417.33 - 106.33 = 311.00MHz$: suppressed by 30dB of the image rejection of mixer 2
$417.33 + 106.33 = 523.66MHz$: suppressed by 30dB of mixer 2 plus the RF bandpass filter

In the example of Fig. 3, the image signals at 519.66 and 523.66 are suppressed by the bandpass characteristic provided by the RF front-end. The bandpass shape can be achieved either with a SAW filter (featuring just a couple of MHz bandwidth), or by the tank circuits at the LNA input and output (this typically yields 30 to 60MHz bandwidth). In any case, the high value of the first IF (IF1) helps to suppress the image signals at $f_{RF\ Low\text{-}High}$ and $f_{RF\ Low\text{-}Low}$.

The two remaining signals at IF1 resulting from 102.33 and 106.33 enter the second mixer MIX2. This mixer features image rejection with so-called single-sideband (SSB) selection. This means either the upper or lower sideband of IF1 can be selected. In the example of Fig. 3, LO2 high-side injection has been chosen to select the IF2 signal resulting from $f_{RF\ High\text{-}High}$.

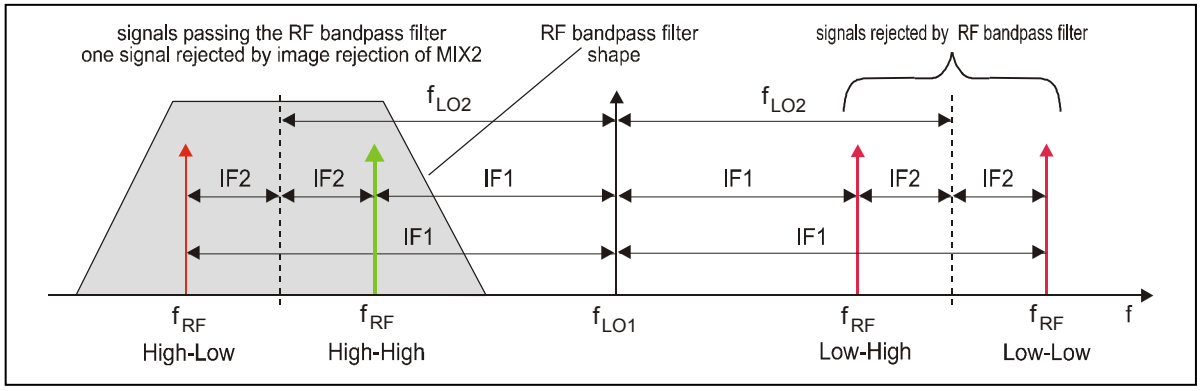


Fig. 3: The four receiving frequencies in a double conversion superhet receiver

It should be mentioned that each high-side injection mixing mirrors the frequency spectrum of the input signal. Only Low-Low and High-High injection mixing preserve the spectrum or in other words a higher frequency at RF remains a higher frequency at IF2. The polarity of the data slicer can be switched in order to compensate this for FSK reception of digital data.

It can be seen from the block diagram of Fig. 1 that there is a fixed relationship between the LO1 signal frequency f_{LO1} and the LO2 signal frequency f_{LO2}.

$$LO2DIV = N_{LO2} = \frac{f_{LO1}}{f_{LO2}} \tag{5}$$

The LO1 signal frequency f_{LO1} is directly synthesized from the crystal reference oscillator frequency f_{RO} by means of an integer-N PLL synthesizer. The PLL consists of a dual-modulus prescaler (P/P+1) with P=32, a program counter N and a swallow counter A.

$$f_{LO1} = \frac{f_{RO}}{R}(N \cdot P + A) = f_{PFD}(N \cdot P + A) = f_{PFD} \cdot N_{tot} \quad (6)$$

Since $LO2 = \frac{LO1}{4 \, or \, 8}$,the channel frequency step, $f_{CH,}$,is **not** equal to the phase-frequency detector (PFD) frequency f_{PFD}.

For LO2 high-side injection, the channel step size f_{CH} is given by

$$f_{CH} = \frac{f_{RO}}{R}\frac{N_{LO2} - 1}{N_{LO2}} = f_{PFD}\frac{N_{LO2} - 1}{N_{LO2}} \quad , \quad (7)$$

while the following equation is valid for LO2 low-side injection:

$$f_{CH} = \frac{f_{RO}}{R}\frac{N_{LO2} + 1}{N_{LO2}} = f_{PFD}\frac{N_{LO2} + 1}{N_{LO2}} \quad . \quad (8)$$

3.1.1. Calculation of Counter Settings

Frequency planning and the selection of the MLX71122's PLL counter settings are straightforward and can be laid out on the following procedure.

For this type of counter, it is necessary that $A < N$.

For discrete frequency tuning without equal channel steps:

Find a combination of R, A and N to obtain f_{VCO} from equations (1), (2), (3) or (4). A large value for R is not always necessary to get high resolution tuning. A combination of N_{TOT} and R can almost always be found which will give sufficient frequency accuracy even with a high PLL reference frequency. For example, 433.92MHz can be tuned with a 10MHz crystal with $R = 17$ and $N_{TOT} = 979$ with an 8.3kHz error.

For equal channel steps without gaps:

It is necessary that $N \geq P$, it follows $(NP + A) \geq P^2$, so $N \geq 32$ and $NP + A = N_{tot} \geq 1024$. (9)

3.1.2. Calculation of LO1 and IF1 frequency for Low Frequency Bands

High-high or high-low injection can be used for the low frequency bands. If equal channel steps are desired, choose a PFD frequency f_{PFD} according to the table below. The R counter values are valid for a 10MHz crystal reference frequency f_{RO}. The PFD frequency is given by $f_{PFD} = f_{RO}/R$.

Injection Type	f_{CH} [kHz]	f_{PFD} [kHz]	R
h-h	10	13.3	750
h-h	12.5	16.7	600
h-h	20	26.7	375
h-h	25	33.3	300
h-h	50	66.7	150
h-h	100	133.3	75
h-h	250	333.3	30

The second step is to calculate the missing parameters f_{LO1}, f_{IF1}, N_{tot}, N and A. While the second IF (f_{IF2}), the N_{LO2} divider ratio and the prescaler divider ratio P are bound to f_{IF2} = 2MHz, N_{LO2} = 4 (or 8) and P =32.

$$f_{LO1} = \frac{N_{LO2}}{N_{LO2}-1}(f_{RF} - f_{IF2}) \quad f_{LO1} = \frac{4}{3}(f_{RF} - 2MHz) \tag{10}$$

$$f_{IF1} = \frac{f_{RF} - N_{LO2} f_{IF2}}{N_{LO2}-1} \qquad f_{IF1} = \frac{f_{RF} - 8MHz}{3} \tag{11}$$

Finally N and A can be calculated with equation (6).

3.1.3. Calculation of LO1 and IF1 frequency for High Frequency Bands

Typical ISM band operating frequencies like 868.3 and 915MHz can be covered without changing the crystal or the VCO inductor. Low-low injection is usually used for the high frequency bands. If equal channel steps are desired, choose a PFD frequency f_{PFD} according to the table below. The R counter values are valid for a 10MHz crystal reference. The PFD frequency is given by $f_{PFD} = f_{RO}/R$.

Injection Type	f_{CH} [kHz]	f_{PFD} [kHz]	R
l-l	20	16	625
l-l	25	20	500
l-l	50	40	250
l-l	100	80	125
l-l	250	200	50
l-l	500	400	25

The second step is to calculate the missing parameters f_{LO1}, f_{IF1}, N_{tot}, N and A. While the second IF (f_{IF2}), the N_{LO2} divider ratio and the prescaler divider ratio P are bound to f_{IF2} = 2MHz, N_{Lo2} = 4 (or 8) and P =32.

$$f_{LO1} = \frac{N_{LO2}}{N_{LO2}+1}(f_{RF} - f_{IF2}) \quad f_{LO1} = \frac{4}{5}(f_{RF} - 2MHz) \tag{12}$$

$$f_{IF1} = \frac{f_{RF} + N_{LO2} f_{IF2}}{N_{LO2} + 1} \qquad f_{IF1} = \frac{f_{RF} + 8MHz}{5} \qquad (13)$$

Finally N and A can be calculated with equation (6).

3.1.4. Counter Setting Examples for SPI Mode

To provide some examples, the following table shows some counter settings for the reception of the well-known ISM and SRD frequency bands. The channel spacing is assumed to be f_{CH} = 100kHz. In below table all frequency units are in MHz.

Inj	f_{RF}	f_{IF1}	f_{LO1}	N_{tot}	N	P	A	f_{PFD}	R	f_{REF}	f_{LO2}	f_{IF2}
h-h	300	97.3	397.3	2980	93	32	4	0.133	75	10	99.3	2
h-h	315	102.3	417.3	3130	97	32	26	0.133	75	10	104.3	2
h-h	434	142	576	4320	135	32	0	0.133	75	10	144	2
h-h	470	154	624	4680	146	32	8	0.133	75	10	156	2
l-l	850	171.6	678.4	8480	256	32	0	0.08	125	10	169.6	2
l-l	868	175.2	692.8	8660	270	32	20	0.08	125	10	173.2	2
l-l	915	184.6	730.4	9130	285	32	10	0.08	125	10	182.6	2
l-l	930	187.6	742.4	9280	290	32	0	0.08	125	10	185.6	2

3.1.5. Counter Settings in ABC Mode – 8+1 Preconfigured Channels

In ABC mode (SPISEL=0), the counter settings are hard-wired. In below table all frequency units are in MHz.

CH	Inj	f_{RF}	f_{IF1}	f_{LO1}	N_{tot}	N	P	A	f_{PFD}	R	f_{REF}	f_{LO2}	f_{IF2}
1	h-l	369.5	125.8	495.3	3715	116	32	3	0.133	75	10	123.8	2
2	h-l	371.1	126.4	497.5	3731	116	32	19	0.133	75	10	124.4	2
3	h-l	375.3	127.8	503.1	3773	117	32	29	0.133	75	10	125.8	2
4	h-l	376.9	128.3	505.2	3789	118	32	13	0.133	75	10	126.3	2
5	h-l	384.0	130.7	514.7	3860	120	32	20	0.133	75	10	128.7	2
6	h-l	388.3	132.1	520.4	3903	121	32	31	0.133	75	10	130.1	2
7	h-l	391.5	133.2	524.7	3935	122	32	31	0.133	75	10	131.2	2
8	h-l	394.3	134.1	528.4	3963	123	32	27	0.133	75	10	132.1	2
9	h-l	395.9	134.6	530.5	3979	124	32	11	0.133	75	10	132.6	2

3.2. PLL Frequency Synthesizer

The MLX71122 contains an integer-N PLL frequency synthesizer. The reference frequency f_R is derived from a stable crystal reference oscillator.

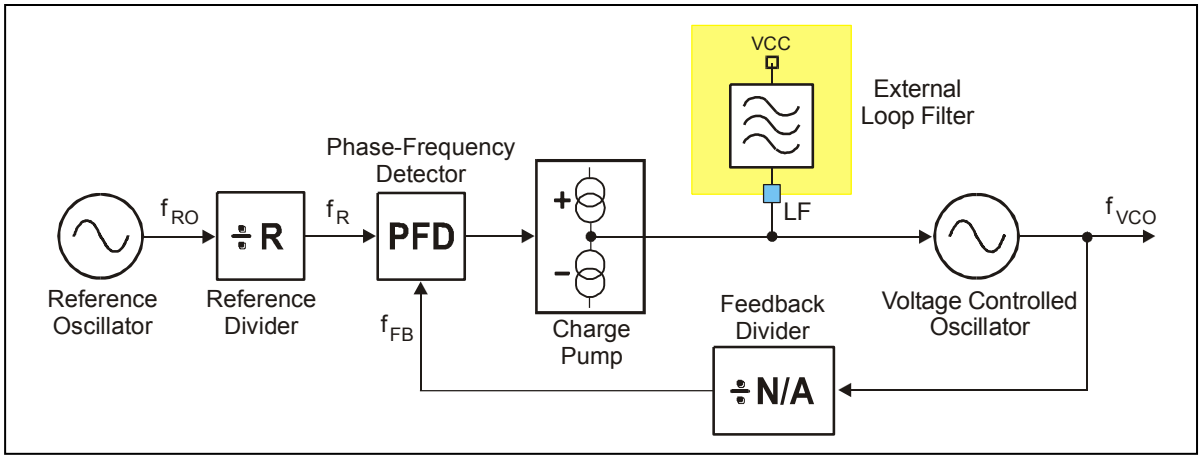


Fig. 4: Integer-N PLL Frequency Synthesizer Topology

The locked state of the PLL is defined by the following relations:

$$\frac{f_{RO}}{R} = f_R = f_{PFD} = f_{FB} = \frac{f_{VCO}}{N_{tot}} = \frac{f_{VCO}}{N \cdot P + A}. \qquad (14)$$

In this formula the total PLL feedback divider ratio is called N_{tot}. The synthesized output frequency f_{VCO} can be changed by reprogramming the reference divider or the feedback divider according to

$$f_{VCO} = N_{tot}\frac{f_{RO}}{R} = (N \cdot P + A)\frac{f_{RO}}{R}. \qquad (15)$$

The R counter is used to set the channel spacing. Different channels can be selected by changing the total feedback divider ratio.

List of Mathematical Acronyms	
A	divider ratio of the swallow counter (part of feedback divider)
f_{FB}	frequency at the feedback divider output
$\text{floor}\,(x)$	The floor function gives the largest integer less than or equal to x. For example, floor(5.4) gives 5, floor(-6.3) gives -7.
f_{PFD}	PFD frequency in locked state
$\frac{f_{RO}}{R} = f_R$	reference frequency of the PLL
f_{RO}	frequency of the crystal reference oscillator
f_{VCO}	frequency of the VCO (equals the LO1 signal of the first mixer)
$N_{tot} = N \cdot P + A$	total divider ratio of the PLL feedback path
N	divider ratio of the program counter (part of feedback divider)
N_{LO2}	LO2DIV divider ratio, to derive the LO2 signal from LO1 (N_1 = 4 or 8)
P	divider ratio of the prescaler (part of feedback divider)
R	divider ratio of the reference divider R

3.2.1. Pulse Swallow Counter

The programmable feedback divider of the PLL is based on a pulse-swallow topology. Fig. 5 depicts its implementation, consisting of a dual-modulus prescaler, an RS latch and two programmable counters.

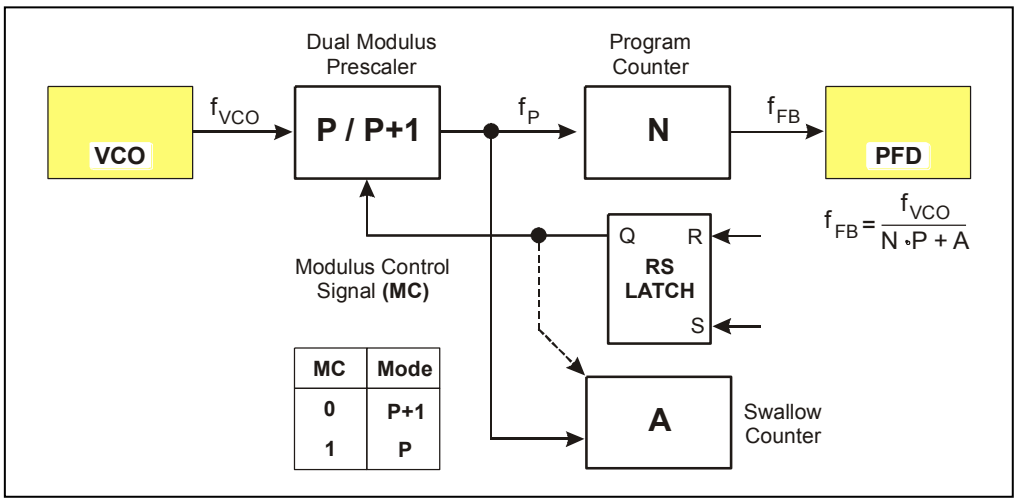


Fig. 5 Pulse Swallow Counter Topology

During one cycle of f_{FB} the prescaler begins the operation by dividing by P+1 until the swallow counter A is full. The RS latch is then set and changes the prescaler modulus to P (via the modulus control signal MC) and disables the swallow counter. The division process continues until the program counter N is full and the RS latch is reset.

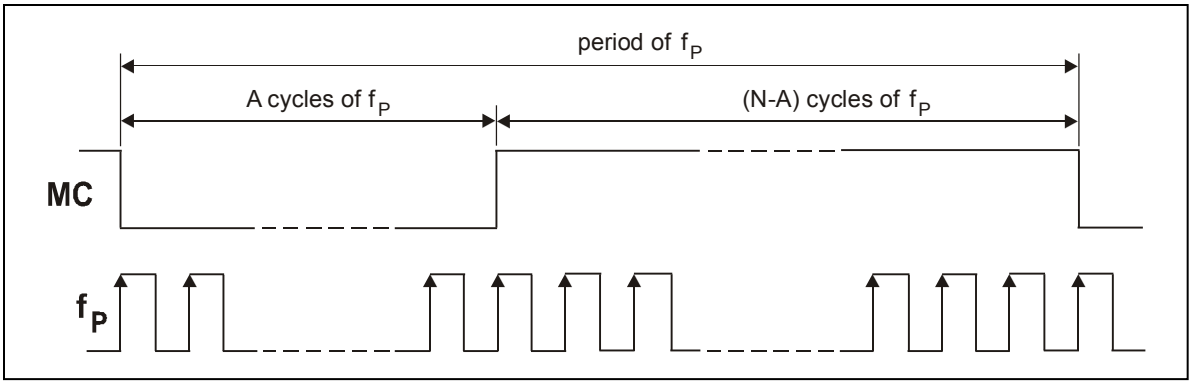


Fig. 6 Pulse Swallow Divider Timing

Therefore the overall feedback divide ratio is:

$$(P+1)\cdot A + P\cdot(N-A) = N\cdot P + A. \qquad (16)$$

Further restrictions can be derived from above equation: A < P and A < N.
Some math shows that for uniform frequency steps without gaps (N ≥ P) the following condition is necessary:

$$N\cdot P + A \geq P\cdot P. \qquad (17)$$

3.2.2. PLL Counter Ranges

In order to cover the frequency range of about 300 to 930MHz the following counter values are implemented in the receiver:

PLL Counter Ranges			
A	***N***	***R***	***P***
0 to 31 (5bit)	3 to 2047 (11bit)	3 to 2047 (11bit)	32

Therefore the minimum and maximum divider ratios for uniform frequency steps are given by:

$$N_{totmin} = 32\cdot 32 = 1024 \qquad N_{totmax} = 2047\cdot 32 + 31 = 65535$$

3.2.3. Reference Oscillator (RO)

The reference oscillator is based on a Colpitts topology with two integrated functional capacitors as shown in figure 7. The circuitry is optimized for a load capacitance range of 10pF to 15pF. The equivalent input capacitance CRO offered by the oscillator input pin ROI is about 15pF. To ensure a fast and reliable start-up and a very stable frequency over the specified supply voltage and temperature range, the oscillator bias circuitry provides an amplitude regulation. Via SPI it is possible to adjust the typical core current with register ROCUR. There are four values available (see 4.1.7). At the default setting 355µA, the amplitude at pin ROI is monitored in order to regulate the current of the oscillator core I_{RO}.

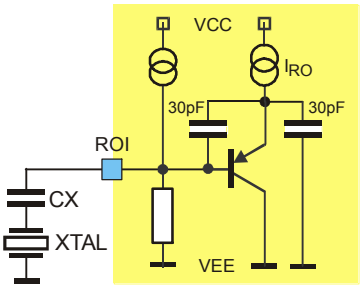


Fig.7: RO schematic

3.2.4. Phase-Frequency Detector (PFD)

The phase-frequency detector (in conjunction with the charge pump) generates a voltage step at the loop filter pin LF. This voltage step is proportional to the phase difference between the digital input signals f_R and f_{FB}. The implementation of the phase detector is phase-frequency type. This circuitry is very useful because it decreases the acquisition time significantly even if both frequencies differ very much. The phase-frequency detector creates Up and Down signals that control the charge pump and that are also used for the lock de-tection circuit. The first rising edge of one of the input signals, after a reset of Up and Down, sets either the Up or the Down signal from LOW to HIGH. The following rising edge of the other signal resets Up and Down. If the register setting PFDPOL (see 4.1.2) is HIGH, the PFD polarity is positive. This means a rising edge of the signal f_R sets Up from LOW to HIGH and a rising edge of the signal f_{FB} sets Down from LOW to HIGH. If PFDPOL is LOW, the PFD polarity is negative and the assignment of Up and Down to the signals f_R and f_{FB} is swapped.

In the MLX71122 receiver the VCO frequency increases if the loop filter output voltage increases and vice versa. The PFD polarity needs to be positive to achieve the correct feedback in the PLL loop. If an external varactor diode is added to the VCO tank, the tuning characteristic may change from positive to negative depending on the particular varactor diode circuitry. Therefore the PFDPOL bit can be used to define the phase-frequency detector polarity.

3.2.5. Charge Pump (CP)

The Charge Pump is controlled by the Up and Down signals of the Phase-Frequency Detector. If the Up signal is HIGH, then the charge pump current I_{CP} is sourced from the positive supply rail to the loop filter pin LF (pin 15). If the Down signal is HIGH, then the current I_{CP} is drained from pin LF to ground.
The gain of the phase detector in conjunction with the charge pump can be expressed as:

$$K_{PD} = \frac{I_{CP}}{2\pi}, \qquad (18)$$

whereas I_{CP} is the charge pump current which is set via register CPCUR (see 4.1.2). Default of I_{CP} is 100µA. The static Up and Down selections of I_{CP} can be used for test purposes.

3.2.6. Loop Filter (LF)

Since the loop filter has a strong impact on the function of the PLL, it must be chosen carefully. The suggested filter topology is shown in Fig. 8.

The loop filter of the PLL is set up by an external resistor and two external capacitors. It constitutes a 2nd order passive filter. This approach allows the user to easily adapt the loop filter bandwidth to different requirements. As a rule of thumb the loop filter bandwidth of an integer-N PLL should be set 10 times smaller than the PFD frequency. This is to achieve a stable PLL with a flat VCO noise floor.

The loop filter bandwidth depends on the external resistor and capacitors as well as on the VCO gain, the charge pump current and the so-called phase margin. A phase margin of 45° is commonly used for highest PLL stability. It is recommended to follow the component lists of section 6 for choosing appropriate values of the loop filter resistor and capacitors.

A good source for a detailed PLL analysis is: “Gardner, F.M., Phase-Locked Loop Techniques, John Wiley & Sons, 1980.”

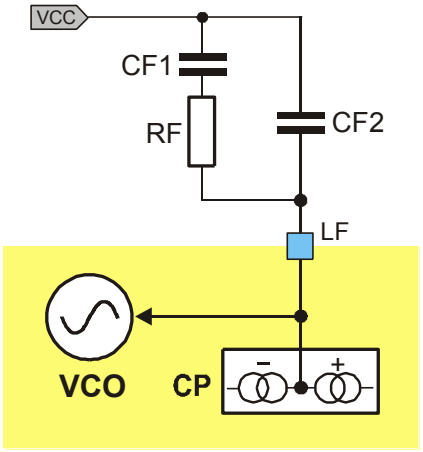


Fig. 8: 2nd order Loop filter

3.2.7. Lock Detector (LD)

In SPI mode a lock-detect signal LD is available at pin 23 if MFO is set to 1000 (binary) in control word R3 (see 4.1.4). The pin output is HIGH when the PLL is locked in. Alternatively the lock-detect signal is visible in bit 10 of R7 (see 4.1.8) if bit SHOWLD in R1 (see 4.1.2) is HIGH. The lock detection circuitry uses the Up and Down signals from the phase-frequency detector to check them for phase coherency. Figure 9 shows an overview of the lock signal generation. The locked state and the unlock condition will be controlled by the register settings of LDTIME and LDERR. During the start-up phase of the PLL, Up and Down signals are quite unbalanced. Therefore the Lock Detector circuit waits the time span that is programmed in divider DIV_LDTIME before a first lock can occur. The time span is dependent on the period of the reference signal f_R. By default it is $16/f_R$ (see 4.1.2). When the PLL approaches steady state, the signals Up and Down begin to overlap. The time span within which the signals are not overlapping is assessed by using a programmable delay gate. If it is shorter than programmed in LDERR (see 4.1.2) then the LD output is set to HIGH. By default the error time should be shorter than 15ns. A second option is shorter than 30ns.
After LD is set to HIGH the divider is disabled and the lock state remains unchanged until the unlock signal resets the divider.

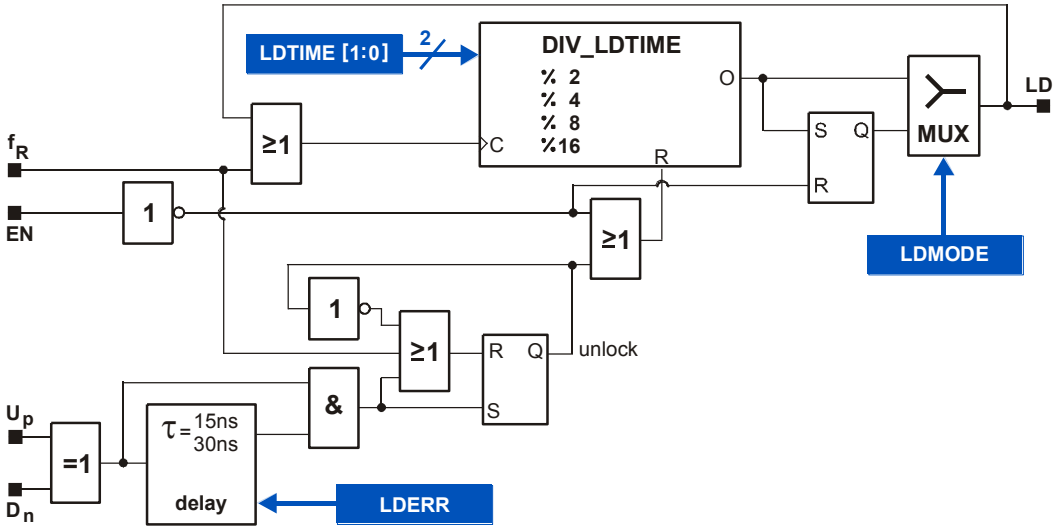


Fig. 9: Lock Detection Circuit