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MLX73290-M

300 to 960MHz Multi-Channel Transceiver With Flex RF Front-End

1. Features and Benefits

- Flex TX/RX RF front-end for antenna and frequency diversity
- Energy harvesting interface
- Transmitter with power detectors
- Receiver with digital RSSI
- Receiver self polling with MCU wake-up
- Multi-band frequency coverage from 300MHz up to 960MHz
- Modulation schemes supported: (G)FSK, (G)MSK, (G)OOK
- Transmitter power of -20 to 13dBm, 64 steps
- Receiver sensitivity of -120dBm (FSK, 433MHz, 15kHz CHBW)
- Supply voltage range of 2.1 to 3.6V
- PLL synthesizer with 60Hz resolution
- Channel filter bandwidth of 9 to 600kHz
- Data rate of 0.3 to 250kbps (GFSK)
- Frequency deviation up to 125kHz
- 32MHz crystal frequency
- Comprehensive supply monitoring & error handling capabilities
- SPI programmable in stand-by mode
- Multi-channel sensing and packet recognition
- 256byte FIFO (can be split 128/128 for RX/TX)
- 4 programmable GPIO ports
- 32L QFN5x5 package
- Compliant to EN 300 220, DASH7, FCC part 15, ARIB STD-T67, IEEE802.15.4 and other standards

2. Application Examples

- Automatic meter reading (AMR)
- Remote controls
- Home and building automation
- Alarm and security systems
- Garage door openers
- Medical applications
- Telemetry
- Industrial appliances
- Automotive keyless entry
- Tire pressure monitoring

3. Ordering Code

Product	Temperature	Package	Option	Packaging Form
MLX73290	R (-40°C to 105°C)	LQ (32L QFN5x5)	BBM-000	RE (reel 5000 pcs.)

4. Introduction

The MLX73290-M is a 300 to 930MHz multi-channel transceiver chip. The IC is designed for general purpose applications for example in the European bands at 433MHz and 868MHz or for similar applications in North America or Asia, e.g. at 315MHz or 915MHz. It is also well-suited for narrow-band applications which meet the ARIB standard STD-T67 in the frequency range 426MHz to 470MHz.

The output power, frequency channel, modulation type and frequency deviation are programmable via the serial programming interface (SPI). The synthesizer operates with a fractional-N PLL and VCO with integrated inductor. The small frequency resolution of the MLX73290-M and its PLL phase noise performance facilitate it for narrow-band operation. There are five selectable modulation schemes: on-off keying (OOK), binary frequency shift keying (FSK) and minimum shift keying (MSK) as well as their Gaussian filtered versions (GFSK and GMSK). The low-IF receiver part comprises fully digital demodulation and self-polling features together with channel scanning and packet recognition.

Contents

5. Version History

Data sheet version	Date	Value
Rev 001	July 2012	First public release, preliminary version
Rev 002	Oct 2012	Corrections, packed handler added, preliminary version
Rev 003	Dec 2012	PA control information added
Rev 004	Mar 2013	Receiver self polling with MCU wake-up, register name OOK_MOD changed to RF_BIAS, performance plots added
Rev 005	Jun 2013	ACR, blocking parameters and more performance plots added
Rev 006	Sep 2013	More GPIO description added
Rev 007	Oct 2013	Flow chart for RF state machine added
Rev 008	May 2015	Temperature codes redefined and general update
Rev 009	Sep 2015	General update, modulation settings added
Rev 010	Dec 2016	Carrier frequency acceptance range added

6. Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD}	0 to 4	V
Operating Temp. Range	T_A	-40 to 105	°C
Storage Temperature Range	T_S	-55 to 125	°C
ESD Sensitivity (HBM)	V_{ESD}	±2	kV
ESD Sensitivity (CDM)	V_{ESD}	±0.5	kV

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7. Pin Definitions and Pin-out

Pin №	Name	Type	Function
1	VPA	Supply	Supply of PA
2	VSSA	Ground	Analog Ground
3	PD1	RF analog	RF Power Detector 1
4	RF1P	RF analog	RF port 1 - positive
5	RF1N	RF analog	RF port 1 - negative
6	NC		Not connected
7	NC		Not connected
8	VSSA	Ground	Analog Ground
9	VHARV	Analog	Energy harvesting input
10	VDDD3	Supply	Battery supply (dedicated to power switch)
11	VMAIN	Supply	Power switch output for host MCU
12	VDIG	Regulated supply	Digital voltage regulator output

Pin №	Name	Type	Function
13	VSSD	Ground	Digital Ground
14	GPIO3	Analog/Digital	General Purpose IO3
15	GPIO2	Analog/Digital	General Purpose IO2
16	CS	Digital	SPI Chip Select
17	GPIO1	Analog/Digital	General Purpose IO1
18	GPIO0	Analog/Digital	General Purpose IO0
19	SDO	Digital	SPI Slave Data Output
20	SDI	Digital	SPI Slave Data Input
21	SCK	Digital	SPI Clock
22	VSSA	Ground	Analog Ground
23	XTALN	Analog	Crystal negative input
24	XTALP	Analog	Crystal positive input
25	VDDA3	Supply	Analog supply
26	VANA	Regulated supply	Analog voltage regulator output
27	VSSA	Ground	Analog Ground
28	RF2N	RF analog	RF port 2 - positive
29	RF2P	RF analog	RF port 2 - negative
30	PD2	RF analog	RF Power Detector 2
31	VSSA	Ground	Analog Ground
32	VDDA3	Supply	Analog Supply
EP	VSSA	Exposed pad	Analog Ground to be connected to GND on PCB

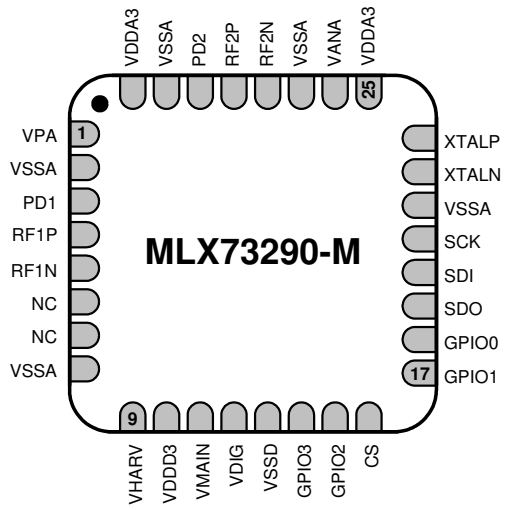

Figure 1: Pin-out of MLX73290-M

Figure 2: Picture of MLX73290-M devices

8. Electrical Specifications

8.1. Normal Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{DD}		2.1	3.0	3.6	V
Operating temperature (R)	T_A	R version	-40	27	105	°C
Input low voltage (CMOS)	V_{IL}	Digital pins	-	-	0.3 * V_{DD}	V
Input high voltage (CMOS)	V_{IH}	Digital pins	0.7 * V_{DD}	-	-	V

8.2. General Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Timers						
Un-calibrated RC Oscillator	f_{RCclk}		19	32	35	kHz
Calibrated RC Oscillator	$f_{RCclkCal}$		-	15.6	-	kHz
General purpose ADC						
Effective Number Of Bits	ENOB		-	10	-	bit
Sample Rate	SR		4	-	16	kS/s
Temperature sensor						
Sensitivity	$temp_{sens}$		-	-1.6	-	mV/°C
Offset	$temp_{off}$	25°C	-	750	-	mV

8.3. RF Characteristics

Operating Conditions: T_A = -40°C to 105°C, V_{DD} = 2.1V to 3.6V (unless otherwise specified)
Typical values at T_A = 25°C and , V_{DD} = 3.0V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
Frequency Range	$f_{RF,band1}$		299	-	331	MHz
	$f_{RF,band2}$		425	-	480	
	$f_{RF,band3}$	reserved for future use	-	-	-	
	$f_{RF,band4}$		850	-	960	
Operating currents						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Sleep mode	I_{SLEEP}	deep sleep	-	200	-	nA
		RCO on	-	400	-	
RF Receive mode	$I_{RX,315MHz}$	100kbps, FSK, NRZ	-	14	-	mA
	$I_{RX,433MHz}$		-	15	-	
	$I_{RX,868MHz}$		-	16	-	
	$I_{RX,915MHz}$		-	17	-	
RF Transmit mode	$I_{TX,315MHz}$	100kbps, FSK, NRZ, 0dBm	-	14	-	mA
		100kbps, FSK, NRZ, 10dBm	-	23	-	
	$I_{TX,433MHz}$	100kbps, FSK, NRZ, 0dBm	-	15	-	
		100kbps, FSK, NRZ, 10dBm	-	25	-	
	$I_{TX,868MHz}$	100kbps, FSK, NRZ, 0dBm	-	24	-	
		100kbps, FSK, NRZ, 10dBm	-	36	-	
	$I_{TX,915MHz}$	100kbps, FSK, NRZ, 0dBm	-	25	-	
		100kbps, FSK, NRZ, 10dBm	-	37	-	
Transmitter						
Max. CW output power at highest power step	$P_{max,315MHz}$	with 50Ω matching network	-20	13	-	dBm
	$P_{max,433MHz}$					
	$P_{max,868MHz}$					
	$P_{max,915MHz}$					
Spurious emissions < 1GHz	P_{spur}	Complies with EN 300 220 , FCC part 15and ARIB	-	-	-54	dBm
Spurious emissions > 1GHz			-	-	-30	dBm
Optimum impedance of matching network	R_{OUT}	single ended at output, Pout=13dBm		50		Ω
Receiver						
FSK receiver sensitivity 2.4kbps NRZ FSK Δf=±4kHz BW=15kHz, BER=10^{-3}	$P_{FSK,315MHz}$	315MHz	-	-120	-	dBm
	$P_{FSK,433MHz}$	433MHz	-	-120	-	dBm
	$P_{FSK,868/915MHz}$	868/915MHz	-	-116	-	dBm
OOK receiver sensitivity 2.4kbps NRZ BW=15kHz, BER=10^{-3}	$P_{OOK315MHz}$	315MHz	-	-115	-	dBm
	$P_{OOK433MHz}$	433MHz	-	-115	-	dBm
	$P_{OOK868/915MHz}$	868/915MHz	-	-114	-	dBm
Image rejection	IMR	after IQ calibration	40	50	-	dB
		w/o IQ calibration		25		
IF frequency	f_{IF}		-	fc/64	-	kHz
Channel filter bandwidth (digital)	CHBW	programmable	9	-	600	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input intercept point	IIP3	at max. gain		-28		dBm
Adjacent channel rejection	ACR	9kHz CHBW, (G)FSK	-	46	-	dB
Blocking	BLK	2MHz offset (50kHz CHBW)	-	52	-	dB
		10MHz offset (50kHz CHBW)	-	71	-	dB
Timings						
PA ramp up/down duration		programmable	0	-	192	µs
Channel switching time	t_{switch}	max frequency step	-	-	300	µs
RX/TX turn-around time	Δt_{RXTX}		-	-	50	µs
Sleep to RX on time	t_{RX}	programmable	200	-	-	µs
Sleep to TX on time	t_{TX}	programmable	200	-	-	µs
Modulator and data rate						
FSK deviation	Δf	Programmable in steps	-	-	±125	kHz
GFSK normalized BW	BT	fixed	-	0.5	-	
OOK modulation depth	M_{OOK}	100% modulation	70	80	-	dB
Data rate	DR_{FSK}	NRZ coding FSK	0.15	-	250	kbps
	DR_{OOK}	NRZ coding OOK	0.15	-	50	kbps
Synthesizer						
Phase noise	N_{PH_10kHz}	@ 10kHz offset	-	-	-94	dBc/Hz
	N_{PH_1MHz}	@ 1MHz offset	-	-	-110	dBc/Hz
Frequency resolution	f_{RES}		57	61	65	Hz
RX/TX switching time	Δt_{RXTX}		-	-	50	µs
RX or TX frequency change			-	-	15	µs
Crystal oscillator						
Crystal oscillator frequency	f_0		30	32	34	MHz
Crystal oscillator start-up time	$t_{ROstart}$		-	0.8	1	ms
Recommended crystal specification						
Crystal frequency accuracy	Δf_0		-	-	±30	ppm
Load capacitance (differential)	C_L	Recommended for ext. crystal	8	12	15	pF
Static capacitance	C_0	Recommended for ext. crystal	-	-	5	pF
Maximum Drive Level	MDL	Recommended for ext. crystal	-	-	100	µW
Equivalent series resistance (ESR)	R_1	Recommended for ext. crystal	-	-	70	Ω

8.4. SPI Characteristics

Operating Conditions: T_A = -40°C to 105°C, V_{DD} = 2.1V to 3.6V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SPI Clock Frequency	f_{SCLK}		-	1	10	MHz
SCK high time	t_{SCKH}	SCK ↑ to SCK ↓	40	-	-	ns
SCK low time	t_{SCKL}	SCK ↓ to SCK ↑	40	-	-	ns
SCK period	t_{SCK}	Between equal edges of SCK	100	-	-	ns
Setup time	t_{SU}	CS and SDI stable to SCK ↑	20	-	-	ns
Hold time	t_{HD}	SCK ↑ to CS or SDI changing	20		-	ns
SDO data delay	t_{SDO}	SCK ↓ to SDO stable	-	20	-	ns
Output enable delay	t_{OE}	SCK ↓ to SDO output enabled	-	20	-	ns
Output disable delay	t_{OD}	CS ↓ to SDO tri-state	-	50	-	ns

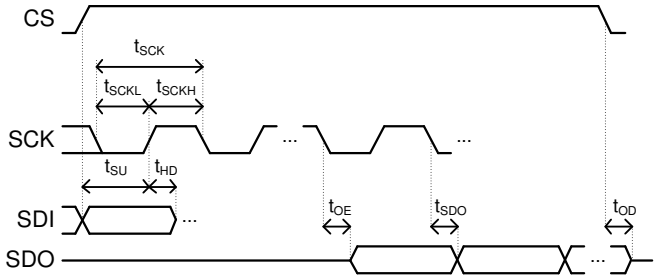

Figure 3: SPI timing specifications

9. Functional Description

9.1. Frequencies and Standards

The MLX73290-M complies with the following frequency bands and radio standards.

freq. band [MHz]	max. ERP [dBm]	channel BW [kHz]	max. data rate [kbps]	Comment
300-330	-20	0.25% of center freq.	20 (OOK, FSK)	SRDs - FCC 15.231 Japan ULP Band
426-469 433-434 446-447	10 10 10	12.5 - 25 not defined 25	5 (FSK) 200 (OOK, FSK) 1.2 (FSK)	Japan (ARIB), Korea SRDs - EN 300 220, DASH7 Europe PMR, US FSR
863-870 902-928	14 -1	25 - 600 200 (typ.)	250 (OOK, FSK) 250 (OOK, FSK)	SRDs - EN 300 220 SRDs - FCC 15.249

9.2. Block Diagram

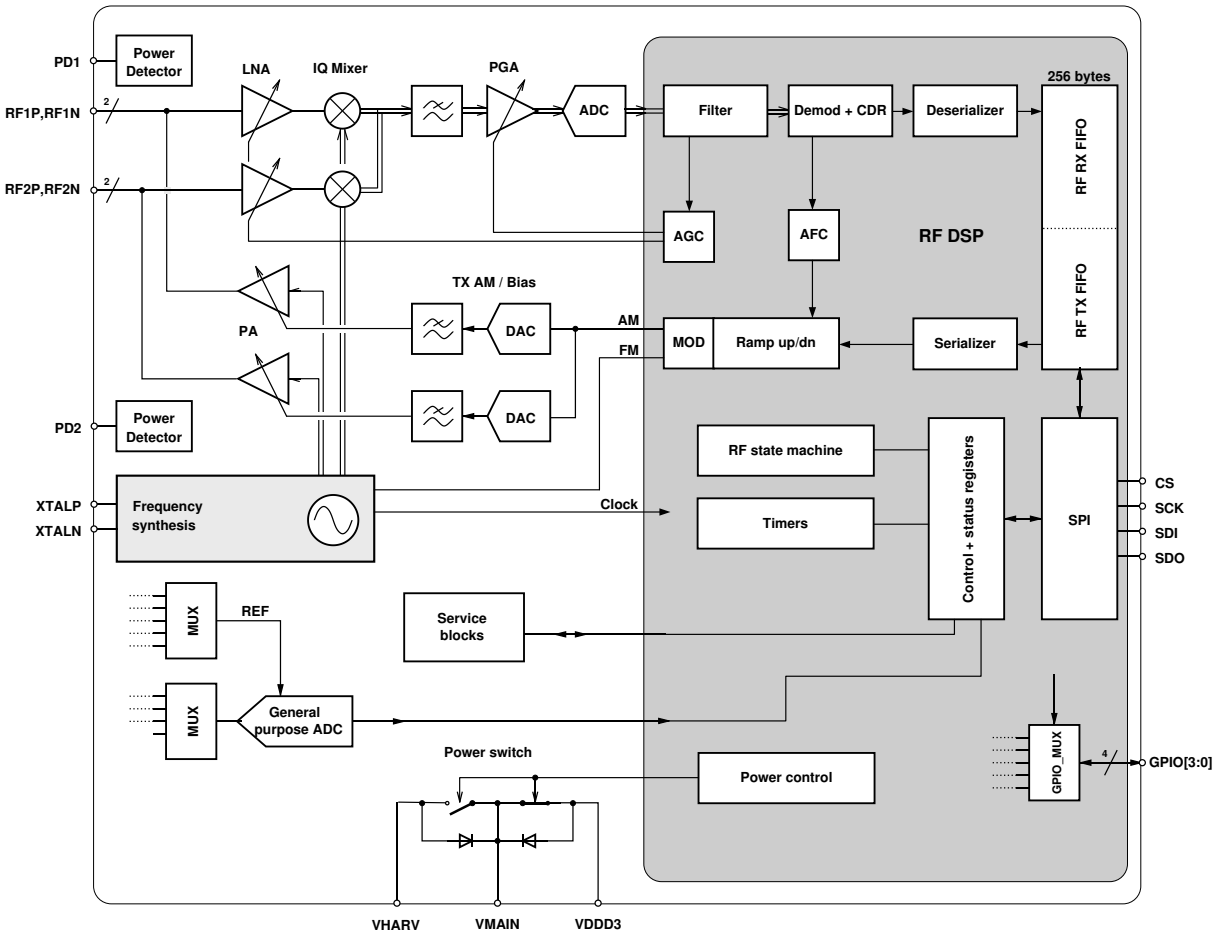

Figure 4: MLX73290-M block diagram (supply pins not shown)

9.3. Detailed Description

The MLX73290-M is fully programmable via its serial programming interface (SPI). The four SPI lines are configured as a standard 3-wire bus (CS, SCLK and SDI) plus an additional data output SDO providing feedback to an external microcontroller. This allows the changing of many parameters of the transceiver; for example to set up operating modes, channels, frequency resolutions, output power, modulation types, frequency deviation, polling modes and more.

The frequency synthesizer uses a fractional-N PLL that can be modulated with a Σ-Δ modulator. The VCO is fully integrated. Frequency deviations of the crystal oscillator (XOSC) can be simply compensated by adding offsets to the control words of the Σ-Δ modulator. Gaussian filtering of the input data signal is implemented for FSK and MSK modulation in order to provide a more narrow output spectrum.

The two TX/RX RF ports are combined differential I/O port for half-duplex operation; the LNAs and the PAs of each port are internally connected. The PA output power is programmable in 64 steps ranging from -20 dBm to +13 dBm. Output power switching of the PAs is always done with a programmable slew rate or Gaussian filtering in order to limit the transient output spectrum.

A low voltage detector disconnects the RF signal from the PAs if the supply voltage drops below a certain threshold value. This prevents the transmission of undesired frequencies at the battery's end of life.

In order to minimize the load of the host MCU, a packet handler takes care of formatting/pre-processing the data in both Receive & Transmit mode.

An on-chip power switch selects the supply voltage either from the battery (VDDA3) or from the energy-harvesting input (VHARV). It also provides the supply for the external host MCU (VMAIN).

Self-polling is realized by an integrated timer with very low power consumption. The polling mode wakes up the receiver or transmitter after a programmable time and scans one or more frequency channels for valid data. It can also be used to transmit the same data in a periodic way.

A transparent transmit or receive mode can also be chosen by selecting clock and data on GPIO pins.

9.4. RF Transceiver

The MLX73290-M is compliant with EN 300 220, FCC part 15 and ARIB STD-67 standards. It also supports DASH7 modes 1 and 2, as well as proprietary OOK, (G)MSK and (G)FSK-modulated communication protocols in ISM and SRD applications between 300 and 960MHz. Data rates between 0.15 and 250kbps, FSK deviations of up to 125kHz and RF output power levels between -20dBm and +13dBm can be used.

9.4.1. Flex TX/RX Front-End

The RF front-end consists of two differential TX/RX ports for half-duplex operation. Possible configurations are described below.

Low-cost, single-antenna TX/RX configuration

- RF port 1 is connected to a single antenna through a matching network (MNW)
- LNA1 is active in RX mode only
- PA1 is active in TX mode only
- Power detector 1 can be used for sensing the power at the antenna
- PA2, LNA2 and power detector 2 are not used

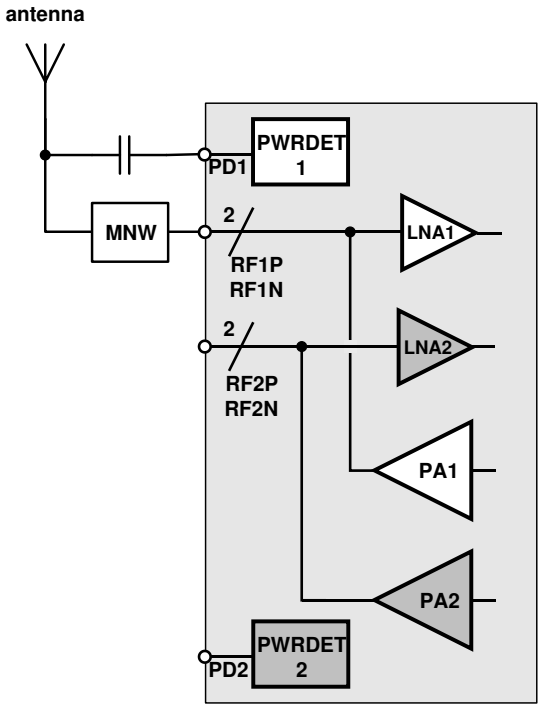

Figure 5

High-end, single-antenna TX/RX configuration

- RF port 1 operates in RX mode only
- RF port 2 operates in TX mode only
- RF port 2 connects to an external PA for boosting the TX power (e.g. up to 20dBm)
- RF port 1 and external PA output are connected to one antenna through a MNW
- External PA can be turned on/off via a GPIO pin
- Power detector 1 can be used for sensing the power at the antenna

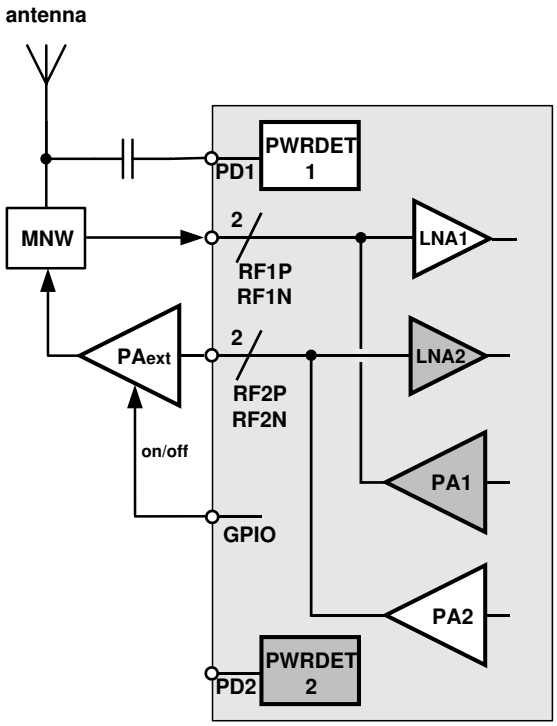

Figure 6

Antenna space or frequency diversity configuration

- RF port 1 is connected to antenna 1
- RF port 2 is connected to antenna 2
- the two RF ports operate at the same frequency

→ **antenna space diversity**

- the two RF ports operate at different frequencies

→ **frequency diversity**

- Power detectors 1 and 2 can be used for sensing the power at the antennas

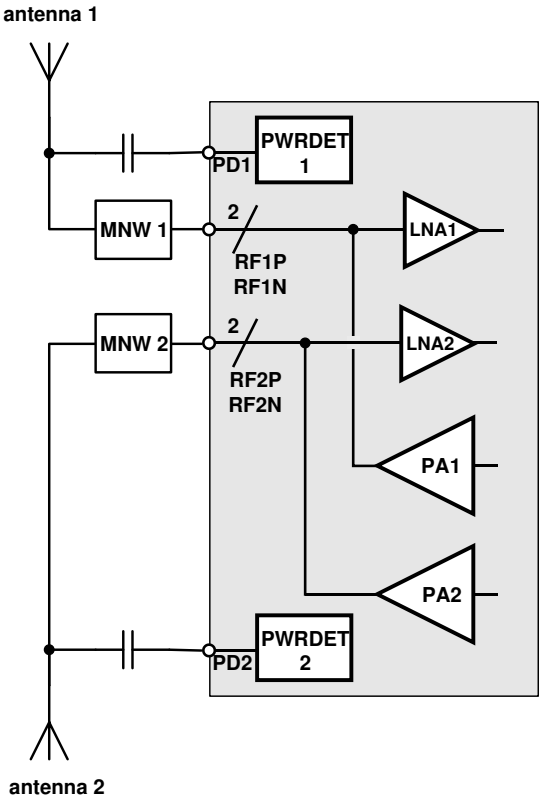

Figure 7

9.4.2. Frequency Synthesizer

At the analog heart of the RF transceiver is a frequency synthesizer based on a Sigma-Delta fractional-N PLL. From a typical 32MHz crystal reference clock, the PLL derives a quadrature LO-signal used for the mixers in the receive mode and to generate the carrier frequency in transmit mode. The PLL division ratio consists of a 6-bit integer part and a 19-bit fractional part, yielding to a resolution of 60Hz. The VCO of the PLL requires to be calibrated; for this purpose a calibration algorithm is implemented in the digital domain of the MLX73290-M device.

9.4.3. Transmit Mode (TX)

In RF transmit mode, the MLX73290-M outputs a CW signal on the two differential RF outputs RFP and RFN. The output power of the two PAs can be configured from -20dBm to 13dBm by the control bits RFTX_PWR1 and RFTX_PWR2 with the following tuning range:

- bits [7:6] for selecting the output stages 1 to 4,
- bits [5:3] for selecting the octave range (octave 000 = power OFF, 111 = power saturation),
- bits [2:0] for linear power tuning.

The frequency of the CW signal can be adjusted with the bits CENTER_FREQ[24:0] according to the formula below.

$$f_{RF} = \frac{f_{XTAL} \cdot CENTER_{FREQ[24:0]}}{2^{19}}$$

The RF transmit band has to be selected accordingly with the bits BAND_SEL[1:0].

A packet handler reads data stored into the RFTX_FIFO to construct an RF packet including the programmable preamble, the synchronization word, a fixed or variable length of payload (up to 255 bytes), an optional address byte, and an optional CRC-16 checksum inserted at the end. The serializer block supports the specific data formats of IEEE 802.15.4 and DASH7 mode 2. The bit order (LSB or MSB first) and bit polarity are configurable. After optional data whitening and Manchester encoding, the data stream of the serialized RF packet enters the OOK or FSK modulator.

In case of OOK modulation, the PLL-based frequency synthesizer is programmed to the wanted carrier frequency and the power amplifier (PA) is switched ON and OFF.

In case of FSK modulation, the data stream is converted to a frequency deviation programmable between 0 and 125 kHz. The FSK signal directly modulates the PLL of the frequency synthesizer.

For both OOK and FSK modulation, the data stream can be selected with optional Gaussian pulse shaping (EN_GAUSSIAN) to reduce the spectral bandwidth of the transmitted RF signal.

9.4.4. Receive Mode (RX)

The receiver chain features an IQ receiver topology. The RF signal is converted to the low IF band by an image reject mixer (the IF is at 500kHz). In order to address a wide dynamic range, the LNA as well as the programmable gain amplifier (PGA) conditions the IF signal. An automatic gain control loop ensures a stable signal level at the

input of the ADC which translates the signal to the digital domain. The base-band signal path features digital channel filtering, demodulation and extraction of clock and data. A de-serializer is used for extracting the payload from an incoming packet and it writes the payload to a FIFO that can be read out by the SPI.

A packet handler scans the demodulated signal for valid bit pattern followed by a programmable synchronization word of 16, 24 or 32 bits (SYNC_WORD[31:0] and SYNC_WORD_LEN[1:0]) and a fixed or variable length of payload (RFRX_FIFO of up to 255 bytes). An optional de-whitening operation as well as CRC-16 checksum verification could be enabled to reduce the load of the external host microcontroller.

9.4.4.1. Automatic Receiver Polling

With the bits POLL_RFRX and EN_POLL, the MLX73290-M can be configured in automatic polling mode, using a programmable interval based on a 16-bit timer clocked with the internal calibrated RC oscillator (typ. At 15.6kHz), pre-scaled by a binary power of 2^{15} giving a maximum interval of 38 hours.

At the end of the waiting periods, the timer restarts and sets the corresponding IRQ flag TMR_FLAG, the MLX73290-M is set in receiver mode looking for a valid synchronization word (SYNC_WORD[31:0]), during a certain time, as defined in the State Machine sec. below. The RX period might be preceded by periodic recalibration as configured by CALIB_MODE. The RF state machine will eventually return to its stopped (idle) state after completion of the task (e.g. packet received) or when an error occurs (e.g. RX termination timer expires, PLL out of lock, FIFO overrun etc.). In the meantime, the polling timer continues to run, so the polling grid is in no way affected by how long it takes the RF transceiver to return to its idle state. This is important for RF protocols with beacons or timeslots at fixed intervals.

The following picture shows the basic functionality of the RF polling feature.

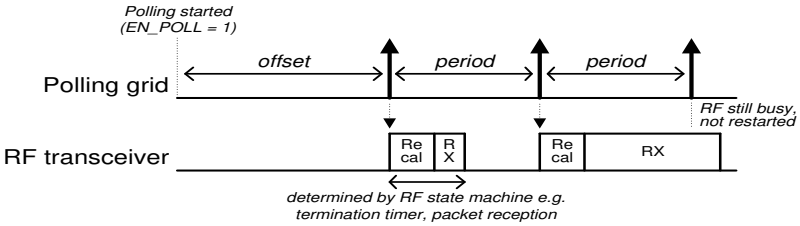

Figure 8: RF self-polling grid

The offset and polling period are configured with the registers POLL_EXP[4:0], POLL_OFFSET[15:0] and POLL_PERIOD[15:0] according to the following formulas:

$$Offset = \frac{2^{(11+POLL_{EXP})} \cdot (1 + POLL_{OFFSET})}{f_{XTAL}} [sec]$$

$$Period = \frac{2^{(11+POLL_{EXP})} \cdot (1 + POLL_{PERIOD})}{f_{XTAL}} [sec]$$

9.4.4.2. RSSI Information

RSSI information is available for the user in the register RSSI_HDR[6:0] which contains the RSSI information measured just after a valid Header is detected.

9.4.4.3. Carrier Frequency Acceptance Range

With its carrier recovery feature the MLX73290-M is able to tolerate a carrier frequency range of up to ±2·DR, with DR being the raw data rate. The carrier frequency acceptance range (CFAR) does not depend on the AFC setting. The AFC just enables the carrier recovery to converge packet after packet to a given value. This potentially allows the preamble length to be reduced, if losing a few packets at the beginning is tolerated.

Fig. 9 illustrates the packet error rate (PER) vs CFAR. The example here is given for DR = 55.6kbps with a ±50kHz FSK modulation. As can be seen, that there is a tradeoff between the preamble length (which is the part of the packet during which the carrier recovery tries to converge) and the PER.

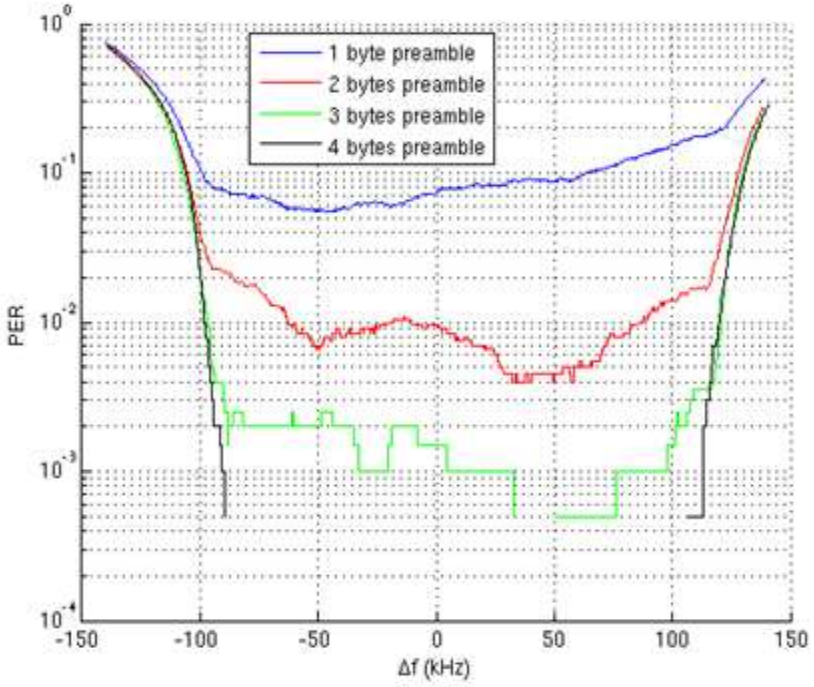

Figure 9: CFAR (Δf) at different preamble lengths

9.4.5. State Machine

The RF state machine supports a wide range of autonomous operations requiring little or no MCU overhead.

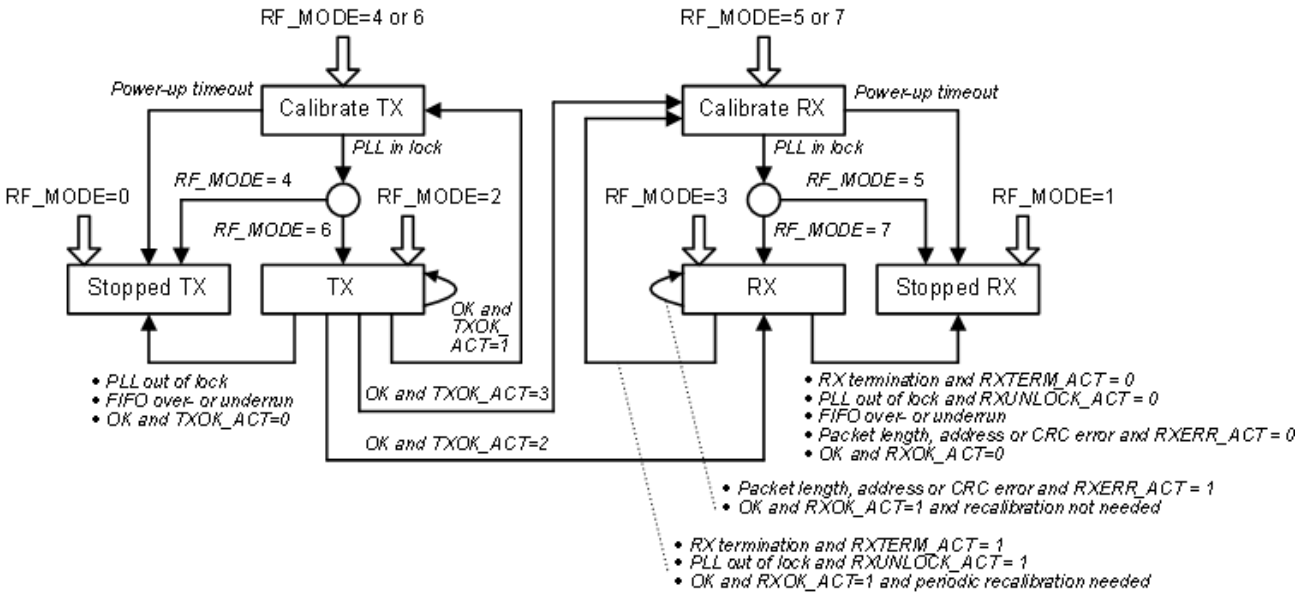

Figure 10: RF state machine flow chart

To request a state change, the host MCU will write to the flag RF_MODE[2:0]:

- Calibrate TX/RX, then stop : to perform just a VCO calibration and nothing more
- Calibrate RX, then RX : to calibrate the VCO, then start reception
- RX waiting for header : to start reception, skipping the VCO calibration
- Calibrate TX, then TX : to calibrate the VCO, then start transmission
- TX transmitting payload : to start transmission, skipping the VCO calibration
- Stopped RX/TX : to abort any operation and return to the idle state

While writing to RF_MODE, the host MCU may also write a 0 to the RFTXFIFO_USE and RFRXFIFO_USE flags in the same register to clear the RF TX and/or RF RX FIFOs.

In receive mode, the MLX73290-M first waits for a matching synchronization word defined in registers SYNC_WORD[31:0], then move to the “RX receiving payload” state and start the reception of the payload. When the entire packet has been received, the RF_RXFLAG flag will be set, and the state machine will take the action selected by RXOK_ACT: it will stop, or resume RX after periodic recalibration as configured by CALIB_MODE (please refer to section Automatic Polling Mode).

After successful reception, the MCU can read RSSI_HDR[6:0] and AFC_HDR[6:0] to obtain the RSSI and AFC values that have been measured during the reception of the packet (just after the SYNC_WORD). It may also read the TMR_HDR[15:0] to determine how much time has elapsed since the start of the received packet after the

SYNC_WORD detection, which is particularly useful in slotted protocols, where the next transmission or reception should start at a certain distance relative to the beginning of the received packet.

If a CRC and/or address check is enabled, and the packet gets rejected on that basis, RXERR_ACT will determine whether the state machine will stop and report a CRC or address error, or flush the RF RX FIFO and resume the reception.

Furthermore there is the option to set a threshold RX_RSSI_TH on the RSSI, below which reception is inhibited, and there is a termination timer programmable between 64µs and 32s (RXTERM_MANT[3:0] and RXTERM_EXP[3:0]). When the timer expires, termination may be postponed while RSSI is above the threshold, or while payload is being received, depending on the setting of the bit RXTERM_COND. Then the state machine will take the action selected by RXTERM_ACT: it will stop or recalibrate and resume reception.

When the PLL gets out of lock, depending on RXUNLOCK_ACT the state machine will stop and report a PLL out-of-lock error or it will take the same actions as for termination. When there is an overrun/underrun on the RFRXFIFO, the state machine will stop and report a FIFO overrun/underrun error (RFRX_FIFO_USE) which can also be output on one GPIO.

Important Note: *To enable the RF RX functionality, the register RF_BIAS[7:0] in Bank 0 has to be set to 0x4C for the 315MHz band, to 0x63 for the 433MHz band and to 0x99 for the 868MHz and 915MHz bands.*

In transmit mode, after transmission of the payload, the state machine will, depending on TXOK_ACT, stop, resume TX after periodic recalibration as configured by CALIB_MODE, or, after optional calibration, enter RX mode.

When DIRECT_MOD > 2 direct modulation with a fixed logic 0 or 1 level, or from one of the GPIO digital input pins is selected. In this case the data-handler is bypassed and it is the responsibility of the microcontroller to terminate the transmission by changing RF_MODE. This mode will allow for the transmission of un-modulated as well as modulated carriers for characterization, test and type approval. A clock at the programmable symbol rate can be output on one of the GPIO pins for transmission of a synchronous bit stream.

When the PLL gets out-of-lock during transmission, the state machine will always abort and report a PLL out of-lock error (PLL_LOCKED). When there is an overrun/underrun on the RFTXFIFO, the state machine will stop and report a FIFO overrun/underrun error (RFTX_FIFO_USE).

By putting KEEP_PLL_ON to ‘1’, the PLL can be kept running regardless the state of the RF transceiver, this is particularly useful for protocols where transmission or reception is triggered by an event and the normal startup delay of the PLL cannot be tolerated.

9.5. Modulation Settings

The below table provides an overview on the modulation settings. Continuous modulation can also be applied through the GPIOs. In this case the selected GPIO pin must be set as a digital input.

Modulation	mod_source	FSK/OOK	Manchester	Data-whitening	Comment
Continuous wave	Fixed logic 1	OOK	disable	disable	
Continuous modulation FSK Manchester	Fixed logic 1 or Fixed logic 0	FSK	enable	disable	
Continuous modulation FSK data whitening	Fixed logic 1 or Fixed logic 0	FSK	disable	enable	
Continuous modulation FSK GPIO	GPIO 0 GPIO 1 GPIO 2 GPIO 3	FSK	enable or disable	enable or disable	refer to sec 5.12 for GPIO input selection
Continuous modulation OOK Manchester	Fixed logic 1 or Fixed logic 0	OOK	enable	disable	
Continuous modulation OOK data whitening	Fixed logic 1 or Fixed logic 0	OOK	disable	enable	
Continuous modulation OOK GPIO	GPIO 0 GPIO 1 GPIO 2 GPIO 3	OOK	enable or disable	enable or disable	refer to sec 5.12 for GPIO input selection

9.6. Packet Handler

The MLX73290-M embeds a packet handler mechanism for managing the encoding/decoding of the transmit/receive bytes contain in the RF FIFO. Different frame formats are supported and can be fully configured by the user. Figure 9 shows the different frame formats supported in transmit and receive modes.

The packet handler is enabled with the bit **en_packet** in transmit mode and with the bit **en_deserializer** in receive mode. Both bits are available in registers 0x18 and 0x27, respectively.

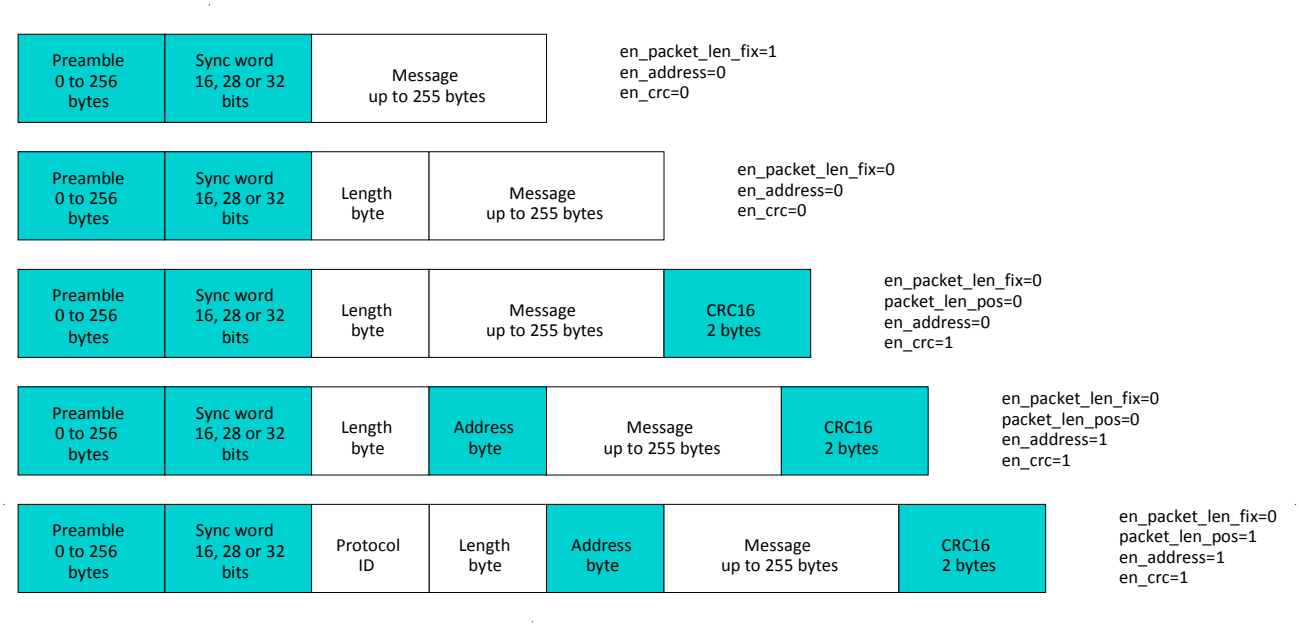

Figure 11: Packet handler - frame formats

9.6.1. Preamble

A preamble can be automatically added to the packet structure even if it is completely handled by the host MCU. This feature can be turned on by simply setting the bit **en_preamble** signal to 1. The length of the preamble is given by the signal **pattern_world_len[1:0]** (number of times that the preamble byte is repeated) and the preamble itself is given by the **preamble[7:0]** in bank 0 (by default to 0x55).

9.6.2. Sync Word

The synchronization word is introduced automatically if the preamble is present. The length of the sync word is given by the **sync_word_len**. The synchronization word is always sent LSB first.

9.6.3. Packet Length

If the packet handler is enabled, it has to know the length of the packet to be sent/received. This one can be fixed or variable depending on the user settings. If the fixed solution is chosen, the **en_packet_len_fix** has to be set to 1. In this case the length of the packet is given by the byte **packet_len[7:0]**.

In the case of a variable packet length (**en_packet_len_fix** set to 0), the length is normally specified as one of the first bytes of the packet. The byte **packet_len_pos[1:0]** specify the position of this byte (e.g. if set to 0, means that the first byte sent/received is defining the packet length).

The packet handler always considers the length of the packet from the first byte after the packet length byte until the last byte before the CRC. The bit **packet_len_corr** specify the correction to apply to the packet length. This gives the possibility for the user to provide/receive frame format with a length byte including itself and/or is included in the CRC computation.

The following picture shows the **packet_len_corr** principle.

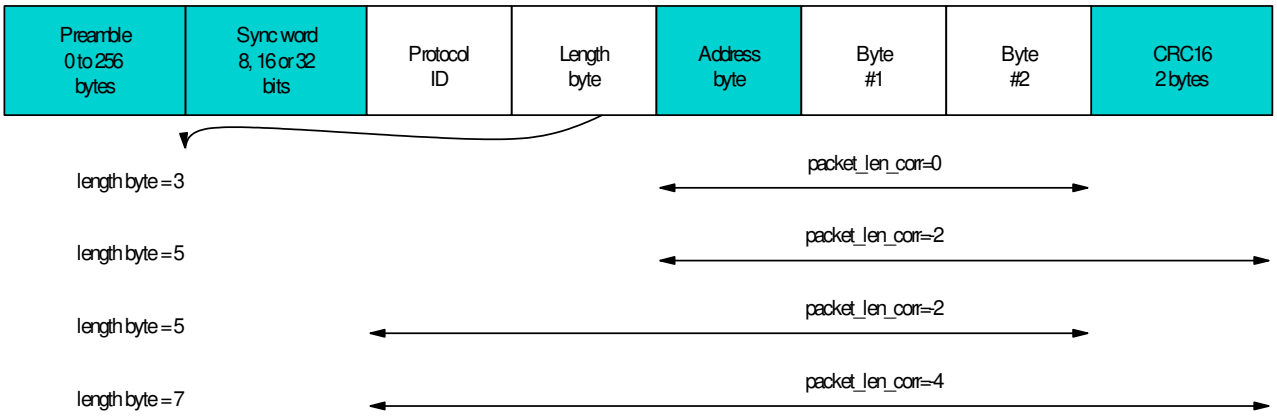

Figure 12: Packet handler - packet correction principle

9.6.4. Address

An address can be inserted automatically after the packet length if the bit **en_address** is set to 1. The address is given by the byte **address[7:0]**.

9.6.5. CRC16

A checksum CRC16 can be automatically computed and added/compared to the packet sent/received, by setting the bit **en_crc** to 1. In case of reception, the status bits **rfrx_flag** and **rf_info[2:0]** will be automatically updated in case of CRC error.

9.6.6. Multi Frame

If the **en_multi_frame** bit is set to 1, the multi-frame mode is enabled. A frame is composed by the data and the corresponding CRC. In this mode, a preamble and a single synchronization word are followed by multiple frames. As long as the **en_multi_frame** bit is set to 1, the packet handler continues to send/receive frames.

5.5.7 Data Whitening

The packet handler also includes a data whitening process during the transmission or the reception of RF packets. In this case, all the data to be sent/received are encoded/decoded using a PN9 polynomial of X^9+X^5+1. The data-whitening process is illustrated in the picture below. The data whitening process is enabled with the bit **en_white**.

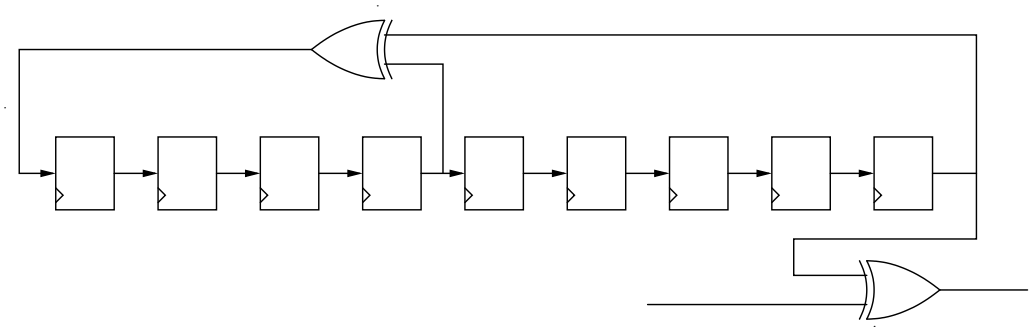

Figure 13: Packet handler – frame data whitening PN9 structure

9.7. Power Management and Energy Harvesting

The power management unit of the MLX73290-M is performing the following operations:

- It measures the battery voltage (VDDA3) at power-on reset (POR) and decides whether the voltage is sufficient to power up the MLX73290-M and to supply the host MCU through pin VMAIN (if ≥ 2.1V).
- If the measured voltage at VDDA3 is below the threshold level (of approx. 2V) then pin VHARV is used to supply the MLX73290-M and the host MCU.
- After power-on, the internal power switch is locked to avoid switching back and forth between modes.
- When the IC is running, the power switch can still be controlled via the SPI to select the supply source between VHARV or VDDA3 (Register 0x0C of Bank0).
- The status of the power management state machine can be queried via SPI (Register 0x03 of Bank0).
- The voltage at VHARV can be read via the general purpose ADC.

Different monitoring blocks are used to report the status of the internal and external voltages, and to keep the digital control blocks in reset mode as long as the supply voltage has not reached a sufficient value:

Power-on reset (POR): This block is to maintain the digital circuitry in reset mode as long as the supply voltage is below a certain level at start-up. When the supply voltage is sufficient, the reset mode is deactivated after a certain delay, which has to be sufficient to ensure correct internal state. While this is not a monitoring function per se, the state of the reset signal gives an indication as to when the supply voltage has reached the necessary level for the digital functionalities to work properly (meaning mainly that the configuration registers are able to retain their state).

Brownout detector (BOD): Detects when the supply voltage drops below a certain threshold, even momentarily. The threshold should correspond to a voltage below which the digital functionalities cannot be guaranteed. The threshold crossing is detected without great precision but with a very low-power consumption (less than 100nA). This monitoring block is mainly intended to be used for brownout detection when the overall power consumption is of key importance so that the band-gap voltage reference cannot be used.

Low-battery detector (LBD): Uses the band-gap reference voltage to detect whether or not the external battery voltage is above or equal its specified minimum level of 2.1V.

9.8. Programmable Timer / Clock Generator

A programmable timer / clock generator may periodically wake up the host MCU or it can provide a clock signal, derived from the RC oscillator, the calibrated RC clock or the crystal clock. A prescaler first divides the selected clock source by a programmable binary power between 1 and 231, and then by an 8-bit linear division ratio between 1 and 256.

The timer period is configured with the bits TMR_MANT[7:0] and TMR_EXP[4:0]. The following formula can be used to calculate the timer period, relative to the clock source selected by the bits TMR_SOURCE[1:0]:

$$TMR_{PERIOD} = \frac{(TM_{MANT} + 1) \cdot 2^{TMR_{EXP}}}{f_{SOURCE}} \text{ [sec]}$$

The timer can be selected in Timer or Clock mode with the bit TMR_MODE. In Timer mode, the timer stops when the flag gets set, and the MCU must clear the flag to restart the timer. In Clock mode, the timer is continuously running thus providing a reference clock for the host MCU.

The timer is, by default configured to output the RC oscillator clock signal on GPIO2 without any division (i.e. ratio 1:1) so that it may act as a clock signal for the MCU. There is also the possibility to configure the timer output to another GPIO.

For more information about the programmable timer, please refer to section **10.4**.

9.9. System Timer

The MLX73290-M embeds a 23-bit free-running counter that can serve as a time reference. When enabled, it increments at 7.8 kHz derived from the calibrated RC clock. Counter overflows (every ~18 minutes) will set a flag, which may wake-up the microcontroller. The firmware can then clear the flag and increment a counter in the microcontroller to extend the counter range to any length. To determine the elapsed time between two events, take a snapshot of this free-running system time at both moments and subtract these two values to find the elapsed time with 128 µs resolution.

For more information about the system timer, please refer to section **10.4**.

9.10. General Purpose ADC

The external host MCU can use a built-in 10-bit general purpose ADC to measure several internal signals selected with the bits ADC_CH_SEL[3:0] (e.g. supply voltages, output of the RF power detectors, 3D LF field strength, temperature sensor, analog level of one of the GPIO pins). The ADC can be configured for continuous sampling or a single measurement (ADC_CONTINU bit set).

The conversion clock can be set to 1/16th, 1/32nd or 1/64th of the crystal clock (ADC_CLK_SEL[1:0]), corresponding to a period of conversion of respectively t_{AD} = 0.5, 1 or 2 µs with a 32MHz crystal. A full conversion cycle takes 128 clocks leading to a conversion time of 64, 128 or 256 µs, resulting in 16, 8 or 4 kS/s throughput.

The conversion is started with the bit ADC_START_EOC and the result stored into the register ADC_CAL[9:0]. Since the conversion results are 10 bit wide, the microcontroller will need to read them as 2 bytes through the SPI interface. This is an asynchronous process, so when the ADC operates in continuous sampling mode, the

completion of a new conversion may coincide with the retrieval of the 2 bytes of the results of the previous conversion. Without special provisions the microcontroller may receive the first byte of the old conversion and the second byte of the new conversion, which could give a false reading. To prevent such inconsistencies, the generic ADC therefore takes a snapshot of the conversion results when the first byte is read, and returns the second part of the snapshot when the second byte is read in the same (burst mode) read access.

The generic ADC maintains a flag, ADC_NEWDATA, to indicate whether new results are available, primarily intended for continuous sampling mode. The completion of a conversion will set the flag, and reading the first byte of the results will clear the flag. The microcontroller may poll this flag to check if a new sample is available, and if so, it may continue reading the two byte result, which will clear the flag.

9.11. SPI Communication

The serial programming interface (SPI) is composed of three inputs and one output as shown in the following table.

SPI pin	I/O	Description
CS	input	SPI Chip Select active high
SDO	output	SPI Slave data output
SDI	input	SPI Slave data input
SCK	input	SPI Clock

The SDO pin is set high impedance by the MLX73290-M when not transmitting SPI information; this allows a configuration using only one pin to successively send/receive information from/to the MLX73290-M. The two configurations using classical 4-pin and optimized 3-pin are illustrated below:

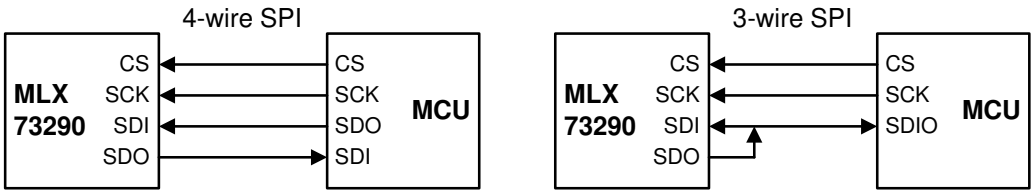

Figure 14: SPI connections

In Read mode, the serial data changes on the falling edges of the serial clock and is latched, during write mode, on the rising clock edges. Data are transmitted MSB first.

Opposite to most conventional SPI devices, the CS chip select input of the MLX73290-M is active **high**. When the CS is set low, the MLX73290-M is deselected as SPI-slave; SCK and SDI can take any level, and SDO is tri-state. When CS goes high, the MLX73290-M becomes selected, and expects from the host MCU, a 7-bit register address preceded by one bit of direction (0 = write, 1 = read).

A so-called Burst mode is implemented in the MLX73290-M which automatically increment the address of the current register to be read/write. This operation is illustrated in the picture below:

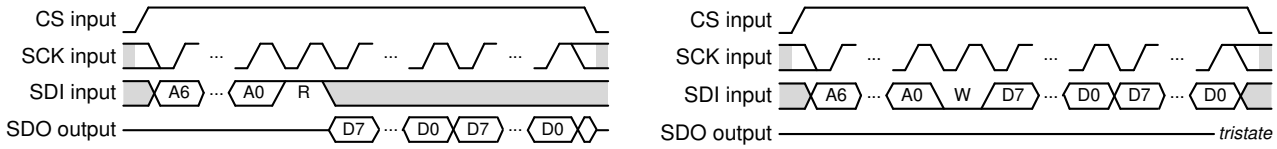

Figure 15: (burst) read/write SPI

The picture above is valid to address standard registers. To address the specific Bank0, the following procedure should be followed.

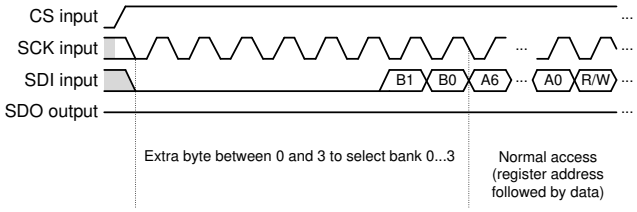

Figure 16: Specific access to Bank0 register

9.12. GPIO Pins

Four general purpose I/O (GPIO) pins are available in the MLX73290-M (GPIO0 to GPIO3). Several digital signals can be output, e.g. to be further used by the host MCU. Each GPIO pin has an 8-bit GPIO*x*_CH_SEL[7:0] setting that configures the I/O type of the corresponding pin (analog/digital, in/output) and the signal routing to/ from the pin.

GPIO*x*_ CH_SEL [7:0]	Signal	I/O type
x0000000	Disabled	Disabled
x0000001	GPIO*x*_Y with pull-down	Digital input
x0000010	GPIO*x*_Y with pull-up	Digital input
x0000011	GPIO*x*_Y	Digital input
x000010x : x0000110	*Reserved*	Disabled
x0000111	Internal analog line, pulled down	Analog I/O
x0001000 : x0001011	*Reserved*	Analog I/O
x0001100	PD1	Analog I/O
x0001101	PD2	Analog I/O
x0001110	TEMPSENS	Analog I/O
0001xxxx	See table 10, signal level	Push-pull digital

001xxxxx 01xxxxxx	inverted when GPIO*x*_CH_SEL[0] = 1	output
1001xxxx 101xxxxx 11xxxxxx	See table 10,signal level inverted when GPIO*x*_CH_SEL[0] = 1	Open collector digital output

The default values of GPIOs after power-on reset (POR) are:

- GPIO0 : READY
- GPIO1 : READY_NOT
- GPIO2 : TMR_FLAG
- GPIO3 : BATTOK

The digital signals are active high (unless otherwise specified). For GPIO*x* as digital output, the following truth table applies:

GPIOx_CH_SEL[6:1]	Signal Name	Description
001000	Fixed logic 0	
001001	READY	MLX73290-M is ready after start-up sequence (POR)
001010	BATTOK	Battery level measured above the minimum level 2.1V.
001011	RCO	Output of un-calibrated internal RC oscillator
010100	LOWBAT	Output of low battery detector on VDDA3
010101	XTAL_RDY	Crystal clock is present and stable
011000	ADC_NEWDATA	New result from general purpose ADC available
011001	SYS_TIME_OVF	Internal system timer overflow
011010	TMR_FLAG	Programmable timer flag
011011	POLL_FLAG	RF Polling timer flag
011100	PLL_CYCLE_SLIP	A PLL cycle-slip has been registered since the last read from this register
011101	PLL_IN_LOCK	PLL successfully locked
011110	RFRX_CLK	RF Clock output after data-handler
011111	RFRX_DATA	RF Data output after data-handler
100000	RFRX_WAIT_HDR	RF state-machine waiting for valid Header
100001	RFRX_PAYLOAD	RF state-machine receiving the payload
100010	RFRX_WAIT_HDR_PAYLOAD	RF state-machine waiting for valid Header or receiving Payload
100011	RFTX_PAYLOAD	RF state-machine transmitting payload
100100	RF_STOPPED	RF state-machine stopped (RX or TX)
100101	RF_STOPPED_ERR	RF state-machine stopped with an error (RX or TX)