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MLX75123 Time-of-Flight Companion Chip

Datasheet

Features & Benefits

- Combines four high speed ADCs with a digital sensor control for Melexis' TOF camera sensors
- Integrated light source control with modulation frequencies between 12-40 MHz
- Programmable modulation frequencies to avoid module to module crosstalk
- Up to 8 raw phases per frame
- Pre-processed difference & sum output modes to reduce the data bandwidth
- Continuous or triggered operation modes
- Configurable over I^2C up to 400kHz
- 12-bit parallel camera interface up to 80Mpix/s
- Region of interest (ROI) selection
- Horizontal & vertical flip/mirror modes
- Per-phase statistics & diagnostics
- Ambient operating temperature ranges of -20 +85°C and -40 +105°C
- AEC-Q100 qualification available!

Description

MLX75123 is a fully integrated companion chip for Melexis' Time-of-Flight (TOF) sensors. It's perfectly suited for automotive and non-automotive applications, including, but not limited to, gesture recognition, driver monitoring, skeleton tracking, people or obstacle detection and traffic monitoring. This sensor interface is designed to connect instinctively to any Melexis TOF sensor and the output can be directly connected to a camera parallel port and I^2C interface of a microcontroller. The chip features a configurable sequencer to control the TOF sensor and will sequentially provide the 12-bit output data from its four built-in high-speed ADCs for an accurate analog to digital conversion. Furthermore, MLX75123 synchronously provides the control signals for a modulated light source (LED or laser based). Combined with a TOF sensor like MLX75023, the MLX75123 offers a cost-effective, integrated, QVGA (320x240) pixel resolution camera solution. This chipset can deliver raw TOF data up to 600 frames per second. The device is available in a compact 7x7mm AQFN package and offers a variety of integration possibilities.

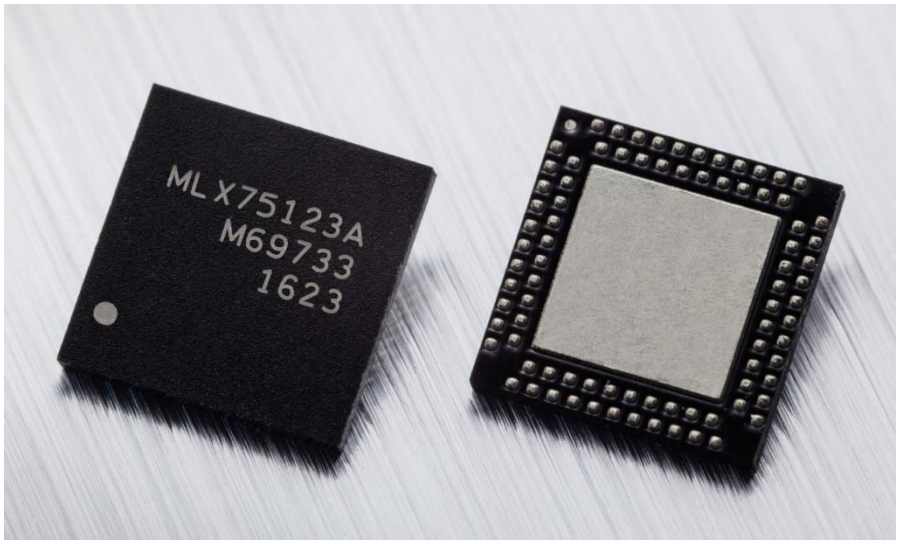


Figure 1 : MLX75123 package

Contents

1. Datasheet Changelog

Version	Date	Changes
1.0	17.01.2017	Initial version
1.1	11.04.2017	Updated section 13.3 : USER[0..3] are visible in Metadata1, not MetaData2 Updated section 7.1 : Clock thresholds depend on VDDD_1V8, not VDD_IO Updated section 13.1 : VIDEO_DRIVE has 2 options (low & high), not 16 Added and updated electrical operating conditions in section 7.2 Updated the power consumption values from section 8 Changed BLOCK_ENABLE register to BLOCK_DISABLE in section 16
1.2	02.08.2017	Added LEDP specifications for single ended mode Updated description of parameters in section 7.2 Updated default register values in section 13 Minor updates to register descriptions Updated default register values from chapter 13
1.3	31.01.2018	Updated ordering information in section 2 Updated description of I2C_SAVEREGMAP in section 12.5 Corrected calculation method for distance & amplitude in section 11 Update footprint recommendations in section 19.1 Several other minor description updates
1.4	23.3.2018	Removed Tx_Py_SETUP registers (not needed for application) Updated Tx_Py_SETTINGS bit[6] value to fixed high Added phase read out calculation Updated multiple register descriptions

Table 1 : Datasheet changelog

2. Ordering Information

Product	Temperature Code	Package	Option Code	Packing Form
MLX75123	R	LA	ABA-000	RE or SP
MLX75123	S	LA	ABA-000	RE
MLX75123	R	LA	BAG-000	RE
MLX75123	S	LA	BAG-000	RE

Table 2 : Order code(s)

Legend:

Temperature Code	R : -40°C to 105°C S : -20°C to 85°C
Package Code	LA : Array QFN package, 84pins
Option Code	ABA-000 : Default product configuration BAG-000 : Samples available in Q3 2018
Packing Form	RE : Reel SP : Sample pack (10 pcs)
Ordering Example	MLX75123RLA-ABA-000-RE

Table 3

3. Application System Architecture

A complete TOF system or camera module typically includes the following main components:

- MLX75123 + MLX75023 TOF chipset
- A synchronized high bandwidth near infrared (NIR) active illumination source (LED or laser)
- Beam shaping optics for the light distribution
- A receiving sensor lens, optimized for maximum NIR transmittance
- A microprocessor (like Freescale i.MX6 or equivalent) or DSP to calculate and process all data

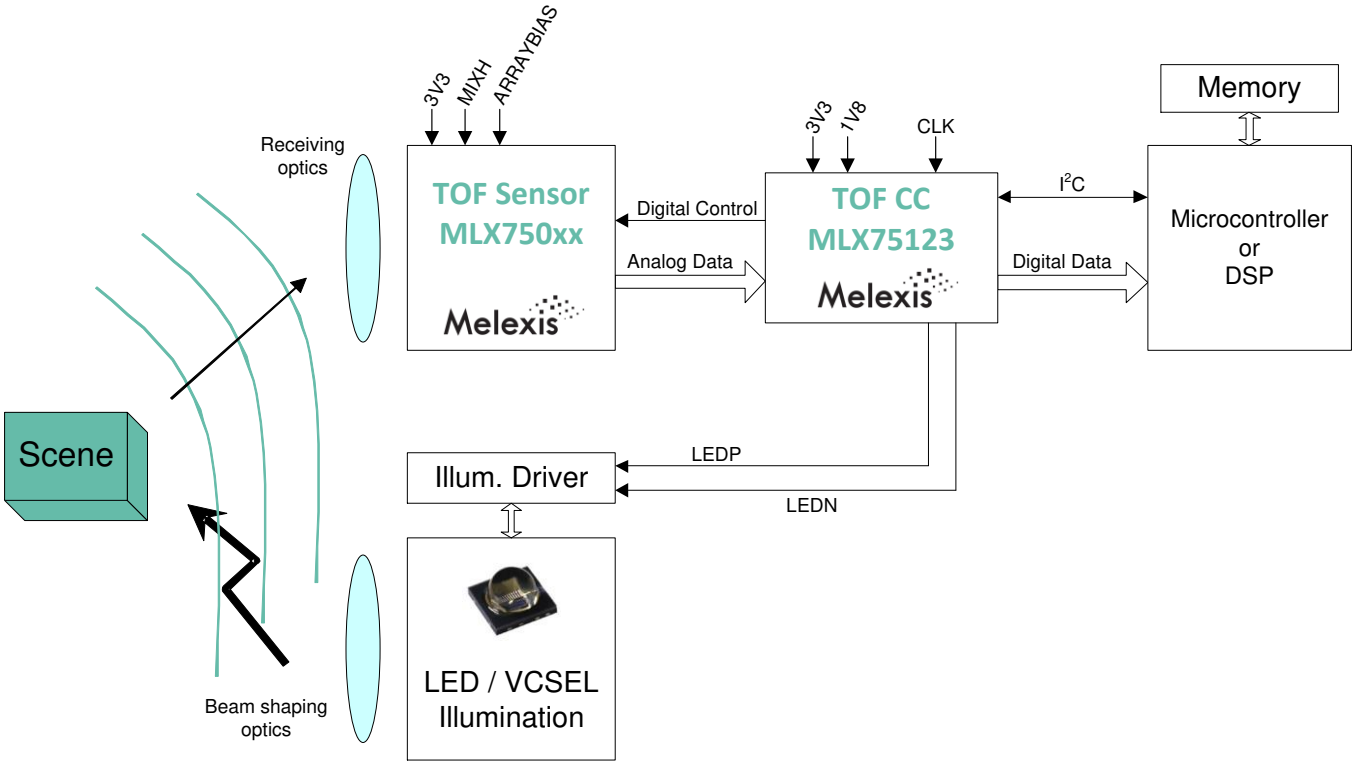


Figure 2

4. System Block Diagram

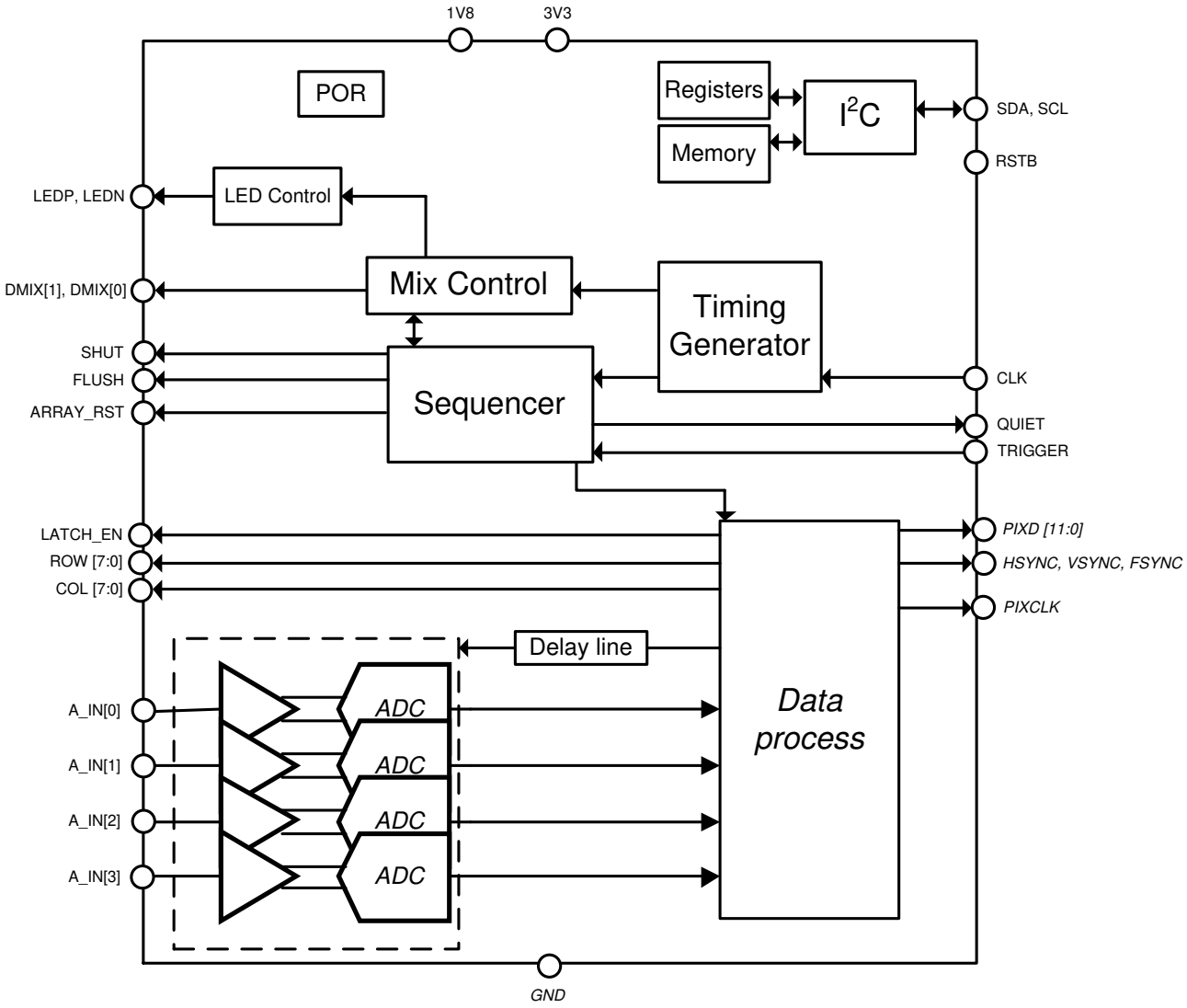


Figure 3 : System block diagram

5. Pinout Description

Designator	Pin #	Function	Description	Domain
PIXCLK	B28	Digital Out	Pixel clock	VDD_IO
HSYNC	B29	Digital Out	Horizontal sync bit	VDD_IO
VSYNC	A32	Digital Out	Vertical sync bit	VDD_IO
FSYNC	A31	Digital Out	Frame sync bit (optional)	VDD_IO
PIXD[11] PIXD[10] PIXD[9] PIXD[8] PIXD[7] PIXD[6] PIXD[5] PIXD[4] PIXD[3] PIXD[2] PIXD[1] PIXD[0]	B22 A25 B23 A26 B24 A27 B25 A28 B26 A29 B27 A30	Digital Out	Pixel data	VDD_IO
QUIET	A15	Digital Out	Configurable indication output	VDD_IO
CLK	B13	Digital In	Input clock	VDD_IO
TRIGGER	A13	Digital In	Frame trigger (= active high)	VDD_IO
RSTB	A14	Digital In	Reset pin (= active low)	VDD_IO
SDA SCL	B11 A12	Digital Out Digital In	I^2C clock and data	VDD_I2C
LEDP LEDN	B31 A34	Digital Out	Single ended or differential LED control signal	VDDD_3V3
DMIX[1] DMIX[0]	B32 A35	Digital Out	Differential pixel modulation signals	VDDD_3V3
LATCH_EN	A4	Digital Out	Pixel array latch enable	VDDD_3V3
SHUT	B2	Digital Out	Pixel array shutter	VDDD_3V3
ARRAY_RST	A3	Digital Out	Pixel array reset signal	VDDD_3V3
FLUSH	B3	Digital Out	Pixel array flush output	VDDD_3V3
ROW[7] ROW[6] ROW[5] ROW[4] ROW[3] ROW[2] ROW[1] ROW[0]	A2 B1 A1 A44 B40 A43 B39 A42	Digital Out	Row addressing	VDDD_3V3
COL[7] COL[6] COL[5] COL[4] COL[3] COL[2] COL[1] COL[0]	A37 B34 A38 B35 A39 B36 A40 B37	Digital Out	Column addressing	VDDD_3V3

Table 4.1

[1] can be selected as active high or active low

Designator	Pin #	Function	Description	Domain
A_IN[3] A_IN[2] A_IN[1] A_IN[0]	B7 A7 A6 B6	Analog In	Analog input of the pixel data	
VDDA_1V8	B14	1V8 Supply	Analog supply in the 1.8V domain for the PLL (referenced to GNDA_1V8)	
VDDA_ADC_1V8	A9 B5	1V8 Supply	Analog supply for the ADC in the 1.8V analog domain (referenced to GNDA_ADC_1V8)	
VDDA_ADC_S_1V8	A10	1V8 Supply	Analog supply for the ADC in 1.8V analog domain for switched circuitry (referenced to GNDA_ADC_S_1V8)	
VDDD_1V8	B20	1V8 Supply	Digital supply in 1.8V digital domain (referenced to GNDD_1V8)	
VDDA_3V3	B4	3V3 Supply	Analog supply for the ADC in the 3.3V analog domain (referenced to GNDA_ADC_1V8)	
VDDD_3V3	A36 B17 B38	3V3 Supply	Digital supply in 3.3V digital domain for the interface with the 75023 (referenced to GNDD_1V8)	
VDD_IO	B21 B30	Supply	Supply pin for interface to application processor (1.8 or 3.3V) (referenced to GNDD_1V8)	
VDD_I2C	B12	Supply	1.8 or 3.3V supply for I2C interface (referenced to GNDD_1V8)	
GNDA_1V8	A16	GND	Analog ground in the 1.8V domain for the PLL	
GNDA_ADC_1V8	A5 B8	GND	Analog ADC ground for 1.8V	
GNDA_ADC_S_1V8	B9	GND	Analog ADC ground for the ADC in 1.8V analog domain switched	
GNDD_1V8	A22	GND	Digital ground in 1.8V digital domain	
GND_IO	A8 B15 A18 A24 A33 B33 A41	GND	Digital ground for the interface to application processor	
TEST[6] TEST[5] TEST[4] TEST[3] TEST[2] TEST[1] TEST[0]	B10 A11 B16 A17 B18 B19 A21	GND	Test pins reserved for Melexis purposes, please connect to GND_IO. (version ABA-000) These pins will become general purpose outputs, controlled via I2C, in version BAG-000	
n.c.	A19 A20 A23		not connected	

Table 4.2

6. Absolute Maximum Ratings[1]

Parameter	Min.	Typ.	Max.[1]	Unit
3V3 supply voltage : VDDA_3V3, VDDD_3V3, VDD_IO, VDD_I2C	-0.2		4	V
1V8 supply voltage : VDDA_1V8, VDDA_ADC_1V8, VDDA_ADC_S_1V8, VDDD_1V8	-0.2		2.3	V
Analog input voltage A_IN[3], A_IN[2], A_IN[1], A_IN[0]	-0.2		VDDA_3V3 + 0.2	V
Digital IO voltage for MLX75023 : COL[x], ROW[x], DMIX[x], LATCH_EN, SHUT, ARRAY_RST, FLUSH	-0.2		VDDD_3V3 + 0.2	V
Digital IO voltage I2C	-0.2		VDD_I2C + 0.2	V
Digital IO voltage for video Interface : HSYNC, VSYNC, FSYNC, PIXCLK, PIXD[x], CLK, TRIGGER, RSTB	-0.2		VDD_IO + 0.2	V
Operating junction temperature	-40		125	°C
Storage temperature	-40		150	°C
ESD : Human Body Model			2	kV

Table 5 : Absolute Maximum Ratings

Note [1]: Absolute maximum ratings should never be exceeded to avoid permanent hardware failure.

7. Electrical Specifications

7.1. Crystal Oscillator Requirements

The clock input requires an accurate and clean input signal. It's recommended to use a crystal oscillator with the following specifications towards this purpose. The clock input ESD protection circuit limits the max. amplitude to VDD_IO+0.2V. This requirement excludes the combination of a 3V3 clock generator together with 1V8 for VDD_IO. The oscillator drift is a less significant parameter and will not impact MLX75123 behaviour because all timing related parameters scale directly with this clock.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency		40		80	MHz
Positive clock threshold	V_{TH+}	1		VDD_IO + 0.2	V
Negative clock threshold	V_{TH-}			0.6	V
Jitter			30	60	ps

Table 6 : Input clock requirements

7.2. Operating Conditions

The operation conditions of MLX75123 are highly dependent on the configuration of the device.
Values listed in the Table 7 are measured at typical application conditions[1] :

- 80 MHz input clock
- 20 MHz modulation frequency
- 250 us integration time
- Four phase acquisition
- 50 distance FPS (= 200 raw frames)
- ± 5pF load on all output buffers

Parameter	Min.	Typ. -40 °C[2]	Typ. 25 °C[2]	Typ. 105 °C[2]	Peak[3]	Max.[6]	Unit
1V8 analog supply voltage	1.7	1.8	1.8			2	V
VDDA_1V8 supply current		4.57	4.52	4.45		tbd	mA
VDDA_ADC_1V8 supply current [3]		39.60	42.44	46.39	221	tbd	mA
VDDA_ADC_S_1V8 supply current [3]		9.58	10.25	11.05	58	tbd	mA
1V8 digital supply voltage	1.7	1.8	1.8	1.8		2	V
VDDD_1V8 supply current		8.5	8.61	8.84		tbd	mA
VDDD_I2C supply current @1V8			n/A [4]			tbd	mA
VDDD_IO supply current @1V8 [3, 5]		16	16.18	16.43	39	tbd	mA
3V3 analog supply voltage	3	3.3	3.3	3.3		3.6	V
VDDA_3V3 supply current			0.001			tbd	mA
3V3 digital supply voltage	3	3.3	3.3	3.3		3.6	V
VDDD_3V3 supply current [3]		1.29	1.28	1.29	7.85	tbd	mA
VDDD_I2C supply current @3V3			n/A [4]			tbd	mA
VDDD_IO supply current @3V3 [3, 5]		37.09	36.47	37.34	37	tbd	mA

Table 7 : Power requirements

Note [1] : A power calculator that simulates the power consumption at different application parameters is available on request

Note [2] : Temperatures listed in Table 7 are ambient temperatures

Note [3] : Some power domains only work for a specific time (for example during sensor read out). The overall (or average) power consumption thus depends on the duty cycle of that domain, but the peak current determines the power supply requirements and decouple techniques. Please refer to chapter 14 for more information.

Note [4] : The power consumption of VDDD_I2C depends on the amount of communication between MLX75123 and the host controller. When the device is only initialized once at start up no further power will be consumed.

Note [5] : The average power consumption of VDDD_IO depends on the actual data content that is being transmitted. Values in Table 7 are considered worst case conditions because in our setup the PIXD lines are toggling heavily.

Note [6] : The max. current consumption measured at the max. supply voltage incl. process & temperature variation for typical application conditions.

Parameter	Min.	Max.	Unit
VDDD_1V8 power on reset (POR)	1.3 - 1.45	1.45 - 1.55	V
POR on/off hysteresis	100		mV

Table 8 : Power on reset behaviour

When VDDD_1V8 drops under its lower threshold the device will reset. To avoid unwanted behaviour on noisy power supplies the device will only turn on again when VDDD_1V8 reaches its upper threshold voltage level.
A hysteresis of min. 100mV over temperature variation is guaranteed.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction to ambient thermal resistance	θ_{JA}		22.18		°C/W
Junction to package resistance [1]	θ_{JC}, θ_{JB}		1.19		°C/W
Moisture sensitivity level (MSL) [2]			3		

Table 9 : Package thermal behaviour

Note [1] : For an AQFN package incl. thermal pad the thermal resistance junction-board is equal to resistance junction-package
Note [2] : According to IPC/JEDEC J-STD-020E moisture/reflow sensitivity classification

Parameter	Min.	Typ.	Max.	Unit
Modulation frequency	12		40	MHz
Modulation frequency duty cycle	12.5	50	87.5	%
Modulation frequency phase accuracy			1	%
Modulation frequency settling time		20	100	us

Table 10 : Modulation frequency parameters

Parameter	Min.	Typ.	Max.	Unit
Input frequency clock (F_{IN})	40	80	80	MHz
Pixel clock frequency (PIXCLK)		F_{in}		MHz
I^2C frequency (SCL)	20		400	kHz
I^2C sink strength (SDA)	3			mA
VDD_IO buffer sink strength [3] (measured @ 200mV)	8.2	17.2	118	mA
VDD_IO buffer source strength [3] (measured @ VDD_IO - 200mV)	5.03	9.37	40	mA
VDDD_3V3 buffer sink strength (measured @ 200mV)	16.2	26.9	37.2	mA
VDDD_3V3 buffer source strength (measured @ VDDD_3V3 - 200mV)	10.6	17	24.8	mA

Table 11 : IO interface description

Note [3] : Measured at VDD_IO = 1V8, the values depend on the selection of VIDEO_DRIVE .
VIDEO_DRIVE can be selected in register CONFIG (0x1004) as explained in section 13.1.
Typical values are with VIDEO_DRIVE at low drive strength, max. values are for high VIDEO_DRIVE setting.

Parameter	Min.	Typ.	Max.	Unit
LVDS mode : recommended load impedance		100		Ohm
LVDS mode : output current		3.5		mA
LVDS mode : common mode voltage		1.2		V
Single ended mode : LEDP buffer sink strength (measured @ 200mV)	16.2	26.9	37.2	mA
Single ended mode : LEDP buffer source strength (measured @ VDDD_3V3 - 200mV)	10.6	17	24.8	mA

Table 12 : LED_P & LED_N electrical description

7.3. ADC Characteristics

MLX75123 has four single, general purpose analog to digital converters. All ADCs are used in a single ended configuration and independently from each other convert one analog output from MLX75023. Each pipelined ADC consists of a concurrently operating series of stages, isolated by a sample-hold buffer. For sampling rates > 25 MSPS it is needed to optimize the sample point with register ADC_DELAY_FT as explained in section 13.1

Parameter	Min.	Typ.	Max.	Unit
ADC resolution		12		bit
ADC input range	0.2		1.9	V
ADC sampling rate	20	$F_{in}/2$	40	MSPS
ADC conversion gain		500		uV/LSB
ADC to ADC gain mismatch		2	5	%
Analog input capacitance DC		5		pF
ADC delay line number of steps		32		
ADC delay line step size		1	3	ns

Table 13 : ADC Characteristics

8. Power Consumption

MLX75123 requires eight different voltage domains, each connected to either 1V8 or 3V3.
An overview of the different types can be found here:

Supply Domain	Voltage (V)	Power (mW)
VDDA_1V8	1.8	8.12
VDDA_ADC_1V8	1.8	77.05
VDDA_ADC_S_1V8	1.8	18.53
VDDD_1V8	1.8	15.57
VDD_IO (at 1V8)	1.8	29.16
VDD_I2C	3.3	n/A
VDDA_3V3	3.3	0.01
VDDD_3V3	3.3	4.24
	TOTAL	**153 mW** [1]

Table 14 : Typical power consumption

Note [1] : Calculations are based on typical application parameters listed in chapter 11.
Note [1] : Calculations are based on the average power consumption of each domain incl. temperature variation.

VDD_I2C and VDD_IO can be connected to 1V8 or 3V3 depending on the microprocessor. For EMC performance and a reduction in power consumption we strongly suggest to connect VDD_IO to 1V8.

We recommend to use independent regulators on each supply, however if from system point of view this is not desirable one could consider three regulators only. In this scenario we suggest to connect certain domains to each other with good decoupling techniques.
1V8 : VDDD_1V8, VDD_IO, VDD_I2C
1V8_Clean : VDDA_1V8, VDDA_ADC_1V8, VDDA_ADC_S_1V8
3V3 : VDDA_3V3, VDDD_3V3

In combination with MLX75023 or MLX75024 an extra MIXH regulator, 3V3_clean and negative ARRAYBIAS supply is required.

8.1. Power Up & Down Sequence

To guarantee a proper operation of MLX75123 it's considered mandatory to apply 1V8 prior to the 3V3 supply voltage. Reversely it's also recommended to disconnect 3V3 before 1V8 on power down. Both conditions are visualized in Figure 4. It's mandatory to keep both supplies within 500mV (δ_V) range of each other during start-up and power down sequences. When 1V8 ramps up too fast, compared to 3V3, a diode will be reversed biased which could lead to permanent HW damage, if 3V3 ramps up too fast, compared to 1V8, internal circuitry could be destroyed because of undefined currents. This sequence can be achieved by a Schottky diode (like PMEG2010) between both domains in combination with digital enable control of the 1V8 and 3V3 regulators.

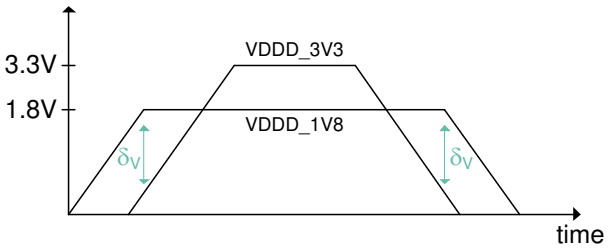


Figure 4 : Voltage domains startup sequence

9. Output Modes

MLX75123 has six different data output modes. The output mode can be changed via register Tx_Py_SETTINGS as described in section 13.2.8 and can change per phase.

One Depthsense® pixel has two outputs, known as tap A and tap B, each in counterphase of one other. To reduce the calculation time from raw to depth information the data output already combines the information from both taps, either as a sum, or as a subtraction. Each pixel output A or B is a 12 bit value in range of 0 - 4095. The error bit in Mode #0 and Mode #2 is used to indicate if this pixel value before the sum or subtraction of A, or B, is between Tx_UPPER_LIMIT and Tx_LOWER_LIMIT thresholds as defined in the registers in section 13.2.5 and 13.2.6. If both tap A and tap B are between these limits this statistics bit will be high, if one of these outputs fails these criteria it will be set to 0. The MLX75023 test rows and ADC test row values are not evaluated against these thresholds, for these pixels the error bit is always 1.

9.1. Mode#0: 11bit A-B + error bit

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
error bit	11bit A-B pixel data										

The 13bit result of this subtraction is internally truncated to a 11bit value which corresponds to (A-B)/4.

9.2. Mode#1: 12bit A-B

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit A-B pixel data											

The 13bit result of this subtraction is internally truncated to a 12bit value which corresponds to (A-B)/2.

9.3. Mode#2: 11bit A+B + error bit

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
error bit	11bit A+B pixel data										

The 13bit result of this sum is internally truncated to a 11bit value which corresponds to (A+B)/4.

9.4. Mode#3: 12bit A+B

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit A+B pixel data											

The 13bit result of this sum is internally truncated to a 12bit value which corresponds to (A+B)/2.

9.5. Mode#4: Raw A

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit A pixel data											

9.6. Mode#5: Raw B

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit B pixel data											

10. Parallel Output Sequence & Timing

The complete output data interface consists out of 16 parallel lines:

- 1 bit PIXCLK → uses same frequency as input CLK
- 1 bit FSYNC → indicates start of a new frame (one pulse per frame start)
- 1 bit VSYNC → indicates start of a new phase (one pulse per phase start, typically 4 pulses per frame)
- 1 bit HSYNC → indicates start of a new row (one pulse for each row start, typically 240 pulses per phase)
- 12 bit pixel data PIXD[11:0]

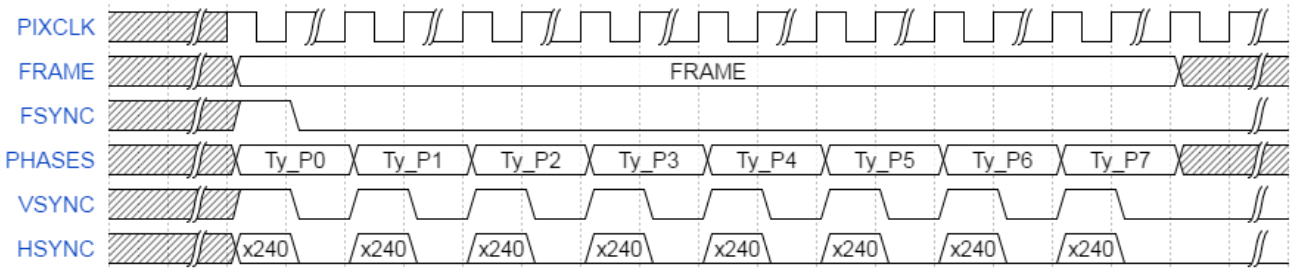


Figure 5 : FSYNC, VSYNC & HSYNC timing diagram[1]

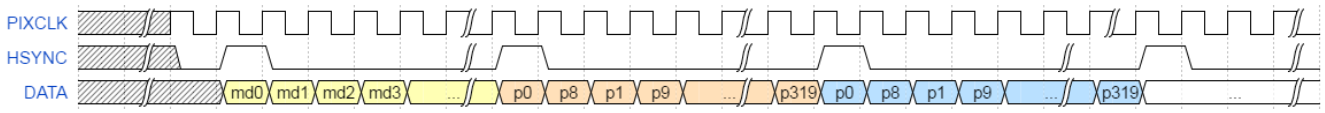
Note [1] : The length of HSYNC, VSYNC and FSYNC is one input clock pulse and is not programmable.

The sequential pixel output per row when used in combination with MLX75023 looks like 0, 8, 1, 9, …, 310, 318, 311, 319. This means that the pixels should be re-ordered on the microcontroller to reconstruct a presentable distance map. This pixel re-ordering can be done on the individual phase data or on the calculated distance map.

The serial output order can be simulated with this Matlab example code:

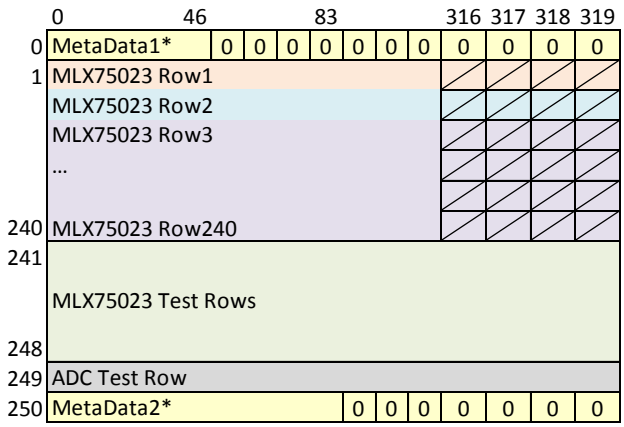
```
for x = 0:1:159
    y = mod(x,8) + 16*floor(x/8);
    z = mod(x,8) + 16*floor(x/8) + 8;
    fprintf('%d, %d, ', y, z);
end
```

On a timing diagram, without ROI, it would look like :



md0, md1, md2, md3, … = MetaData
p0, p8, p1, p9, … , p319 = PixelData / row

During a phase the maximum # of rows is limited to 251, depending on the features that are enabled or disabled.



- 1x MetaData1 line (optional)
- 240x Pixel row data
- 8x MLX75023 Test Rows (optional)
- 1x ADC Test Row (optional)
- 1x MetaData2 line (optional)

11. Distance Calculation

The distance data per pixel [in mm] can be calculated by the following formulas: (Matlab code)

```
p0 = TwoComp(phase0,16);
p180 = TwoComp(phase180,16);
p90 = TwoComp(phase90,16);
p270 = TwoComp(phase270,16);

I = p0 - p180;
Q = p270 - p90;

ampData = sqrt(I.^2 + Q.^2);
Phase = atan2(Q, I);
unAmbiguousRange = 0.5*299792458/modulationFrequency*1000;
coef_rad = unAmbiguousRange / (2*pi);
distData = (Phase+pi) * coef_rad + AbsoluteDistanceOffset;
while sum(distData(distData<0)) ~= 0
    distData(distData<0) = distData(distData<0) + unAmbiguousRange;
end
```

- *phase0, phase180, phase90, phase270* is the raw QVGA A-B data from the sensor at different phase intervals
- *TwoComp* is a local function that converts the unsigned data from Mode#1 A-B for each of the raw phases
- *UnAmbigiousRange* is the maximum range determined by the system modulation frequency (at modulation frequency of 20MHz this would be ~7.5m, at 40MHz it will be ~3.75m)
- *coef_rad* is a conversion coefficient from radians to degree
- *AbsoluteDistanceOffset* is a negative value obtained after calibration to measure the absolute distance (default value = 0)
- The *while* loop avoids negative distance values after the absolute distance calibration

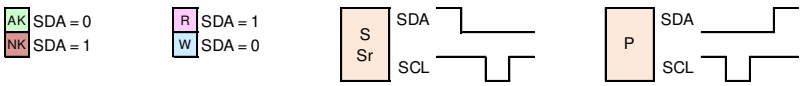
12. I2C Commands

MLX75123 features a standard (up to 400kHz) inter-integrated circuit communication interface, also known as I^2C.
This device acts as a I^2C slave with address 0x0067. This address can be reprogrammed via register I2C_ADDRESS.
More information on custom I^2C addresses can be found in chapter 13.1 .
The size of both the register addresses & register data is 16bit.

I^2C follows a strict timing sequence, the master device will initiate all communication, it's in control of the SCL line, data will be transmitted via SDA line. Each slave monitors the I^2C bus and will respond to the master when needed.

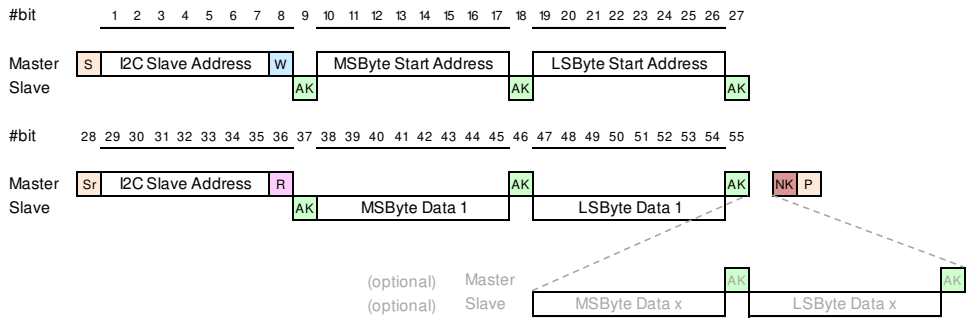
The following sections describe these timings for each of the individual commands.

Legend:



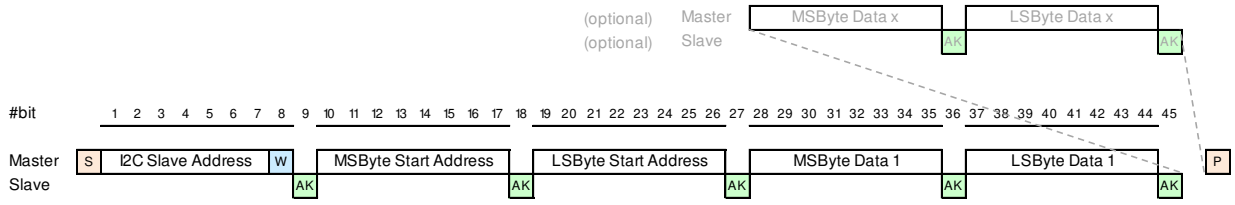
12.1. I^2C_READ

This command allows you to read the registers listed in chapter 13. Normally it will read 1x register only, but the slave will continue to transmit data of sequential register addresses until the master terminates the communication.



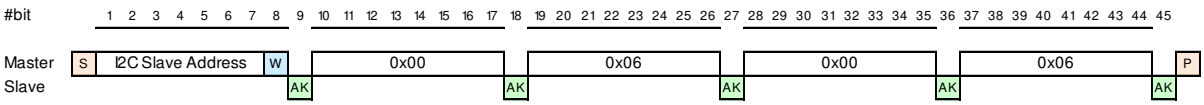
12.2. I^2C_WRITE

This command allows you to write the registers listed in chapter 13. Normally you write 1x register only, but optionally the master can continue to transmit data of sequential register addresses to reduce the communication time when a lot of registers should be written.



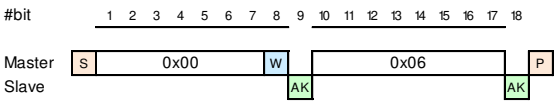
12.3. I²C_RESET

This command will reset only MLX75123.



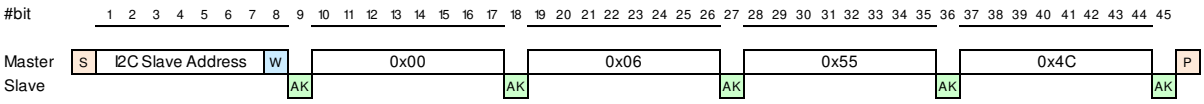
12.4. I²C_GLOBAL_RESET

This command will reset all I²C devices on the bus which support this standardized, but optional, command.



12.5. I²C_SAVEREGMAP

On MLX75123 start-up all registers will be copied from the non-volatile memory into the volatile RAM, where they can be changed via the I²C communication. When the device is restarted it will load all default values from the EEPROM again. It's possible to save your own custom register map into the EEPROM with the following I2C command sequence:



followed by an I²C_WRITE of register 0x0000 with value 0x0100. When a copy into NVRAM is completed the register value will change from 0x0100 to 0x0000 (= self-clearing bit). It is advised to poll the register until it has value 0 before continuing any other communication to the device. Please note that an I²C_READ of register 0x0000 is only possible after the above mentioned I2C command sequence. A full write cycle lasts about ±11 milliseconds. It's very important that during this time the device operation is not interrupted by either a HW or a SW reset, as this can lead to memory corruption.

For long term reliability of the NVRAM there's a maximum defined of I²C_SAVEREGMAP cycles possible. The limit depends on the junction temperature and operating conditions:

- Max.100000 store cycles at 25°C
- Max.10000 store cycles at 125°C

13. Registers

MLX75123 has internal memory that is used to store the default register values and that can be used to store customer specific parameters like unique module no. identifiers. On start up this EEPROM is loaded into the RAM where it can be accessed during normal operation. Commands to read/write custom RAM settings into the EEPROM are available.
The complete memory map can be found here, it's strongly linked to values that can be read out from the metadata.

Memory Address	Description
0x1000	Configuration Parameters I
…	
0x1010	
0x1012	Table 1 Properties
…	
0x1022	
0x1024	T1_P0_SETTINGS
…	
0x1030	
0x1032	T1_P1_SETTINGS
…	
0x103E	
0x1040	T1_P2_SETTINGS
…	
0x104C	
0x104E	T1_P3_SETTINGS
…	
0x105A	
0x105C	T1_P4_SETTINGS
…	
0x1068	
0x106A	T1_P5_SETTINGS
…	
0x1076	
0x1078	T1_P6_SETTINGS
…	
0x1084	
0x1086	T1_P7_SETTINGS
…	
0x1092	

Memory Address	Description
0x1094	Table 2 Properties
…	
0x10A4	
0x10A6	T2_P0_SETTINGS
…	
0x10B2	
0x10B4	T2_P1_SETTINGS
…	
0x10C0	
0x10C2	T2_P2_SETTINGS
…	
0x10CE	
0x10D0	T2_P3_SETTINGS
…	
0x10DC	
0x10DE	T2_P4_SETTINGS
…	
0x10EA	
0x10EC	T2_P5_SETTINGS
…	
0x10F8	
0x10FA	T2_P6_SETTINGS
…	
0x1106	
0x1108	T2_P7_SETTINGS
…	
0x1114	
0x1116	Configuration Parameters II
0x1118	
0x111A	USER DEFINED (these can be read out in MetaData1)
0x111C	
0x111E	
0x1120	
0x1122	USER DEFINED
…	
0x1198	

13.1. Configuration Parameters Registers

General parameters that influence the behaviour of MLX75123 can be changed in the following registers.

Name : **I²C_ADDRESS**

Address : 0x1000

Default Value : 0x0067

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	**I²C_ADDRESS [6:0]**						

I²C_ADDRESS : Programmable 7bit I²C slave address.
A change of this register should be followed by a I2C_SAVEREGMAP operation (section 12.5) and a device reset before this new address will be active. Address 0x0032 should not be used.

Name : **START_DELAY**

Address : 0x1002

Default Value : 0x00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	**START_DELAY**								

START_DELAY : Defines the time between the NVRAM to EEPROM copy and the 3V3_READY signals are available and the start of the digital block for the first frame acquisition. It ranges from 0 - 5.12ms at 80MHz input clock, in steps of 9 bit.

Name : **CONFIG**

Address : 0x1004

Default Value : 0x0000

Bit	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
	-	-	**VIDEO_ DRIVE**	**LED_MODE**	-	-	-	-

VIDEO_DRIVE : Select the drive strength of the video output buffers
- 0 : low drive strength
- 1 : high drive strength

By default the drive strength is set high for board debug processes, however the low drive strength is advised to reduce noise & EMC impact to a minimum in application conditions.

LED_MODE : Select single ended or differential LED control signals
- 0 : LED_P in single ended output mode (with LED_N connected to ground)
- 1 : LED_P and LED_N in LVDS mode

Changing this register should be followed by an I2C_SAVEREGMAP operation (section 12.5) and a device reset before the changes to become active.

Name : **Bx_LATCH**

Address : 0x1006

Default Value : 0xFF11 (in configuration with sensor MLX75023)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BxCOL_LATCH								**BxROW_LATCH**							

BxCOL_LATCH : Pattern to be applied to BxCOL[7:0] bits at initialization/power-up phase of the MLX75023.
BxROW_LATCH : Pattern to be applied to BxROW[7:0] bits at initialization/power-up phase of the MLX75023
0x11 : BxROW_LATCH pattern to apply for MLX75023 in application mode
0x13 : BxROW_LATCH pattern to apply for MLX75023 with 4 test columns enabled

Note : Bx_LATCH is only applied once during startup, for change(s) during operation the value has to be copied to NVRAM (see section 12.5) and a MLX75123 reset has to be applied.
Note : For a configuration with MLX75024 this register value HAS to change to 0x0000.

Name : **PIXEL1**

Address : 0x1008

Default Value : 0xF39D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIXEL1_Y								**PIXEL1_X**							

MLX75123 offers the functionality to read out any pixel in addition to the normal read-out sequence. This feature can be used to read out single pixels or test structures from the sensor array. This register hold the X & Y coordinates of one pixel. This pixel will be read out only once per frame, at the start of each frame and the result (available in the metadata) will be constant for all phase frames. PIXEL1_Y and PIXEL2_Y should be from 2 neighbouring rows

Name : **PIXEL2**

Address : 0x100A

Default Value : 0xF39C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIXEL2_Y								**PIXEL2_X**							

MLX75123 offers the functionality to read out any pixel in addition to the normal read-out sequence. This feature can be used to read out single pixels or test structures from the sensor array. This register hold the X & Y coordinates of one pixel. This pixel will be read out only once per frame, at the start of each frame and the result (available in the metadata) will be constant for all phase frames. PIXEL1_Y and PIXEL2_Y should be from 2 neighbouring rows

Name : **ADC_DELAY_FT**

Address : 0x1010

Default Value : 0x0000

Bit	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
	-	-	**PROG_DELAY**					**FRAME_ TABLE**

PROG_DELAY : The setting for the delay line that shall be applied during a full frame (0 = default sampling point)
This setting is not being applied during the automatic delay line sweep.
This register using GRAY coding : 0, 1, 3, 2, 6, 7, 5, 4, 12, 13, 15, 14, 10, 11, 9, 8,
24, 25, 27, 26, 30, 31, 29, 28, 20, 21, 23, 22, 18, 19, 17, 16 (listed in order of magnitude)
For increasing values, a delay is added, thus the sample point occurs later in time.

Note : Operation at non optimized PROG_DELAY settings can cause vertical stripe image artefacts in the image.
More information on this effect and the optimization procedure is available upon request.

FRAME_TABLE : Selection of the Frame Table to be used.
0 : Frame Definition Table 1 is used to generate the frames
1 : Frame Definition Table 2 is used to generate the frames
A definition of these tables can be found in registers 0x1012 and 0x1094

Name : **DELAY_CONFIG**

Address : 0x1116

Default Value : 0x0000

Bit	15	14	13	12	11	10	9	8
	MOD_INV	**ADC_LATENCY**					-	-

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

MOD_INV : Inverts the sensor (DMIX0/1) modulation signal

ADC_LATENCY : Changes the digital sampling point of the ADCs. Results in a full column shift of the image. Changes to ADC_LATENCY should be programmed into NVRAM (see section 12.5) and are only applied after sensor reset.

Name : **BxROW_IDLE**

Address : 0x1118

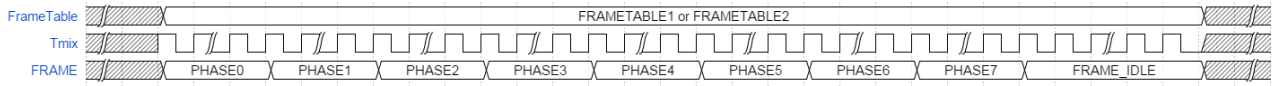
Default Value : 0x00F4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	**BxROW_IDLE**							

BxROW_IDLE : Pattern to be applied to BxROW[7:0] bits during reset, integration & sampling phases

13.2. FrameTable & Phase Registers

MLX75123 has two different FrameTable definitions. Each table consists of eight individual configurable phases as indicated in Table 15. The FrameTable used to capture the frames can be selected register 0x1010 *ADC_DELAY_FT*.



FrameTable Definition	Phase Definition
T1_SETTINGS	T1_P0_SETTINGS
T1_IDLETIME	T1_P0_INTEGRATION
T1_MODE	T1_P0_PREHEAT
T1_FRAMECOUNT	T1_P0_PREMIX
T1_UPPER_LIMIT	T1_P0_IDLE
T1_LOWER_LIMIT	T1_P0_SETUP
T1_ROI_START & T1_ROI_SIZE	… Phase1
	… Phase2
	… Phase3
	… Phase4
	… Phase5
	… Phase6
	… Phase7
T2_SETTINGS	T2_P0_SETTINGS
T2_IDLETIME	T2_P0_INTEGRATION
T2_MODE	T2_P0_PREHEAT
T2_FRAMECOUNT	T2_P0_PREMIX
T2_UPPER_LIMIT	T2_P0_IDLE
T2_LOWER_LIMIT	T2_P0_SETUP
T2_ROI_START & T2_ROI_SIZE	… Phase1
	… Phase2
	… Phase3
	… Phase4
	… Phase5
	… Phase6
	… Phase7

Table 15 : Frametable configuration