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MLX80002/MLX80004

Enhanced Universal Dual/Quad LIN Transceiver
Datasheet

Melexis
INSPIRED ENGINEERING

1. Features and Benefits

- LIN 2.x/SAE J2602 and ISO17987-4 compliant
- Quad/Dual - enhanced master transceiver function for each channel
- Backward compatible to quad-channel master transceiver MLX80001
- Lowest space (QFN4x4, wettable flanks) and minimized external components
- Quad/Dual versions with same package and foot print for cost/space optimized design
- Slew rate selection and High Speed Flash mode
- Wide operating voltage range V_S = 5 to 27 V
- Fully compatible to 3.3V and 5V devices
- Very low standby current consumption of (typ) 10µA in sleep mode
- WAKE input for local wake-up capability
- Remote and local wake-up source recognition
- Control output INH for external components
- Integrated termination (resistor & decoupling diode) for both LIN master & slave nodes
- TxD dominant time out function in slave configuration
- RxD dominant time out function in master configuration
- Sleep timer
- Low EME (emission) and high EMI (immunity) level
- High impedance LIN pin in case of loss of ground or battery
- Enhanced ESD robustness
    - +/- 10kV according to IEC 61000-4-2 for pins LIN, Vs and WAKE

2. Ordering Information

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX80002	K	LW	CAA-001	RE
MLX80004	K	LW	BAA-001	RE

Legend:

Temperature Code:	K = -40 to 125°C
Package Code:	LW = Quad Flat Package (QFN), wettable flanks
Option Code:	BAA-001 = Design Revision
Packing Form:	RE = Reel
Ordering example:	MLX80004 KLW-BAA-001-RE

3. General Description

The MLX80004(2) is a quad/dual LIN transceiver physical layer device for a single wire data link capable of operating in applications using baud rates up to 20kBd. It is compliant to LIN2.x as well as to the SAE J2602 specifications. The IC furthermore can be used in ISO9141 systems. The MLX80004 is functionally compatible to the MLX80001 quad master LIN transceiver.

The device is flexible for use in LIN – master applications and slave applications as well.
Due to the integrated master termination and the high ESD/EMC robustness of the device a minimum space and number of external components is required.

The number of LIN – channels can be easily adapted on the application requirements by combinations of quad and dual channel devices within the same foot print.

Because of the very low power consumption of the MLX80004 while being in sleep mode it's suitable for ECU applications with hard standby current requirements. The implemented high resistive LIN - termination in sleep mode as well as the RxD dominant time-out feature allows a comfortable handling of LIN short circuits to GND.

In order to reduce the power consumption in case of failure modes, the integrated sleep timer takes care for switching the IC into the most power saving sleep mode after Power-On or Wake-Up events are not followed by a mode change response of the microcontroller.

The MLX80004/2 has an improved EMI performance and ESD robustness according to the OEM Common Hardware Requirements for LIN in Automotive Applications Rev.1.2.

By using the MODE0/1 pins the application can be easily adapted on the required baud rate in order to optimize the EMC emissions. A high speed Flash Mode with disabled slew rate control is available as well.

To fulfill different OEM requirements, the integrated master termination can be disabled and external master resistors and decoupling diodes can be used. In this mode the MLX80004/2 can be used in slave applications as well.

4. Table of Contents

5. Block Diagram

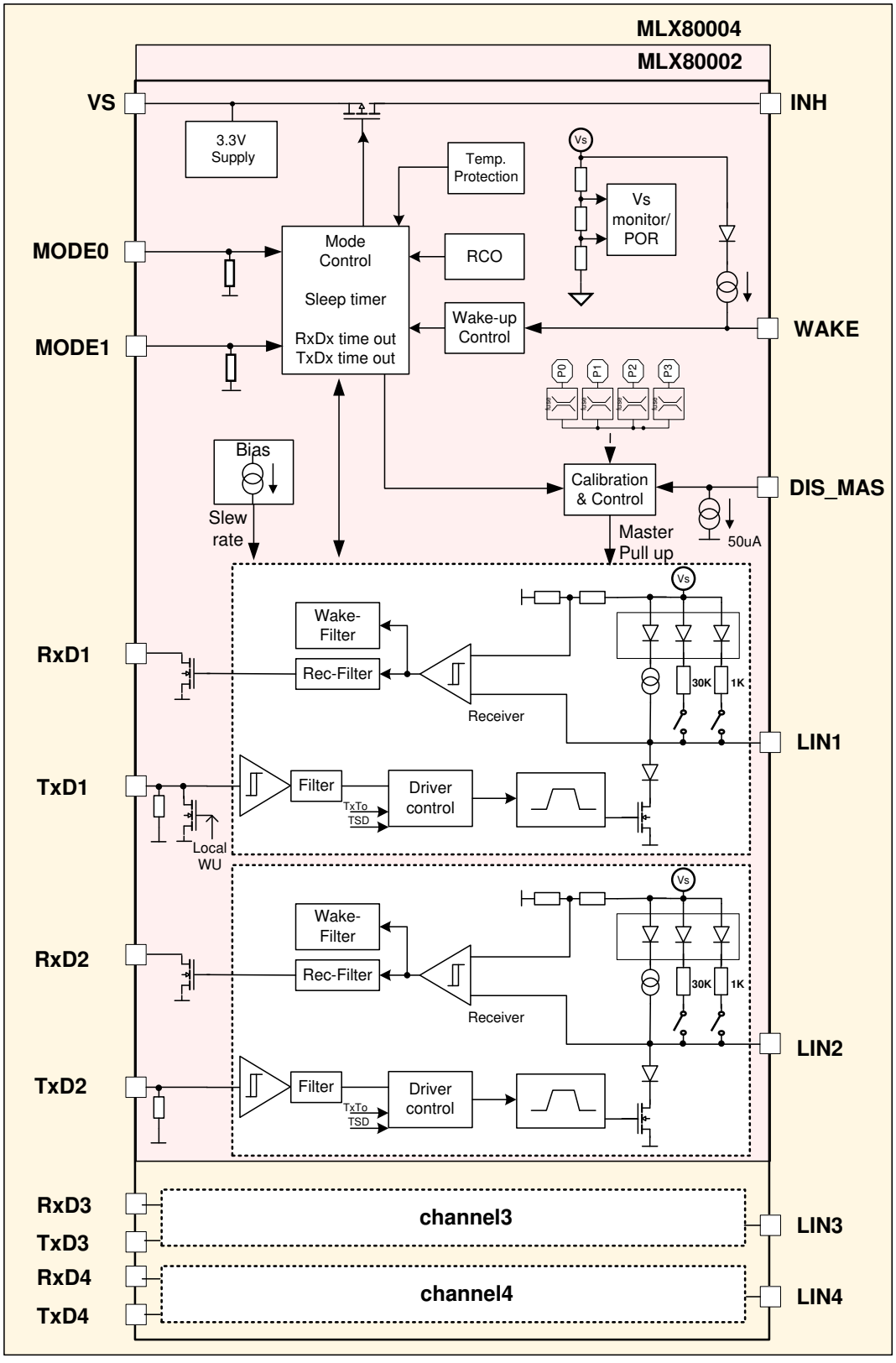

Figure 1: Block Diagram MLX80004/2.

6. Pin Description

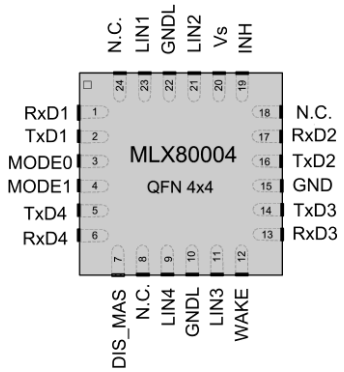

Figure 2: Pinout MLX80004 QFN24 package

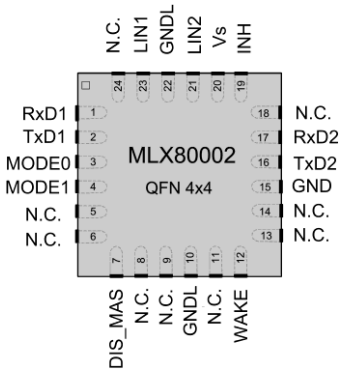

Figure 3: Pinout MLX80002 QFN24 package

Table 1: Pin List

Pin	MLX80004	MLX80002	I/O-Type	Description
1	RxD1		O	Receive Data LIN Ch1, open drain
2	TxD1		I	Transmit Data LIN Ch1 (+ local WU-Flag)
3	MODE0		I	Operating Mode Selection Input 1
4	MODE1		I	Operating Mode Selection Input 2
5	TxD4	N.C.	I	Transmit Data LIN Ch4
6	RxD4	N.C.	O	Receive Data LIN Ch4, open drain
7	DIS_MAS		I	disable integrated master resistor
8	N.C.			
9	LIN4	N.C.	I/O	LIN Bus Ch4
10	GNDL		G	Ground LIN
11	LIN3	N.C.	I/O	LIN Bus Ch3
12	WAKE		I	local wake up input, low active
13	RxD3	N.C.	O	Receive Data LIN Ch3, open drain
14	TxD3	N.C.	I	Transmit Data LIN Ch3
15	GND		G	Ground
16	TxD2		I	Transmit Data LIN Ch2
17	RxD2		O	Receive Data LIN Ch2, open drain
18	N.C.			
19	INH		O	HV High Side Control Pin
20	VS		P	Battery Voltage
21	LIN2		I/O	LIN Bus Ch2
22	GNDL		G	Ground LIN
23	LIN1		I/O	LIN Bus Ch1
24	N.C.			
EPad	GND / GNDL		G	Exposed Pad of Package (grounded heatsink)[1]

[1] For enhanced thermal and electrical performance, the exposed pad of the QFN package should be soldered to the board ground plane (and not to any other voltage level).

7. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 60 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

7.1. Operating Conditions

Table 2: Operating Conditions

Nr.	Parameter	Symbol	Min	Max	Unit	Remark
101	Battery supply voltage [1] [2]	V_S	5	27	V	
102	Extended battery supply voltage	Vs_NON_OP	5	40	V	Parameter deviations allowed
103	Operating ambient temperature	T_{amb}	-40	+125	°C	
104	Voltage on low voltage I/Os (RxDx, TxDx, MODEx	RxDx, TxDx, MODEx	-0.3	5.5	V	

[1] Vs is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4 to 1V,
[2] Operating voltage range of the LIN2.x/SAE J2602 plug & play specification is 7V…18V

7.2. Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Nr.	Parameter	Symbol	Condition	Min	Max	Unit
201	Battery Supply Voltage	V_S	Respective to GND	-0.3	40	V
202	Transients at battery supply voltage	$V_{VS.tr1}$	ISO 7637/2 pulse 1[1]	-100		V
203	Transients at battery supply voltage	$V_{VS.tr2}$	ISO 7637/2 pulse 2[1]		75	V
204	Transients at high voltage signal pins	$V_{LIN..tr1}$	ISO 7637/3 pulses 1[2]	-30		V
205	Transients at high voltage signal pins	$V_{LIN..tr2}$	ISO 7637/3 pulses 2[2]		30	V
206	Transients at high voltage signal and power supply pins	$V_{HV..tr3}$	ISO 7637/2 pulses 3A, 3B [3]	-150	100	V
207	DC voltage LINx	V_{LIN_DC}	Respective to GND and V_S Loss of Ground(V_{GND}=V_S)	-20 -30	40 40	V
208	DC voltage WAKE	V_{WAKE_DC}	Respective to GND and V_S Loss of Ground(V_{GND}=V_S)	-20 -30	40 40	V
209	DC voltage INH, DIS_MAS	V_{INH_DC} V_{DISMAS_DC}		-0.3	V_S + 0.3	V
210	DC voltage low voltage I/O's (RxDx,TxDx,MODEx)	V_{lv_DC}		-0.3	7	V
211	ESD voltage, IEC 61000-4-2 [4]	V_{ESD}	Pin LIN, VS, WAKE	-10	10	kV
212	ESD voltage, HBM (CDF-AEC-Q100-002)	V_{ESD}	Pin LIN, V_S, WAKE, INH vs GND	-8	8	kV
			All other pins	-3	3	kV
213	ESD voltage, CDM (CDF-AEC-Q100-011)	V_{ESD}		-1000	1000	V
214	Maximum latch - up free current at any Pin	I_{LATCH}		-500	500	mA
215	Thermal impedance	Θ_{JA}	JEDEC 1s2p board		50	K/W
216	Storage temperature	T_{stg}		-55	150	°C
217	Junction temperature	T_{vj}		-40	150	°C

[1] ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >10uF blocking capacitor.
[2] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 100nF.
[3] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 1nF. ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >10uF blocking capacitor
[4] IEC 61000-4-2 validated by external Lab during product qualification (see application examples)

7.3. Static Characteristics

Table 4: Static Characteristics
Unless otherwise specified all values in the following tables are valid for V_S = 5 to 27V and T_j= -40 to 150°C. All voltages are referenced to ground (GND), positive currents flow into the IC.

Nr.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN VS							
301	Undervoltage lockout	V_{S_UV}		2.4		4.8	V
302	Undervoltage lockout hysteresis[1]	$V_{S\_UV\_hys}$		0.1	0.3	0.7	V
303	Supply current, sleep mode	I_{Ssl}	V_{M0DEx} = 0V, Tj ≤ 85C V_{WAKE} = V_{LINx} = V_S ≤14V		9	15	µA
			V_{M0Dex} = 0V, Tj ≤ 125C V_{WAKE} = V_{LINx} = V_S ≤ 18V			20	µA
304	Supply current standby mode	I_{SBY}	V_{M0Dex} = 0V, after POR or WU	100	200	400	µA
305	Supply current active mode, dominant Standard transceiver mode	I_{Sd_slave}	V_{M0Dex} = 5V,V_{TxD1-4} = 0V DIS_MAS = Vs (80004)		12	15	mA
			V_{M0Dex} = 5V,V_{TxD1-2} = 0V DIS_MAS = Vs (80002)		7	9	
306	Supply current active mode, dominant Enhanced master mode	I_{Sd_master}	V_{M0Dex} = 5V,V_{TxD1-4} = 0V DIS_MAS = 0V (80004)		100	125	mA
			V_{M0Dex} = 5V,V_{TxD1-2} = 0V DIS_MAS = 0V (80002)		50	65	
307	Supply current active mode, recessive	I_{Sr}	V_{M0Dex} = 5V,V_{TxD1-4} = 5V		3	5	mA
PIN LINx – Transmitter							
310	Transmitter internal capacitance[1]	C_{LIN}	Capacitance on pins LINx to GND		30	40	pF
311	Short circuit bus current	I_{BUS_LIM}	V_{LIN} = V_S, V_{M0Dex} = 5V,V_{TxDx} = 0V	40	100	200	mA
312	Pull up resistance bus, normal & standby mode	R_{SLAVE}	V_{DIS_MAS} = V_S	20	30	60	kΩ
313	Pull up resistance bus, normal & standby mode	R_{Master}	V_{DIS_MAS} = 0V	900	1000	1100	Ώ
314	Pull up current bus, sleep mode	I_{SLAVE_SLEEP}	V_{LINx} = 0V, V_S = 12V, V_{M0Dex} = 0V,V_{TxDx} = 5V	-100	-60	-20	µA
315	Voltage drop at int. diode in pull up path R_{SLAVE} [1]	$V_{SerDiode}$		0.4		1	V
316	Receiver dominant input leakage current including pull up resistor	$I_{BUS\_PAS\_dom}$	V_{LINx} =0V, V_S =12V, V_{M0Dex} = 5V,V_{TxDx} = 5V, V_{DIS_MAS} = V_S	-400			µA
317	Receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{LINx}=18V, V_S =5V, V_{M0Dex} = 5V,V_{TxDx} = 5V, Tamb<125°C			20	µA
318	Bus reverse current loss of battery [2]	$I_{BUS\_NO\_BAT}$	V_S = 0V, 0V < $V_{LIN\ x}$< 18V Tamb<125°C			20	µA
319	Bus current during loss of ground [2]	$I_{BUS\_NO\_GND}$	V_S = V_{GND} = 12V, 0 < V_{LINx} < 18V	-10		50	µA
320	Transmitter dominant voltage [2]	Vol_{BUS}	Rload = 500Ω, V_S = 5V	0		1.2	V
			Rload = 500Ω, V_S >= 7V	0		0.2×V_S	
321	Transmitter recessive voltage [2]	Voh_{BUS}	V_{M0Dex} = 0/5V,V_{TxDx} = 5V	0.8×V_S		1×V_S	V

Nr.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN LINx – Receiver							
322	Receiver dominant voltage	V_{BUSdom}				0.4×V_S	V
323	Receiver recessive voltage	V_{BUSrec}		0.6×V_S			V
324	Center point of receiver threshold	V_{BUS_CNT}	V_{BUS_cnt} = (V_{BUSdom}+ V_{BUSrec})/2	0.475×V_S	0.5×V_S	0.525×V_S	V
325	Receiver hysteresis	V_{HYS}	V_{HYS} = (V_{BUSrec} –V_{BUSdom})			0.175×V_S	V
PIN MODE0/1, TxD2/3/4							
331	High level input voltage	V_{ih_xx}	Rising edge	2			V
332	Low level input voltage	V_{il_xx}	Falling edge			0.8	V
333	pull down resistor	R_{pd_xx}	V_{ih_xx} = 5V	200	350	600	kΩ
334	Leakage Current	I_{leak_xx}	V_{il_xx} = 0V	-5		5	µA
PIN TxD1							
341	High level input voltage	V_{ih_TxD1}	Rising edge	2			V
342	Low level input voltage	V_{il_TxD1}	Falling edge			0.8	V
343	pull down resistor	R_{pd_TxD1}	V_{TxD1} = 5V	200	350	600	kΩ
344	Low level output voltage	V_{ol_txd1}	I_{TxD1} = 2mA Local WU flag			0.6	V
345	Leakage Current	I_{leak_TxD1}	V_{TxD1} = 0V	-5		5	µA
PIN RxDx							
351	Low level output voltage	V_{ol_rxdx}	I_{RxDx} = 2mA			0.6	V
352	Leakage Current high	I_{leakh_rxdx}	V_{RxDx} = 5V,V_{TxDx} = 5V, $V_{M0/1}$ = 5V	-5		5	µA
353	Leakage Current low	I_{leakl_rxdx}	V_{RxDx} = 0V,V_{TxDx} = 5V, V_{M0Dex} = 5V	-5		5	µA
PIN INH							
361	On resistance INH	R_{on_INH}	V_S =12V, T_j ≤125°C		20	50	Ω
362	Leakage current INH high	I_{leakh_inh}	V_{M0Dex} = 0V,V_{INH} = 27V	-5		5	µA
363	Leakage current INH low	I_{leakl_inh}	V_{M0Dex} = V_{INH} =0V,	-5		5	µA
PIN WAKE							
371	High level input voltage	V_{ih_WAKE}	Sleep mode	V_S-1V			V
372	Low level input voltage	V_{il_WAKE}	Sleep mode			V_S-3.3V	V
373	Pull up current WAKE	I_{WAKE_PU}	V_{WAKE} = 0	-30	-10	-1	µA
374	Leakage current WAKEhigh	I_{WAKE_lk}	V_{WAKE} = V_S =27V	-5		5	µA

Nr.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN DIS_MAS							
381	High level input voltage	$V_{ih\_DIS\_MAS}$	Active modes	4		V_S+0.3V	V
382	Low level input voltage	$V_{il\_DIS\_MAS}$	Active modes			1.9	V
383	Pull down current DIS_MAS	$I_{DIS\_MAS\_PD}$	Active modes		50	60	µA
384	Leakage current DIS_MAS_low	$I_{DIS\_MAS\_lkl}$	V_{DIS_MAS} = 0V	-5		5	µA
385	Leakage current DIS_MAS_high	$I_{DIS\_MAS\_lkh}$	V_{DIS_MAS} = 27V, sleep mode	-5		5	µA
Thermal Protection							
391	Thermal shutdown[1]	T_{sd}		155	170	190	°C
392	Thermal hysteresis[1]	T_{hys}			10	30	°C

[1] No production test, guaranteed by design and qualification
[2] In accordance to SAE J2602

7.4. Dynamic Characteristics

Table 5: Dynamic Characteristics

Unless otherwise specified all values in the following table are valid for V_S = 5 to 27V and T_j = -40 to 150°C.

Nr.	Parameter	Symbol	Condition	Min	Typ	Max	Unit
401	Propagation delay receiver [1]	t_{rx_pdf}	C_{RxD} =25pF falling edge			6	µs
402	Propagation delay receiver [1]	t_{rx_pdr}	C_{RxD} =25pF rising edge			6	µs
403	Propagation delay receiver symmetry	t_{rx_sym}	Calculate t_{rx_pdf} - t_{rx_pdr}	-2		2	µs
404	Receiver debounce time [2]	t_{rx_deb}	LIN rising & falling edge	0.5		4	µs
411	LIN duty cycle 1 [2] [3] [5]	D1	20kbps operation, normal mode Vs = 7 to 18V	0.396			
412	LIN duty cycle 2 [2] [3] [5]	D2	20kbps operation, normal mode Vs = 7 to 18V			0.581	
413	LIN duty cycle 3 [2] [3] [5]	D3	10.4kbs operation, low speed mode Vs = 7 to 18V	0.417			
414	LIN duty cycle 4 [2] [3] [5]	D4	10.4kbs operation, low speed mode Vs = 7 to 18V			0.590	
415	$t_{REC(MAX)}$ – $t_{DOM(MIN)}$ [4] [5]	Δt3	10.4kbs operation, low speed mode			15.9	µs
416	$t_{DOM(MAX)}$ – $t_{REC(MIN)}$ [4] [5]	Δt4	10.4kbs operation, low speed mode			17.28	µs
421	Remote Wake-up filter time	t_{wux_remote}	sleep mode, LIN dominant time before rising edge	30		150	µs
422	Local Wake-up filter time	t_{wu_local}	sleep mode, WAKE falling edge	10		50	µs
431	Delay from Standby to Sleep Mode	t_{dsleep}	V_{MODEx} = 0	150		500	ms
432	TxDx dominant time out time	t_{TxDx_to}	active modes, V_{TxDx} = 0	27		60	ms
433	RxDx dominant time out time	T_{RxDx_to}	active modes, V_{LINx} = 0, V_{DIS_MAS} = 0	27		60	ms
441	MODEx – debounce time	T_{MODE_deb}	active <-> sleep mode transitions	1	2	5	µs
442	DIS_MAS – debounce time	$T_{DIS\_MAS\_deb}$	master <-> slave transitions	1	2	5	µs

[1] This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/us
[2] See Figure 4– LIN timing diagram
[3] Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal master termination disabled
[4] in accordance to SAE J2602, see Figure 5
[5] for supply voltage ranges Vs=5…7V and Vs=18…27V parametric deviations are possible

7.4.1. Duty Cycle Calculation

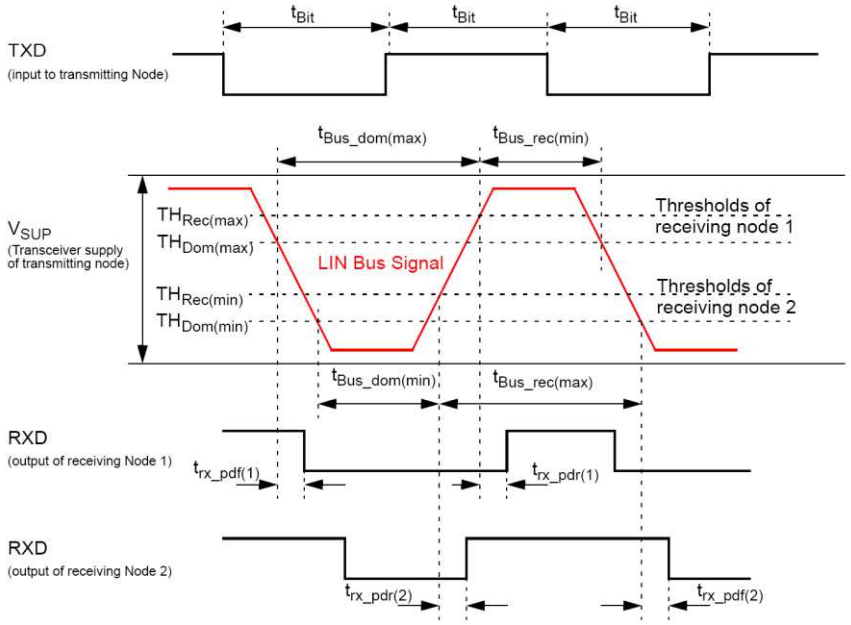

Figure 4: LIN timing diagram (reference LIN2.1 specification)

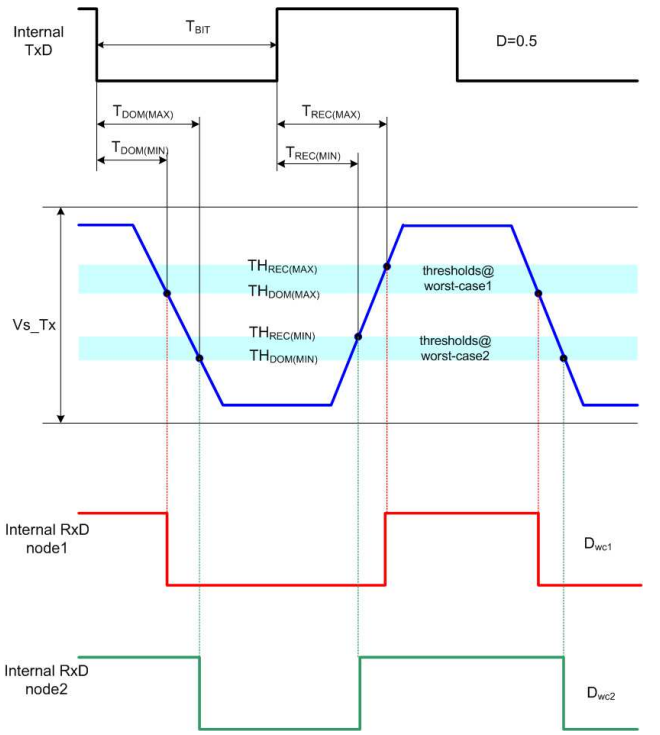

Figure 4: LIN timing diagram, relation between propagation delay and duty cycle (reference SAE J2602 specification)

As shown in Figure 4, both worst case duty cycles can be calculated as follows :

$$D_{wc1} = t_{BUS\_rec(min)} / (2\ t_{Bit})$$
$$D_{wc2} = t_{BUS\_rec(max)} / (2\ t_{Bit})$$

Thresholds for duty cycle calculation for the plug & play specification in accordance to LIN2.0 / SAE J2602:

Baud rate	20kBd	10.4kBd
T_{BIT}	50µs	96µs
D_{wc1}	D1	D3
D_{wc2}	D2	D4
$TH_{REC(MAX)}$	0.744 × V_{S_TX}	0.778 × V_{S_TX}
$TH_{DOM(MAX)}$	0.581 × V_{S_TX}	0.616 × V_{S_TX}
$TH_{REC(MIN)}$	0.422 × V_{S_TX}	0.389 × V_{S_TX}
$TH_{DOM(MIN)}$	0.284 × V_{S_TX}	0.251 × V_{S_TX}

Table 6: Data Transmission Rates

8. Functional Description

The MLX80004/2 is the physical layer interface between the master/slave microcontroller and the single wire LIN bus network.

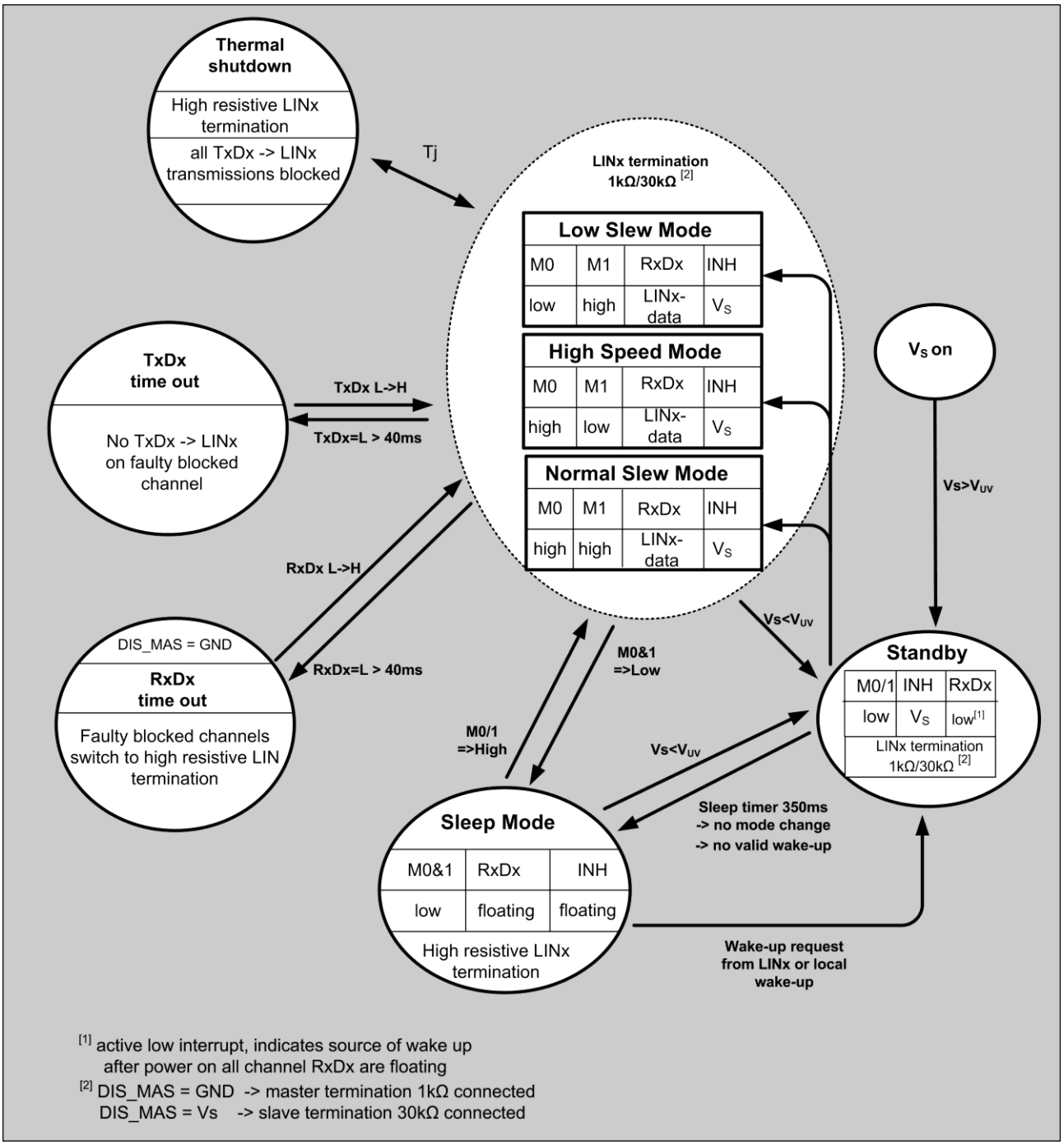

Figure 5: State Diagram of the MLX80004/2

8.1. Operating Modes

Table 7: Operating Modes

Mode	MODE0	MODE1	TxDx	RxDx	INH	LIN transceiver
Standby	0	0	weak pulldown/ active low [1]	floating/ active low [2]	Vs	Off
Active	1 1 0	1 0 1	weak pulldown/ input for transmit data stream	output for LIN data stream	Vs	On [3] [4] [5]
Sleep	0	0	weak pull down	floating	floating	Off

[1] Indicates the wake up flag in case of local wake up
[2] After power on RxDx is floating. If any wake up(local or remote) occurs it will be indicated by active low
[3] Active low interrupt at pin RxD will be removed when entering normal mode
[4] Wake up source flag at pin TxD1 will be removed when entering normal mode
[5] Active modes will be entered by a low -> high transition on pin MODEx. When recessive level (high) on pin TxDx is present the transmit path will be enabled

8.2. Initialization and Standby mode

When the battery supply voltage Vs exceeds the specified threshold V_{S_UV}, the MLX80004/2 automatically enters an intermediate standby mode. The INH output becomes HIGH (Vs) and can be used for a battery driven interrupt or to switch on an external ECU – voltage regulator. The pins RxDx are floating and the integrated master (slave) pull up resistor with decoupling diode pulls the pin LIN. The transmitter and the receiver are disabled.
If no mode change occurs to any active mode via a MODE0/1 LOW to HIGH transition within the time stated (typically 350ms), the IC enters the most power saving sleep mode and the INH output will become floating (logic 0).
Furthermore the standby mode will be entered after a valid local or remote wake up event, when the MLX80004/2 is in sleep mode. The entering of the standby mode after wake up will be indicated by an active LOW interrupt on pin RxDx.
The MLX80004/2 enters the standby mode as well in case of a battery under-voltage condition. That happens while being in sleep mode or any active mode.

8.3. Active Modes

By entering the active modes the MLX80004/2 can be used as interface between the single wire LIN bus and the microcontroller. The incoming bus traffic is detected by the receiver and transferred via the RxDx output pin to the microcontroller. (see Figure 4, LIN timing diagram)
The active modes can be entered being in sleep or standby mode, when the pin(s) MODE0/1 are driven HIGH.

MODE0	MODE1	Mode
L	L	Sleep Mode
H	L	High Speed Mode (slew rate control disabled)
L	H	Low speed mode
H	H	Normal Mode

Table 8: Mode Selection Table

8.3.1. High Speed mode

This mode allows high speed data download up to 100Kbit/s. The slew rate control is disabled. The falling edge is the active driven edge, the speed of the rising edge is determined by the network time constant.

8.3.2. Low speed mode

This mode is the recommended operating mode for J2602 applications with a maximum baud rate of 10.4kBd. The slew rate control of any channel is optimized for minimum radiated noise, especially in the AM band.

8.3.3. Normal speed mode

Transmission bit rate in normal mode is up to 20kbps. The slew rate control of any channel is optimized for maximum allowed bit rate in the LIN specification package 2.x.

8.4. Sleep Mode

The most power saving mode of the MLX80004/2 is the sleep mode. The mode change into sleep mode is possible regardless of the voltage levels on the LINx bus, pins WAKE or TxDx. The MLX80004/2 offers two procedures to enter the sleep mode:

- The sleep mode will be entered if both the pins MODE0 and MODE1 are being driven LOW for longer than the specified filter time (t_{MODE_deb}) when in active modes.

- If the MLX80004/2 is in standby mode after power-on or wake-up, a sleep counter is started and switches the transceiver into sleep mode after the specified time (typ. 350ms) if the microcontroller of the ECU will not confirm the active operation by setting MODE0/1 pins to logic HIGH. This feature allows faulty blocked LIN nodes to reach the most power saving sleep mode anyway.

Being in sleep mode the INH pin becomes floating and can be used to switch off the ECU voltage regulator in order to minimize the current consumption of the complete LIN node (preferred feature in slave applications). The transmitters are disabled and the pins RxDx are disconnected from the receive path and become floating. The master(slave) termination resistor (LIN pull up resistor with decoupling diode between pins LIN and Vs) is disconnected, only a weak LIN pull up current of typically 50uA is applied to the LINx bus (see chapter 9 Fail-safe Features)

8.5. Wake Up

When in sleep mode the MLX80004/2 offers three wake-up procedures:

- In applications with continuously powered ECU a wake up via mode transition to active modes is possible by setting the MODEx pins to high level. (see chapter 4.3 Active Modes)
- Remote wake-up via LINx bus request
  After a falling edge on the LINx bus followed by a dominant voltage level for longer than the specified value(t_{wu_remote}) and a rising edge on pin LINx will cause a remote wake up (see Figure 6 at page 19)
- Local wake-up via a negative edge on pin WAKE
  A negative edge on the pin WAKE and a dominant voltage level for longer than the specified time (t_{wu_local}) will cause a local wake-up. The current for an external switch has to be provided by an external pull up resistor R_{WK}. For a reverse current limitation in case of a closed external switch and a negative ground shift or an ECU loss of ground a protection resistor R_{WK_prot} between pin WAKE and the switch is recommended. (see Figure 7 at page 20)
  The pin WAKE provides a weak pull up current towards the battery voltage that provides a HIGH level on the pin in case of open circuit failures or if no local wake up feature is required. In such applications it is recommended to connect the pin WAKE to pin Vs via a resistor of 10k ohms.

8.6. Wake Up Source Recognition

The device can distinguish between a local wake-up event (pin WAKE) and a remote wake-up event in dependence of the requesting LINx bus.

Local Wake Up
In case of a local wakeup via WAKE pin, the wake up request is indicated by an active LOW on pin RxD1. The wake-up source flag is set and is indicated by an active LOW on pin TxD1.
The wake-up source flag can be read if an external pull up resistor at TxD1 towards the microcontroller supply voltage has been added and the MLX80004/2 is still in standby mode:

When the microcontroller confirms an active mode operation by setting the pin MODE0/1 to HIGH, both the wake-up request on pin RxD1 as well as the wake-up source flag on pin TxD1 are reset immediately.

Remote Wake Up
In case of a remote wake-up via a LINx bus, the source of the wake-up request will be indicated by the RxDx pin that belongs to the LINx pin. (example: LOW level on RxD4 and floating RxD1-3 indicate a wake-up request on LIN4).
The wake up source flag at TxD1 remains floating.
This allows following the wake-up request of the requesting LIN bus while remaining the other LIN bus channels in recessive mode (no wake up occurs in these LIN networks).

After a mode transition into any active mode by setting the pin MODE0/1 to HIGH, the active LOW wake-up request on pin RxDx is reset immediately.

If the device is not set into an active mode after a wake up request (either local or remote) then it will return into sleep mode after t_{dsleep}.

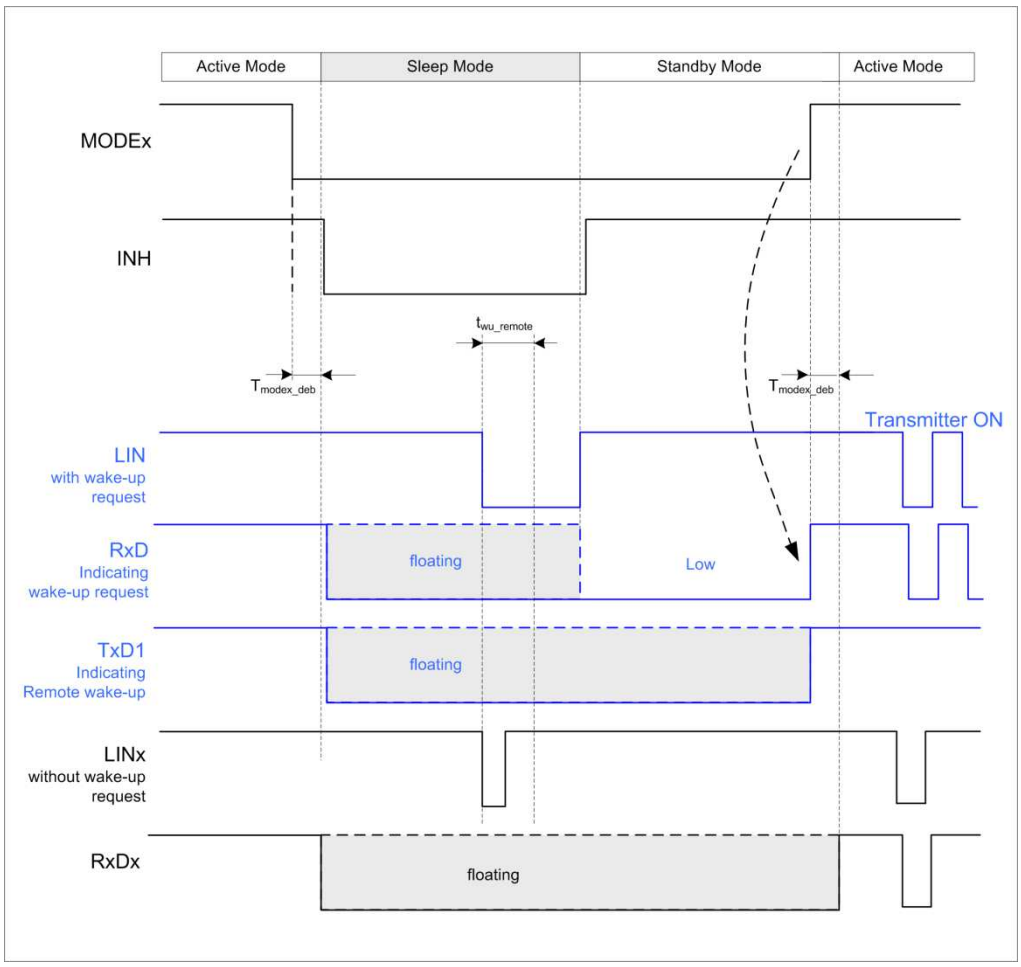

Figure 6: remote wake up and wake-up source recognition

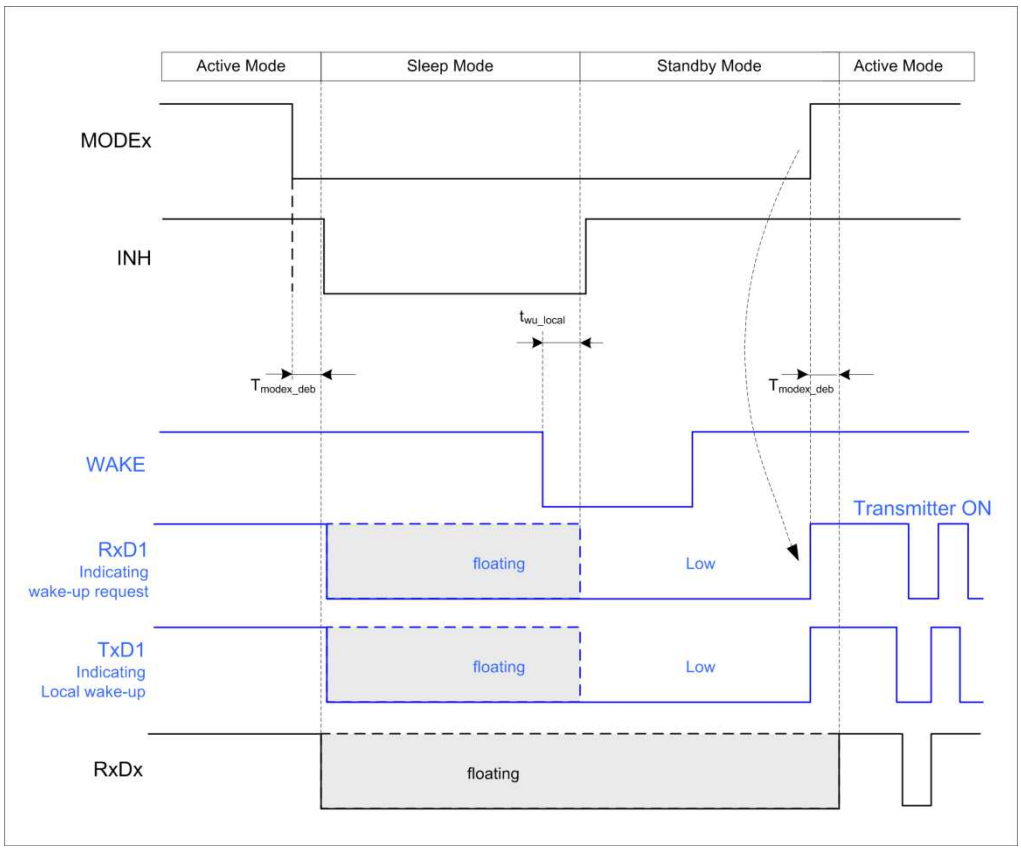

Figure 7: local wake up and wake-up source recognition

8.7. Master / Slave configuration

The target applications of the MLX80004/2 are BCM master modules with multiple LIN channels. In order to be able to use the same module for a wide variety of applications with different stages of extension, a space efficient and cost effective adaptation on the number of LIN channels is desired.
The MLX80004/2 device family offers the combination of quad and dual channel LIN transceiver within the same advanced package and a compatible foot print.
By the integration of the LIN master-termination (decoupling diode and 1K resistor) the external circuitry can be minimized in terms of space as well as BOM (bill of material). The RxD time-out feature allows the handling of a LIN short to ground failure without software support by the microcontroller. This application mode is called enhanced master mode, compatible to the functionality of the quad – LIN transceiver MLX80001.

In case of different BCM requirements it may happen that the *external* master termination is desired only. To cover these applications the pin DIS_MAS has been introduced:

DIS_MAS	Mode	LIN termination	Supported fail safe features
GND	Enhanced Master Mode	Active mode : Diode & 1kΩ sleep mode :Diode & 60µA	• RxDx time-out, independent disconnect of master termination in case of LINx short to ground • TxDx time-out, independent disable of faulty dominant blocked transmit path
Vs	Standard Transceiver Mode	Active mode : Diode & 30kΩ sleep mode :Diode & 60µA	• TxDx time-out, independent disable of faulty dominant blocked transmit path

Table 9: Time Out Modes

In case of externally mounted master termination (standard transceiver mode), the handling of a LIN short to ground is not possible. By using the standard transceiver mode, the MLX80004/2 can be used in slave applications as well. To pull the pin DIS_MAS to high even in case the external ECU regulator is switched off in sleep mode. The pin shall be connected to Vs via an external resistor. (see Figure 8 at page 24, application example)
In the standard transceiver mode, only the TxDx time-out feature is enabled.

9. Fail-safe Features

9.1. Loss of battery

If the ECU is disconnected from the battery, the bus pin is in high impedance state. There is no impact to the bus traffic and to the ECU itself. Reverse current is limited to < 20µA

9.2. Loss of Ground

In case of an interrupted ECU ground connection there is no influence to the bus lines. The current from the ECU to the LINx pins is limited by the weak pull up current of the pin LINx, the integrated master termination (DIS_MAS = GND) as well as the integrated slave termination (DIS_MAS = V_s) is disconnected in order to fulfill the SAE J2602 requirements for the loss of ground current (<100µA @12V).

9.3. Short circuit to battery

The transmitter output currents are limited to the specified value in case of short circuit to battery in order to prevent high current densities and thermal hot spots in the LIN drivers. In dependency of the ambient temperature as well as the battery voltage the junction temperature can exceed the specified value and a thermal overload condition occurs (see chapter 4.5)

9.4. Ground shift and short circuit to ground

If the LIN bus wiring is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the LIN bus and no distortion of the bus traffic occurs.

A LIN bus short to ground condition can cause an undesired current flow. The MLX80004/MLX80002 offers different opportunities to handle the LIN short to ground, see chapter 8.7.

9.5. Thermal overload

The MLX80004 and the MLX80002 is protected against thermal overloads. If the chip junction temperature exceeds the specified value, all transmitters are disabled and the master termination is switched off in order to reduce the power consumption. The receiver is still working during the thermal shutdown state. The pins RxDx indicate the voltage level from the LINx pins also if the circuit is in thermal shut down. The circuit returns automatically to the normal mode after thermal recovery.

9.6. Undervoltage lock out

If the battery supply voltage is missing or decreased under the specified value (V_{S_UV}), all transmitters are disabled to prevent undefined bus traffic.
While in sleep mode, the MLX80004/2 enters the standby mode if Vs drops below the internal power on reset threshold ($V_{INH} = V_s$).

9.7. Open Circuit protection

- The pins TxDx provide a weak pull down. The transmitter cannot be enabled.
- The pins MODE0/MODE1 provide a weak pull down to prevent undefined active mode transitions.
- If the battery supply voltage is disconnected, the pins RxDx are floating
- The pin WAKE provides a weak pull up current towards supply voltage Vs to prevent local wake-up requests.
- The pin DIS_MAS provides a pull down current of 50uA.

9.8. TxDx faulty start protection

After power-on or wake-up a dominant level on TxDx will not lead to a dominant LINx level if the IC is being switched into an active mode. Only in case of recessive level before applying the first dominant level the transmit path will be enabled.

9.9. RxDx dominant time-out

A dominant LINx level longer than the specified time (typ. 40ms) indicates a faulty blocked bus. The master pull-up resistor of the affected LIN channel will be disconnected from the network in order to prevent thermal overload conditions or failure currents from the battery without any intervention from the microcontroller. Only a weak pull-up current (typ.60uA) is applied on the LIN bus. The RxD time-out will be reset with the next dominant -> recessive transition on the LIN bus if the failure disappears.
The RxDx time-out is only active in the Enhanced Master Mode, while the master termination is enabled.

9.10. TxDx dominant time-out

In case of a faulty blocked permanent dominant level on pin TxDx the transmit path will be disabled after the specified time t_{TxDx_to} (typ. 40ms). The data transmission is released again as soon as the failure disappears by the next rising edge of TxDx. The TxDx time-out is active in both, the *Standard Transceiver* and *Enhanced Master Mode*.

10. Application Example

10.1. Enhanced Master Mode

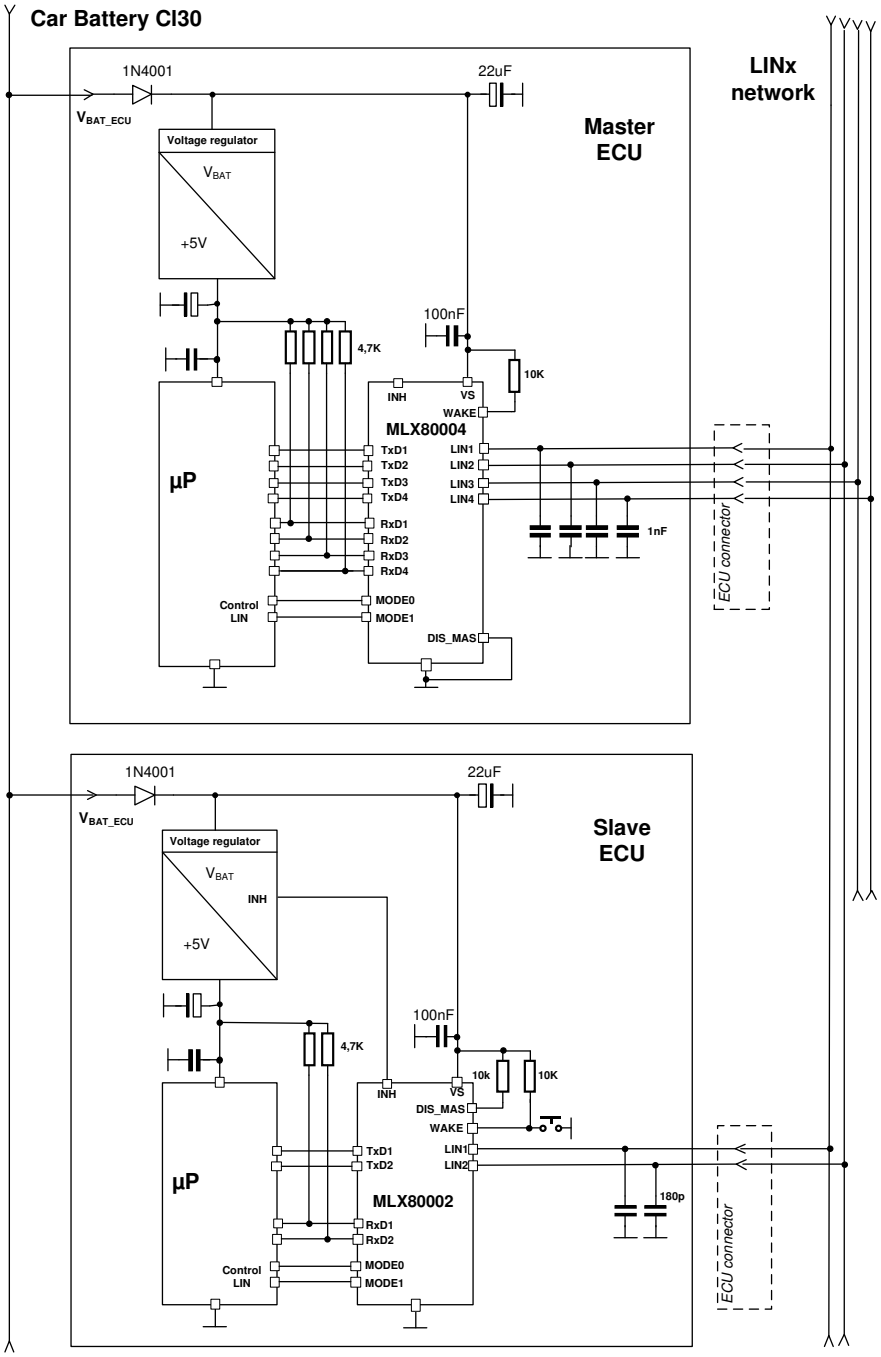

Figure 8:

Application example using enhanced master mode with minimized external components and LIN short to GND feature.

Note: All pins of MLX80004/MLX80002 with „N.C.“ are internally not connected.

10.2. Standard Transceiver Mode

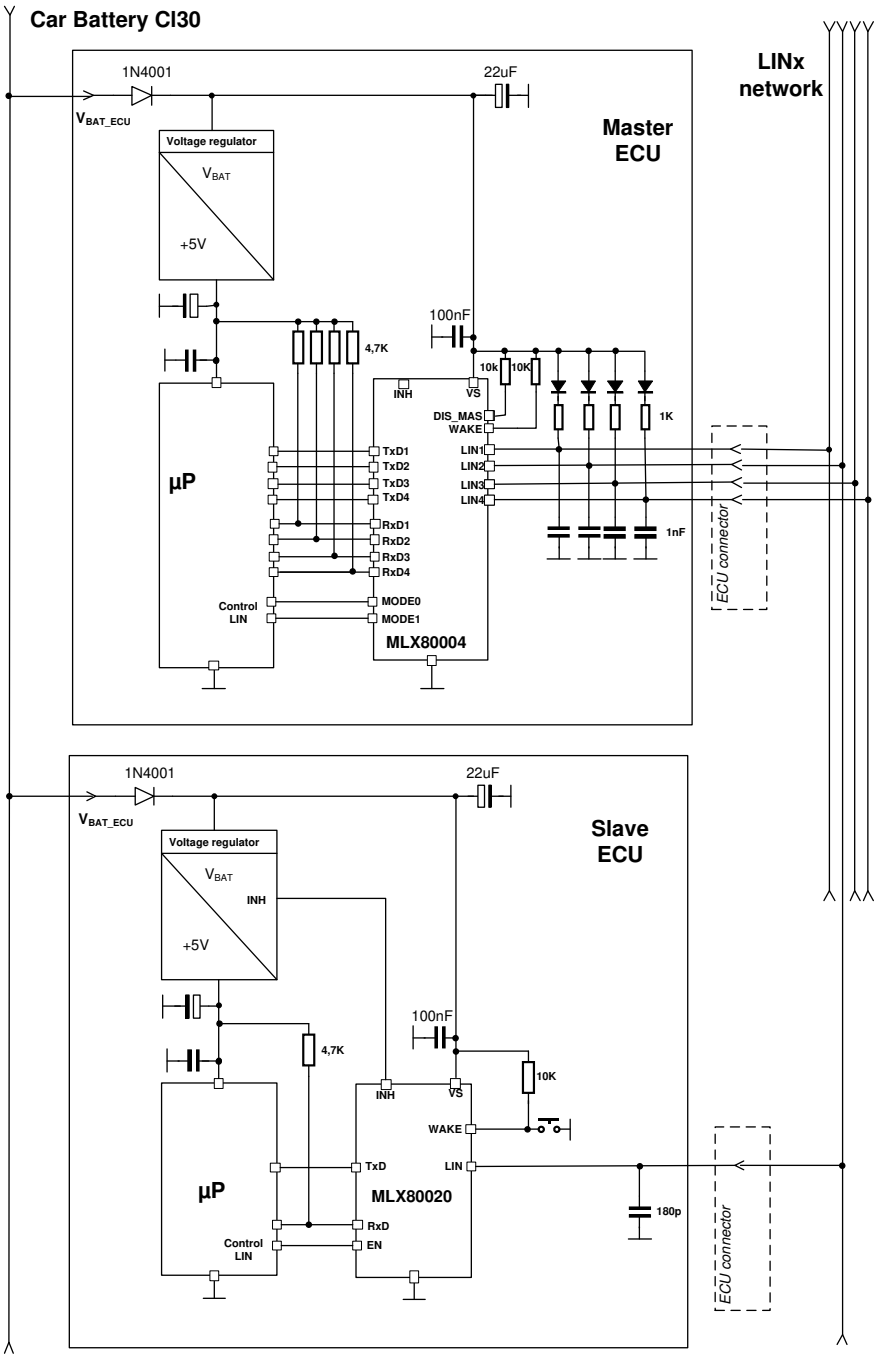

Figure 9:

Application example using standard transceiver mode without LIN short to GND feature.

Note: All pins of MLX80004/MLX80002 with „N.C.“ are internally not connected.