Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

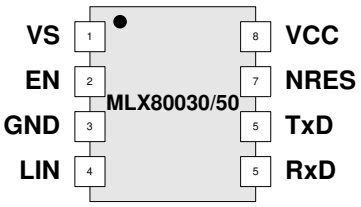
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MLX80050/51/30/31

LIN System Basis ICs

Datasheet

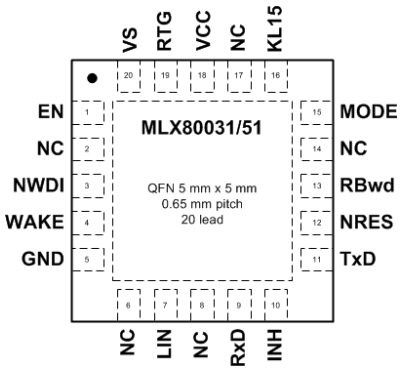


Features

- LIN 2.x / SAE J2602 compliant
- Operating voltage V_{SUP} = 5 ... 27 V
- 3 modes: Normal, Silent and Sleep
- Linear low drop voltage regulator:

  MLX80030/31:
  - Normal mode 3.3V/70mA ±2%
  - Silent mode 3.3V/20mA ±2%

  MLX80050/51:
  - Normal mode 5V/70mA ±2%
  - Silent mode 5V/20mA ±2
- Low current consumption (typ)
  - Sleep mode 20 µA
  - Silent mode “noload” 45 µA
- Output current limitation
- LIN-Bus Transceiver
  - Baud rate up to 20 kBaud
  - Slew rate control for best EME behaviour
  - Low slew mode for optimized SAE J2602 transmission
  - High impedance LIN pin in case of loss of ground or battery
  - Bus input voltages -24V to 30V independent from VBat
- Remote and local wake up source recognition
- VCC undervoltage detection at NRES output (start-up delay 4ms)
  - Vres threshold 3.0 V (MLX80030/31); Vres threshold 4.1V (MLX80050/51)
- Programmable Window Watchdog (only MLX80031/51)
- VSUP undervoltage detection (POR), Over temperature shutdown
- TxD dominant time out function, Standby mode time out after 350ms
- Automotive temperature range of –40°C to 125°C
- Interface I/O’s independent from voltage regulator output
- Enhanced ESD robustness according to IEC 61000-4-2
  - Direct discharge for pin LIN >20kV (only Lin cap connected) and for pin VBAT >15kV
  - Indirect discharge for pin LIN >15kV
- Load dump protected (40V)



Order Code	Temp. Range	Package	Delivery	Remark
MLX80050 KDC-CAA-000-RE	-40 - 125 °C	SOIC8	Reel	Silent Mode enabled
MLX80051 KLW-CAA-000-RE	-40 - 125 °C	QFN_WF20/5x5	Reel	Silent Mode enabled
MLX80030 KDC-CAA-000-RE	-40 - 125 °C	SOIC8	Reel	Silent Mode enabled
MLX80031 KLW-CAA-000-RE	-40 - 125 °C	QFN_WF20/5x5	Reel	Silent Mode enabled

Short Description

The MLX8005x/3x consist of a low-drop voltage regulator 5V/3.3V/70mA combined with a Reset/Watchdog unit and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conform to LIN specification revision 2.x and SAE J2602. The watchdog times of the integrated window watchdog can be adapted on application needs via external resistors. With the help of an external bipolar transistor it is possible to extend the output current of the integrated voltage regulator. The combination of voltage regulator and bus transceiver as well as watchdog unit makes it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

Contents

1. List of Tables

2. List of Figures

3. Electrical Specification

All voltages are referenced to ground (GND), positive currents flow into the IC.

Absolute Maximum Ratings

Table 1: Absolute maximum ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VS	V_S	Respective to GND	-0.3	40	V
Transient voltage ISO 7637/2		pulse 1, 2	-100	100	V
Transient voltage ISO 7637/2		pulse 3A; 3B, coupling 1nF	-150	100	V
DC voltage LIN	V_{LIN_DC}	Respective to GND and VS Loss of Ground (VGND = VS)	-20 -30	40 40	V
DC voltage WAKE	V_{WAKE_DC}	Respective to GND and VS Loss of Ground (VGND = VS)	-20 -30	40 40	V
DC voltage INH	V_{INH_DC}		-0.3	V_S+0.3	V
DC voltage VCC	V_{VCC_DC}		-0.3	7	V
DC voltage RTG	V_{RTG_DC}		-0.3	7	V
Input voltage at low voltage I/O's (EN, TxD, RxD, NRES, WDI, RB_{WD}, MODE)	V_{IN}		-0.3	7	V
ESD voltage	V_{ESDIEC}	IEC 61000-4-2, direct ESD Pin LIN with LIN cap 220pF Pin VS to GND	 20 15		kV
	$V_{ESDIECind}$	IEC 61000-4-2, indirect ESD Pin LIN with LIN cap 220pF	15		kV
	V_{ESDHBM}	HBM (CDF-AEC-Q100-002) Pin LIN Pin WAKE, KL15, VS Other pins	 ±6 ±4 ±2		 kV kV kV
	V_{ESDCDM}	CDM (AEC-Q100-011)	±500		V
Power dissipation	P_0		Internal limited, see also chapter 9.1		
Thermal resistance from junction to ambient	R_{THJA_SOIC8}	JEDEC 1s0p board, no air flow		150	K/W
	R_{THJA_QFN20}	JEDEC 1s0p board, no air flow		50	K/W
Junction temperature	T_J		-40	150	°C
Storage temperature	T_{STG}		-55	150	°C

3.1. DC Characteristics

Unless otherwise specified all values in the following tables are valid for V_S = 5 to 27V and T_{AMB} = -40 to 125°C. All voltages are referenced to ground (GND), positive currents flow into the IC.
For MLX80031/51 apply: RTG connected to VCC.

Table 2: Voltage Regulator and Reset Unit

	Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
Supply Voltage Pin VS								
	Nominal DC operating voltage	V_S		5		27	V	A
1.01	V_S under voltage reset	V_{SUVR_OFF}	V_S ramp up	4.1		5.0	V	A
1.02	V_S under voltage reset	V_{SUVR_ON}	V_S ramp down	3.7		4.8	V	A
1.03	V_S under voltage reset hysteresis	V_{SUVR_HYS}	V_{SUVR_OFF} - V_{SUVR_ON}	0.04	0.3	0.7	V	A
Supply currents MLX80030, MLX80050								
2.00	Supply current, normal mode	I_{VS_nor}	$V_S \leq 14V$, $V_{EN} > 2V$, LIN recessive, no load at VCC	400	750	1500	µA	A
2.01	Supply current, sleep mode	I_{VS_sleep}	$V_S \leq 14V$ T_A = -40 °C T_A = 25 °C $T_A \leq 85$ °C $T_A \leq 125$ °C		15	 30 20 30 45	µA	A
2.02	Supply current, silent mode	I_{VS_sil}	$V_S \leq 14V$, LIN recessive no load at VCC T_A = -40 °C T_A = 25 °C $T_A \leq 85$ °C $T_A \leq 125$ °C		65	 85 95 100 125	µA	A
Supply currents MLX80031, MLX80051								
2.00	Supply current, normal mode	I_{VS_nor}	$V_S \leq 14V$, $V_{EN} > 2V$, RB_{WD} = 60k LIN recessive, no load at VCC	400	750	1500	µA	A
2.01	Supply current, sleep mode	I_{VS_sleep}	$V_S \leq 14V$ T_A = -40 °C T_A = 25 °C $T_A \leq 85$ °C $T_A \leq 125$ °C		15	 30 20 30 45	µA	A
2.02	Supply current, silent mode	I_{VS_sil}	$V_S \leq 14V$, LIN recessive no load at VCC T_A = -40 °C T_A = 25 °C $T_A \leq 85$ °C $T_A \leq 125$ °C		65	 85 95 100 125	µA	A

Voltage Regulator Pin VCC								
MLX80050, MLX80051 (RTG connected to VCC)								
3.01	Output voltage VCC	V_{CCn5}	$6V \le V_S \le 18V$ $1mA \le I_{LOAD} \le 70mA$ $T_A = 25°C$ $T_A = -40°C$ to $125°C$	4.90 4.85	5.0	5.10 5.15	V	A
	Output voltage VCC under disturbances functional state A	$V_{CCndis5}$	$6V \le V_S \le 18V$, $T_A = 25°C$ $R_{LOAD} = 330\ \Omega$	4.75		5.25	V	C
3.02	Drop-out voltage [2]	V_{D10_5}	$V_S > 4V$, $I_{VCC} = 10mA$		75	120	mV	C
3.03		V_{D30_5}	$V_S > 4V$, $I_{VCC} = 30mA$		220	350	mV	C
3.04		V_{D70_5}	$V_S > 4V$, $I_{VCC} = 70mA$		500	800	mV	C
3.05	Line regulation	V_{LNR5}	$6V \le V_S \le 18V$, $I_{VCC} = 30mA$ $6V \le V_S \le 18V$, $I_{VCC} = 70mA$			20 100	mV	A
3.06	Load regulation	V_{LDR10_5}	$1\ mA < I_{LOAD} < 10\ mA$			50	mV	A
3.07		V_{LDR30_5}	$1\ mA < I_{LOAD} < 30\ mA$			90	mV	A
3.08		V_{LDR70_5}	$1\ mA < I_{LOAD} < 70\ mA$			150	mV	A
3.09	Output current limitation [3]	I_{VCCLIM_5}	$V_S > 6V$ $T_A = -40\ °C$ $25\ °C \le T_A \le 125\ °C$	-135 -150	-110	-75 -80	mA	A
3.10	Load capacity	C_{LOAD}		2.2	22		µF	D
MLX80030, MLX80031 (RTG connected to VCC)								
3.01	Output voltage VCC	V_{CCn3}	$4\ V \le V_S \le 18\ V$ $1m\ A \le I_{LOAD} \le 70\ mA$ $T_A = 25\ °C$ $T_A = -40\ °C$ to $125\ °C$	3.234 3.201	3.3	3.366 3.399	V	A
	Output voltage VCC under disturbances functional state A	$V_{CCndis3}$	$6\ V \le V_S \le 18\ V$, $T_A = 25\ °C$ $R_{LOAD} = 330\ \Omega$	3.135		3.465	V	C
3.02	Drop-out voltage [2]	V_{D10_3}	$V_S > 3\ V$, $I_{VCC} = 10\ mA$			100	mV	C
3.03		V_{D30_3}	$V_S > 3\ V$, $I_{VCC} = 30\ mA$			300	mV	C
3.04		V_{D70_3}	$V_S > 3\ V$, $I_{VCC} = 70\ mA$			700	mV	C
3.05	Line regulation	V_{LNR_3}	$5\ V \le V_S \le 18\ V$, $I_{VCC} = 30mA$ $5V \le V_S \le 18V$, $I_{VCC} = 70mA$			20 100	mV	A
3.06	Load regulation	V_{LDR10_3}	$1\ mA < I_{LOAD} < 10\ mA$			50	mV	A
3.07		V_{LDR30_3}	$1\ mA < I_{LOAD} < 30\ mA$			90	mV	A
3.08		V_{LDR70_3}	$1\ mA < I_{LOAD} < 70\ mA$			150	mV	A
3.09	Output current limitation [3]	I_{VCCLIM_3}	$V_S > 4\ V$ $T_A = -40\ °C$ $25\ °C \le T_A \le 125\ °C$	-135 -150	-110	-75 -80	mA	A
3.10	Load capacity	C_{LOAD}		2.2	22		µF	D

Output Pin NRES								
4.01	Output voltage low	V_{OL_NRES}	I_{NRES} = 1 mA			0.25	V	A
4.02	Leakage current low	I_{leak_RxD}	V_{NRES} = 0 V	-5		5	µA	A
4.03	Leakage current high	I_{leak_RxD}	V_{NRES} = V_{CC}	-5		5	µA	A
	Output voltage high NRES under disturbances to fulfil functional state A	V_{OH_NRES}	R_{load} = 2.7 k to VCC	V_{CC} -1			V	C
MLX80050, MLX80051								
5.01	VCC reset threshold on NRES pin	V_{RES5V}	t > t_{rr}	3.9	4.10	4.3	V	A
5.02	V_{RES} Hysteresis V_{RESHYS} = |$V_{RES(ON)}$ – $V_{RES(OFF)}$|	$V_{RESHYS5V}$				200	mV	C
MLX80030, MLX80031								
5.01	VCC reset threshold on NRES pin	V_{RES3V}	t > t_{rr}	2.75	2.95	3.15	V	A
5.02	V_{RES} Hysteresis V_{RESHYS} = |$V_{RES(ON)}$ – $V_{RES(OFF)}$|	$V_{RESHYS3V}$				100	mV	C
Input Pin EN								
6.01	Input voltage low	V_{IL_EN}				0.8	V	A
6.02	Input voltage high	V_{IH_EN}		2.0			V	A
6.03	Hysteresis	V_{HYS_EN}		50	100	700	mV	C
6.04	Pull-down resistor	R_{pd_EN}	V_{EN} =VCC	50	125	250	kΩ	A
Input Pin WAKE (MLX80031, MLX80051)								
7.01	High level input voltage	V_{IH_WAKE}	Sleep mode	V_S-1V			V	A
7.02	Low level input voltage	V_{IL_WAKE}	Sleep mode			V_S-3.3V	V	A
7.03	Pull up current WAKE	I_{WAKE_PU}	Normal & sleep	-30	-15	-1	µA	A
7.04	Leakage current WAKE high	I_{WAKE_lk}	V_S = 18V	-5		5	µA	A
Input Pin KL15 (MLX80031, MLX80051)								
8.01	High level input voltage	V_{IH_KL15}	Rv = 50kΩ	4		V_S+0.3V	V	A
8.02	Low level input voltage	V_{IL_KL15}	Rv = 50kΩ	-1		2	V	A
8.03	Pull down current KL15	I_{KL15_PD}			30	65	µA	A
Input Pin MODE (MLX80031, MLX80051)								
23.01	Input voltage low	V_{IL_MODE}				0.8	V	A
23.02	Input voltage high	V_{IH_MODE}		2.0			V	A
23.03	Hysteresis	V_{HYS_MODE}		50	100	600	mV	C
23.04	Pull-down resistor	R_{pd_MODE}	V_{MODE} = VCC	200		600	kΩ	A

Input Pin NWDI (MLX80031, MLX80051)								
9.01	Input voltage low	V_{IL_NWDI}				0.8	V	A
9.02	Input voltage high	V_{IH_NWDI}		2.0			V	A
9.03	Hysteresis	V_{HYS_NWDI}		50	100	600	mV	C
9.04	Pull-up resistor to VCC	R_{pu_NWDI}	VN_{WDI} = 0V	125	250	375	kΩ	A
9.05	Min low pulse width	T_{minlow_NWDI}	one WD_OSC clock period	1			1	D
Watchdog Oscillator pin RBWD (MLX80031, MLX80051)								
10.01	Voltage at RB_{WD}	V_{RBwd}	I_{OUT} = -50 µA		1.2		V	A
10.02	Range of RB_{WD} resistance	RB_{WD}		20		150	kΩ	B
10.03	RB_{WD} short resistance threshold to enable fail-safe state	RB_{WDSH}	see paragraph 7.3	0		330	Ω	B
Output INH (MLX80031, MLX80051)								
11.01	ON Resistance	R_{ON_INH}	V_S = 12V		20	60	Ω	A
11.02	Leakage current INH high	I_{leakH_INH}	Sleep Mode, V_{INH} = 18V, V_S = 18V	-5		5	µA	A
11.03	Leakage current INH low	I_{leakL_INH}	Sleep Mode, V_{INH} = 0V, V_S = 18V	-5		5	µA	A
Thermal Protection								
	Thermal shutdown	T_{JSHD}		155	170	190	°C	D
	Thermal hysteresis	T_{JHYS}			10	30	°C	D

Notes:

[1] A = 100% serial test, B = Operating parameter, C = characterization data, D = Value guaranteed by design

[2] The nominal VCC voltage is measured at VSUP = 12V. If the VCC voltage is 100mV below its nominal value then the voltage drop is VD = VSUP – VCC

[3] Functionality range of current limitation at silent mode is limited by reset threshold VRES. Below them the IC change to normal mode.

Validity for IVCC_MAXsil: VCCn (min) ≤ VCC ≤ VRES

Table 3: LIN DC Characteristics

Parameter		Symbol	Condition	Min	Typ	Max	Unit	T[1]
General								
12.01	Pull up current LIN (recessive)	$I_{INLINpu}$	V_{LIN} = 18 V, V_S = 6V			80	µA	A
12.02	Pull up resistor LIN	R_{LINpu}	V_S = 12V, V_{LIN} = 0V	20	30	60	kΩ	A
12.03	Reverse current LIN (dominant)	$I_{INLINdom}$	V_S = 12V, V_{LIN} = 0V	-400			µA	A
12.04	Reverse current LIN (recessive)	$I_{INLINrec}$	$V_{LIN} \geq V_S$, 8V ≤ V_{LIN} ≤ 18V, 8V ≤ V_S ≤ 18V	0		23	µA	A
12.05	Reverse current LIN (loss of battery)	I_{INLIN_lob}	V_S = 0V, 0V ≤ V_{LIN} ≤ 18V	0		23	µA	A
12.06	Reverse current LIN (loss of ground)	I_{INLIN_log}	V_S= 12V, 0V ≤ V_{LIN} ≤ 18V	-10		50	µA	A
	Voltage drop serial Diode	$V_{SerDiode}$		0.4	0.7	1.0	V	D
	Battery Shift	V_{Shift_BAT}	related to VS	0		11.5	%	D
	Ground Shift	V_{Shift_GND}	related to VS	0		11.5	%	D
	Ground-Battery shift difference	V_{Shift_diff}	related to VS	0		8	%	D
Receiver								
12.07	Receiver dominant voltage	V_{BUSdom}	7.0 V ≤ V_S ≤ 18 V			0.4*V_S	V	A
	Receiver recessive voltage	V_{BUSrec}		0.6*V_S				A
12.08	Centre point of receiver threshold V_{thr_cnt} = (V_{thr_rec}+V_{thr_dom})/2	V_{thr_cnt}		0.475*V_S	0.5*V_S	0.525*V_S		A
12.09	Receiver Hysteresis V_{hys} = V_{thr_rec}-V_{thr_dom}	V_{hys}			0.15*V_S	0.175*V_S		A
Transmitter								
12.10	Transmitter dominant voltage	Vol_{bus}	R_{load} = 500Ω, V_S = 5V	0		1.2	V	D
			R_{load} = 500Ω, V_S >= 7V	0		0.2*V_S		A
12.11	Current limitation LIN	I_{LIM}	V_{LIN} = V_S, TxD = 0V	40	120	200	mA	A
12.12	Transmitter recessive voltage	Voh_{BUS}	No load, V_{EN} = 0/5V, VTxD = 5V	0.8*V_S		V_S	V	A

Input/Output Pin TxD								
13.01	Input voltage low TxD	V_{IL_TxD}	rising			0.8	V	A
13.02	Input voltage high TxD	V_{IH_TxD}		2			V	A

13.03	Hysteresis	V_{HYS_TxD}		50		700	mV	C
13.04	Pull-up resistor to VCC	R_{pu_TxD}	V_{TxD} = 0V	125	250	375	kΩ	A
13.06	Low level output current	I_{OL_TxD}	local wake-up request; standby mode; V_{TxD} = 0.4V	1.5			mA	A
Output Pin RxD								
14.01	Output voltage low RxD	V_{OL_RxD}	I_{RxD} = 2 mA			0.6	V	A
14.02	Pull-up resistor to VCC	R_{pu_RxD}	V_{RxD} = 0V	3	5	7	kΩ	A
14.03	Leakage current high	I_{leak_RxD}	V_{RxD} = VCC	-5		5	µA	A
	Output voltage high RxD under disturbances to fulfil functional state A	V_{OH_RxD}	R_{load} = 2.7k to VCC	V_{CC} -1			V	C

Notes:

[1] A = 100% serial test, B = Operating parameter, C = characterization data, D = Value guaranteed by design

3.2. AC Characteristics

6V ≤ V_S ≤ 27V, -40°C ≤ T_A ≤ 125°C, RTG connected to VCC, unless otherwise specified

Table 4: AC Characteristics

Parameter		Symbol	Condition	Min	Typ	Max	Unit	T[1]
Reset parameter on NRES								
16.01	Reset time	t_{Res}	V_S = 14V	2.5	4	5.5	ms	A
16.02	Reset rising time	t_{rr}	V_S = 14V	3.0	6.5	12	µs	A
Watchdog parameter on NRES (MLX80031, MLX80051)								
17.01	Watchdog-Oscillator Period	$t_{WDOSC20}$	RB_{WD} = 20kΩ ±1%	6.87	8.09	9.30	µs	A
17.02		$t_{WDOSC60}$	RB_{WD} = 51kΩ ±1%	16.06	18.90	21.73	µs	A
17.03		$t_{WDOSC100}$	RB_{WD} = 100kΩ ±1%	30.58	35.98	41.37	µs	A
17.04		$t_{WDOSC150}$	RB_{WD} = 150kΩ ±1%	45.40	53.41	61.42	µs	A
	Watchdog Close Window	t_{CW}	tCW = cycles * tWDOSC		1053		cycles	D
	Watchdog Open Window	t_{OW}	tOW = cycles * tWDOSC		1105		cycles	D
17.05	Watchdog Reset Low Time	t_{WDres}		3	4	5	ms	A
	Watchdog Lead Window	t_{LDT}	tOWS = cycles * tWDOSC		7895		cycles	D
17.06	Watchdog Safety Oscillator	$t_{WDsafety}$	RBWD open / RBWD gnd	30	50	75	µs	A

Parameter		Symbol	Condition	Min	Typ	Max	Unit	T[1]
Wake-up and Mode Control								
18.01	Remote Wake-up filter time	t_{wu_remote}		30	70	150	µs	A
18.02	Wake-up filter time on WAKE (only MLX80051,MLX80031)	t_{wu_WAKE}	Sleep or Silent Mode, WAKE falling edge	10		50	µs	A
18.03	Wake-up filter time on KL15 (only MLX80051,MLX80031)	t_{wu_KL15}	Sleep or Silent Mode, KL15 rising edge	80	168	250	µs	A
18.04	Propagation delay from Normal Mode to Sleep Mode via EN	t_{pd_sleep}	V_{EN} = 0V	5	15	20	µs	A
18.05	Propagation delay from Standby Mode to Normal Mode via EN	t_{pd_norm}	V_{EN} = 5V	5	15	20	µs	A
18.06	Propagation delay from Silent Mode to Normal Mode via EN	$t_{pd\_sil\_n}$	V_{EN} = 5V Silicon Revision C	5	15	40	µs	A
18.07	Propagation delay: go to silent mode after EN=H/L	t_{pd_sil}	check falling edge on RBwd, EN = 0V Silicon Revision C			20	µs	A
	Setup time TxD to EN for low slew mode	$t_{set\_TxD\_EN}$		5			µs	B
	Hold time TxD after EN for low slew mode	$t_{hold\_TxD\_EN}$		20			µs	B
18.08	Debouncing time EN	t_{deb_EN}		2	5	20	µs	A
18.09	TxD dominant time out	t_{TxD_to}	Normal Mode, V_{TxD} = 0V	27		60	ms	A
18.10	Standby time out	t_{sby_to}	Standby Mode, V_{EN}= 0V	150		500	ms	A
18.11	Wake up time vs. EN	t_{wu_EN}	Wake form sleep via EN=L/H	2	5	20	µs	A
General LIN Parameter								
19.01	Receiver propagation delay LIN -> RxD	t_{dr_RxD} t_{df_RxD}	$C_{L(RXD)}$ = 50 pF			6	µs	A
19.02	Symmetry prop. delay LIN->RxD	t_{dsym_RxD}	t_{dr_RXD} - t_{df_RXD}	-2		2	µs	A
19.03	Receiver debouncing time	t_{deb_LIN}		1.5	2.8	4.0	µs	D

19.04	slew rate rising edge LIN	dV/dTrise	Normal Mode LIN-Load: 1kΩ/1nF	1.0	1.5	2.5	V/µs	C
19.05	slew rate falling edge LIN	dV/dTfall		-2.5	-1.5	-1.0	V/µs	C
19.06	slew rate rising edge LIN	dV/dTrise	Low Slew Mode LIN-Load: 1kΩ/1nF	0.3	0.8	1.3	V/µs	C
19.07	slew rate falling edge LIN	dV/dTfall		-1.3	-0.8	-0.3	V/µs	C
	Internal capacity	C_{LIN}	Pulse at LIN via 10kOhm with 0/10V; VS = open		25	35	pF	D
LIN transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (20kbit/s)								
Conditions:	Normal slew mode; V_S =7.0V to 18V; LIN loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF TxD signal: t_{Bit} = 50µs, t_{wH} = T_{wL} = t_{Bit}; t_{rise} = t_{fall} < 100ns							
	Minimal recessive bit time	$t_{rec(min)}$		40	50	58	µs	
	Maximum recessive bit time	$t_{rec(max)}$		40	50	58	µs	
20.01	Duty cycle 1	D_1	$D_1 = t_{rec(min)} / (2*t_{Bit})$	0.396				A
20.02	Duty cycle 2	D_2	$D_2 = t_{rec(max)} / (2*t_{Bit})$			0.581		A
Transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (10.4kbit/s)								
Conditions:	Low slew mode; V_S =7.0V to 18V; LIN loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF TxD signal: t_{Bit} = 96µs, t_{wH} = T_{wL} = t_{Bit}; t_{rise} = t_{fall} < 100ns							
	Minimal recessive bit time	$t_{rec(min)}$		80	96	113	µs	
	Maximum recessive bit time	$t_{rec(max)}$		80	96	113	µs	
21.01	Duty cycle 1	D_3	$D_3 = t_{rec(min)} / (2*t_{Bit})$	0.417				A
21.02	Duty cycle 2	D_4	$D_4 = t_{rec(max)} / (2*t_{Bit})$			0.590		A
LIN transceiver parameter according to SAE J2602 (10.4kbit/s)								
Conditions:	Low slew mode; V_S =7.0V to 18V; LIN loads: 1kΩ/1nF;660Ω/6.8nF;500Ω/10nF TxD signal: t_{Bit} = 96µs, t_{wH} = T_{wL} = t_{Bit}; t_{rise} = t_{fall} < 100ns							
22.01	Minimal recessive delay TxD -> LIN	$t_{x\_rec\_min}$				48	µs	A
22.02	Maximum recessive delay TxD -> LIN	$t_{x\_rec\_max}$				48	µs	A
22.03	Minimal dominant delay TxD -> LIN	$t_{x\_dom\_min}$				48	µs	A
22.04	Maximum dominant delay TxD -> LIN	$t_{x\_dom\_max}$				48	µs	A
22.05	Maximum rec. to dom. delay	$T_{r\_d\_max}$	$t_{x\_rec\_max}$ - $t_{x\_dom\_min}$			15.9	µs	A
22.06	Maximum dom. to rec. delay	$T_{d\_r\_max}$	$t_{x\_dom\_max}$ - $t_{x\_rec\_min}$			17.2	µs	A

Notes:

[1] A = 100% serial test, B = Operating parameter, C = characterization data, D = Value guaranteed by design

3.3. Timing diagrams

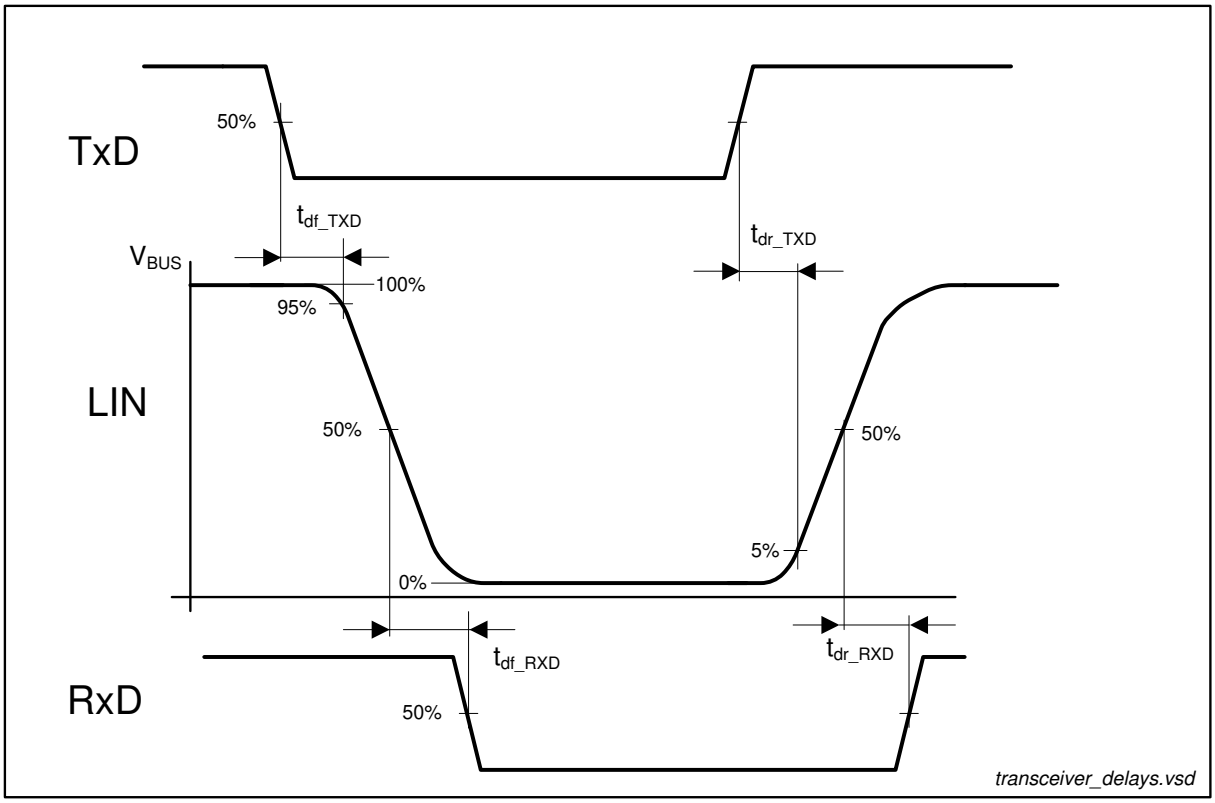


Figure 1: LIN propagation delays

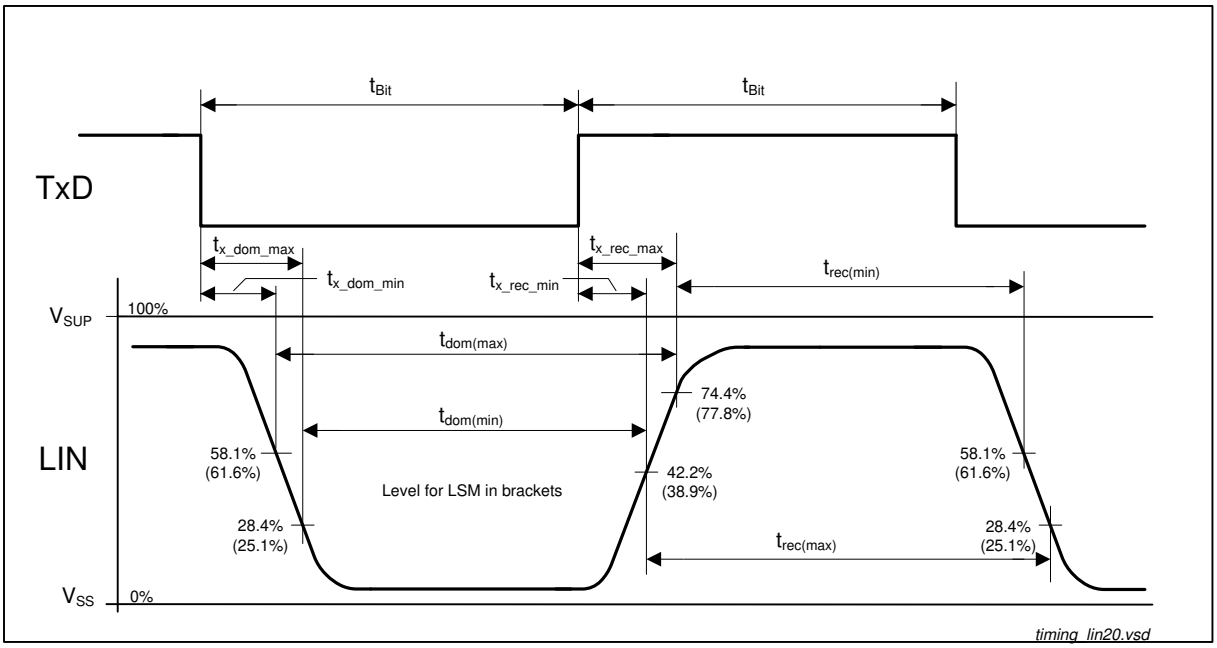


Figure 2: LIN duty cycles

4. Pin Configuration

4.1. MLX80030 and MLX80050 - SOIC8

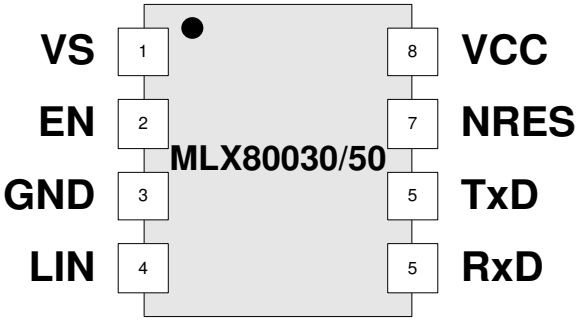


Table 5: MLX80050/30 pin list in SOIC8

Pin	Name	IO-Typ	Description
1	VS	P	Battery supply voltage
2	EN	I	Mode control pin, enables the normal operation mode when HIGH
3	GND	G	Ground
4	LIN	I/O	LIN bus transmitter/receiver pin, (low = dominant)
5	RxD	I/O	Received data from LIN bus, low in dominant state; internal pull-up resistor
6	TxD	I/O	Transmit data input (low = dominant)
7	NRES	O	Undervoltage reset output (open drain), low active
8	VCC	P	Voltage regulator output

4.2. MLX80031 and MLX80051 in QFN20

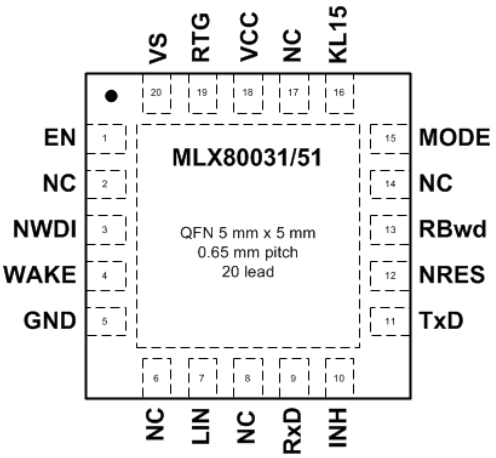


Table 6: MLX80051/31 pin list in QFN20

Pin	Name	IO-Typ	Description
1	EN	I	Mode control pin, enables the normal operation mode when HIGH
2	NC		not connected
3	NWDI	I	Watchdog trigger input; negative edge; pull-up
4	WAKE	I	High voltage input for local wake up, negative edge triggered
5	GND	G	Ground
6	NC		not connected
7	LIN	I/O	LIN bus transmitter/receiver pin, (low = dominant)
8	NC		not connected
9	RxD	I/O	Received data from LIN bus, low in dominant state; internal pull-up resistor
10	INH	O	High side switch; High voltage
11	TxD	I/O	Transmit data input (low = dominant)
12	NRES	O	Reset output (open drain), low active
13	RB_{WD}	I/O	Bias resistor for watchdog oscillator
14	NC		not connected
15	MODE	I	Input to control window watchdog
16	KL15	I	High voltage input for local wake up, positive edge triggered
17	NC		not connected
18	VCC	I	Voltage regulator sense input
19	RTG	P	Voltage regulator output
20	VS	P	Battery supply voltage
	EP	G	Exposed pad should be connected to Ground

3. Functional Description

The MLX8003x/5x consists of a low drop 3.3V/5V voltage regulator capable to drive 70mA and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller. Additionally integrated is a Window-Watchdog/RESET unit with a fixed power-on-reset delay of 4 ms and an adjustable watchdog time defined by an external bias resistor.

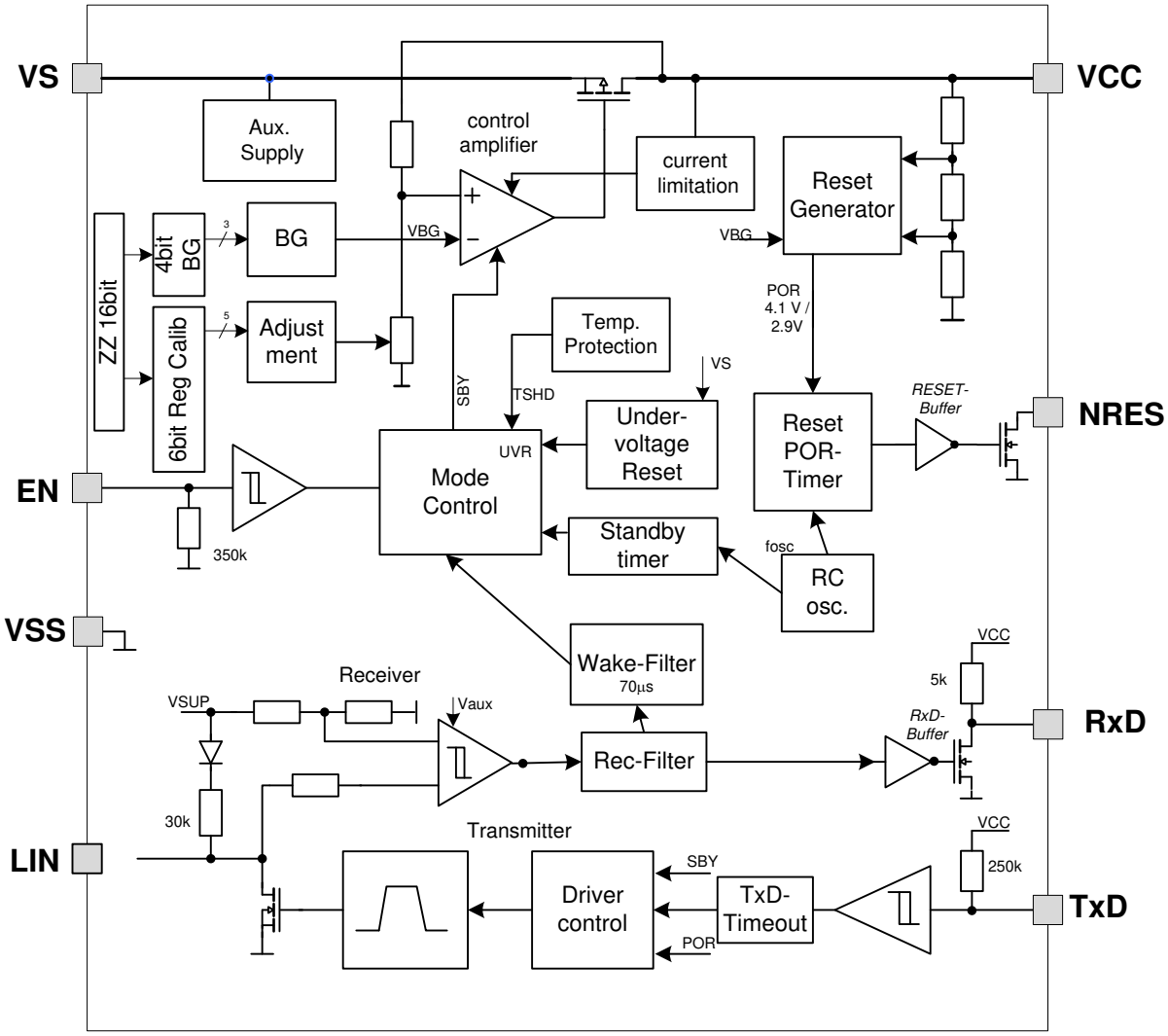


Figure 3: MLX80050/30 Block Diagram

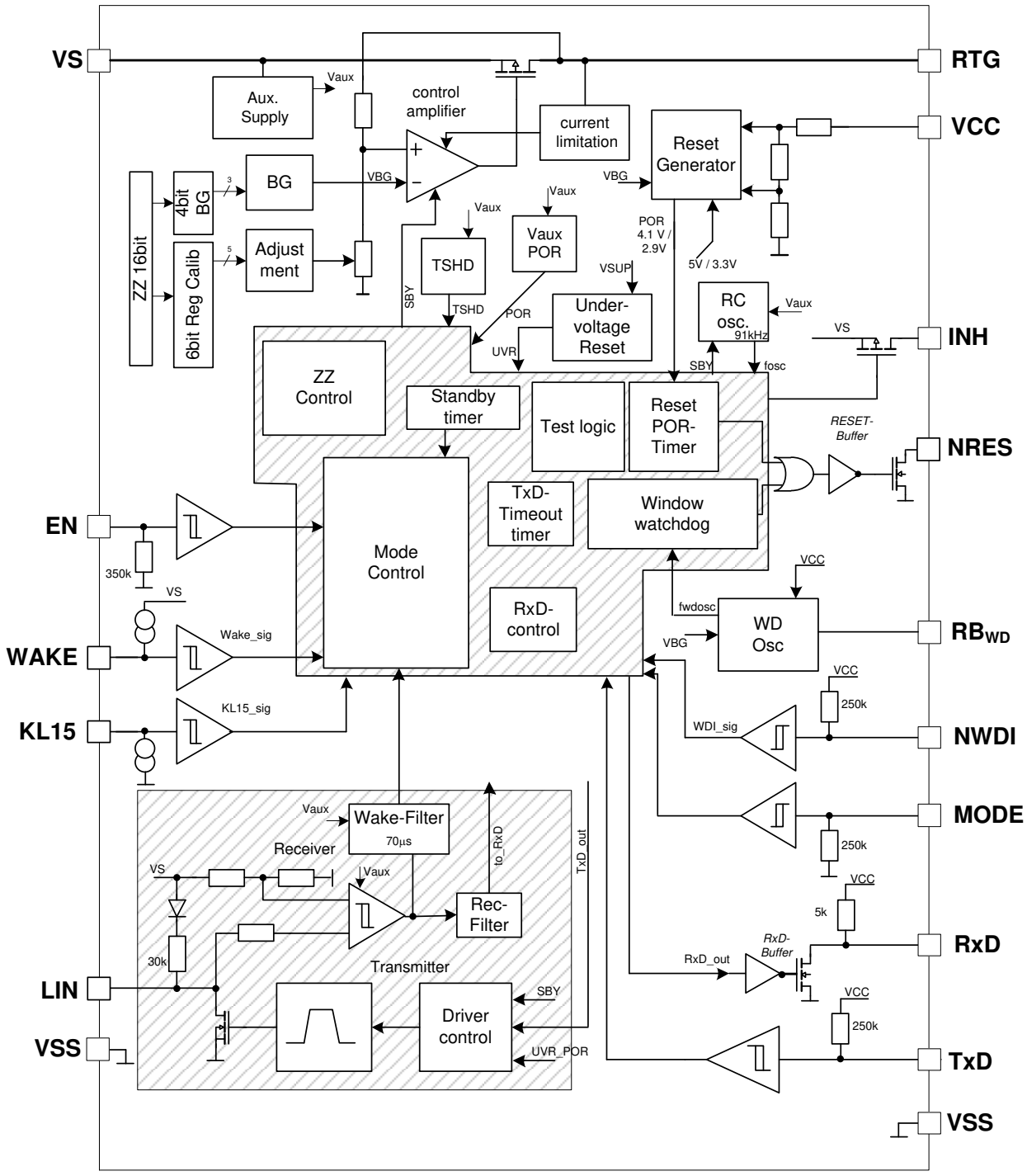


Figure 4: MLX80051/31 Block Diagram

3.1. Supply Pin VS

VS is the operational voltage pin of MLX8005x/3x. The voltage range is VS = 6 to 18V. After switching on VS, the MLX8003x/5x starts at Standby Mode and the VCC voltage regulator ramps up. An undervoltage detection unit prevent an undefined operation for Vs < 4V.

VS- Power-ON

If VS is switched on, the MLX8003x/5x starts in Standby Mode. A combination of dynamic POR and under voltage reset circuitry generates a POR signal, which switches the MLX8003x/5x on. This power on behaviour is independent from the status of the EN-pin.

Power-on reset and under-voltage reset operate independent from each other, which secures the independence from the rise time of VS.

3.2. EN input pin

The ENable input is the mode control pin of MLX8003x/5x in combination with the TxD input.

The MLX8003x/5x is switched into the Sleep Mode with a falling edge and into normal mode with a rising edge at the EN pin. The state machine goes to Normal Mode after t_{Res} (see also Table 4: AC Characteristics). The Normal Mode will be kept as long as EN remains high.

The Normal Mode can be entered from Standby Mode, when the pin EN is driven HIGH. To prevent unwanted mode transitions, the EN input contains a debounce filter as specified (t_{EN_deb}).

The pin EN contains a weak pull down resistor. The input thresholds are compatible to 3.3V and 5V supply systems.

MLX80031/51:

Additionally the positive edge on pin EN results in an immediate reset of the active low interrupt on pin RxD as well as the wake-up source recognition flag on pin TxD.

3.3. Ground pin GND

This is the reference pin of the IC. The absence of GND connection will not influence or disturb the communication between other LIN bus nodes.

3.4. LIN

This bidirectional pin consists of a low side driver in the output path and a high-voltage comparator in the input path. Furthermore is integrated a LIN pull-up resistor between LIN and VS pin. Low side driver consist a current limitation.

3.5. Receiver Output RxD

The pin RxD is a buffered open drain output. Output signals can be shifted by the external pull up resistor to 3.3V and 5V supply systems.

3.6. Transmit Input TxD

The transmit data stream of the LIN protocol controller applied to the pin TxD is converted into the LIN bus signal with slew rate control in order to minimize electromagnetic emissions.

The pin TxD contains a weak pull up resistor. The input thresholds are compatible to 3.3V and 5V supply systems. To enable the transmit path, the TxD pin has to be driven recessive (HIGH) after or during the normal mode has been entered.

3.6.1. TxD dominant time-out feature

With the first dominant level on pin TxD after the transmit path has been enabled, the dominant time-out counter is started. In case of a faulty blocked permanent dominant level on pin TxD the transmit path will be disabled after the specified time t_{TxD_to}. The time-out counter is reset by the first negative edge on pin TxD.

3.7. Output NRES

The NRES pin outputs the reset state as well as the watchdog condition in MLX80031 and MLX80051.

3.8. Voltage regulator pins VCC and RTG

The MLX80030/50 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±2% (MLX80050/51) or 3.3V ±2% (MLX80030/31) with a load current of max. 70mA. The current limitation unit limits the output current for short circuits or overload to 130mA by decreasing the VCC voltage. This way the power dissipation is held constant at a maximum value.

The voltage regulator has two pins, output pin RTG and sense input pin VCC. For MLX80030/50 both, RTG and VCC, are commonly bonded to pin VCC on the package.

Devices MLX80031/51 has both pins bonded and provides the possibility to use an external npn transistor to boost the maximum load current. In this case the basis of the npn transistor has to be connected to the RTG pin and the emitter to the VCC pin. In case of using the internal voltage regulator, both pins have to be connected to each other.

3.9. INH Output (only MLX80031/51)

INH switches to high (VS connected to INH) in case of Standby or Normal Mode. INH is switched off at Silent and Sleep Mode. The pin will be used for switch on an external power supply or for switch off the external 1k master resistor in master node applications.

3.10. WAKE Input (only MLX80031/51)

High voltage input pin for local wake-up functionality. With a falling edge on WAKE the IC wakes-up from Silent Mode or Sleep Mode to Standby Mode.

The pin WAKE provides a weak pull up current source towards Vs which provides a HIGH level on the pin in case of open circuit failures or if no local wake-up feature is required. In such applications it is recommended to connect the pin WAKE directly to pin Vs in order to prevent influences due to EMI.

3.11. KL15 Input (only MLX80031/51)

High voltage input pin for local wake-up functionality. With a rising edge on KL15 the IC wakes-up from Silent Mode or Sleep Mode to Standby Mode.

The pin KL15 provides a weak current sink towards GND which provides a LOW level on the pin in case of open circuit failures or if no local wake-up feature is required. In such applications it is recommended to connect the pin KL15 directly to GND in order to prevent influences due to EMI. KL15 is typically connected to the ignition terminal and generates a local wake-up at start of ignition.

3.12. Watchdog Trigger Input NWDI (only MLX80031/51)

This input is used to trigger the integrated window watchdog in MLX80031/51. Every falling edge on NWDI in watchdog open window is used to reset the watchdog timer. An internal pull up resistor of 250k secures a stable high condition if this pin is open. The NWDI input is a low voltage CMOS input. The minimum low time of NWDI is one WD_OSC clock period to allow falling edge detection.

3.13. Watchdog Oscillator Resistor RB_{WD} (only MLX80031/51)

A resistor between RBWD and GND defines the window watchdog times as trigger time.

3.14. Mode Input MODE (only MLX80031/51)

Special pin for to disable the window watchdog function. For normal watchdog operation connect the MODE pin to GND directly or via external resistor. With MODE pin on 3.3V/5V the window watchdog is switched off.

4. Operational Modes

The MLX8003x/5x provides four main operating modes “Standby”, “Normal”, “Silent” and “Sleep”. The main modes are fixed states defined by basic actions (VS start, EN or wake-up).

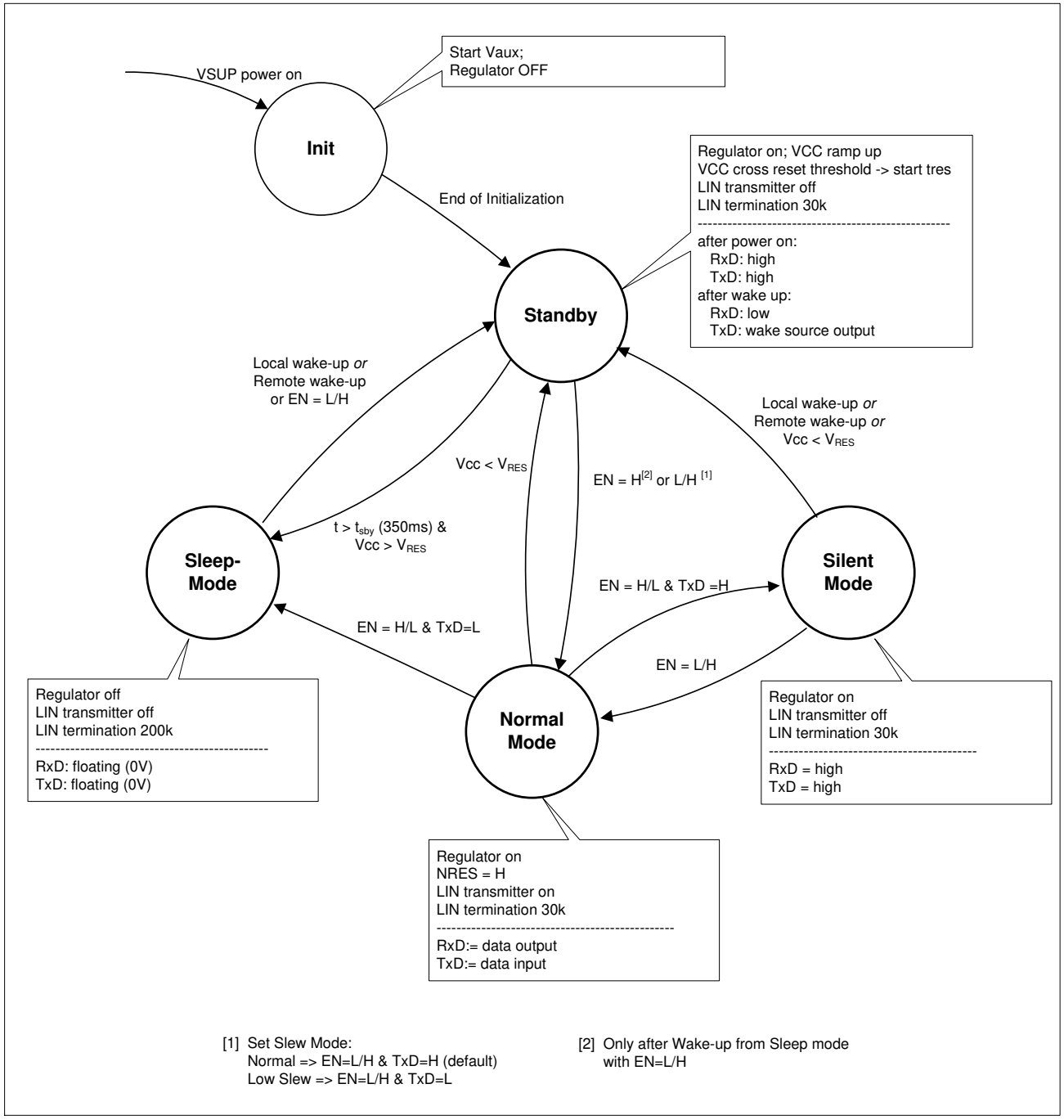


Figure 5: MLX8005x3x state diagram of modes of operation

4.1. Modes Overview

Table 7: MLX80050/30 Operation Modes

Mode	VCC	TxD	RxD	LIN	remarks
Standby	3.3V/5V	high	high	recessive	entered after power on or wake up
Normal	3.3V/5V	input for transmit data stream	output for LIN data stream	follows TxD	[1]
Silent	3.3V/5V	high	high	recessive	high = 3.3V/5V
Sleep	0	floating	floating	recessive	remote wake up to enter Standby Mode, EN = H to go to Normal Mode

[1] Normal mode will be entered form Standby Mode by a low -> high transition on pin EN and from Sleep Mode by EN = H after startup of the regulator. When recessive level (high) on pin TxD is present the transmit path will be enabled

Table 8: MLX80051/31 Operation Modes

Mode	VCC	TxD	RxD	LIN	INH	Watchdog	remarks
Standby	3.3V/5V	High/ active low[1]	high/ active low[2]	recessive	ON	ON	entered after power on or wake up
Normal	3.3V/5V	input for transmit data stream	output for LIN data stream	follows TxD	ON	ON	[3] [4] [5]
Silent	3.3V/5V	high	high	recessive	OFF	OFF	
Sleep	0	floating	floating	recessive	OFF	OFF	Local or remote wake up to enter Standby Mode, EN = H to go to Normal Mode

[1] Indicates the wake up flag in case of local wake up
[2] After power on RxD is going high via pull-up to Vcc. If any wake up(local or remote) occurs it will be indicated by active low
[3] Active low interrupt at pin RxD will be removed when entering normal mode
[4] Wake up source flag at pin TxD will be removed when entering normal mode
[5] Normal mode will be entered from Standby Mode by a low -> high transition on pin EN and from Sleep Mode by EN = H after startup of the regulator. When recessive level (high) on pin TxD is present the transmit path will be enabled

4.2. Initialisation and Standby mode

When the battery supply voltage VS exceeds the specified threshold V_{SUVR_OFF}, the MLX8003x/5x automatically enters the Standby Mode. Following internal procedure is running:

First:

- Start of internal supply Vaux and POR of Vaux
- Start of internal RC oscillator

Second and parallel after POR:

- Start of voltage regulator

The output voltage V_{CC} ramps up to nominal value. The pin RxD is floating and the integrated slave pull up resistor with decoupling diode pulls the pin LIN. The transmitter as well as the receiver is disabled.

If there occurs no mode change to Normal Mode via an EN LOW to HIGH transition within the time stated (typically 350ms), the IC enters the most power saving Sleep Mode.

Furthermore the standby mode will be entered after a valid local or remote wake up event, when the MLX8003x/5x is in Sleep or Silent mode. The entering of the standby mode after wake up will be indicated by an active LOW interrupt on pin RxD.

4.3. Normal Mode

This mode is the base mode. The bus transceiver is able to send with a max baud rate of 20kbit/s.

The whole MLX8003x/5x is active. The incoming bus traffic is detected by the receiver and transferred via the RxD output pin to the microcontroller.

Exit the Normal Mode with one of the following conditions:

1. High-to-low edge on EN pin with TxD = H -> switch to Silent Mode
2. High-to-low edge on EN pin with TxD = L -> switch to Sleep Mode
3. Undervoltage monitor on VCC detects a low voltage reset condition (VCC < V_{RES}) -> switch back to stand-by mode.

Low Slew Mode

The first rising edge on EN after power-on defines the slew rate of the device. With TxD = High at this point works the MLX8003x/5x with normal slew rate (default state). TxD = Low activates the Low Slew Mode, as long as VS > V_{SUVR_OFF}.

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.

4.4. Silent Mode

The Silent Mode is a special mode for application with active Sleep Mode on LIN, but the connected MCU still needs to be supplied with VCC.

With a falling edge on EN input in combination with TxD=high switches the MLX8003x/5x from Normal Mode to the Silent Mode with reduced internal current consumption.

In Silent Mode the voltage regulator is on with a 2% tolerance. The transmitter is disabled and the pin RxD is disconnected from the receive path and is floating. The slave termination resistor (LIN pull up resistor with decoupling diode between pins LIN and VS) is disconnected; only a weak current source is applied to the LIN bus. Value is typical -75uA, limits -20…-100uA.

Exit the silent mode with one of the following conditions:

1. Low-to-high edge on the EN pin -> switch back to normal mode
2. Remote wake up (all versions) or local wake up request (MLX80031/51 only) -> switch to standby mode
3. Undervoltage monitor on VCC detects a low voltage reset condition (VCC < V_{RES}) -> switch back to stand-by mode.

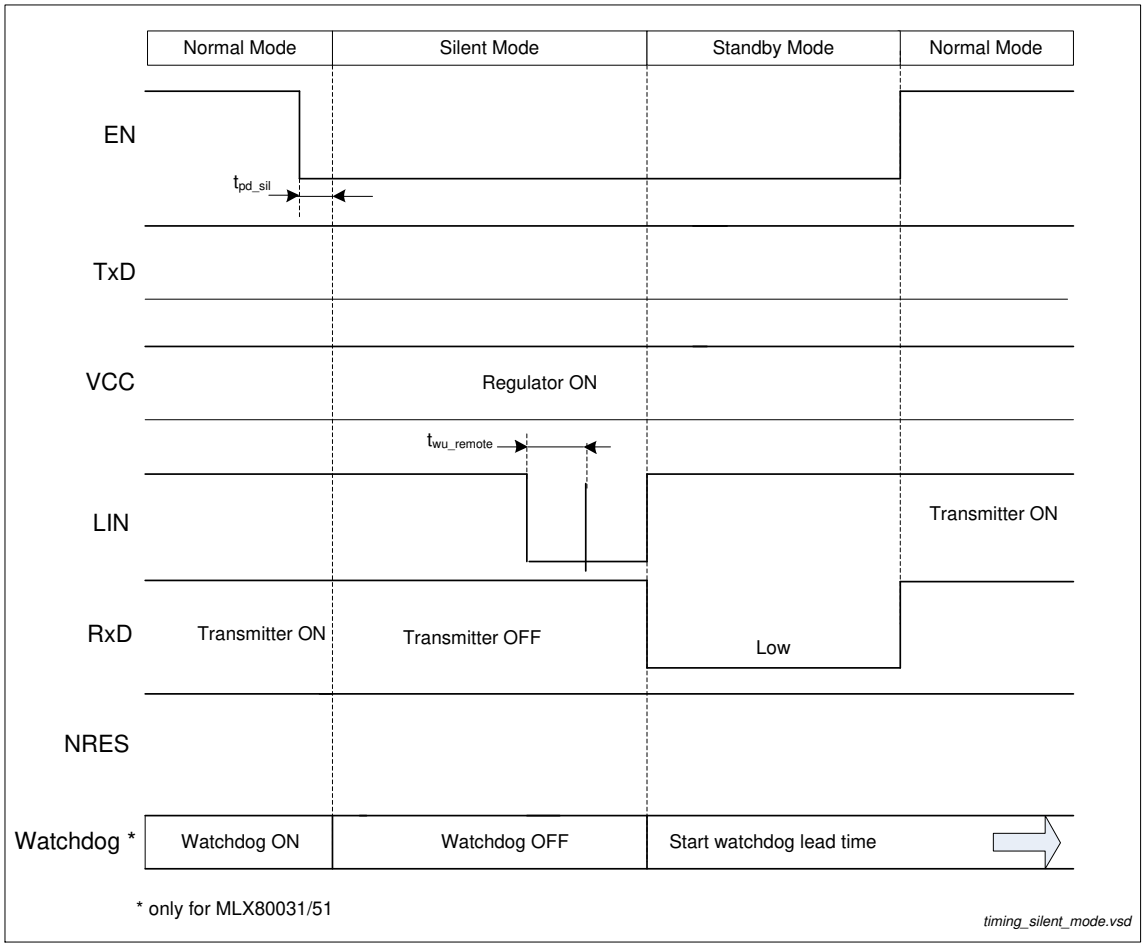


Figure 6: LIN wake-up from Silent Mode

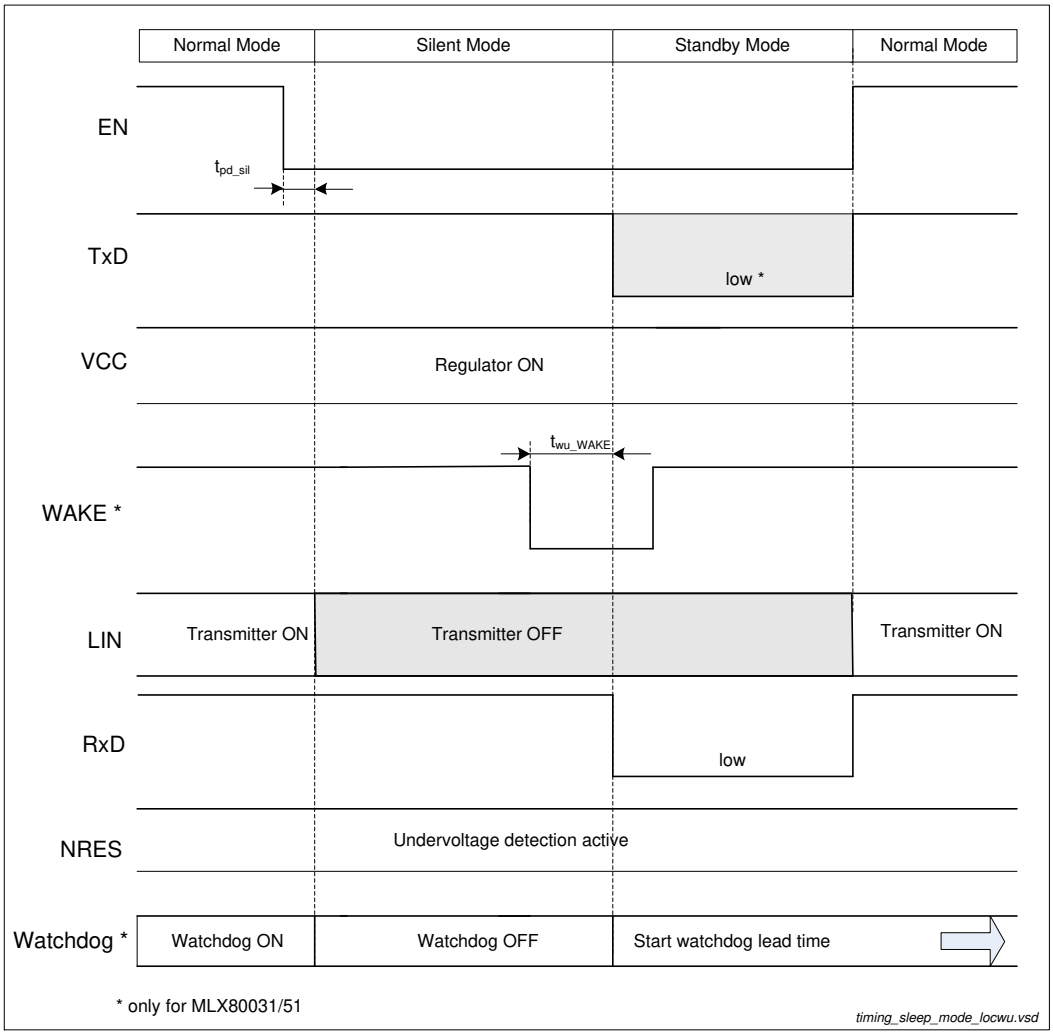


Figure 7 Local Wake-up from Silent Mode via WAKE

4.5. Sleep Mode

The most power saving mode of the MLX8003x/5x is the Sleep Mode. The MLX8003x/5x offers two procedures to enter the sleep mode:

- The mode is selected from normal mode with a falling edge on EN in combination with TxD = L.
- If the MLX8003x/5x is in Standby Mode after power-on or wake-up, a sleep counter is started and switches the transceiver into Sleep Mode after the specified time (typ. 350ms) even when the microcontroller of the ECU will not confirm the normal operation by setting the EN pin to logic HIGH. This new feature allows faulty blocked LIN nodes to reach always the most power saving mode.

Being in Sleep Mode the voltage regulator switched off in order to minimize the current consumption of the complete LIN node. The transmitter is disabled and the pin RxD is disconnected from the receive path and is low (follows VCC). The slave termination resistor (LIN pull up resistor with decoupling diode between pins LIN and VS) is disconnected, only a weak current source is applied to the LIN bus (see chapter 8 fail-safe features)