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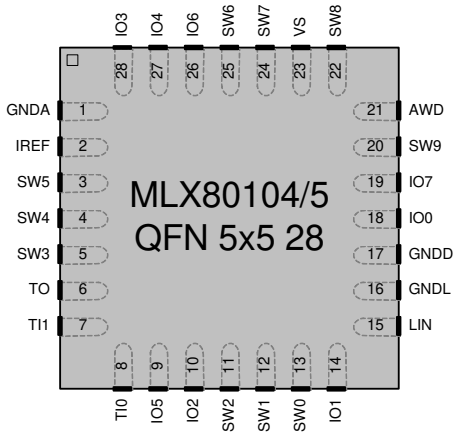
MLX80104/5

LIN Slave Controller for Switches

Datasheet

Features



Application Controller

- Internal 12 MHz RC-Oscillator
- 16-bit MULAN MCU with 16kB ROM or OTP, 512 Byte RAM, 192 Byte EEPROM with ECC

LIN Protocol Controller according to LIN 2.x and SAE J2602

- Baud rate up to 19.2 kBaud
- Frame processing
- Low interrupt load to the application

LIN Transceiver according to LIN 2.x and SAE J2602

- Slew rate control for best EME behaviour
- High EMI immunity

IO Configuration

- 18 fully configurable high current/high voltage inputs/outputs (7mA/26.5V)
- Ground shift tolerant I/Os
- All IOs configurable pull up or pull down characteristics
- Eight PWM outputs (8-bit, 80Hz to 30kHz)
- Ten 10-bit ADC channels
- Eight Interrupt capable Inputs
- Configurable Wake up sources (LIN, IOs, ADC)
- Constant current output (2mA) for external low voltage loads via bipolar transistor
- IOs fully diagnosable
- Integrated window watchdog and additional independent analogue watchdog

Voltage Regulator

- Low standby current consumption of typ 25µA in sleep mode
- Over-temperature shutdown, 45V load dump protected

Other Features

- Automotive Temperature Range of –40°C to 125°C
- Small MLF 5x5 28pin package
- Ready-to-use firmware available (UniROM)

Order Code	*Temp. Range*	*Package*	*Delivery*	*Remark*
MLX80104 KLQ-DAG-000-RE	-40 - 125 °C	QFN 5x5	Reel	ROM, See 22 Marking
MLX80104 KLW-DAG-000-RE	-40 - 125 °C	QFN 5x5 WF	Reel	ROM, See 22 Marking
MLX80105 KLQ-EAA-000-RE	-40 - 125 °C	QFN 5x5	Reel	OTP, See 22 Marking
MLX80105 KLW-EAA-000-RE	-40 - 125 °C	QFN 5x5 WF	Reel	OTP, See 22 Marking

Short Description

This IC is a fully integrated LIN Slave for matrix switch or single switch Applications in automotive environment. It is suitable for bus systems according to LIN 2.x as well as SAE J2602.
The combination of physical layer LIN transceiver and LIN protocol controller along with easy to configure switch inputs and PWM outputs make it possible to develop in a short timeframe simple, but powerful and cheap switch slave nodes for LIN Bus systems.

Contents

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List of Tables

1. General Overview

1.1 Block Diagram

Figure 1 shows the principle block diagram of MLX80104/5.

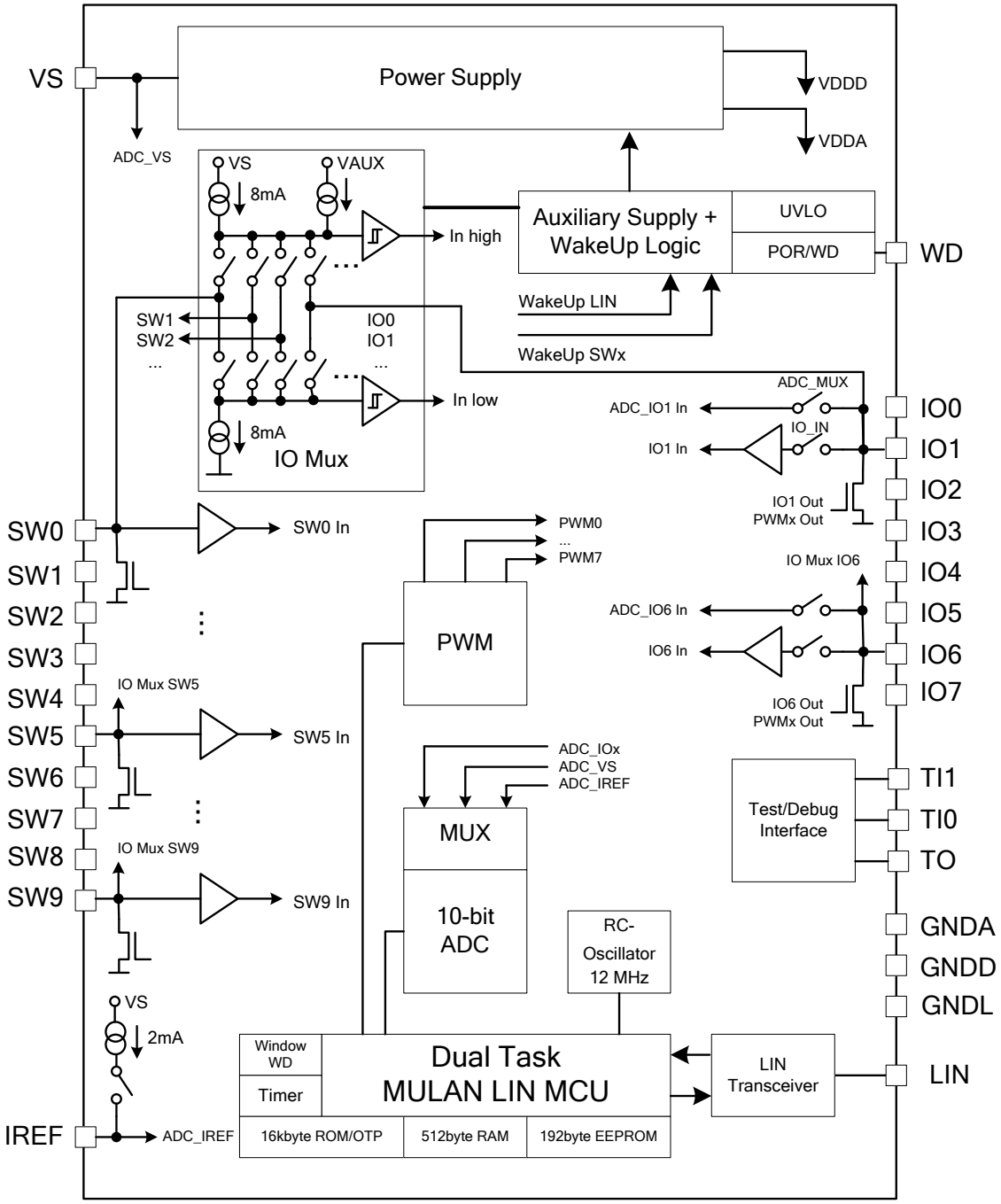

Figure 1 - Block Diagram

2. Electrical Characteristics

All voltages are referenced to ground (GND). Positive currents flow into the IC.

2.1 Absolute Maximum Ratings

In accordance with the Maximum Rating System (IEC 60134). The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

Parameter	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S		-0.3	40	V
Short term supply voltage	V_{S_ld}	ISO 7637/2 pulse 5; t < 400 ms	-0.3	40	V
Transients at supply voltage	V_{S_tr1}	ISO 7637/2 pulse 1[1]	-100		V
Transients at supply voltage	V_{S_tr2}	ISO 7637/2 pulses 2 [1]		+50	V
Transients at high voltage signal pins	V_{LINx_tr1}	ISO 7637/3 pulse 1 [2]	-100		V
Transients at high voltage signal pins	V_{LINx_tr2}	ISO 7637/3 pulses 2 [2]		+50	V
Transient at high voltage signal and power supply pins	V_{HV_tr3}	ISO 7637/2 pulses 3A, 3B [3]	-150	+100	V
DC voltage on LIN, SWx, IOx pins	V_{LIN_DC}	T<500ms, V_S = 18V V_S = 0V	-22 -40	40	V
DC voltage on IREF, AWD pin	V_{logic_DC}		-0.3	7	V
ESD capability	V_{ESDIEC}	IEC 61000-4-2 Pin LIN, VS to GND	-6	6	kV
	V_{ESDHBM}	HBM (AEC-Q100-002) [4] Pin LIN, VS to GND Other pins	 -8 -2	 8 2	 kV kV
	V_{ESDCDM}	CDM (AEC-Q100-011)	-750	750	V
Maximum latch – up free current at any pin	I_{LATCH}		-500	500	mA
Maximum power dissipation	P_{tot}	T_{amb} = +125 °C		0.78	W
		T_{amb} = + 85 °C		2	
Thermal impedance	Θ_{JA}	JEDEC 1s2p board, none air flow		32	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

Table 1 - Absolute Maximum Ratings

[1] ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[2] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 100nF.
[3] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 1nF.
ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[4] Equivalent to discharging a 100pF capacitor through a 1.5Kohm resistor conforms to AEC-Q100-002

2.2 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery supply voltage [1]	V_S	5	18	V
Short time battery supply voltage [2]	V_{S_S}	18	27	V
Operating ambient temperature	T_{amb}	-40	+125	°C

Table 2 - Operating Conditions

[1] V_s is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4…1V, V_{BAT_ECU} = 6…27V.
[2] Short time: t < 1 min

2.3 Static Characteristics

(V_S = 5 to 27V, T_A = -40 to +125°C, unless otherwise specified)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Pin VS							
3.00	Supply current, active without switch current	I_S			6	20	mA
3.01	Undervoltage lockout	V_{S_UV}				5	V
3.02	Supply current, sleep mode	I_{Ssl_typ}	V_S = 12V		25	50	µA
3.03	Supply current, sleep mode	I_{Ssl}	V_S = 18V			90	µA
PIN LIN							
3.10	Short circuit bus current	I_{BUS_LIM}	V_{LIN}= V_S = 18V, TxD = 0	40	120	200	mA
3.11	Pull up resistor LIN	R_{SLAVE}	V_{LIN}=0, TxD open	20	30	60	kΩ
3.12	Pull up current LIN, Sleep mode	$I_{BUS\_PU\_Sleep}$	V_{LIN}=0, V_S=12V, sleep mode	-100	-75		µA
3.13	LIN reverse current, recessive	$I_{BUS\_PAS\_rec}$	V_{LIN}>V_S , 5V <V_{LIN} <18V, 5V <V_S <18V , TxD open			20	µA
	Receiver input leakage current	$I_{BUS\_PAS\_dom}$	V_S = 12V, V_{LIN}=0	-1			mA
3.14	LIN reverse current loss of battery	$I_{BUS\_NO\_BAT}$	V_S=0V, 0V < V_{LIN} < 18V			23	µA
3.15	LIN current during loss of Ground [3]	$I_{BUS\_NO\_GND}$	V_S=V_{GND}=12V, 0V<V_{LIN}<18V	-100		20	µA
3.16	Transmitter dominant voltage	V_{ol_LIN}	load=500Ω, TxD=0			0.2	Vs
3.17	Recessive output voltage	V_{oh_LIN}	TxD open	0.8		1	Vs
3.18	Lin input capacitance [1]	C_{LIN}	Pulse response via 1kΩ, V_{Pulse}=12V, V_S=14V		25	35	pF
3.19	Voltage drop serial diode [1]	$C_{SerDiode}$		0.4	0.7	1.0	V
3.30	Receiver dominant voltage	V_{BUSdom}				0.4*V_S	V
3.31	Receiver recessive voltage	V_{BUSrec}		0.6*V_S			V
3.32	Centre point of receiver threshold	V_{BUS_cnt}	V_{BUS_cnt} =(V_{th_dom} + V_{th_rec})/2	0.475*Vs	0.5*Vs	0.525*Vs	V
3.33	Receiver hysteresis	V_{HYS}	V_{HYS} =(V_{th_dom} -V_{th_rec})			0.175*Vs	V

Parameter		Symbol	Condition	Min	Typ	Max	Unit
PIN SWx, IOx in normal mode							
3.40	Central current source on resistance pull up configuration	R_{ih_SWx}	Pull up mode, voltage shift max 0.1*Vs			1	KΩ
3.41	Central current source on resistance pull down configuration	R_{il_SWx}	Pull down mode, voltage shift max 0.1*Vs			1	KΩ
3.42	High level input voltage	V_{ih_SWx}	Input mode	1.4			V
3.43	Low level input voltage	V_{il_SWx}	Input mode			0.9	V
3.44	On resistance SWx	R_{ON_IO}	Low side mode, V_{SWx}=0.5V		50	100	Ω
3.45	Source current central current source	I_{ih_SWx}	Vs=5V Vs=13V (T_A = 25°C) Vs=18V	1.5 7		 12	mA
3.46	Sink current central current source	I_{il_SWx}	Vs=5V Vs=13V (T_A = 25°C) Vs=18V	1.5 7		 12	mA
3.47	Leakage current low level input	I_{leakl_SWx}	V_{il_SWx} = 0, V_S = 18V	-10		10	µA
3.48	Leakage current high level input	I_{leakh_SWx}	V_{ih_SWx} = 18V, V_S = 18V	-10		10	µA
PIN IREF							
3.60	Input voltage range	V_{IREF}		0		Vs	V
3.61	Output current	I_{IREF}		1.3	2	3.1	mA
3.62	Leakage current low level input	I_{leakl_IREF}	V_{IREF} = 0, V_S = 18V	-10		10	µA
3.63	Leakage current high level input	I_{leakh_IREF}	V_{IREF} = 3.4V, V_S = 18V	-10		10	µA
PIN AWD							
3.70	Input voltage range	V_{AWD}		0		3.4	V
3.71	Pull down current	I_{PD_AWD}			2		µA
3.72	Pull up current	I_{PU_AWD}			20		µA
3.73	RESET threshold	V_{AWD_IRQ}			0.5		V
3.74	Interrupt threshold	V_{AWD_Int}			1.5		V
3.75	Down threshold	V_{AWD_d}			2.5		V
Wakeup capability SWx,IOx							
3.80	Wake up pull up resistance SWx, IOx [4]	$R_{ih\_WU\_SWx}$	Pull up mode, voltage shift max 0.1Vs	500		1000	Ω
3.81	Wake up pull down resistance SWx, IOx [4]	$R_{il\_WU\_SWx}$	Pull down mode, voltage shift max 0.1Vs	500		1000	Ω
3.82	High level input voltage	$V_{ih\_WU\_SWx}$	Input mode	1.4			V
3.83	Low level input voltage	$V_{il\_WU\_SWx}$	Input mode			0.9	V
3.84	On resistance in sleep mode SWx/IOx	$R_{ON\_WU\_IO}$	Low side mode (S3x), $V_{SWx/IOx}$=0.5V		50	100	Ω

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Thermal Protection							
3.90	Thermal shutdown [1]	T_{sd}		155		180	°C
3.91	Thermal recovery [1]	T_{rec}		126		150	°C
ADC Resolution (INL)							
3.67	ADC accuracy	V_{mess_diff}	One time measurement			5	LSB
3.68			Three time measurement			2	LSB
Switches							
On - resistance [2] [5]		R_{SW_on}	carbon on gold	0	150	1000	Ω
Off - resistance [2]		R_{SW_off}	Open switch	500			KΩ

Table 3 - Static Characteristics

[1] Parameter not tested in production, guaranteed by qualification.
[2] Switch parameter not determined by the IC, values are calculation basis for all currents and thresholds
[3] The current is determined by the master pull-up. To prevent discharging of the battery, the master pull up will be disconnected under Loss of Ground conditions
[4] Resistance is valid for the sum of switch resistance and the ESD protection resistance
[5] A 500Ohm series resistor is required in case of the remote switch outside of the module and the switch is in this case directly supplied from the battery

2.4 Dynamic Characteristics

(V_S = 7 to 27V, T_A = -40 to +125°C, unless otherwise specified)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
PIN LIN							
4.01	Propagation delay receiver [1]	t_{rx_pdf}	C_{RxD} = 25pF, rising and Falling edge			6	µs
4.02	Propagation delay receiver symmetry [2]	t_{rx_sym}	t_{tx_pdf} - t_{rx_pdr}	-2		2	µs
4.03	Receiver debounce time [2]	t_{rx_deb}	LIN rising and falling edge	0.5		4	µs
4.04	LIN duty cycle 1 [3,4]	D1	20kbps operation, normal mode t_{Bit} = 50µs, D1=$t_{LIN\_rec(min)}$/(2*t_{Bit})	0.396			
4.05	LIN duty cycle 2 [3,4]	D2	20kbps operation, normal mode t_{Bit} = 50µs, D2=$t_{LIN\_rec(max)}$/(2*t_{Bit})			0.581	
4.06	LIN duty cycle 3 [3,4]	D3	10.4kbps operation, low speed, t_{Bit} = 96µs, D3=$t_{LIN\_rec(min)}$/(2*t_{Bit})	0.417			
4.07	LIN duty cycle 4 [3,4]	D4	10.4kbps operation, low speed, t_{Bit} = 96µs, D3=$t_{LIN\_rec(max)}$/(2*t_{Bit})			0.590	
4.08	$t_{rec(max)}$ – tdom(min)	Δt3	10.4kbps operation, low speed mode			15.9	µs
4.09	$t_{rec(min)}$ – tdom(max)	Δt4	10.4kbps operation, low speed mode			17.28	µs
4.12	Wake up filter time	t_{WU}	Sleep mode, LIN rising and falling edge	15		150	µs
PIN SWx/IOx							
4.21	Local wake-up filter time	t_{wu_local}	Sleep mode rising and falling edge	10	25	50	µs
ADCx							
4.22	Conversion time ADC	t_{conv}		12			µs
PIN IOx							
4.24	Slew Rate IOx[5]	t_{Slew_IOx}	Low side mode, V_S=6V, R_{pullup} =2.5kΩ, C_{load} = 20pF			2.5	µs
General							
	Device start up time [6] [7]	t_{SUP}	After POR,UVR, Wakeup	3	5	10	ms

Table 4 - Dynamic Characteristics

[1] This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/us
[2] See figure – Receiver debounce and propagation delay
[3] See figure – Duty cycle measurement and calculation
[4] Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled
[5] Only information
[6] Only characterization, guaranteed by design
[7] This time contains the activation time of hardware components and the software initialisation time. To get first valid switch status information, the programmed switch debouncing time must be added.

3. MULAN – MULtiple CPU with Analog and Network support

3.1 General

The MULAN CPU is a dual task implementation of the Melexis LIN Controller (MLX4) and the MLX16-8 CPU core. It is possible to run two tasks simultaneously with this architecture, one task for communication and the other task is free for the customer application. The communication between both tasks is done via API commands. The complete firmware including API for the LIN controller is supported by Melexis. The Customer only needs to program the application software on the MLX16-8 CPU. For a detailed description of this CPU please see the MLX16-8 data book.

3.2 MULAN Block Diagram

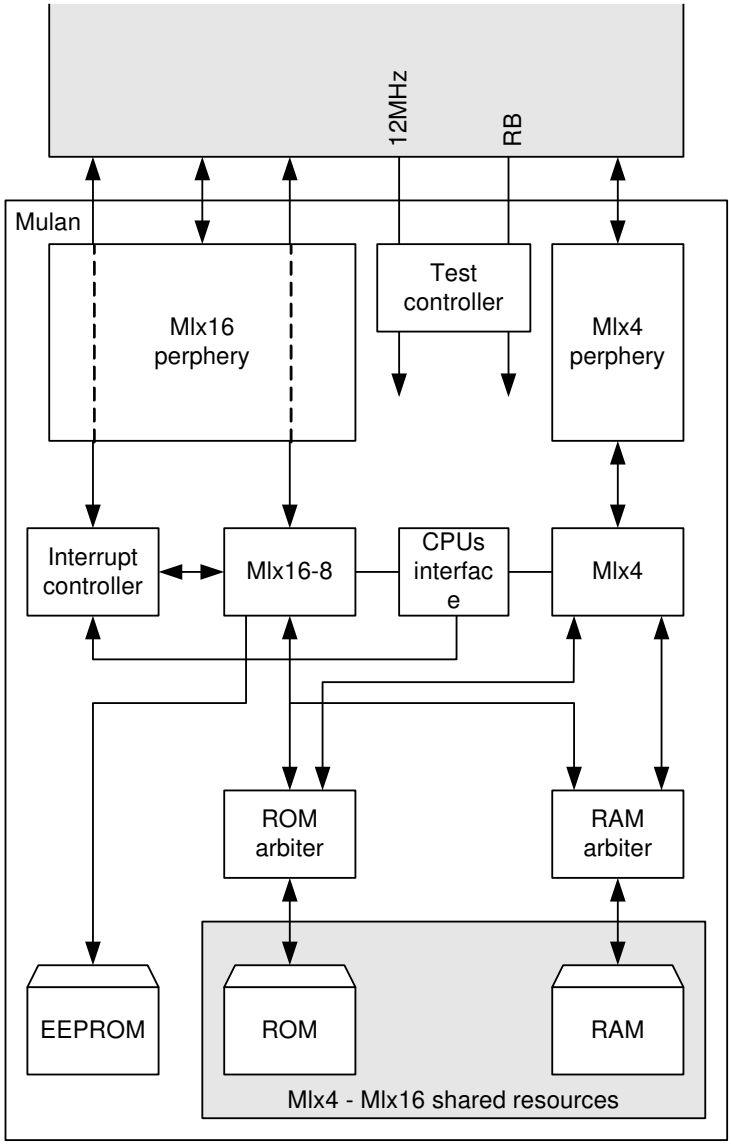

Figure 2 - Block Diagram of MULAN CPU

3.3 CPU Timing

MULAN use two CPUs:
A 4 bit CPU to handle a low speed protocol such as LIN.
A 16 bit CPU for an application firmware.

This construction has the following advantages:
The user does not need to take care of the real time problems of a protocol.
The protocol is handled by a Melexis firmware that can be updated when the protocol evolves.
The application CPU throughput is not affected by the protocol handling.
There is a native inter-task protection, e.g. an application crash does not affect the protocol handling.

Both CPUs share a common 12 MHz clock, a common ROM for program memory and a common RAM for data. Two memory arbiters are used for resolving conflicts with a common strategy: The Mlx4 always has priority.
Most of the time there is no conflict as the CPUs are interleaved as shown on Figure 3.

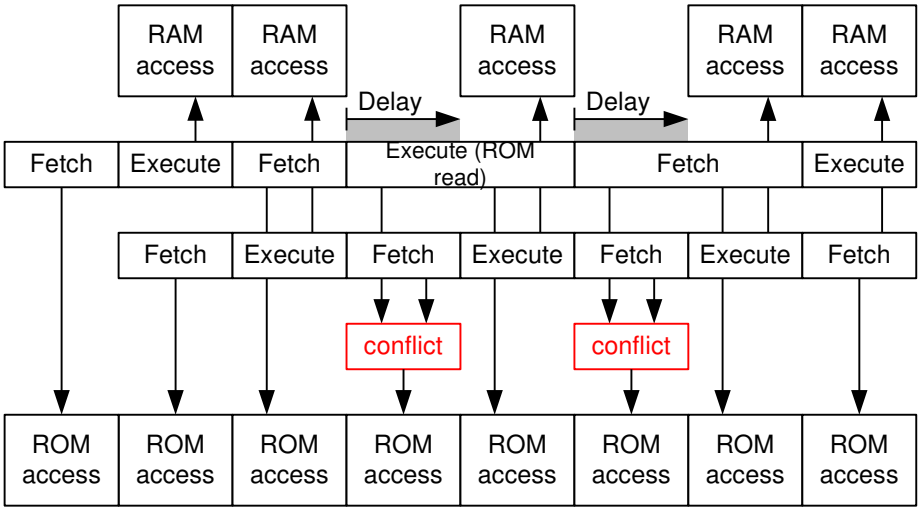

Figure 3 - CPU interleaving

3.4 MLX16-8

The 16 bit CPU is an Mlx16-8. This core is an evolution of the Mlx16 to increase GCC code generation efficiency. The change is limited to a few added instructions. A detailed description can be found in the Mlx16-8 datasheet. For readers familiar with the Mlx16, the list of instructions added is:

- CALLF : Call Far (anywhere within 64K)
- FSB : Find first bit set (in a word)
- MOVSB [X++], [Y++] : Copy array of bytes
- MOVSW [X++], [Y++] : Copy array of words
- Push #Word : Push a constant word into the stack
- SFB : Set first bit (in a word)

Moreover a new address mode has been added to allow direct access to any location. It is similar to dp: Addressing mode but allows any address within 64K at expense of an extra word of op-code.

4. Address Space

Mlx4 and Mlx16 share a common ROM and RAM. From the 2 CPUs a unified 16 bit bus is created (Von Neumann architecture). This bus is hooked to the ROM, the RAM, the EEPROM and the Mlx16-8 peripherals. Two arbiters are in charge of creating a unique memory address and corresponding access signals for ROM and RAM.

4.1 Memory Mapping

The unified 16 bit bus accesses devices as shown on Table 5.

Mlx16-8

Memory space					Allowed: Fetch	Allowed: Write	Allowed: System
E030	- FFFF	Not used					
E000	- E02F	Mlx16 System Ports	48 Bytes				
C020	- DFFF	Not used					
C000	- C01F	Mlx16 User ports	32 Bytes				
B000	- BFFF	Not used					
A200	- AFFF	Not used					
A000	- A1FF	RAM (2)	RAM: 512 Bytes			(2)	
80C0	- 9FFF	Not used					
8014	- 80BF	EEPROM (1)	EEPROM: 172 Bytes				
8000	- 8013	EEPROM Melexis Area (1)	EEPROM: 20 Bytes				
4000	- 7FFF	Not used					
2000	- 3FFF	ROM	ROM: 8kBytes, Mlx16 code				
1000	- 1FFF	ROM	ROM: 4kBytes, Mlx4 or Mlx16 code				
0000	- 0FFF	ROM	ROM: 4kBytes, Minimum Mlx4 code				

(1): Fetch enabled in this area for patch codes
(2): See RAM sharing for Mlx4-Mlx16 distribution and protection

Table 5 - Unified memory mapping

There are some restrictions for accessing certain areas depending on the type of access:

- Mlx4 can fetch anywhere from 0x0000 to 0x1FFF (12 bits word address)
- Mlx16 can fetch from:
  - ROM: Normal case
  - EEPROM: For patched code
  - RAM: For test purposes
- Mlx4 and Mlx16 can read any RAM location (limited to 256 bytes for Mlx4)

The predefined pages of the Mlx16-8 are encoded as shown on Table 5. Some have fixed values (in grey) while others have value that depends of the ROM size. Table 6 gives examples for most common ROM sizes.

	ROM	
Name	**16K**	**Note**
Fp0:	3F00	Last ROM page (used by interrupt controller)
Fp1:	3E00	Could be used for C runtime
Fp2:	3D00	Could be used for C runtime
Fp3:	3C00	Could be used for C runtime
Fp4:	3B00	Could be used for C runtime
Fp5:	A100	In (large) RAM for fast patches (copied from EEPROM)
Fp6:	A000	In RAM Dp: for test routines
Fp7:	8000	In EEPROM to allow single instruction patch start
Dp:	A000	Mlx16 private RAM
Io:	C000	Standard Ports
Ep:	8000	EEPROM (First page)

Legend:

	Fixed address for any ROM size
	Address depending on the ROM size

Table 6 - MLX16 pre-defined pages

4.2 RAM Sharing

A RAM size of 512 bytes is available for the MLX80104/5. This area is used by both CPUs.

While Mlx4 sees its private and shared RAM areas as 2 consecutive spaces, Mlx16 sees the private area of Mlx4 at the top of its RAM address space and the shared area at its bottom. This arrangement has the following advantages:

- Shared area is in Mlx16 Dp: address space, so Mlx16 has a fast access to it.
- The Mlx16-8 private area is in a single piece which makes GCC more efficient.

4.3 ROM/OTP Sharing

The MLX80104/5 has integrated 16Kbyte ROM or OTP. This area is used from both CPUs. The LIN Task + LIN API use 5kbytes while the rest (11kbytes) is available for the application running on the MLX16

Each CPU has is own separate program code in the ROM/OTP area but there is no specific mechanism to isolate them. The linker program merges the two programs and verifies that there is no overlapping, but if at execution time an error causes one CPU to jump into the code of the other one, it will of course execute unpredictable instructions and this situation will be detected either by watchdog overflow or protection error.

4.4 EEPROM

With the EEPROM it is possible to store non-volatile information. The EEPROM block is a 96 x 16bit Electrically Erasable Programmable Read Only Memory (EEPROM) with single power supply, single-error correction (SEC) and double-error detection (DED). An internal charge pump generates high voltage needed for the Erase/Write operations.

The EEPROM is Mlx16 private. The required EEPROM data for the Mlx4 execution is placed in RAM by the Mlx16 before it releases Mlx4 reset.
The EEPROM is organized in words (16 bits). Reading byte-wise is possible, but writing is only possible word-wise.

4.4.1. Static/dynamic Characteristics

Parameter	Remark	min	Typ	Max	Unit
Number of erase/write cycles	T_{amb} = 25°C	100 000			
	T_{amb} = 125°C	10 000			
Data retention time	T_{amb} = 85°C	10			Years
Erase/Write time	T_{amb} = -40…125°C	4		8	ms

4.4.2. Reserved EEPROM Segments

Segment name	Segment range (word addresses)	Description
Melexis area	0x8000 – 0x8013	Melexis calibration data
Patch0 start address	0x8014	start address and enable bit for firmware patch 0
Patch1 start address	0x8016	start address and enable bit for firmware patch 1
User area	0x8018 – 0x809E	User data
Patch0 area	0x80A0 – 0x80AE	Patch0
Patch1 area	0x80B0 – 0x80BE	Patch1

The using of firmware patches is optional but recommended. In case no firmware patch is used, these areas can be used for user data.

4.4.3. Write Timing

The EEPROM requires a 5ms delay for write and erase operations. This is generated from a 250 KHz internal clock. A write or erase access to the EEPROM starts a 5ms delay period that can be monitored by either polling port bit EE_BUSY or waiting for the interrupt EE_IT.

Note:
While the EEPROM is being written, both CPUs are still running. An attempt to read or write to EEPROM by Mlx16 while it is busy generates an exception interrupt.

4.4.4. Read timing

The read access time of the EEPROM is 4 clock periods. This delay is created using the master clock.

4.4.5. Read

A read is done “on the fly” by adding wait states in the instruction.

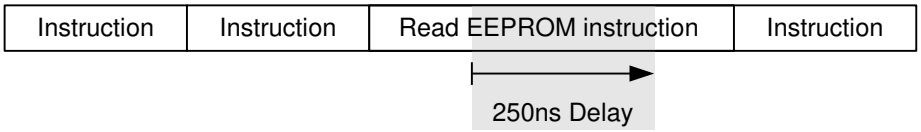

Figure 4 - EEPROM read

4.4.6. Write/Erase

The MLx16 supports 2 operations: Read and Write, while EEPROM requires 3 operations: Read, Write, and Erase. EEPROM Write and Erase are both accomplished by an Mlx16 write instruction.
As write and erase delays are long, the Mlx16 does not delay its instruction till completion. A specific hardware buffers address and data and the CPU continues its execution while the write/erase is ongoing.
The CPU has 2 options to know when the write/erase delay is terminated. It can either poll bit EE_BUSY (0 when not busy, 1 when busy) for a 0 value, or it can enable interrupt EE_IT that will be triggered when EE_BUSY goes from 1 to 0.

In order to minimize the risk of erroneous write/erase of the EEPROM, those accesses are only possible in system mode, e.g. application should call a secure system function to erase or write.

Since some applications require the EEPROM should never be written there is an extra protection for the EEPROM. The system port CONTROL has a bit EN_EEPROM_WE (0 at reset) that must be set to enable write and erase, or else the operation is cancelled and a protection interrupt is generated.

EEPROM Control register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE001	**EEPROM**	EE_BUSY	Reserved	Reserved	Reserved	Reserved	Reserved	EE_CTL[1]	EE_CTL[0]

EE_BUSY Will be always high in case there is a write process running
EE_CTL[1:0] Controls the EEPROM read and write mode
- 00 Write
- 01 Erase
- 10 Block write, write access to any EEPROM address will overwrite the complete EEPROM
- 11 Block erase, write access to any EEPROM address will reset the complete EEPROM to 1

System Control register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE000	**CONTROL**	Reserved	EEPROM_ WE	OUTC_WE	OUTB_WE	OUTA_WE	Reserved	HALT	M4_PORB

EEPROM_WE Write enable bit EERPOM
- 1 = EEPROM content can be changed
- 0 = EEPROM content can **not** be changed

OUTC_WE Write enable bit
- 1 = ANA_OUTC can be changed
- 0 = ANA_OUTC can **not** be changed

OUTB_WE Write enable bit
- 1 = ANA_OUTB can be changed
- 0 = ANA_OUTB can **not** be changed

OUTA_WE Write enable bit
- 1 = ANA_OUTA can be changed
- 0 = ANA_OUTA can **not** be changed

HALT Writing to the bit will halt the MLX16
M4_PORB Mlx4 Reset: Writing to the bit resets the MLX4

System Various register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE000	**VARIOUS**	EE_DED	EE_SEC	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

EE_DED EEPROM double-error detection
1 = EEPROM double-error detected
0 = EEPROM double-error **not** detected

EE_SEC EEPROM single-error correction
1 = EEPROM single-error detected and corrected
0 = EEPROM single-error **not** detected

4.5 OTP (MLX80105 only)

The MLX80105 has integrated 16Kbyte OTP. This area is used by both CPUs. The LIN Task + LIN API use 5kbytes while the rest (11kbytes) is available for the application running on the MLX16

Each CPU has is own separate program code in the OTP area but there is no specific mechanism to isolate them. The linker program merges the two programs and verifies that there is no overlapping, but if at execution time an error causes one CPU to jump into the code of the other one, it will of course execute unpredictable instructions and this situation will be detected either by watchdog overflow or protection error.

From the functional point of view the MLX80104 (ROM) behaves the same as the MLX80105 (OTP).

5. IO Registers

5.1 General

There are 2 port spaces for the Mlx16:

- System protected ports (starting at address 0xE000), Mlx16 bit USER must be cleared.
- User ports (starting at address 0xC000), not protected, Mlx16 bit USER must be set.

The Mulan port map has an open window of 16 bytes of custom user ports and of 12 bytes of custom system ports (not included in Mulan). Reading to non existing custom ports will have no effect and reading from non existent custom ports will always return 0.

5.2 System Protected ports

Table 7 shows the available system ports. All of these ports are system protected, meaning they are only accessible with bit USER=0. All of these registers are located outside of the IO-Segment.

Name	Address	Access Mode	Description	Page
MLX	0xE02F	Byte	MLX Reserved	
SEL_XTAL	0xE02E	Word/Byte	Selection of internal/external Oscillator	43
MLX	0xE02D	Byte	MLX Reserved	
STATUS	0xE02C	Word/Byte	Wakeup Source and central pull up/down input comparator	27
SW_IN_H	0xE02B	Byte	SW8..9 Input comparator	28
SW_IN_L	0xE02A	Word/Byte	SW0..7 Input comparator	28
IO_IN	0xE029	Byte	IO0..8 Input comparator	29
IO_AWD	0xE028	Word/Byte	Watchdog Acknowledge	44
IO_IRQ	0xE027	Byte	Interrupt source of IO generated interrupts	29
IO_EN	0xE026	Word/Byte	Enable IO pins	29
IO_INT_ENF	0xE025	Byte	Enable IO interrupt on falling edges	29
IO_INT_ENR	0xE024	Word/Byte	Enable IO interrupt on rising edges	29
MLX	0xE023	Byte	MLX Reserved	
MLX	0xE022	Word/Byte	MLX Reserved	
ANA_OUTC_H	0xE021	Byte	ADC reference calibration	68
ANA_OUTC_L	0xE020	Word/Byte	RC Oscillator trimming, enable external system clock source	68
ANA_OUTB_H	0xE01F	Byte	Current references and bandgap trimming, slew rate LIN transceiver	68
ANA_OUTB_L	0xE01E	Word/Byte	Switch current source trimming, VDDD and VDDA trimming	68
ANA_OUTA_H	0xE01D	Byte	Setting EEPROM write delay, timer controlled wake up enable	68
ANA_OUTA_L	0xE01C	Word/Byte	Power down enable LIN transceiver	68
PATCH3_A_H	0xE01B	Byte	4th Patch start address high byte, patch enable	70
PATCH3_A_L	0xE01A	Word/Byte	4th Patch start address low byte	70
PATCH2_A_H	0xE019	Byte	3rd Patch start address high byte, patch enable	70
PATCH2_A_L	0xE018	Word/Byte	3rd Patch start address low byte	70
PATCH1_A_H	0xE017	Byte	2nd Patch start address high byte, patch enable	70
PATCH1_A_L	0xE016	Word/Byte	2nd Patch start address low byte	70
PATCH0_A_H	0xE015	Byte	1st Patch start address high byte, patch enable	70
PATCH0_A_L	0xE014	Word/Byte	1st Patch start address low byte	70

Name	Address	Access Mode	Description	Page
PATCH3_I_H	0xE013	Byte	4th Patch jump instruction high byte	70
PATCH3_I_L	0xE012	Word/Byte	4th Patch jump instruction low byte	70
PATCH2_I_H	0xE011	Byte	3rd Patch jump instruction high byte	70
PATCH2_I_L	0xE010	Word/Byte	3rd Patch jump instruction low byte	70
PATCH1_I_H	0xE00F	Byte	2nd Patch jump instruction high byte	70
PATCH1_I_L	0xE00E	Word/Byte	2nd Patch jump instruction low byte	70
PATCH0_I_H	0xE00D	Byte	1st Patch jump instruction high byte	70
PATCH0_I_L	0xE00C	Word/Byte	1st Patch jump instruction low byte	70
MLX	0xE00B	Byte	MLX reserved	
MLX	0xE00A	Word/Byte	MLX reserved	
PEND_H	0xE009	Byte	Pending Interrupts high byte	53
PEND_L	0xE008	Word/Byte	Pending Interrupts low byte	53
MASK_H	0xE007	Byte	Interrupt mask high byte	53
MASK_L	0xE006	Word/Byte	Interrupt mask low byte	53
PRIO_H	0xE005	Byte	Interrupt priority high byte	53
PRIO_L	0xE004	Word/Byte	Interrupt Priority low byte	53
SHRAMH	0xE003	Byte	Upper limit for the RAM not accessible by MLX16	
SHRAML	0xE002	Word/Byte	Lower limit for the RAM not accessible by MLX16	
EEPROM	0xE001	Byte	EEPROM control register	19
CONTROL	0xE000	Byte	System control register	19

Table 7 - System Protected Ports Overview

5.3 Standard ports

Table 8 shows the available system ports. All of these ports are system protected, meaning they are only accessible with bit USER=1. All of these registers are located outside of the IO-Segment.

Name	Address	Access Mode	Description	Page
MLX	0xC01F	Byte	MLX reserved	
MLX	0xC01E	Word/Byte	MLX reserved	
SW_CONFIG	0xC01D	Byte	Current configuration central current source, IREF enable	27
S3H	0xC01C	Word/Byte	IO pin open drain enable (S3)	29
S2H	0xC01B	Byte	IO pin central current source pull down enable (S2)	27
S1H	0xC01A	Word/Byte	IO pin central current source pull up enable (S1)	27
S3L_H	0xC019	Byte	SW8..9 pin open drain enable (S3)	28
S3L_L	0xC018	Word/Byte	SW0..7 pin open drain enable (S3)	28
S2L_H	0xC017	Byte	SW8..9 pin central current source pull down enable (S2)	27
S2L_L	0xC016	Word/Byte	SW0..7 pin central current source pull down enable (S2)	27
S1L_H	0xC015	Byte	SW8..9 pin central current source pull up enable (S1)	27
S1L_L	0xC014	Word/Byte	SW0..7 pin central current source pull up enable (S1)	27
PWM_DATA_READ	0xC013	Byte	PWM duty cycle value (read only)	
PWM_DATA_WRITE	0xC012	Word/Byte	PWM duty cycle write register	
PWM_AD	0xC011	Byte	PWM channel selection	57
PWM_CTL	0xC010	Word/Byte	PWM configuration register	58
MLX	0xC00F	Byte	MLX reserved	
MLX	0xC00E	Word/Byte	MLX reserved	
MLX	0xC00D	Byte	MLX reserved	
MLX	0xC00C	Word/Byte	MLX reserved	
ADC_IN_H	0xC00B	Byte	ADC result high byte	50
ADC_IN_L	0xC00A	Word/Byte	ADC result low byte	50
ADC_CTL_H	0xC009	Byte	ADC reference voltage and channel selection	50
ADC_CTL_L	0xC008	Word/Byte	ADC configuration and status	50
TIMER_H	0xC007	Byte	Timer register high byte, Timer enable	60
TIMER_L	0xC006	Word/Byte	Timer register low byte	60
XIN	0xC005	Byte	Thermal error	66
WTG	0xC004	Word/Byte	Digital Watchdog tag register	47
WDCTRL	0xC003	Byte	Digital watchdog control register	
WDT	0xC002	Word/Byte	Digital Watchdog timeout register	
VER	0xC001	Byte	Hardware revision	
VARIOUS	0xC000	Word/Byte/Bit	System status	

Table 8 - Standard Ports Overview

6. IO Ports

The MLX80104/5 contains two types of ports. All of them are proof to battery voltage.
In case of ECU loss of battery (LOB) and a short of the wiring harness to an external supply line the MLX80104/5 will be reverse powered. Please refer to chapter “Operating under Disturbance”.

6.1 Common Features of Pin SWx and IOx

The ports *SW0..9* as well as the ports *IO0..7* allow a very flexible control of up to 18 single switches or a switch matrix or any combination of both, supplied by an internal current source of typically >7mA. The switch control is sequential and periodical, so that only one port will be supplied at the same time.
If switches are placed outside and connected via a wiring harness to the ECU the MLX80104/5 allows full diagnosis of short circuits or broken line.
All ports provide a programmable wake up function and a 10mA open drain low side switch (matrix row connection to GND).
If ports are not used for switch detection, they can be configured passive (tristate behaviour) or as general purpose 10mA open drain output with port monitor. The input thresholds are compatible to 3.3V/5V supply systems. The accuracy of the input threshold allows a monitoring of external voltages without ADC. It allows connection of external supplied encoders, halls or similar.
Furthermore this architecture supports driving of logic output signals for other ECU components via an external pull up resistor as well as the driving of high side or low side loads by providing base current for an external pnp transistor.