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MLX90363

Triaxis® Magnetometer IC
With High Speed Serial Interface

Features and Benefits

- ☐ Tria⊗is® Magnetometer (BX, BY, BZ)
- ☐ On Chip Signal Processing for Robust Position Sensir
- ☐ High Speed Serial Interface (SPI compatible – Full Duplex)
- ☐ Enhanced Self-Diagnostics Features
- ☐ 5V and 3V3 Application Compatible
- ☐ 14 bit Output Resolution
- ☐ 48 bit ID Number
- ☐ Single Die – SO8 Package RoHS Compliant
- ☐ Dual Die (Full Redundant) – TSSOP16 Package RoHS Compliant

Applications

- ☐ Absolute Contactless Position Sensor

Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90363	K	DC	ABB-000	RE
MLX90363	K	DC	ABB-000	TU
MLX90363	K	GO	ABB-000	RE
MLX90363	K	GO	ABB-000	TU
MLX90363	E	DC	ABB-000	RE
MLX90363	E	DC	ABB-000	TU
MLX90363	E	GO	ABB-000	RE
MLX90363	E	GO	ABB-000	TU
MLX90363	L	DC	ABB-000	RE
MLX90363	L	DC	ABB-000	TU
MLX90363	L	GO	ABB-000	RE
MLX90363	L	GO	ABB-000	TU

Legend:

Temperature Code: L for Temperature Range - 40°C to 150°C,
K for Temperature Range - 40°C to 125°C,
E for Temperature Range - 40°C to 85°C.

Package Code: DC for SOIC-8, GO for TSSOP-16.

Option Code: xxx-000: Standard version

Packing Form: RE for Reel
TU for Tube

Ordering example: MLX90363LGO-ABB-000-TU

1. Functional Diagram

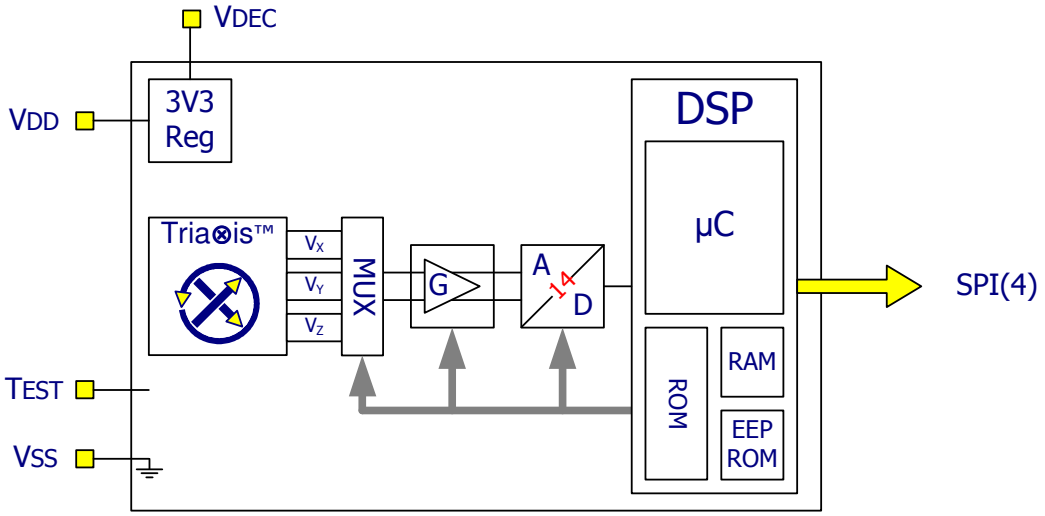


Figure 1 – Block Diagram

2. Description

The MLX90363 is a monolithic magnetic sensor IC featuring the Tria⊗is® Hall technology. Conventional planar Hall technology is only sensitive to the flux density applied orthogonally to the IC surface. The Tria⊗is® Hall sensor is also sensitive to the flux density applied parallel to the IC surface. This is obtained through an Integrated Magneto-Concentrator (IMC®) which is deposited on the CMOS die .

The MLX90363 is sensitive to the three (3) components of the flux density applied to the IC (i.e. B_X, B_Y and B_Z). This allows the MLX90363 to sense any magnet moving in its surrounding and decode its position through an appropriate signal processing.

Using its Serial Interface the MLX90363 can transmit a digital output (SP – 64 bits per frame).

The MLX90363 is intended for Embedded Position Sensor applications (vs. Stand-Alone “Remote” Sensor) for which the output is directly provided to a microcontroller (Master) close to the magnetometer IC MLX90363 (Slave). The SPI protocol confirms this intent.

The MLX90363 is using full duplex SPI protocol and requires therefore the separated SPI signal lines: MOSI, MISO, /SS and SLCK[1].

[1] The MLX90316 multiplexes the MOSI/MISO lines. The application diagrams of the MLX90363 and MLX90316 are therefore not compatible.

TABLE of CONTENTS

FEATURES AND BENEFITS 1
APPLICATIONS 1
1. FUNCTIONAL DIAGRAM 2
2. DESCRIPTION 2
3. GLOSSARY OF TERMS – ABBREVIATIONS – ACRONYMS 5
4. PINOUT 5
5. PIN DESCRIPTION 6
6. ABSOLUTE MAXIMUM RATINGS 6
7. DETAILED DESCRIPTION 7
8. MLX90363 ELECTRICAL SPECIFICATION 8
9. MLX90363 ISOLATION SPECIFICATION 8
10. MLX90363 TIMING SPECIFICATION 9
10.1. TIMING SPECIFICATION FOR 5V APPLICATION DIAGRAM 9
10.2. TIMING SPECIFICATION FOR 3V3 APPLICATION DIAGRAM 10
11. MLX90363 ACCURACY SPECIFICATION 11
12. MLX90363 MAGNETIC SPECIFICATION 13
13. MLX90363 CPU & MEMORY SPECIFICATION 13
14. MLX90363 SERIAL INTERFACE 14
14.1. ELECTRICAL LAYER AND TIMING SPECIFICATION 14
14.2. SERIAL PROTOCOL 16
14.3. MESSAGE GENERAL STRUCTURE 16
14.4. REGULAR MESSAGES 18
14.4.1. Note for the regular message "X – Y – Z – diagnostic" (Marker = 2) *18*
14.5. TRIGGER MODE 1 19
14.6. TRIGGER MODE 2 21
14.7. TRIGGER MODE 3 22
14.8. TRIGGER MODES TIMING SPECIFICATIONS 23
14.9. OPCODE TABLE 26
14.10. TIMING SPECIFICATIONS PER OPCODE, AND NEXT ALLOWED MESSAGES 26
14.11. NOP COMMAND AND NOP ANSWER 27
14.12. OSCCOUNTERSTART AND OSCCOUNTERSTOP COMMANDS 27
14.13. PROTOCOL ERRORS HANDLING 29
14.14. READY, ERROR AND NTT MESSAGES 30
14.15. DIAGNOSTICSDETAILS COMMANDS 31
14.16. MEMORYREAD MESSAGE 32
14.17. EEPROMWRITE MESSAGE 33
14.18. REBOOT 35
14.19. STANDBY 35
14.20. START-UP SEQUENCE (SERIAL COMMUNICATION) 36
14.21. ALLOWED SEQUENCES 37
15. MLX90363 TRACEABILITY INFORMATION 38
16. MLX90363 END-USER PROGRAMMABLE ITEMS 38

17. MLX90363 DESCRIPTION OF END-USER PROGRAMMABLE ITEMS 39

17.1. USER CONFIGURATION: DEVICE ORIENTATION 39
17.2. USER CONFIGURATION: MAGNETIC ANGLE FORMULA 39
17.3. USER CONFIGURATION: 3D=0 FORMULA TRIMMING PARAMETERS SMISM AND ORTH_B1B2 39
17.3.1. Magnetic Angle ∠XY 39
17.3.2. Magnetic Angle ∠XZ and ∠YZ 40
17.4. USER CONFIGURATION: 3D=1 FORMULA TRIMMING PARAMETERS KALPHA, KBETA, KT 40
17.5. USER CONFIGURATION: FILTER 41
17.6. VIRTUAL GAIN MIN AND MAX PARAMETERS 41
17.7. HYSTERESIS FILTER 42
17.8. EMC FILTER ON SCI PINS 42
17.9. IDENTIFICATION & FREE BYTES 42
17.10. LOCK 42

18. MLX90363 SELF DIAGNOSTIC 43

19. MLX90363 FIRMWARE FLOWCHARTS 44

19.1. START-UP SEQUENCE 44
19.2. SIGNAL PROCESSING (GETX) 45
19.3. FAIL-SAFE MODE 45
19.4. AUTOMATIC GAIN CONTROL 46

20. RECOMMENDED APPLICATION DIAGRAMS 47

20.1. MLX90363 IN SOIC-8 PACKAGE AND 5V APPLICATION DIAGRAMS 47
20.2. MLX90363 IN SOIC-8 PACKAGE AND 3V3 APPLICATION DIAGRAMS 47
20.3. MLX90363 IN TSSOP-16 PACKAGE AND 5V APPLICATION DIAGRAMS 48
20.4. MLX90363 IN TSSOP-16 PACKAGE AND 3V3 APPLICATION DIAGRAMS 49

21. STANDARD INFORMATION REGARDING MANUFACTURABILITY OF MELEXIS PRODUCTS WITH DIFFERENT SOLDERING PROCESSES 50

22. ESD PRECAUTIONS 50

23. PACKAGE INFORMATION 51

23.1. SOIC8 – PACKAGE DIMENSIONS 51
23.2. SOIC8 – PINOUT AND MARKING 52
23.3. SOIC8 – IMC POSITIONNING 53
23.4. TSSOP16 – PACKAGE DIMENSIONS 54
23.5. TSSOP16 – PINOUT AND MARKING 55
23.6. TSSOP16 – IMC POSITIONNING 55

24. DISCLAIMER 57

3. Glossary of Terms – Abbreviations – Acronyms

- Gauss (G), Tesla (T): Units for the magnetic flux density – 1 mT = 10 G
- TC: **T**emperature **C**oefficient (in ppm/Deg.C.)
- NC: **N**ot **C**onnected
- Byte: 8 bits
- Word: 16 bits (= 2 bytes)
- ADC: **A**nalog-to-**D**igital **C**onverter
- LSB: **L**east **S**ignificant **B**it
- MSB: **M**ost **S**ignificant **B**it
- DNL: **D**ifferential **N**on-**L**inearity
- INL: **I**ntegral **N**on-**L**inearity
- RISC: **R**educed **I**nstruction **S**et **C**omputer
- ASP: **A**nalog **S**ignal **P**rocessing
- DSP: **D**igital **S**ignal **P**rocessing
- ATAN: trigonometric function: arctangent (or inverse tangent)
- IMC: **I**ntegrated **M**agneto-**C**oncentrator (IMC®)
- CoRDiC: **Co**ordinate **R**otation **Di**gital **C**omputer (i.e. iterative rectangular-to-polar transform)
- EMC: **E**lectro-**M**agnetic **C**ompatibility
- FE: **F**alling **E**dge
- RE: **R**ising **E**dge
- MSC: **M**essage **S**equence **C**hart
- FW: **F**irm**w**are
- HW: **H**ard**w**are

4. Pinout

Pin #	SOIC-8	TSSOP-16
1	V_{DD}	V_{DEC1}
2	MISO	V_{SS1} (Ground$_1$)
3	Test	V_{DD1}
4	SCLK	$MISO_1$
5	/SS	$Test_2$
6	MOSI	$SCLK_2$
7	V_{DEC}	$/SS_2$
8	V_{SS} (Ground)	$MOSI_2$
9		V_{DEC2}
10		V_{SS2} (Ground$_2$)
11		V_{DD2}
12		$MISO_2$
13		$Test_1$
14		$SCLK_1$
15		$/SS_1$
16		$MOSI_1$

For optimal EMC behavior, it is recommended to connect the unused pins (Test) to the Ground (see section 19).

5. Pin Description

Name	Direction	Type	Function / Description
VDD	VDD	Analog	Supply (5V and 3V3 application diagrams)
MISO	OUT	Digital	Master In Slave Out
Test	I/O	Both	Test Pin
SCLK	IN	Digital	Clock
/SS	IN	Digital	Slave Select
MOSI	IN	Digital	Master Out Slave IN
VDEC	I/O	Analog	5V Application Diagrams Decoupling Pin 3V3 Application Diagrams Supply (Shorted to VDD)
VSS (Ground)	GND	Analog	Ground

6. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, VDD[2]	+ 18 V
Reverse VDD Voltage	– 0.3 V
Supply Voltage, VDEC	+ 3.6 V
Reverse VDEC Voltage	– 0.3 V
Positive Input Voltage	+ 11 V
Reverse Input Voltage	– 11 V
Positive Output Voltage	VDD + 0.3 V
Reverse Output Voltage	– 0.3 V
Operating Ambient Temperature Range, TA	– 40°C … + 150°C
Storage Temperature Range, TS	– 40°C … + 150°C
Magnetic Flux Density	± 700 mT

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] Maximum rise time: 10µs. Rise time faster than 10µs might induce an extra current consumption.

7. Detailed Description

The three components of the applied flux density are measured through the Tria⊗is front end:

$$V_X \propto B_X$$
$$V_Y \propto B_Y$$
$$V_Z \propto B_Z$$

Those three (3) Hall voltages corresponding to the three (3) components of the applied flux density are provided to the ADC (Analog-to-Digital Converter). The Hall signals are processed through a fully differential analog chain featuring the classic offset cancellation technique (Hall plate 2-Phases spinning and chopper-stabilized amplifier).

The amplitude of V_Z is smaller than the two (2) components V_X and V_Y due to the fact that the magnetic gain of the IMC only affects the components parallel to the IC surface.

The conditioned analog signals are converted through a 14 bit ADC and provided to a DSP block for further processing. The DSP stage is based on a 16 bit RISC micro-controller whose primary function is the extraction of the position information (magnetic angle(s)) from the raw signals (after front-end compensation steps) through one the following operations:

$$\alpha = ATAN\left(\frac{k \cdot V_1}{V_2}\right)$$

where V_1 = V_X or V_Y or V_Z , V_2 = V_X or V_Y or V_Z and k (or SMISM) is a programmable factor to match the amplitude of k V_1 and V_2.

$$\alpha = ATAN\left(\frac{\sqrt{(k_\alpha V_3)^2 + (k_t V_2)^2}}{V_1}\right) \text{ and } \beta = ATAN\left(\frac{\sqrt{(k_\beta V_3)^2 + (k_t V_1)^2}}{V_2}\right)$$

where V_1 = V_X or V_Y or V_Z, V_2 = V_X or V_Y or V_Z, V_3 = V_X or V_Y or V_Z and k_α, k_β and k_t are programmable parameters.

The DSP functionality is governed by the micro-code (firmware – FW) of the micro-controller which is stored into the ROM (mask programmable). In addition to the “ATAN” (“Arctangent”) function, the FW controls the whole analog chain, the programming/calibration and also the self-diagnostic modes.

Due to the fact that the “ATAN” operation is performed on the ratios “V_1/V_2”, “V_3/V_1” and “V_3/V_2”, the output is intrinsically self-compensated vs. flux density variations (due to airgap change, thermal or ageing effects) affecting both signals. This feature allows an improved thermal accuracy compared to a conventional linear Hall sensor.

The end-user programmable parameters are stored in EEPROM featuring a Hamming Error Correction Coding (ECC).

The programming steps do not require dedicated pins or programming tool. The operation is performed through the Master and the Serial Protocol using a dedicated and protected function[3].

[3] For debug/demo purpose, Melexis can provide the Melexis Programming Unit PTC-04 with the SPI daughterboard (PTC-04-DB-SPI) and software library (PSF – Product Specific Functions).

8. MLX90363 Electrical Specification

DC Operating Parameters at V_{DD} = 5V (5V Application Diagram) or V_{DD} = 3.3V (3V3 Application Diagram) and for T_A as specified by the Temperature suffix (E, K and L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	V_{DD5}	5V Application Diagram	4.5	5	5.5	V
Nominal Supply Voltage	V_{DD33}	3V3 Application Diagram	3.15	3.3	3.45	V
Supply Current [4]	I_{DD}			12.5	15.5	mA
Standby Current	$I_{STANDBY}$			3.5	4.5	mA
Supply Current at V_{DD} MAX	I_{DDMAX}	V_{DD} = 18V			18	mA
POR Rising Level	POR LH	Voltage referred to V_{DEC}	2.6	2.8	3.1	V
POR Falling Level	POR HL	Voltage referred to V_{DEC}	2.5	2.7	2.9	V
POR Hysteresis	POR Hyst	Voltage referred to V_{DEC}		0.1		V
MISO Switch Off Rising Level	MT8V LH	VDD level for disabling MISO[5]	7.5		9.5	V
MISO Switch Off Falling Level	MT8V HL	VDD level for disabling MISO[5]	6		7.5	V
MISO Switch Off Hysteresis	MT8V Hyst	VDD level for disabling MISO[5]	1		2	V
Input High Voltage Level	V_{IH}		65%*V_{DD}	-	-	V
Input Low Voltage Level	V_{IL}		-	-	35%*V_{DD}	V
Input Hysteresis	V_{HYS}			20%*V_{DD}		V
Input Capacitance	C_{IN}	Referred to GND		20		pF
Output High Voltage Level	V_{OH}	Current Drive I_{OH} = 0.5 mA	V_{DD}-0.4			V
Output Low Voltage Level	V_{OL}	Current Drive I_{OH} = 0.5 mA			0.4	V
Output High Short Circuit Current	I_{shortH}	V_{OUT} forced to 0V		20	30	mA
Output Low Short Circuit Current	I_{shortL}	V_{OUT} forced to V_{DD}		25	30	mA

9. MLX90363 Isolation Specification

Only valid for the package code GO i.e. dual die version.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Resistance		Between 2 dies	4			MΩ

[4] For the dual version, the supply current is multiplied by 2
[5] Above the MT8V threshold, no SPI communication is possible.

10. MLX90363 Timing Specification

10.1. Timing Specification for 5V Application Diagram

DC Operating Parameters at V_{DD} = 5V and for T_A as specified by the Temperature suffix (E, K)[6].

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck		15.2		18.8	MHz
Frame Rate	FR	Trigger Mode 1 (Trg. Mod. 1), Markers 0&2, SCI 2MHz All other modes, markers and SCI Frequencies			1000 500	s^{-1} s^{-1}
Watchdog time-out	Wd	See Section 18	15.3	18.8	20	ms
Power On to First *SCI* message (Start-up Time)	tStartUp	See Section 14.20	20			ms
SCI protocol: Slave-select rising-edge to falling-edge	tShort		120			us
SCI protocol: EEPROMWrite Time	teewrite	Trimmed oscillator	32			ms
Diagnostic Loop Time	tDiag	FR = 1000 s^{-1},Trg.Mod.1, Mark 0&2 FR = 500 s^{-1} FR = 200 s^{-1}			40 20 10	ms ms ms
Internal 1MHz signal	t1us	Ck = 19MHz		1		us
MISO Rise Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
MISO Fall Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
Magnetic Flux Density Frequency		Sinewave Flux Density[7] FR = 1000 s^{-1} FR = 500 s^{-1} FR = 100 s^{-1}			 4 8 18	 Hz Hz Hz
		FR = 1000 s^{-1}[8] FR = 500 s^{-1}[8] FR = 200 s^{-1}[8]			28 14 5.6	Hz Hz Hz

[6] Please contact Melexis for Timing specification for “L” Temperature suffix
[7] Sensitivity monitors enable (See section 18). Beyond that frequency, the Sensitivity monitor should be disabled.
[8] Limitation linked to the Automatic Gain Control. Beyond that frequency, there is a reduced immunity to norm change (like vibration). See also Section 19.4.

10.2. Timing Specification for 3V3 Application Diagram

DC Operating Parameters at V_{DD} = 3.3V and for T_A as specified by the Temperature suffix (E, K)[9].

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck		13.1		18.8	MHz
Frame Rate	FR	Trigger Mode 1 (Trg. Mod. 1), Markers 0&2, SCI 2MHz All other modes, markers and SCI Frequencies			862 430	s^{-1} s^{-1}
Watchdog time-out	Wd	See Section 18	15.3		23.2	ms
Power On to First *SCI* message (Start-up Time)	tStartUp	See Section 14.20	23.2			ms
SCI protocol: Slave-select rising-edge to falling-edge	tShort		139			us
SCI protocol: EEPROMWrite Time	teewrite	3.3V Trimmed oscillator	37			ms
Diagnostic Loop Time	tDiag	FR = 862 s^{-1},Trg.Mod.1, Mark 0&2 FR = 430 s^{-1} FR = 215 s^{-1}			46.4 23.2 11.6	ms ms ms
Internal 1MHz signal	t1us	Ck = 19MHz		1		us
MISO Rise Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
MISO Fall Time		C_L = 30pF, R_L = 10 kΩ		35	60	ns
Magnetic Flux Density Frequency		FR = 862 s^{-1}[10] FR = 430 s^{-1}[10] FR = 215 s^{-1}[10]			24 12 4.8	Hz Hz Hz

[9] Please contact Melexis for Timing specification for "L" Temperature suffix.
[10] Limitation linked to the Automatic Gain Control. Beyond that frequency, there is a reduced immunity to norm change (like vibration). See also Section 19.4.

11. MLX90363 Accuracy Specification

DC Operating Parameters at V_{DD} = 5V (5V Application Diagram) or V_{DD} = 3.3V (3V3 Application Diagram) and for T_A as specified by the Temperature suffix (E, K and L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals X, Y and Z	R_{ADC}			14		bit
Serial Interface Resolution	R_{SI}	On the angle value On the X,Y,Z values		14 12		bit bit
Offset on the Raw Signals X, Y and Z	X0, Y0, Z0	T_A = 25°C	-30		+30	LSB_{14}
Mismatch on the Raw Signals X, Y and Z	 $SMISM_{XY}$ $SMISM_{XZ}$ $SMISM_{YZ}$	T_A = 25°C Between X and Y Between X and Z(11) Between Y and Z(11)	 -1 -30 -30		 1 +30 +30	 % % %
Magnetic Angle Phase Error	 $ORTH_{XY}$ $ORTH_{XZ}$ $ORTH_{YZ}$	T_A = 25°C Between X and Y Between X and Z(12) Between Y and Z(12)	 -0.3 -10 -10		 0.3 10 10	 Deg Deg Deg
Intrinsic Linearity Error(13)	Le	T_A = 25°C, Magnetic Angle ∠XY Magnetic Angle ∠XZ, ∠YZ(14)	 -1 -20		 1 20	 Deg Deg
Supply Dependency		5V Application Diagram V_{DD} = 4.5 … 5.5V	 -0.1		 0.1	 Deg
		3V3 Application Diagram V_{DD} = 3.20 … 3.40V Temperature suffix E and K 20mT 50mT Temperature suffix L 20mT 50mT	 -0.8 -0.4 -1 -0.6		 0.8 0.4 1 0.6	 Deg Deg Deg Deg

MLX90363 Accuracy Specification continues…

[11] The Mismatch between X or Y and Z can be reduced through the calibration of the SMISM (or k) factor in the end application. See section 17.3.2 for more information

[12] The Magnetic Angle Phase error X or Y and Z can be reduced through the calibration of the ORTH_B1B2 factor in the end application. See section 17.3.2 for more information

[13] The Intrinsic Linearity Error is a consolidation of the IC errors (offset, sensitivity mismatch, phase error) taking into account an ideal rotating field. Once associated to a practical magnetic construction and the associated mechanical and magnetic tolerances, the output linearity error increases.

[14] The Intrisic Linearity Error for Magnetic Angle ∠XZ, ∠YZ can be reduced through the programming of the SMISM (or k) factor and ORTH_B1B2. By applying the correct compensation, a non linearity error of +/-1 deg can be reached. See section 17.3.2 for more information

… MLX90363 Accuracy Specification						
Thermal Offset Drift[15]		Temperature suffix E and K Temperature suffix L	-30 -45		+30 +45	LSB_{14} LSB_{14}
Thermal Drift of Sensitivity Mismatch[16]		XY axis, XZ axis, YZ axis Temperature suffix E and K Temperature suffix L	 - 0.5 - 0.7		 + 0.5 + 0.7	 % %
Thermal Drift of Magnetic Angle Phase Error		XY axis, XZ axis, YZ axis	0.1		0.1	Deg
Magnetic Angle Noise[17]		Temperature suffix E and K 20mT, No Filter 50mT, No Filter 50mT, FILTER=1 Temperature suffix L 20mT, No Filter 50mT, No Filter 50mT, FILTER=1			 0.20 0.10 0.07 0.25 0.12 0.08	 Deg Deg Deg Deg Deg Deg
Raw signals X, Y, Z Noise[17]		Temperature suffix E and K 20mT, No Filter 50mT, No Filter 50mT, FILTER_TYPE =1 Temperature suffix L 20mT, No Filter 50mT, No Filter 50mT, FILTER=1			 12 6 4 14 7 4	 LSB_{14} LSB_{14} LSB_{14} LSB_{14} LSB_{14} LSB_{14}

[15] For instance, Thermal Offset Drift equal ± 30LSB_{14} yields to max. ± 0.32 Deg. error. This is only valid if the Virtual Gain is not fixed (See Section 17.6).See Front End Application Note for more details.
[16] For instance, Thermal Drift of Sensitivity Mismatch equal ± 0.4% yields to max. ± 0.1 Deg. error. See Front End Application Note for more details.
[17] Noise is defined by ± 3 σ for 1000 successive acquisitions. The application diagram used is described in the recommended wiring (Section 20). For detailed information, refer to section Filter in application mode (Section 17.5).

12. MLX90363 Magnetic Specification

DC Operating Parameters at V_{DD} = 5V (5V Application Diagram) or V_{DD} = 3.3V (3V3 Application Diagram) and for T_A as specified by the Temperature suffix (E, K and L).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density in X or Y	B_{XY}[18]		20	50	70[19]	mT
Magnetic Flux Density in Z	B_Z[18]		24	75	126	mT
Magnet Temperature Coefficient	TCm		-2400		0	ppm/°C
IMC Gain[20]	GainIMC		1.2	1.4	1.8	

13. MLX90363 CPU & Memory Specification

The digital signal processing is based on a 16 bit RISC µController featuring

- ROM & RAM
- EEPROM with hamming codes (ECC)
- Watchdog
- C Compiler

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				14		kByte
RAM				256		Byte
EEPROM				64		Byte
CPU MIPS		Ck = 15 MHz		3.5		MIPS

[18] The condition must be fulfilled for at least one field B_X, B_Y or B_Z.
[19] Above 70 mT, the IMC starts saturating yielding an increase of the linearity error.
[20] This is the magnetic gain linked to the Integrated Magneto Concentrator structure. It applies to B_X and B_Y and not to B_Z. This is the overall variation. Within one lot, the part to part variation is typically ± 10% versus the average value of the IMC gain of that lot.

14. MLX90363 Serial Interface

The MLX90363 serial interface allows a master device to operate the position sensor. The MLX90363 interface allows multi-slave applications and synchronous start of the data acquisition among the slaves. The interface offers 2 Mbps data transfer bit rate and is full duplex. The interface accepts messages of 64 bits wide only, making the interfacing robust.
In this document, the words *message*, *frame* and *packet* refer to the same concept.

14.1. Electrical Layer and Timing Specification

Message transmissions start necessarily at a falling edge on */SS* and end necessarily at a rising edge on the */SS* signal. This defines a message. The serial interface counts the number of transmitted bits and declares the incoming message invalid when the bit count differs from 64. The master must therefore ensure the flow described below:

1. Set pin */SS* Low
2. Send and receive 8 bytes or four (4x) 16 bit words
3. Set pin */SS* High

The *MISO* and *MOSI* signals change on *SCLK* rising edge and are captured on *SCLK* falling edge. The most-significant-bit of the transmitted byte or word comes first [21].

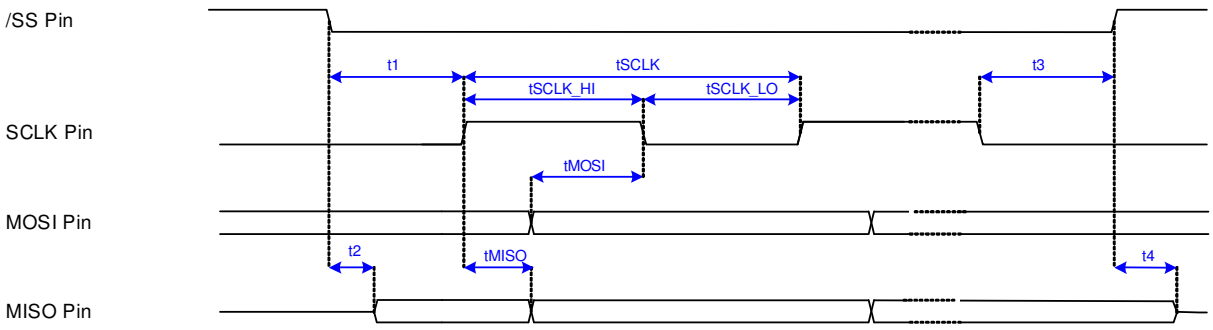


Figure 2 – Serial Interface Timing Diagram

The interface is sensitive, in Trigger mode 2 (see section 14.6), to *Sync* pulses. A *Sync* pulse is negative pulse on */SS*, while *SCLK* is kept quiet.

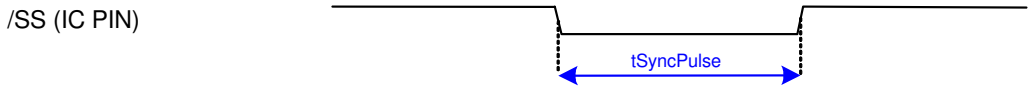


Figure 3 – Sync Pulse Timing Diagram

[21] For instance, for master compatible w/ the Motorola SPI protocol, the configuration bits must be *CPHA*=1, *CPOL*=0, *LSBFE*=0.

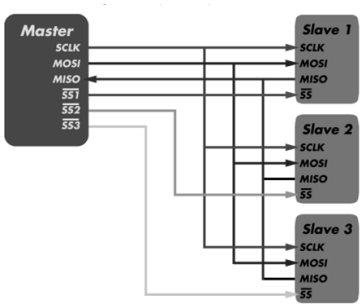
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock Period	tSCLK	EE_PINFILTER = 1	450	500		ns
		EE_PINFILTER = 2	900	1000		ns
		EE_PINFILTER = 3	1800	2000		ns
Clock Low Level	tSCLK_HI	EE_PINFILTER = 1	225			ns
		EE_PINFILTER = 2	450			ns
		EE_PINFILTER = 3	900			ns
Clock High Level	tSCLK_LO	EE_PINFILTER = 1	225			ns
		EE_PINFILTER = 2	450			ns
		EE_PINFILTER = 3	900			ns
Clock to Data Delay	tMISO	EE_PINFILTER = 1 , Cload = 30pF			210	ns
		EE_PINFILTER = 2 , Cload = 30pF			300	ns
		EE_PINFILTER = 3 , Cload = 30pF			510	ns
Data Capture Setup Time	tMOSI		30			ns
/SS FE to SCLK RE	t1	EE_PINFILTER = 1	225			ns
		EE_PINFILTER = 2	450			ns
		EE_PINFILTER = 3	900			ns
/SS FE to MISO Low Impedance	t2	EE_PINFILTER = 1		90	120	ns
		EE_PINFILTER = 2		180	210	ns
		EE_PINFILTER = 3		370	420	ns
SCLK FE to /SS RE	t3		225			ns
/SS RE to MISO High Impedance	t4	EE_PINFILTER = 1		90	120	ns
		EE_PINFILTER = 2		180	210	ns
		EE_PINFILTER = 3		370	420	ns
Sync Pulse Duration	tSyncPulse	EE_PINFILTER = 1	520		10000	ns
		EE_PINFILTER = 2	610		10000	ns
		EE_PINFILTER = 3	820		10000	ns

Table 1 - Serial Interface Timing Specifications

Melexis recommends using the multi-slave application diagram as shown on the right.

The *SCLK*, *MISO* and *MOSI* wires interconnect the slaves with the master. A slave is selected by its dedicated */SS* input. A slave *MISO* output is in high-impedance state when the slave is not selected.

Slaves can be triggered synchronously by sending *Sync* pulses on the different */SS*. The pulses must not overlap to avoid electrical short-circuits on the *MISO* bus.



14.2. Serial Protocol

The serial protocol of MLX90363 allows the SPI master device to request the following information:

- Position (magnetic angle Alpha)
- Raw field components (X,Y and Z)
- Self-Diagnostic data

It allows customizing the calibration of the sensor, when needed, at the end-of-line, through EEPROM programming.

The serial protocol offers a transfer rate of 1000 messages/sec. A regular message holds position and diagnostic information. The data acquisition start and processing is fully under the control of the SPI master. The user configuration bits, stored in EEPROM, are programmable with this protocol.

Data integrity is guaranteed in both directions by an 8 bit CRC covering the content of the incoming and outgoing messages. In a dual sensors application, a *Sync* pulse allows a synchronous start of the raw signals acquisition.

14.3. Message General Structure

A message has a unique *Opcode*. The general structure of a message consists of 8 bytes (byte #0, transmitted first, to byte #7 transmitted last).

Byte #7 (the last byte transmitted) holds an 8 bit CRC. The byte #6 holds a *Marker* plus either an *Opcode* or a *rolling counter*.

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	(4)							(3)	0	(2)							(1)
3									2								(5)
5									4								
7	CRC								6	Marker		Opcode or Roll Counter					

Table 2 – General Structure of a message and bit naming convention

(1) This bit is named Byte0[0] (2) This bit is named Byte0[7]
(3) This bit is named Byte1[0] (4) This bit is named Byte1[7]
(5) This bit is named Byte2[0]

A blank cell refers necessarily to a bit 0.

In a byte, the most-significant-bit is transmitted first (for instance, Byte0[7] is transmitted first, Byte0[0] transmitted last).
Parameter *CRC*[7:0] is Byte7[7:0], Parameter *Marker*[1:0] is Byte6[7:6],
Parameter *Opcode*[5:0] (or *Roll Counter*[5:0]) is Byte6[5:0]

CRCs are encoded and decoded according the following algorithm (language-C):

```
crc = 0xFF;
crc = cba_256_TAB[ Byte0 ^ crc ];
crc = cba_256_TAB[ Byte1 ^ crc ];
crc = cba_256_TAB[ Byte2 ^ crc ];
crc = cba_256_TAB[ Byte3 ^ crc ];
crc = cba_256_TAB[ Byte4 ^ crc ];
crc = cba_256_TAB[ Byte5 ^ crc ];
crc = cba_256_TAB[ Byte6 ^ crc ];
crc = ~crc;
```

The Table 3 corresponds to the CRC-8 polynomial “0xC2”.

cba_256_TAB	0	1	2	3	4	5	6	7
0	0x00	0x2f	0x5e	0x71	0xbc	0x93	0xe2	0xcd
1	0x57	0x78	0x09	0x26	0xeb	0xc4	0xb5	0x9a
2	0xae	0x81	0xf0	0xdf	0x12	0x3d	0x4c	0x63
3	0xf9	0xd6	0xa7	0x88	0x45	0x6a	0x1b	0x34
4	0x73	0x5c	0x2d	0x02	0xcf	0xe0	0x91	0xbe
5	0x24	0x0b	0x7a	0x55	0x98	0xb7	0xc6	0xe9
6	0xdd	0xf2	0x83	0xac	0x61	0x4e	0x3f	0x10
7	0x8a	0xa5	0xd4	0xfb	0x36	0x19	0x68	0x47
8	0xe6	0xc9	0xb8	0x97	0x5a	0x75	0x04	0x2b
9	0xb1	0x9e	0xef	0xc0	0x0d	0x22	0x53	0x7c
10	0x48	0x67	0x16	0x39	0xf4	0xdb	0xaa	0x85
11	0x1f	0x30	0x41	0x6e	0xa3	0x8c	0xfd	0xd2
12	0x95	0xba	0xcb	0xe4	0x29	0x06	0x77	0x58
13	0xc2	0xed	0x9c	0xb3	0x7e	0x51	0x20	0x0f
14	0x3b	0x14	0x65	0x4a	0x87	0xa8	0xd9	0xf6
15	0x6c	0x43	0x32	0x1d	0xd0	0xff	0x8e	0xa1
16	0xe3	0xcc	0xbd	0x92	0x5f	0x70	0x01	0x2e
17	0xb4	0x9b	0xea	0xc5	0x08	0x27	0x56	0x79
18	0x4d	0x62	0x13	0x3c	0xf1	0xde	0xaf	0x80
19	0x1a	0x35	0x44	0x6b	0xa6	0x89	0xf8	0xd7
20	0x90	0xbf	0xce	0xe1	0x2c	0x03	0x72	0x5d
21	0xc7	0xe8	0x99	0xb6	0x7b	0x54	0x25	0x0a
22	0x3e	0x11	0x60	0x4f	0x82	0xad	0xdc	0xf3
23	0x69	0x46	0x37	0x18	0xd5	0xfa	0x8b	0xa4
24	0x05	0x2a	0x5b	0x74	0xb9	0x96	0xe7	0xc8
25	0x52	0x7d	0x0c	0x23	0xee	0xc1	0xb0	0x9f
26	0xab	0x84	0xf5	0xda	0x17	0x38	0x49	0x66
27	0xfc	0xd3	0xa2	0x8d	0x40	0x6f	0x1e	0x31
28	0x76	0x59	0x28	0x07	0xca	0xe5	0x94	0xbb
29	0x21	0x0e	0x7f	0x50	0x9d	0xb2	0xc3	0xec
30	0xd8	0xf7	0x86	0xa9	0x64	0x4b	0x3a	0x15
31	0x8f	0xa0	0xd1	0xfe	0x33	0x1c	0x6d	0x42

Table 3 – cba_256_TAB Look-up table Polynomial “C2”

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	0xFF								0	0xC1							
3	0xFF								2	0x16							
5	0xFF								4	0xD4							
7	0x23								6	0x86							

Table 4 – Example of valid CRC

14.4. Regular Messages

The MLX90363 offers three types of regular messages:

- "α" – diagnostic
- "α – β" – diagnostic
- X – Y – Z – diagnostic

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	E1	E0	ALPHA [13:8]						0	ALPHA [7:0]							
3	0								2	0							
5	0								4	VG[7:0]							
7	CRC								6	0	0	ROLL					

Table 5 – "α" message

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	E1	E0	ALPHA [13:8]						0	ALPHA [7:0]							
3			BETA [13:8]						2	BETA [7:0]							
5	0								4	VG[7:0]							
7	CRC								6	0	1	ROLL					

Table 6 – "α – β" message

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1	E1	E0	X COMPONENT [13:8]						0	X COMPONENT [7:0]							
3			Y COMPONENT [13:8]						2	Y COMPONENT [7:0]							
5			Z COMPONENT [13:8]						4	Z COMPONENT [7:0]							
7	CRC								6	1	0	ROLL					

Table 7 – "X – Y – Z" message

The bits byte6[7] and byte6[6] are markers. They allow the master to recognize the type of regular message (00b, 01b, 10b). The marker is present in all messages (incoming and outgoing). The marker of any message which is not a regular message is equal to 11b.

The bits E1 and E0 report the status of the diagnostics (4 possibilities) as described in the Table 8 – See section 18 for more details.

E1	E0	Description
0	0	First Diagnostics Sequence Not Yet Finished
0	1	Diagnostic Fail
1	0	Diagnostic Pass (Previous cycle)
1	1	Diagnostic Pass – New Cycle Completed

Table 8 - Diagnostics Status Bits

14.4.1. Note for the regular message "X – Y – Z – diagnostic" (Marker = 2)

In the case of marker = 2, the X,Y,Z components are given after offset compensation and filtering (see signal processing in section 19.2). These components are gain dependent (see also section 17.6).

The sensitivity in the X and Y direction is always higher than the Z direction by the IMC Gain factor (see parameter GainIMC in section 12). Melexis therefore recommends multiplying the Z component by the GainIMC factor inside the master in order to use the MLX90363 as a 3D magnetometer.

14.5. Trigger Mode 1

The master sends a GET1 command to initiate the magnetic field acquisition and post-processing. It waits *tSSREFE*, issues the next GET1 and receives at the same time the regular message resulting from the previous GET.

The field sensing, acquisition and post-processing is starting on */SS* rising edge events.

Although GET1 commands are preferably followed by another GET1 command or a NOP command, any other commands are accepted by the slave.

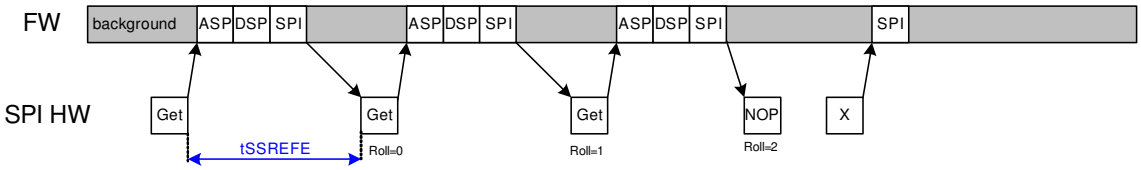


Figure 4 – Trigger mode 1

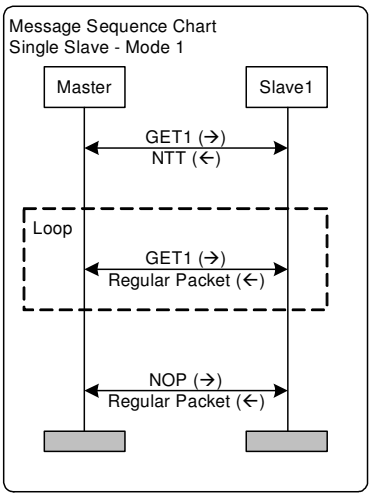


Figure 5 – Trigger Mode 1 Message Sequence Chart

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1								RST	0								
3	*Time – Out*								2	*Value*							
5									4								
7	CRC								6	Marker	0	1	0	0	1	1	

Table 9 – GET1 MOSI Message (Opcode = 19)

Note: The NOP message is described at section “14.11”

- The parameter *Marker* defines the regular data packet type expected by the master:

Marker = 0 refers to frame type “ALPHA + Diagnostic”.
Marker = 1 refers to frame type “ALPHA + BETA + Diagnostic”.
Marker = 2 refers to frame type “Components X + Y + Z +Diagnostic”.

- The parameter *Rst* (Byte1[0]) when set, resets the rolling counter attached to the regular data packets.

- The parameter *TimeOutValue* tells the maximum life time of the Regular Data Message.
  The time step is t1us (See table in Section 10), the maximum time-out is 65535 * t1us. The time-out timer starts when the message is ready, and stops on the SS rising edge of the next message.

  On time-out occurrence, there are two possible scenarios:
  Scenario 1. SS is high, there is no message exchange. In this case, a NTT message replaces the regular message in the SCI buffer.
  Scenario 2. SS is low, the regular packet is being sent out. In this case, the timeout violation is reported on the next message, this later being an NTT message.

14.6. Trigger Mode 2

The Trigger Mode 1 works without *Sync* pulses, as the GET1 command plays the role of a sync pulse. When a delay between the regular message readback and the start of acquisition is needed, or when two or more slaves should be triggered synchronously, the use of a sync pulse is required, and this is the meaning of the Trigger Mode 2.

Principle: The master first enables the trigger mode 2 by issuing a GET2 command.
The master then sends a *Sync* Pulse, at the appropriate time, to initiate the magnetic field acquisition and post-processing.
Finally the master reads the response message with a NOP or a GET2. The GET2 command re-initiates a sync pulse triggered acquisition, whereas the NOP command would just allow the master to receive the latest packet.

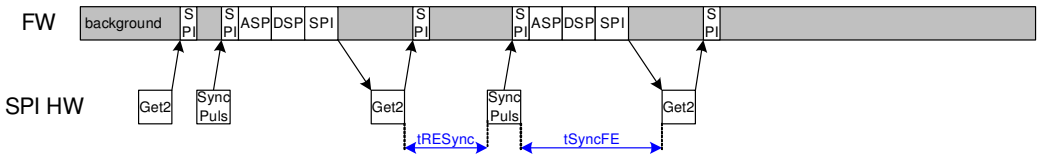


Figure 6 – Trigger Mode 2 – Single Slave Approach

A timing constraint between GET2 and the sync pulse (*tRESync*) should be met.

When this timing is smaller than the constraint, the sync pulse might not be taken in account, causing the next GET2 to return a NTT packet.

GET1 and GET2/SyncPulse can be interlaced.

Multi-slave approach: The way of working described below fits the multi-slave applications where synchronous acquisitions are important. GET2 commands are sent one after the other to the slaves. Then the Sync Pulses are sent almost synchronously (very shortly one after the other).

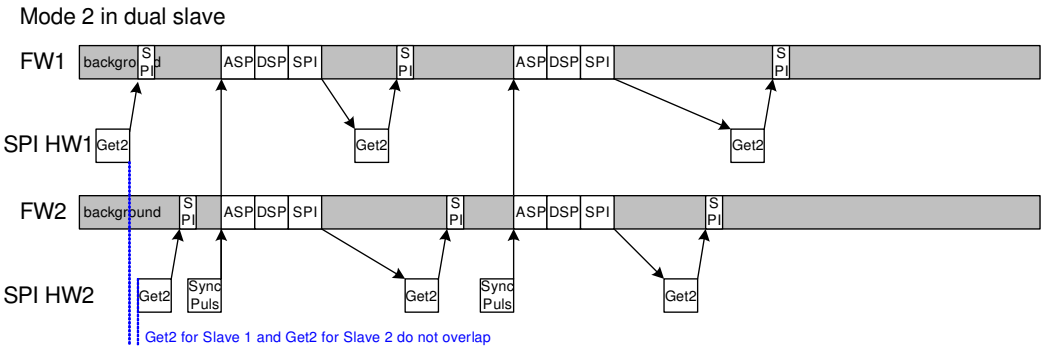


Figure 7 – Trigger mode 2 - Multi-slave approach, example for two slaves

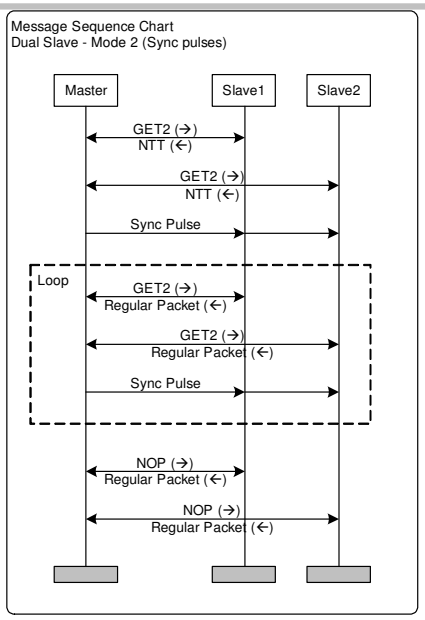


Figure 8 – Trigger mode 2 Message Sequence Chart

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1								RST	0								
3	*Time – Out*								2	*Value*							
5									4								
7	CRC								6	Marker	0	1	0	1	0	0	

Table 10 – GET2 MOSI Message (Opcode = 20)

Parameter definition: See GET1 (Section 14.5).

14.7. Trigger Mode 3

Principle: The acquisition sequences are triggered by a GET message, but unlike the Mode 1, the resulting data (position …) is buffered. The slave-out messages contain the buffered data of the previous GET message, and not the newly computed values corresponding to the current GET slave-in request. The buffering releases constraints on the SCI clock frequency (*SCLK*). The Mode 3 offers frame rates as high as Mode 1, if not higher, with slower *SCLK* frequencies. When the clock frequency is limited (400 kbps or less), and when it matters to reach a certain frame rate, Mode 3 is preferred over Mode 1. In any other cases, for instance when the shortest response time represents the main design criteria, Mode 1 is preferred.

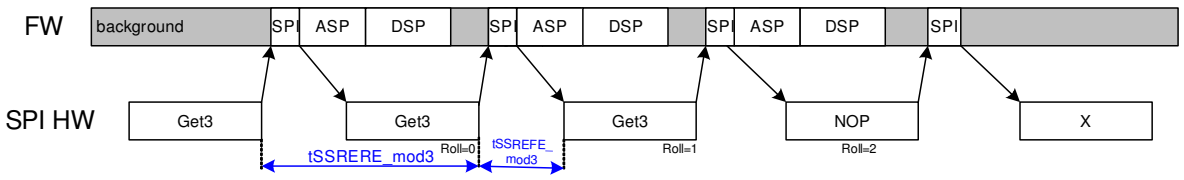


Figure 9 – Trigger mode 3

GET3 sequences must end with a NOP.

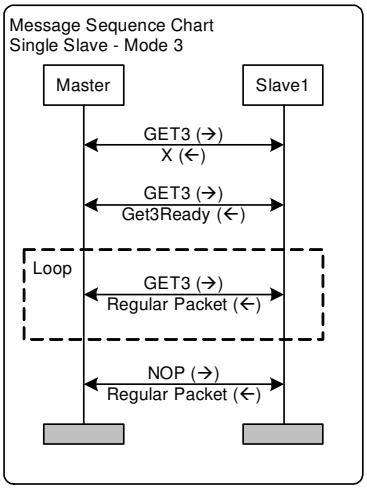


Figure 10 – Trigger mode 3 Message Sequence Chart

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1								RST	0								
3	*Time – Out*								2	*Value*							
5									4								
7	CRC								6	Marker	0	1	0	1	0	1	

Table 11 – GET3 MOSI Message (Opcode = 21)

Parameter definition: See GET1 (Section 14.5)

#	7	6	5	4	3	2	1	0	#	7	6	5	4	3	2	1	0
1									0								
3									2								
5									4								
7	CRC								6	1	1	1	0	1	1	0	1

Table 12 – Get3Ready Slave-Out Message (Opcode = 45)

14.8. Trigger Modes Timing Specifications

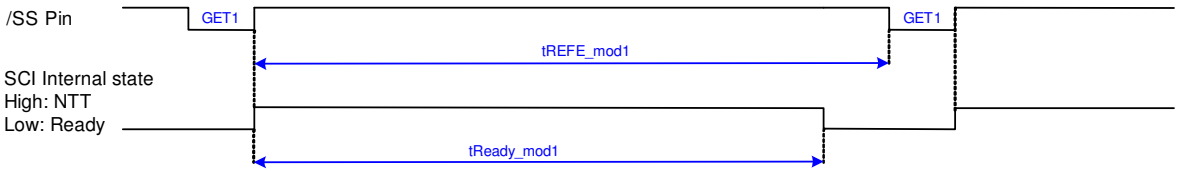


Figure 11 – Trigger mode 1 timing diagram

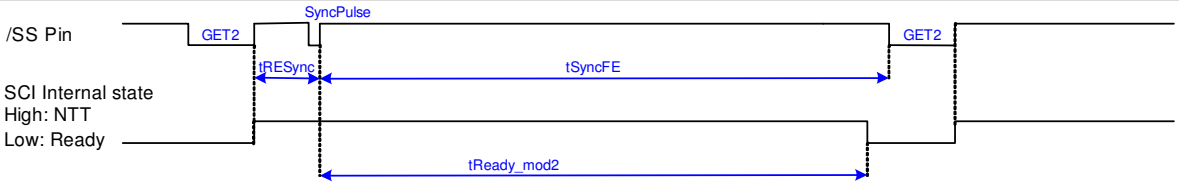


Figure 12 – Trigger mode 2 timing diagram

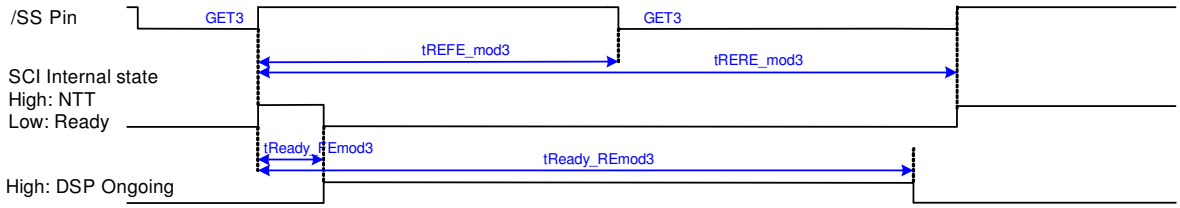


Figure 13 – Trigger mode 3 timing diagram

5V Application Diagram

Items	Definition	Marker	Min	Typ	Max	Unit
tREFE_mod1	Get1 SS Rising Edge to next Get1 SS Falling Edge	0	920			µs
		1	1050			µs
		2	920			µs
tReady_mod1	Get1 SSRE to SO Answer ReadyToTransmit	0			920	µs
		1			1050	µs
		2			920	µs

Table 13 – Trigger Modes Timing Specification (Mode 1, V_{DD}=5V)

Items	Definition	Marker	Min	Typ	Max	Unit
tSyncFE	Sync Pulse (RE) to Get2 Falling Edge	0	874			µs
		1	1004			µs
		2	874			µs
tReady_mod2	Sync Pulse (RE) to SO Answer ReadyToTransmit	0			874	µs
		1			1004	µs
		2			874	µs
tRESync	Get2 SS Rising Edge to Sync Pulse (RE)		80			µs

Table 14 – Trigger Modes Timing Specification (Mode 2, V_{DD}=5V)

Items	Definition	Marker	Min	Typ	Max	Unit
tRERE_mod3	Get3 SS RE to RE	0	950			µs
		1	1080			µs
		2	950			µs
tReadyRE_mod3	Get3 SS RE to DSP Completion	0			950	µs
		1			1080	µs
		2			950	µs
tREFE_mod3	Get3 SS Rising to Falling		90			µs
tReadyFE_mod3	Get3 SS RE to SO Answer ReadyToTransmit				90	µs

Table 15 – Trigger Modes Timing Specification (Mode 3, V_{DD}=5V)

3V3 Application Diagram

Items	Definition	Marker	Min	Typ	Max	Unit
tREFE_mod1	Get1 SS Rising Edge to next Get1 SS Falling Edge	0	1067			µs
		1	1218			µs
		2	1067			µs
tReady_mod1	Get1 SSRE to SO Answer ReadyToTransmit	0			1067	µs
		1			1218	µs
		2			1067	µs

Table 16 – Trigger Modes Timing Specification (Mode 1, V_{DD} = 3.3V)

Items	Definition	Marker	Min	Typ	Max	Unit
tSyncFE	Sync Pulse (RE) to Get2 Falling Edge	0	1014			µs
		1	1165			µs
		2	1014			µs
tReady_mod2	Sync Pulse (RE) to SO Answer ReadyToTransmit	0			1014	µs
		1			1165	µs
		2			1014	µs
tRESync	Get2 SS Rising Edge to Sync Pulse (RE)		93			µs

Table 17 – Trigger Modes Timing Specification (Mode 2, V_{DD} = 3.3V)

Items	Definition	Marker	Min	Typ	Max	Unit
tRERE_mod3	Get3 SS RE to RE	0	1102			µs
		1	1253			µs
		2	1102			µs
tReadyRE_mod3	Get3 SS RE to DSP Completion	0			1102	µs
		1			1253	µs
		2			1102	µs
tREFE_mod3	Get3 SS Rising to Falling		105			µs
tReadyFE_mod3	Get3 SS RE to SO Answer ReadyToTransmit				105	µs

Table 18 – Trigger Modes Timing Specification (Mode 3, V_{DD} = 3.3V)