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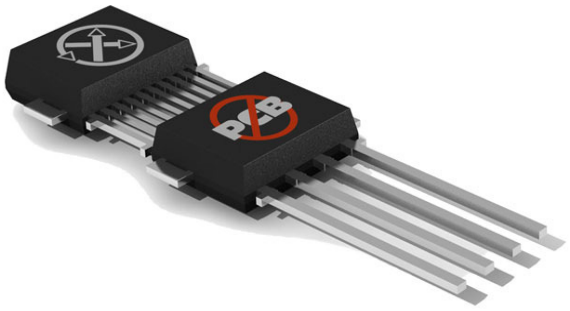
MLX90364

Triaxis® Position Sensor Assembly

Features and Benefits

Absolute Rotary & Linear Position Sensor IC
Robust Dual Mold Package (DMP) feat. 4 Decoupling Capacitors (ESD/EMC)
Reliable NoPCB Module Integration
Triaxis Hall Technology
Simple Magnetic Design
Programmable Transfer Characteristic (Multi-Points – Piece-Wise-Linear)
Selectable Output Mode: Analog (Ratiometric) – Pulse Width Modulation (PWM)
12 bit Resolution - 10 bit Thermal Accuracy
Open/Short Diagnostics
On Board Diagnostics
Over-Voltage Protection
Under-Voltage Detection
48 bit ID Number option
Automotive Temperature Range
AEC-Q100 & AEC-Q200 Qualified
DMP-4 RoHS Compliant



Applications

Absolute Rotary Position Sensor
Absolute Linear Position Sensor
EGR Valve Position Sensor
Turbo Actuator
Throttle Position Sensor
Clutch,Shift & Fork Position Sensor
Ride Height Position Sensor
Float Level Sensor

Ordering Information

Product Code	Temperature Code	Package Code	Option code	Packing form code
MLX90364	L	VS	ADB[1]-200	RE
MLX90364	L	VS	ADB[1]-201	RE
MLX90364	L	VS	ADB-203	RE
MLX90364	L	VS	ADB[1]-250	RE
MLX90364	L	VS	ADB[1]-251	RE
MLX90364	L	VS	ADB[1]-253	RE
MLX90364	L	VS	ADD-200	RE
MLX90364	L	VS	ADD-201	RE
MLX90364	L	VS	ADD-203	RE
MLX90364	L	VS	ADD-250	RE
MLX90364	L	VS	ADD-251	RE
MLX90364	L	VS	ADD-253	RE
MLX90364	L	VS	ADD-400	RE
MLX90364	L	VS	ADD-401	RE
MLX90364	L	VS	ADD-403	RE
MLX90364	L	VS	ADD-300	RE
MLX90364	L	VS	ADD-301	RE
MLX90364	L	VS	ADD-303	RE

Legend:

Temperature Code: L for Temperature Range - 40°C to 150°C,

Package Code: VS for DMP-4

Option Code: AAA-**123:**

AAA: die version

1: Supply capacitance
- 2 : 2x 100nF
- 4 : 2x 220nF
- 3 : 1x 220nF

2 : Output capacitance
- 0 : 100nF
- 5 : 10nF

3: Trim and form option:
- 0: Standard (straight leads) see section 20.1
- 1: Trim and Form STD1 2.54 see section 20.2
- 3: Trim and Form STD2 2.54 see section 20.3

Packing Form: RE for Reel (face-up)
RX for Reel (face down)
SP Sample Pack

Ordering Example: MLX90364LVS-ADB-200-SP

[1] Version ADB is not recommended for a new design, please use version ADD

1. Functional Diagram

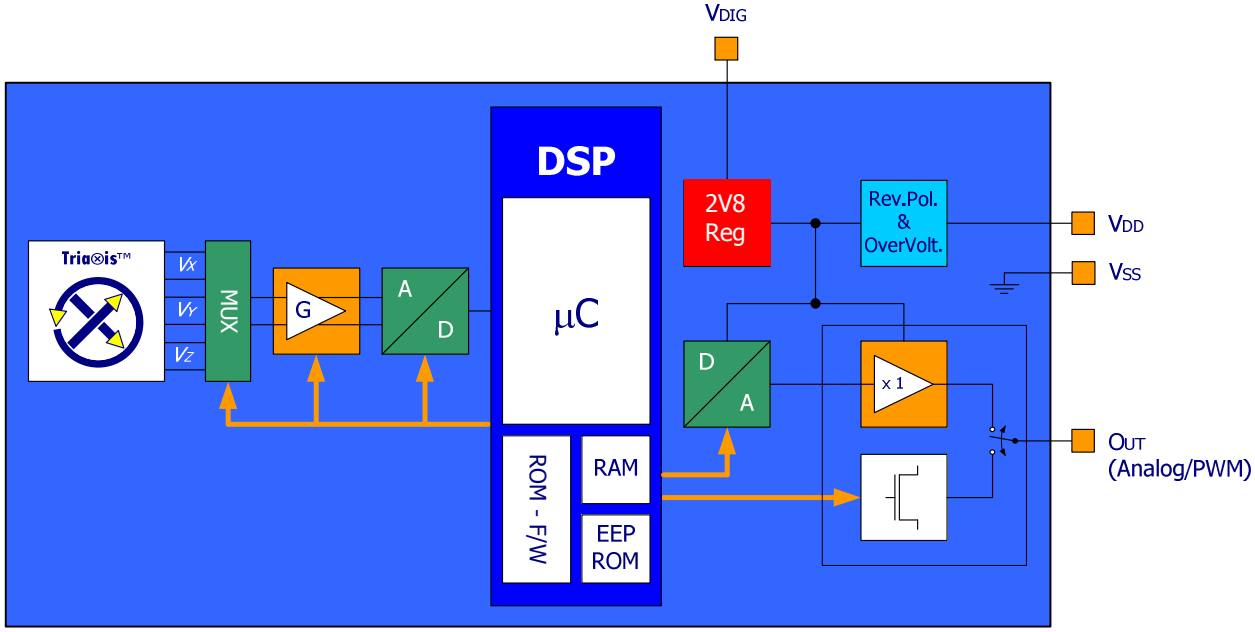


Figure 1: MLX90364 Block Diagram

2. Description

The MLX90364 Triaxis® Position Sensor Assembly is a high accuracy linear and angular position sensor which eliminates need for inclusion of a printed circuit board (PCB) within sensing modules.

This device is based on a Dual Mold Package (DMP) construction, which integrates a Triaxis position sensing die together with the decoupling capacitors necessary to meet the strenuous ESD and EMC requirements. No PCB is needed.

The Triaxis position sensing die is nothing but the one used for the MLX90365 in conventional surface-mount packages (SOIC-8 – single die & TSSOP-16 – dual die).

The decoupling capacitors are X8R type and well suited for package integration and the target operating temperature range.

Similarly to other Triaxis products, the MLX90364 is sensitive to the flux density applied orthogonally and parallel to the IC surface i.e. the 3 components of the flux density applied to the IC (i.e. BX, BY and BZ).

This allows the MLX90364 with the correct magnetic circuit to decode the absolute position of any moving magnet (e.g. rotary position from 0 to 360 Degrees or linear displacement, stroke).

MLX90364 reports a programmable ratiometric analog output signal compatible with any resistive potentiometer or programmable linear Hall sensor. Through programming, the MLX90364 provides also a digital PWM (Pulse Width Modulation) output characteristic.

MLX90364 Triaxis® Position Sensor Assembly enables the realization of position sensor modules for which a PCB is no longer needed: this yield to an increase of the electrical, mechanical and environmental robustness of the final application.

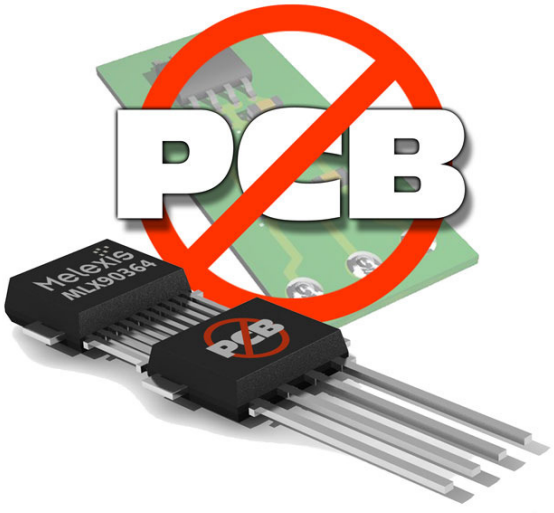


Figure 2 NoPCB – MLX90364 makes conventional PCB redundant

Table of Contents

3. Glossary of Terms – Abbreviations – Acronyms

- Gauss (G), Tesla (T): Units for the magnetic flux density – 1 mT = 10 G
- TC: Temperature Coefficient (in ppm/Deg.C.)
- NC: Not Connected
- PWM: Pulse Width Modulation
- %DC: Duty Cycle of the output signal i.e. TON /(TON + TOFF)
- ADC: Analog-to-Digital Converter
- DAC: Digital-to-Analog Converter
- LSB: Least Significant Bit
- MSB: Most Significant Bit
- DNL: Differential Non-Linearity
- INL: Integral Non-Linearity
- RISC: Reduced Instruction Set Computer
- ASP: Analog Signal Processing
- DSP: Digital Signal Processing
- CoRDiC: Coordinate Rotation Digital Computer (i.e. iterative rectangular-to-polar transform)
- EMC: Electro-Magnetic Compatibility
- ALS: Analog Low Speed
- AHS: Analog High Speed
- DLS: Digital Low Speed
- DHS: Digital High Speed
- DMP: Dual Mold Package

4. Pinout

Pin #	
1	VSS (Ground)
2	VDD
3	OUT
4	VSS (Ground)

5. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD} (overvoltage)	+ 24 V
Reverse Voltage Protection	– 12 V (breakdown at -14 V)
Positive Output Voltage	+ 18 V (breakdown at 24 V)
Output Current (I_{OUT})	+ 30 mA (in breakdown)
Reverse Output Voltage	– 0.3 V
Reverse Output Current	– 50 mA (in breakdown)
Operating Ambient Temperature Range, T_A	– 40°C … + 150°C
Storage Temperature Range, T_S	– 40°C … + 150°C
Magnetic Flux Density	± 1 T

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
These max ratings are guaranteed by mean of a qualification test where the device is supplied at 24V for 48h, the Output voltage is supplied at 18V for 48h and the device is reversely supplied at -12V for 1h.

6. Description

As described on the block diagram the three vector components of the magnetic flux density (B_X, B_Y and B_Z) applied to the IC are sensed through the sensor front-end. The respective Hall signals (V_X, V_Y and V_Z) are generated at the Hall plates and amplified.

The analog signal processing is based on a fully differential analog chain featuring the classic offset cancellation technique (Hall plate 2-Phases spinning and chopper-stabilized amplifier).

The conditioned analog signals are converted through an ADC (15 bits) and provided to a DSP block for further processing. The DSP stage is based on a 16 bit RISC micro-controller whose primary function is the extraction of the position from two (out of three) raw signals (after so-called front-end compensation steps) through the following function:

$$\alpha = \angle(V_1, k \cdot V_2)$$

where alpha is the magnetic angle <(B1, B2), V_1 = V_X or V_Y or V_Z , V_2 = V_X or V_Y or V_Z and k is a programmable factor to match the amplitude of V_1 and k V_2.

The DSP functionality is governed by the micro-code (firmware – F/W) of the micro-controller which is stored into the ROM (mask programmable). In addition to the magnetic angle extraction, the F/W controls the whole analog chain, the output transfer characteristic, the output protocol, the programming/calibration and also the self-diagnostic modes.

The magnetic angular information is intrinsically self-compensated vs. flux density variations. This feature allows therefore an improved thermal accuracy vs. position sensor based on conventional linear Hall sensors.

In addition to the improved thermal accuracy, the realized position sensor features excellent linearity performances taking into account typical manufacturing tolerances (e.g. relative placement between the Hall IC and the magnet).

Once the position (angular or linear stroke) information is computed, it is further conditioned (mapped) vs. the target transfer characteristic and it is provided at the output(s) as either a ratiometric analog output level through a 12 bit DAC followed by a buffer or a digital PWM output.

For instance, the analog output can be programmed for offset, gain and clamping to meet any rotary position sensor output transfer characteristic:

$$\begin{aligned} Vout(\alpha) &= ClampLo && \text{for } \alpha \le \alpha min \\ Vout(\alpha) &= Voffset + Gain \times \alpha && \text{for } \alpha min \le \alpha \le \alpha max \\ Vout(\alpha) &= ClampHi && \text{for } \alpha \ge \alpha max \end{aligned}$$

where Voffset, Gain, ClampLo and ClampHi are the main adjustable parameters for the end-user.

The linear part of the transfer curve can be adjusted through a multi-point calibration:

This back-end step consists into either

- up to 4 arbitrary points (5 segments + clamping levels) calibration or
- a Piece-Wise-Linear (PWL) output transfer characteristics - 17 equidistant points w/ programmable origin over 16 different angle ranges from 65 to 360 degrees.

The calibration parameters are stored in EEPROM featuring a Hamming Error Correction Coding (ECC).

The programming steps do not require any dedicated pins. The operation is done using the supply and output nodes of the IC. The programming of the MLX90364 is handled at both engineering lab and production line levels by the Melexis Programming Unit PTC-04 with the dedicated MLX90316 daughterboard and MLX90365 software tools (DLL – User Interface).

7. MLX90364 Electrical Specification

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Nominal Supply Voltage	VDD		4.5	5	5.5	V
Supply Current	Idd	Power saving Enabled, All modes For Outmode=1 Power saving Disabled, All modes For Outmode=1		 6 8	10(2) 10(2) 12 12	mA
Supply Current (Pwm mode) (3)	I_{peak}	Peak current in Pwm mode 7		30	40	mA
Isurge Current(4)	Isurge				20	mA
Power-On reset (rising)	HPOR_LH	Refer to internal voltage Vdig	2	2.25	2.5	V
Power-On reset Hysteresis	HPOR_Hyst		50		200	mV
Start-up Level (rising)	MT4V LH		3.8	4.0	4.2	V
Start-up Hysteresis	MT4V Hyst		50		200	mV
PTC Entry Level (rising)	MT7V_LH		5.8	6.2	6.6	V
PTC Entry Level Hysteresis	MT7V_Hyst		50		200	mV
Output Short Circuit Current	I_{short}	Vout = 0 V Vout = 5 V Vout = 18 V (T_A = 25°C)			15 15 18	mA mA mA
Output Load (Analog mode)	R_{L_ana}	Pull-down to Ground Pull-up to 5V	4.7(5) 4.7(5)	10 10	∞ ∞	kΩ kΩ
Output Load (Pwm mode)	R_{L_pwm}	Pull-down to Ground Pull-up to 5V	1 1	10 10	∞ ∞	kΩ kΩ
Analog Saturation Output Level	Vsat_lo	Pull-up load $R_L \geq 10$ kΩ to 5 V Pull-up load $R_L \geq 5$ kΩ to 18V		0.5 2	2 3	%VDD
	Vsat_hi	Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 10$ kΩ	95 97.5	97 98.5		%VDD
Digital Saturation Level Open drain Output (R_{L_PWM} to Vbat)	Vo_min	Pull-up load $R_{L\_PWM} \leq 1$ kΩ to 5V Pull-up load $R_{L\_PWM} \leq 1$ kΩ to 18V Pull-up load $R_{L\_PWM} \leq 5.6$ kΩ to 5V Pull-up load $R_{L\_PWM} \leq 5.6$ kΩ to 18V	98 90 96 73			%Vbat
Active Diagnostic Output Level (Digital saturation output level)	Diag_lo	Pull-up load $R_L \geq 10$ kΩ to 5 V Pull-up load $R_L \geq 5$ kΩ to 18V		0.5 2	2 3	%VDD
	Diag_hi	Pull-down load $R_L \geq 5$ kΩ Pull-down load $R_L \geq 10$ kΩ	95 97.5	97 98.5		%VDD

[2] To reach 10mA, the power saving optionshould be enabled. This option switches off and on internal blocks dynamically. It can be disabled in case of extreme emission requirements or if an analog output is required with a resistor on either supply or output line. .

[3] This current is due to the charge of output capacitors in PWM push-pull mode.

[4] The specified value is valid during early start-up time only; the current might dynamically exceed the specified value, shortly, during the Start-up phase.

[5] The minimum specified value is mandatory to reach passive diagnostic output levels. A minimum 1k load resistor can be used otherwise.

Passive Diagnostic Output Level (Broken Track Diagnostic) [6]	BVSSPD	Broken VSS & Pull-down load $R_L \geq 10\ k\Omega$	97.5			%VDD
	BVSSPU	Broken VSS & Pull-up load $R_L \geq 1k\Omega$	99.5	100		%VDD
	BVDDPD	Broken VDD & Pull-down load $R_L \geq 1k\Omega$		0	0.5	%VDD
	BVDDPU	Broken VDD & Pull-up load $R_L \geq 5k\Omega$			2	%VDD
Digital output Ron	Ron	Diag_Low Diag_Hi	15 120		30 300	Ohm
Clamped Output Level	Clamp_lo	Programmable	0		100	%VDD[7]
	Clamp_hi	Programmable	0		100	%VDD[7]

As an illustration of the previous table, the MLX90364 fits the typical classification of the output span described on the Figure 3.

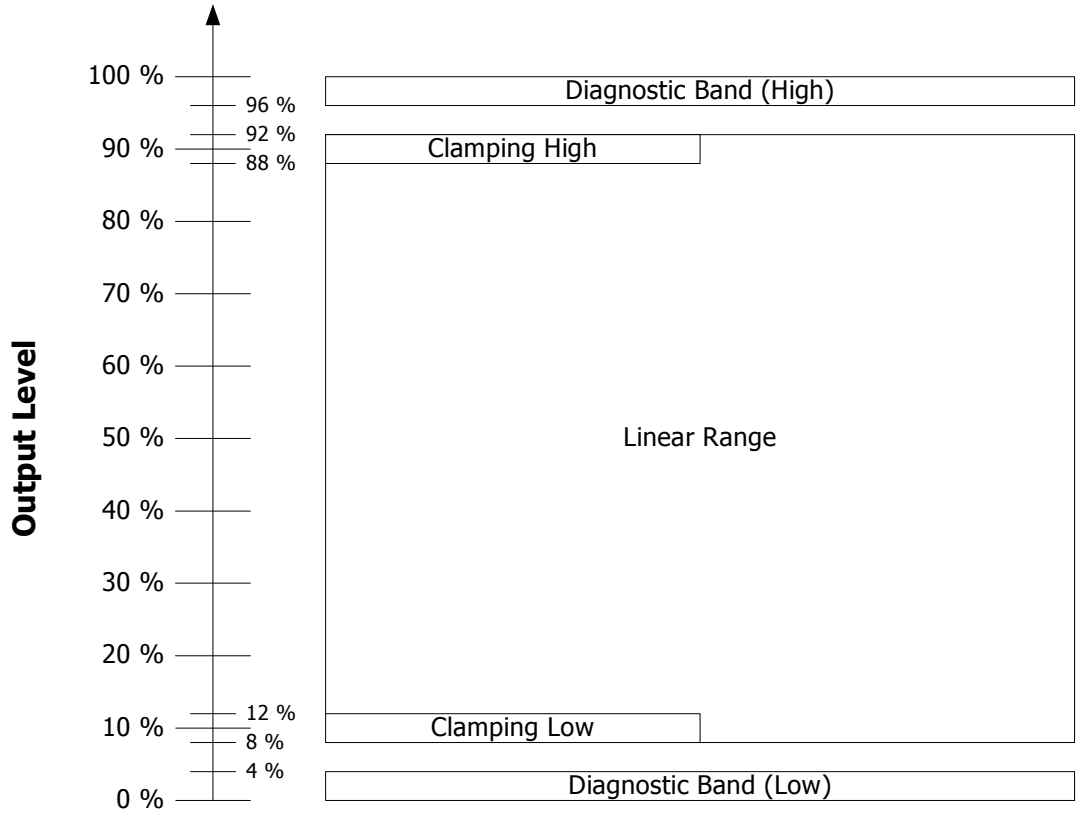


Figure 3 Example of Output Span Classification for typical application.

[6] For detailed information, see also section 16

[7] Clamping levels need to be considered vs the saturation of the output stage (see Vsat_lo and Vsat_hi)

8. MLX90364 Timing Specification

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Main Clock Frequency	Ck	All contributors included thermal drfit	12.6	13.3	14	MHz
Main Clock Frequency Thermal Drift	Δ^TCk				± 3%	Ck_{NOM}
Refresh Rate			275	290	305	µs
Step Response Time	Ts	Filter=0[8] Filter=1 Filter=2		657[9] 876 1095	896 1195 1494	µs
Watchdog	Twd		114.5	118	121.5	ms
Phase Shift	PS	Filter=0		0.16		Deg/Hz
Start-up Cycle	Tsu	Analog OUT Slew-rate excluded			5	ms
Analog OUT Slew-rate			25	37		V/ms

9. MLX90364 PWM Timing Specification

DC Operating Parameters at nominal supply voltage = VPU (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Digital Output Rise Time		LOW SIDE DRIVER – Mode 5 R_L = 1 kΩ PU PUSH-PULL – Mode 7 R_L = 1 kΩ PU		80 27	130 50	µs µs
Digital Output Fall Time		LOW SIDE DRIVER – Mode 5 R_L = 1 kΩ PU PUSH-PULL – Mode 7 R_L = 1 kΩ PU		27 27	50 50	µs µs
Start-up Cycle	Tsu	PWM OUT Slew-rate excluded				

[8] See section 15.6 for details concerning Filter parameter
[9] This represents a theoretical average response time

		100Hz 250Hz 1000Hz		11.8 5.8 5.8	13 7 7	ms

10. MLX90364 Accuracy Specification

10.1. Normal Magnetic range: 20 mT ≤ B < 70 mT

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ADC Resolution on the raw signals sine and cosine[10]	R_{ADC}			15		bits
Thermal Offset Drift #1[11] at the DSP input (excl. DAC and output stage)		T_A from -40 to 125degC T_A from -40 to 150degC	-60 -90		+60 +90	LSB_{15}
Thermal Offset Drift #2 (DAC and Output Stage)			-0.2		+0.2	%VDD
Thermal Drift of Sensitivity Mismatch[12]		XY axis XZ (YZ) axis	- 0.5 -1		+ 0.5 +1	% %
Magnetic Angle phase error		T_A = 25°C – XY axis T_A = 25°C – XZ axis T_A = 25°C – YZ axis	-0.3 -2 -2		0.3 2 2	Deg.
Thermal Drift of Magnetic Angle phase error		XY axis, XZ (YZ) axis		0.01		Deg.
XY – Intrinsic Linearity Error[13]	Le	T_A = 25°C – factory trim. "SMISM"	-1		1	Deg
XZ - Intrinsic Lin. Error[13]	Le	T_A = 25°C – "k" trimmed for XZ	-2.5	±1.25	2.5	Deg
YZ - Intrinsic Lin. Error[13]	Le	T_A = 25°C – "k" trimmed for YZ	-2.5	±1.25	2.5	Deg
Analog Output Resolution	R_{DAC}	12b DAC (Theoretical, Noise free) INL (before EOL calibration) DNL	 -4 0.05	0.025 1	 +4 3	%VDD/LSB_{12} LSB_{12} LSB_{12}
Output stage Noise		Clamped Output		0.05	0.075	%VDD
Noise pk-pk[14]		Filter 0, B1 or B2 > 40mT		0.10	0.2	Deg

[10] 16 bits corresponds to 15 bits + sign. Internal computation is performed using 16 bits.
[11] For instance, in case of a rotary position sensor application, Thermal Offset Drift #1 equal ± $60LSB_{15}$ yields to max. ± 0.3 Deg. angular error for the computed angular information (output of the DSP). This is only valid if k = 1.
[12] For instance, in case of a rotary position sensor application, Thermal Drift of Sensitivity Mismatch equal ± 0.5% yields to max. ± 0.15 Deg. angular error for the computed angular information (output of the DSP). See "MLX90364 Front-End Application Note" for more details.
[13] The Intrinsic Linearity Error refers to the IC itself (offset, sensitivity mismatch, orthogonality) taking into account an ideal rotating field for B_X and B_Y. Once associated to a practical magnetic construction and the associated mechanical and magnetic tolerances, the output linearity error increases. However, it can be improved with the multi-point end-user calibration. The intrinsic Linearity Error for Magnetic angle ∠XZ and ∠YZ can be reduced through the programming of the k factor.
[14] Noise pk-pk (peak-to-peak) is here intended as 6 times the Noise standard Deviation. The application diagram used is described in the recommended wiring. For detailed information, refer to section Filter in application mode (Section 15.6).

		Filter 2, B1 or B2 > 20mT		0.10	0.2	Deg
Ratiometry Error (Analog output only)		4.5V ≤ VDD ≤ 5.5V LT4V ≤ VDD ≤ MT7V	-0.05 -0.1		+0.05 +0.1	%VDD %VDD

10.2. Extended Range #1 : 15 mT ≤ B < 20 mT

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Offset on Raw Signals X,Y,Z	X0,Y0,Z0	T_A = 25 Deg.C.	-120		+120	bits
Thermal Offset Drift #1 at the DSP input (excl. DAC and output stage)		T_A from -40 to 125degC T_A from -40 to 150degC	-120 -180		+120 +180	LSB_{15}
Noise pk-pk		Filter 0			75	LSB_{15}

In case of the use of the MLX90364 in those extended ranges, Melexis recommends validating the headroom of the internal diagnostic and if necessary to disable the diagnostic mode related to the amplitude of the flux strength and/or amplification factor of the device.

10.3. Extended Range #2: 10 mT ≤ B < 15 mT

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Offset on Raw Signals X,Y,Z	X0,Y0,Z0	T_A = 25 Deg.C.	-180		+180	bits
Thermal Offset Drift #1 at the DSP input (excl. DAC and output stage)		T_A from -40 to 125degC T_A from -40 to 150degC	-180 -270		+180 +270	LSB_{15}
Noise pk-pk		Filter 0			112	LSB_{15}

In case of the use of the MLX90364 in those extended ranges, Melexis recommends to validate the headroom of the internal diagnostic and if necessary to disable the diagnostic mode related to the amplitude of the flux strength and/or amplification factor of the device.

11. MLX90364 PWM Accuracy Specification

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for T_A as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM Output Resolution	R_{PWM}	12 bits		0.025		%DC/LSB
PWM % DC Jitter[15]	J_{DC}	LOW SIDE DRIVER – Mode5 200Hz, RL = 1 kΩ PU PUSH-PULL – Mode7 200Hz, RL = 1 kΩ PU		 ±0.015 	 ±0.075 ±0.075	%DC
PWM Freq Jitter[15]	J_{PWM}	LOW SIDE DRIVER – Mode5 100-1000 Hz, R_L = 1 kΩ PU PUSH-PULL – Mode7 100-1000 Hz, R_L = 1 kΩ PU		 ±0.05 ±0.05	 ±0.2 ±0.2	Hz
PWM % DC thermal drift		LOW SIDE DRIVER – Mode5 100Hz, R_L = 1 kΩ PU 200Hz, RL = 1 kΩ PU PUSH-PULL – Mode7 100Hz, R_L = 1 kΩ PU 200Hz, RL = 1 kΩ PU		 0.02 0.02 0.02 0.02	 0.03 0.03 0.03 0.03	%DC

Parameter	Symbol	Test Conditions
PWM TON, Tperiod	T_{ON} T_{PWM}	 Trigger level = 50 % VPush-pull
Rise time Fall time		10% and 90% of amplitude
Jitter	J on J period	± 3 σ for 1000 successive acquisitions
Duty Cycle	% DC	T_{on} / T_{Period}

[15] Jitter is defined by ± 3 σ for 1000 successive acquisitions with clamped output.

12. MLX90364 Magnetic Specification

DC Operating Parameters at nominal supply voltage (unless otherwise specified) and for TA as specified by the Temperature suffix L.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Magnetic Flux Density	B_X, B_Y[16]				70[17]	mT
Magnetic Flux Density	B_Z				126	mT
Magnetic Field Norm	Norm	$\sqrt{[B_X^2 + B_Y^2 + (Bz/1.2)^2]}$	20[18]	40		mT
IMC Gain[19]	GainIMC		1.2	1.3	1.4	
Magnet Temperature Coefficient	TCm		-2400		0	ppm/°C

13. MLX90364 CPU & Memory Specification

The DSP is based on a 16 bit RISC µController. This CPU provides 2.5 Mips while running at 10 MHz.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ROM				10		kB
RAM				384		B
EEPROM				128		B

[16] The condition must be fulfilled for at least one field BX,or BY.
[17] Above 70 mT, the IMC starts saturating yielding to an increase of the linearity error.
[18] Below 20 mT, the performances slightly degrade due to a reduction of the signal-to-noise ratio, signal-to-offset ratio.
[19] This is the magnetic gain linked to the Integrated Magneto Concentrator structure. It applies to BX and BY and not to BZ. This is the overall variation.

14. MLX90364 End-User Programmable Items

Parameter	Comments	Standard	# bit
OUT mode	Define the output stage mode	1	3
DIAG mode	Diagnostic mode	7	3
DIAG Level	Diagnostic Level	0	1
MAPXYZ	Mapping fields for output angle	0	2
CLAMP_HIGH	Clamping High (50%)	50%	16
CLAMP_LOW	Clamping Low (50%)	50%	16
FILTER	Filter mode selection	0	2
SMISM	Sensitivity mismatch factor X,Y	MLX	15
k	Sensitivity mismatch factor X (Y) , Z	MLX	15
SEL_k	Affected signal component by k: B1 or B2 (in combination of MAPXYZ)	0	1
GAINMIN	Low threshold for virtual gain	0h	8
GAINMAX	High threshold for virtual gain	28h	8
GAINSATURATION	Gain Saturates on GAINMIX and GAINMAX	0h	1
FIELDTHRESH_Low	Field limit under which a fault is reported	10mT	8
FIELDTHRESH_High	Field limit above which a fault is reported	FFh	8
PWM	PWM function	0h	1
PWMPOL	PWM polarity	0h	1
PWMT	PWM Frequency (trimmed at 200Hz)	MLX	8
DC_FAULT	PWM Duty Cycle if Fault	1h	8
DC_FTL	PWM Duty Cycle if Field Strength Too Low	1h	8
DC_WEAK	PWM Duty Cycle if Weak Magnet	1h	8
WEAKMAGTHRESH	Weak Magnet threshold Byte (1lsb = 1mT)	0h	8
DP	Discontinuity point	0h	15
CW	Clock Wise	0h	1
FHYST	Hysteresis filter	0h	8
MELEXISID1	Melexis identification reference	MLX	16
MELEXISID2	Melexis identification reference	MLX	16
MELEXISID3	Melexis identification reference	MLX	16
4POINTS	Selection of correction method 4 or 16 pts	1h	1
LNR_S0	4pts – Initial Slope	0 %/deg	16
LNR_A_X	4pts – AX Coordinate	0 deg	16
LNR_A_Y	4pts – AY Coordinate	10 %	16
LNR_A_S	4pts – AS Coordinate	0.22%/deg	16
LNR_B_X	4pts – BX Coordinate	360 deg	16
LNR_B_Y	4pts – BY Coordinate	100%	16
LNR_B_S	4pts – BS Coordinate	0 %/deg	16
LNR_C_X	4pts – CX Coordinate	360 deg	16
LNR_C_Y	4pts – CY Coordinate	100%	16
LNR_C_S	4pts – CS Coordinate	0 %/deg	16
LNR_D_X	4pts – DX Coordinate	360 deg	16
LNR_D_Y	4pts – DY Coordinate	100%	16
LNR_D_S	4pts – DS Coordinate	0 %/deg	16
W	17pts – Output angle range	0h	4
CUSTOMERID1	Cust. id reference	Bin1	16

CUSTOMERID2	Cust. id reference	203h (ADB) 204h (ADD)	16
CUSTOMERID3	Cust. id reference	Sense info	16
LNR_Yn	17pts – Y-coordinate point n (n = 2,1,2 …16)	N/A	16
DIAG Settings	16 Bit Diagnostics enablling	FDFFh	16
CRC_DISABLE	Enable EEPROM CRC check (3131h= disable)	0h	16
MEMLOCK (ADD version)	Write-protects USER/MLX EEPROM param.	0h	2

15. Description of End-User Programmable Items

15.1. Output Mode

The MLX90364 output type is defined by the Output Mode parameter.

Output mode[2:0]	Type	Descriptions	Comments
0	Disable	Output HiZ	Not recommended
1	Analog	Analog Rail-to-Rail	Analog
5	Digital	open drain NMOS	PWM
6	Digital	open drain PMOS	PWM
7	Digital	Push-Pull	PWM

15.1.1. Analog Output Mode

The Analog Output Mode is a rail-to-rail and ratiometric output with a push-pull output stage configuration allows the use of a pull-up or pull-down resistor.

15.1.2. PWM Output Mode

If PWM output mode is selected, the output signal is a digital signal with Pulse Width Modulation (PWM). The PWM polarity is selected by the PWMPOL parameter:

- PWMPOL = 1 for a low level at 100%
- PWMPOL = 0 for a high level at 100%

The PWM frequency is selected by the PWMT parameter. The following table provides typical code for different target PWM frequency and for both low and high speed modes.

PWW F (Hz)	PWMT (LSB) @13.3MHz	PWM res. (us)	PWM res. (%)	PWM res. (bit)
100	44333	0.240	0.0024	15.0
250	17733	0.240	0.006	14.0
500	8866	0.240	0.012	13.0

Notes:

- A more accurate trimming can be performed to take into account initial tolerance of the main clock.
- The PWM frequency is subjected to the same tolerances as the main clock (see $\Delta^{T}Ck$).

15.2. Output Transfer Characteristic

There are 2 different possibilities to define the transfer function (LNR):

- With 4 arbitrary points (defined on X and Y coordinates) and 5 slopes
- With 17 equidistant points for which only the Y coordinates are defined.

Parameter	LNR type	Value	Unit
CLOCKWISE	**Both**	**0 → CounterClockWise 1 → ClockWise**	**LSB**
DP	Both	0 … 359.9999	deg
LNR_A_X LNR_B_X LNR_C_X LNR_D_X	Only 4 pts	0 … 359.9999	deg
LNR_A_Y LNR_B_Y LNR_C_Y LNR_D_Y	Only 4 pts	0 … 100	%
LNR_S0 LNR_A_S LNR_B_S	Only 4 pts	-17 ... 0 … 17	%/deg
LNR_C_S LNR_D_S	Only 4 pts	-17 … 0 … 17	%/deg
LNR_Y0 LNR_Y1 … LNR_Y16	Only 16 pts	-50 … + 150	%
W	Only 16 pts	65.5 … 360	Deg
CLAMP_LOW	Both	0 … 100	%
CLAMP_HIGH	Both	0 … 100	%

15.2.1. Enable scaling Parameter (only for LNR type 4 pts)

This parameter enables to scale LNR_x_Y from -50% - 150% according to the following formula

$$(\text{Scaled Out})\%V_{DD} = 2 \times \text{Out}\%V_{DD} - 50\%$$

15.2.2. CLOCKWISE Parameter

The CLOCKWISE parameter defines the magnet rotation direction.

- CCW is defined by the 1-2-3-4 pin order direction for the Dual Mold Package.
- CW is defined by the reverse direction: 4-3-2-1 pin order direction for the Dual Mold Package.

Refer to the drawing in the sensitive spot positioning sections (Section 20.5)

15.2.3. Discontinuity Point (or Zero Degree Point)

The Discontinuity Point defines the 0° point on the circle. The discontinuity point places the origin at any location of the trigonometric circle. The DP is used as reference for all the angular measurements.

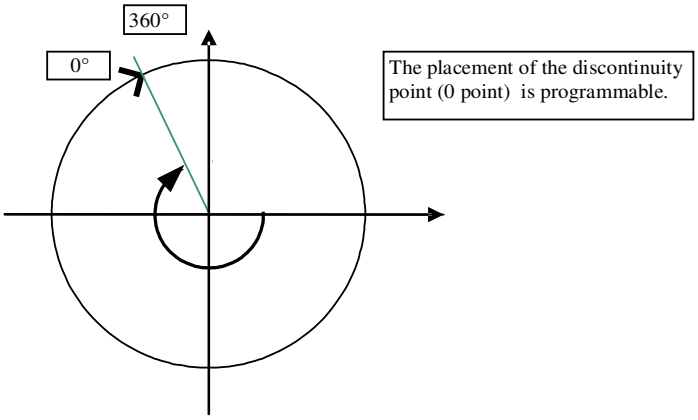


Figure 4: Discontinuity Point Positioning

15.2.4. 4-Pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90364 transfer function from the digital angle value to the output voltage is described by the drawing below. Six segments can be programmed but the clamping levels are necessarily flat.

Two, three, or even six calibration points are then available, reducing the overall non-linearity of the IC by almost an order of magnitude each time. Three or six calibration point will be preferred by customers looking for excellent non-linearity figures. Two-point calibrations will be preferred by customers looking for a cheaper calibration set-up and shorter calibration time.

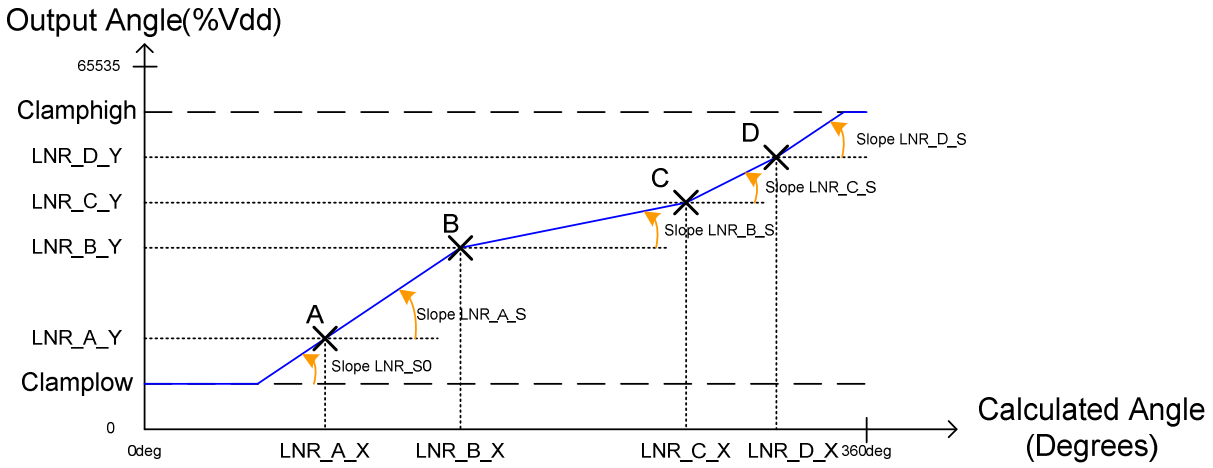


Figure 5: 4 points linearization

15.2.5. 17-Pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90364 transfer function from the digital angle value to the output voltage is described by the drawing below. In the 16-Pts mode, the output transfer characteristic is Piece-Wise-Linear (PWL).

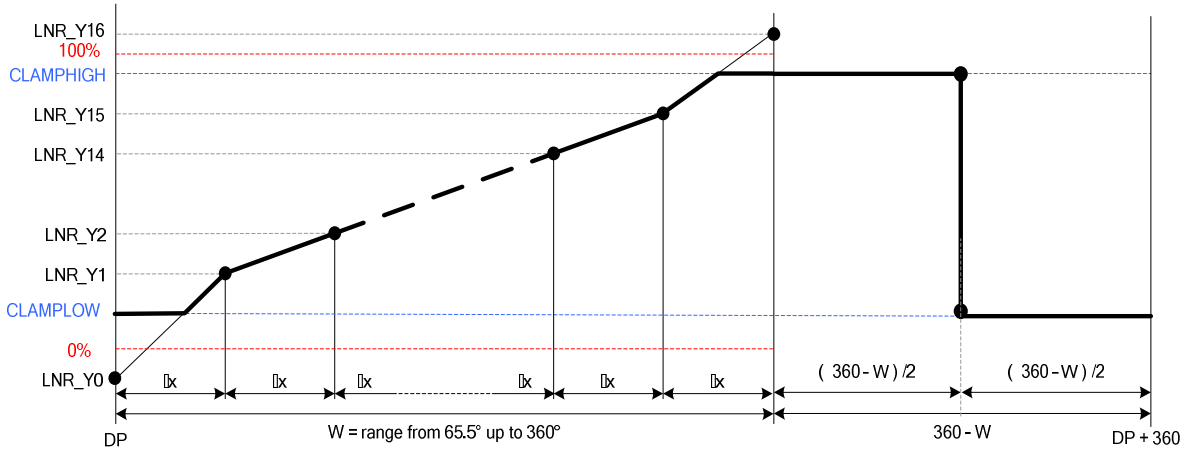


Figure 6: Input range from 65.5° up to 360°

All the Y-coordinates can be programmed from -50% up to +150% to allow clamping in the middle of one segment (like on the figure), but the output value is limited to CLAMPLOW and CLAMPHIGH values.

Between two consecutive points, the output characteristic is interpolated.

The parameter W determines the input range on which the 17 points (16 segments) are uniformly spread:

W	Range	Δx
0 (0000b)	360.0deg	22.5deg
1	320.0deg	20.0deg
2	288.0deg	18.0deg
3	261.8deg	16.4deg
4	240.0deg	15.0deg
5	221.5deg	13.8deg
6	205.7deg	12.9deg
7	192.0deg	12.0deg

W	Range	Δx
8	180.0deg	11.3deg
9	144.0deg	9.0deg
10	120.0deg	7.5deg
11	102.9deg	6.4deg
12	90.0deg	5.6deg
13	80.0deg	5.0deg
14	72.0deg	4.5deg
15 (1111b)	65.5deg	4.1deg

Outside of the selected range, the output will remain in clamping levels.

15.2.6. CLAMPING Parameters

The clamping levels are two independent values to limit the output voltage range. The CLAMPLOW

parameter adjusts the minimum output voltage level. The CLAMPHIGH parameter sets the maximum output voltage level. Both parameters have 16 bits of adjustment and are available for both LNR modes. In analog mode, the resolution will be limited by the D/A converter (12 bits) to 0.024%V_{DD}. In PWM mode, the resolution will be 0.024%DC.

15.3. Identification

Parameter	Value
MELEXISID1 MELEXISID2 MELEXISID3	0 … 65535 0 … 65535 0 … 65535
CUSTOMERID1 CUSTOMERID2 CUSTOMERID3	0 … 65535 0 … 65535 0 … 65535

Identification number: 48 bits (3 words) freely useable by Customer for traceability purpose.

15.4. Lock

The MEMLOCK write protects all the EEPROM parameters set by the Melexis and user. Once the lock is enabled, it is not possible to change the EEPROM values anymore.
Note that the Memlock bits should be set by the solver function “MemLock" and is only applicable for the ADD-version.

15.5. Sensor Front-End

Parameter	Value
MAPXYZ	0 .. 3
SMISM	0 .. 32768
k	0 .. 32768
SEL_k	0 or 1
GAINMIN GAINMAX GAINSATURATION	0 … 41 0 … 41 0.. 1

15.5.1. MAPXYZ

The MAPXYZ parameter defines which fields are used to calculate the angle. The different possibilities are described in the tables below.
This 2 bits value selects the first (B1) and second (B2) field components according the table below.

MAPXYZ	B1	B2	Angular
0 – 00b	X	Y	XY mode

1 – 01b	Zx	X	XZx mode
2 – 10b	Y	Zx	YZx mode
3 – 11b	Y	Zy	YZy mode

Note: MAPXYZ = 3 is not recommended.

15.5.2. SMISM, k and SEL_k Parameters

(i) SMISM

When the mapping (B1=X, B2=Y) is selected, SMSIM defines the sensitivity mismatch factor that is applied on B1, B2; When another B1, B2 mapping is selected, this parameter is "don't care".
This parameter is trimmed at factory; Melexis strongly recommends TO NOT overwrite it for optimal performances.

(ii) k

When the mapping (B1=X, B2=Y) is **NOT** selected, k defines the sensitivity mismatch factor that is applied on B1or B2 (according to parameter SEL_k – see below). If the mapping (B1=X, B2=Y) is selected, this parameter is unused.
This parameter is optimized for MAPXYZ=01 (B1=Z, B2=X) by factory trimming. If another mapping value is selected, Melexis recommends to fine tune K in order to reach a smaller linearity error (Le, see section 10).

(iii) SEL_k

When the mapping (B1=X, B2=Y) is **NOT** selected, SEL_k defines the component on which the sensitivity mismatch factor k (see above): SEL_k = 0 means B1→ k · B1 and SEL_k = 1 means B2 → k · B2.

15.5.3. GAINMIN and GAINMAX Parameters

GAINMIN and GAINMAX parameters define the boundaries of the virtual gain code. Outside of these thresholds, the "GAIN out of Spec" fault is set.
If GAINSATURATION parameter is set, the virtual gain code is saturated at GAINMIN and GAINMAX, and no Diagnostic fault is set since the saturations applies before diagnostic check.

15.6. Filter

Parameter	Value
FILTER	0 … 2
FHYST	0 … 255

The MLX90364 includes 2 types of filters:

- Hysteresis Filter: programmable by the FHYST parameter
- Low Pass FIR Filters controlled with the FILTER parameter

15.6.1. Hysteresis Filter

The FHYST parameter is a hysteresis filter. The output value of the IC is not updated when the digital step is smaller than the programmed FHYST parameter value. The output value is modified when the

increment is bigger than the hysteresis. The hysteresis filter reduces therefore the resolution to a level compatible with the internal noise of the IC. The hysteresis must be programmed to a value close to the noise level. (1 lsb = +/- 0.012%)

15.6.2. FIR Filters

The MLX90364 features 2 FIR filter modes controlled with Filter = 1…2. Filter = 0 corresponds to no filtering. The transfer function is described below:

$$y_n = \frac{1}{\sum_{i=0}^{j} a_i} \sum_{i=0}^{j} a_i x_{n-i}$$

The filters characteristics are given in the following table:

Filter No	0	1	2
j	0	1	3
Type	Disable	Finite Impulse Response	
Coefficients a_i	1	11	1111
Title	No filter	ExtraLight	Light
99% Response Time	1	2	4
Efficiency RMS (dB)	0	3.0	6.0

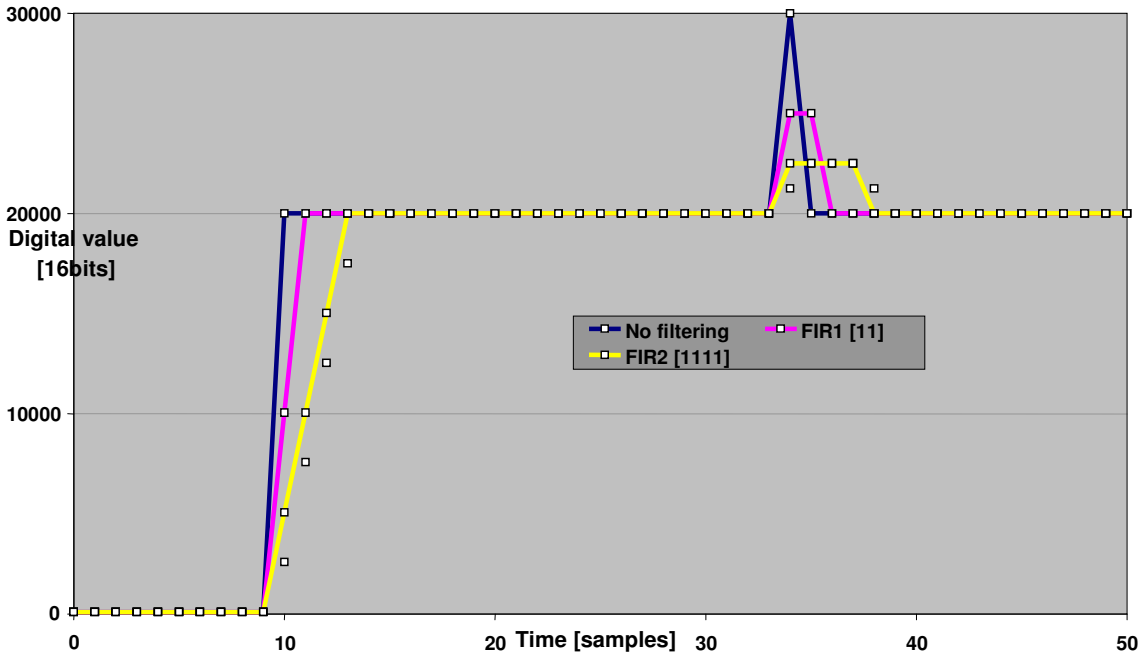


Figure 7: Step and impulse response of the different filters

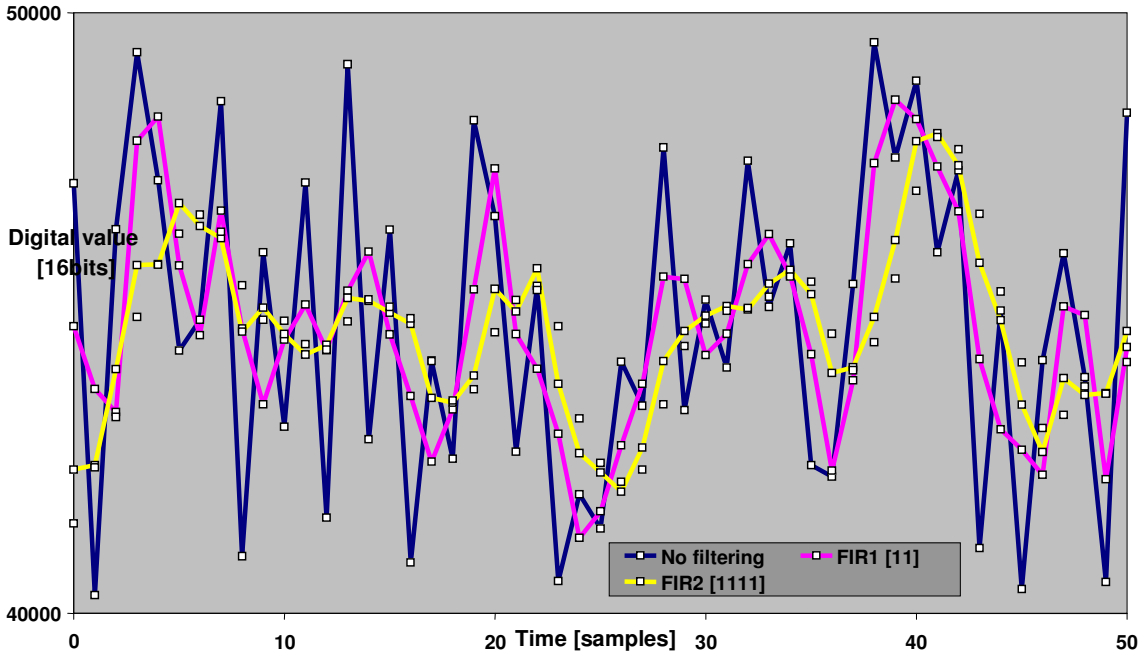


Figure 8: Noise response of the different filter

15.7. Programmable Diagnostic Settings

15.7.1. DIAG mode

Defines the Output Stage mode in case of Diag.

DIAG mode [2:0]	Type	Descriptions	Comments
0	Disable	Output HiZ	Not recommended
5	Digital	open drain NMOS	
6	Digital	open drain PMOS	
7	Digital	Push-Pull	

15.7.2. DIAG Level

Determines the reporting level (diagnostic low, diagnostic high) during start-up (both analog and PWM mode), or during a fault reporting (Only in Analog mode).

In PWM mode, the fault reporting level shall in principle be 0 when the leading edge is a rising edge, (resp. 1 for a falling edge) in order to detect the first cycle after start-up. MLX recommends then DIAG Level = PWMPOL.

15.7.3. Field Strength Diagnostic

(i) FIELDTHRESHLOW
Defines the field strength limit under which a fault is reported.
The run-time field strength estimation (FieldStrength) is compared to 2^8 * FIELDTHRESHLOW.
The sensitivity of FIELDTHRESHLOW is typically 1mT/LSB. By default it is programmed to 10mT