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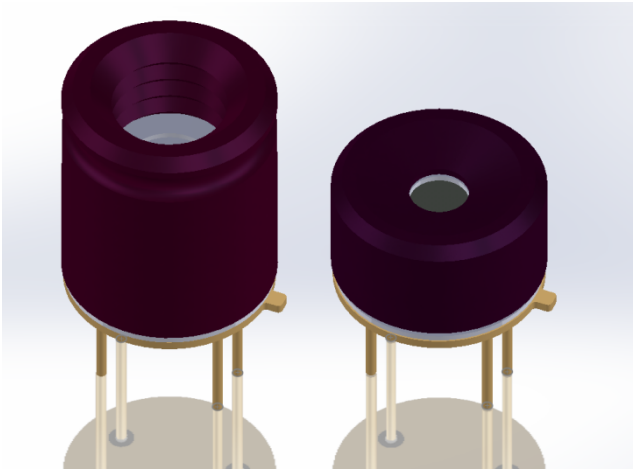
MLX90640 32x24 IR array

Datasheet

1. Features and Benefits

- Small size, low cost 32x24 pixels IR array
- Easy to integrate
- Industry standard four lead TO39 package
- Factory calibrated
- Noise Equivalent Temperature Difference (NETD) 0.1K RMS @1Hz refresh rate
- I^2C compatible digital interface
- Programmable refresh rate 0.5Hz…64Hz
- 3.3V supply voltage
- Current consumption less than 23mA
- 2 FOV options – 55°x35° and 110°x75°
- Operating temperature -40°C ÷ 85°C
- Target temperature -40°C ÷ 300°C
- Complies with RoHS regulations



2. Application Examples

- High precision non-contact temperature measurements
- Intrusion / Movement detection
- Presence detection / Person localization
- Temperature sensing element for intelligent building air conditioning
- Thermal Comfort sensor in automotive Air Conditioning control system
- Microwave ovens
- Industrial temperature control of moving parts
- Visual IR thermometers
- Driver software for MCU available at: https://github.com/melexis/mlx90640-library.git

3. Description

The MLX90640 is a fully calibrated 32x24 pixels thermal IR array in an industry standard 4-lead TO39 package with digital interface.

The MLX90640 contains 768 FIR pixels. An ambient sensor is integrated to measure the ambient temperature of the chip and supply sensor to measure the VDD. The outputs of all sensors IR, Ta and VDD are stored in internal RAM and are accessible through I^2C.

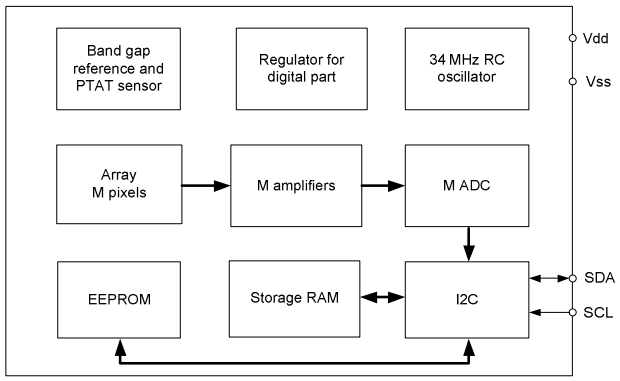


Figure 1 Block diagram

Contents

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4. Ordering Information

Product	Temperature	Package	Option Code	Custom Configuration	Packing Form	Definition
MLX90640	E	SF	BAA	000	TU	32x24 IR array
MLX90640	E	SF	BAB	000	TU	32x24 IR array

Legend:

Temperature Code:	**E: -40°C to 85°C**
Package Code:	"SF" for TO39 package
Option Code:	xAx – TGC is disabled and may not be changed
Option Code:	xxA – FOV = 110°x75° xxB – FOV = 55°x35°
Custom configuration	000 – standard product
Packing Form:	"TU" - Tubes
Ordering Example:	"MLX90640ESF-BAA-000-TU"

Table 1 Ordering information

5. Glossary of Terms

TC	**T**emperature **C**oefficient (in ppm/°C)
POR	**P**ower **O**n **R**eset
IR	**I**nfra-**R**ed
Ta	**A**mbient **T**emperature – the temperature of the TO39 package
IR data	**I**nfrared **d**ata (raw data from ADC proportional to IR energy received by the sensor)
ADC	**A**nalog To **D**igital **C**onverter
TGC	**T**emperature **G**radient **C**oefficient
FOV	**F**ield **O**f **V**iew
nFOV	**F**ield **O**f **V**iew of the N-th pixel
I^2C	**I**nter-**I**ntegrated **C**ircuit communication protocol
SDA	**S**erial **Da**ta
SCL	**S**erial **Cl**ock
LSB	**L**east **S**ignificant **B**it
MSB	**M**ost **S**ignificant **B**it
Fps	**F**rames **p**er **S**econd – data refresh rate
MD	**M**aster **D**evice
SD	**S**lave **D**evice
ASP	**A**nalog **S**ignal **P**rocessing
DSP	**D**igital **S**ignal **P**rocessing
ESD	**E**lectro **S**tatic **D**ischarge
EMC	**E**lectro **M**agnetic **C**ompatibility
CP	**C**ompensation **P**ixel
NC	**N**ot **C**onnected
NA	**N**ot **A**pplicable
TBD	**T**o **B**e **D**efined

Table 2 Glosarry of terms

6. Pin Definitions and Descriptions

Pin #	Name	Description
1	SDA	I^2C serial data (input / output)
2	VDD	Positive supply
3	GND	Negative supply (Ground)
4	SCL	I^2C serial clock (input only)

Table 3 Pin definition

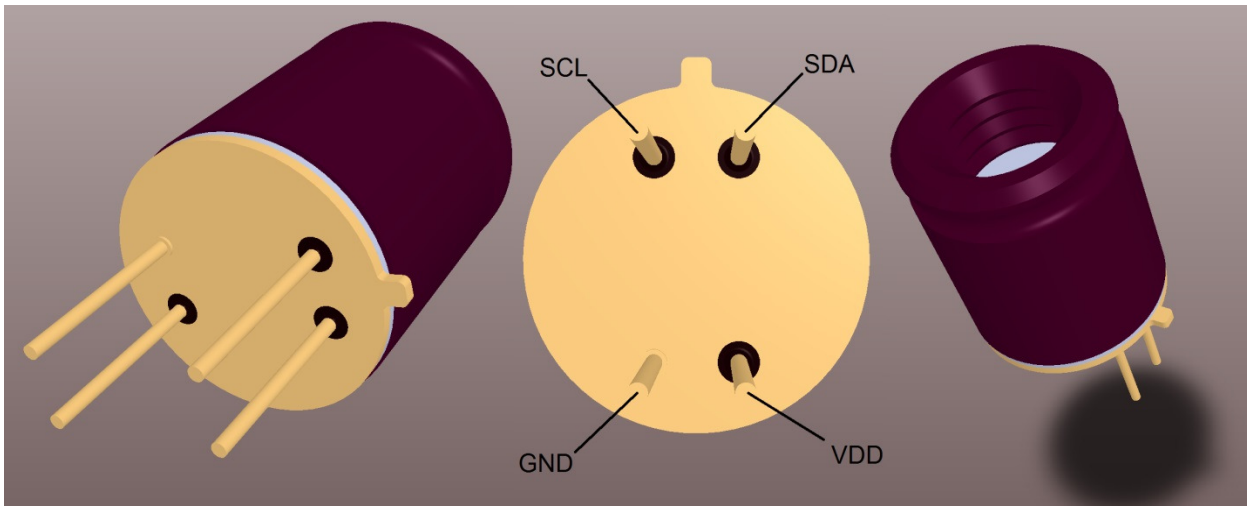


Figure 2 MLX90640 Overview and pin description

7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage (over voltage)	V_{DD}			5	V	
Supply Voltage (operating max voltage)	V_{DD}			3.6		
Reverse Voltage (each pin)				-0.3	V	
Operating Temperature	T_{AMB}	-40		+85	°C	
Storage Temperature	T_{ST}	-40		+125	°C	Not in plastic tubes
ESD sensitivity (AEC Q100 002)		4			kV	
SDA DC sink current				40	mA	

Table 4 Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

8. General Electrical Specifications

Electrical Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}	15	20	25	mA	
POR level up analog	V_{POR_UP}	2.2		2.6	V	VDD rising
POR level down analog	V_{POR_DOWN}			2.55	V	VDD falling
POR hysteresis	V_{POR_hys}		50		mV	
Default I^2C address		0x01	0x33	0xFF		
Input high voltage (SDA, SCL)	V_{IH}	0.7*V_{DD}			V	Over Ta and V_{DD}
Input low voltage (SDA, SCL)	V_{LOW}			0.3*V_{DD}	V	Over Ta and V_{DD}
SDA output low voltage	V_{OL}			0.4	V	Over Ta and V_{DD} I_{SINK}=3mA
SDA leakage	I_{SDA_leak}			± 10	µA	V_{SDA}=3.6V, Ta=85°C
SCL leakage	I_{SCL_leak}			± 10	µA	V_{SCL}=3.6V, Ta=85°C
SDA capacitance	C_{SDA}			10	pF	
SCL capacitance	C_{SCL}			10	pF	
Acknowledge setup time	$T_{SUAC(MD)}$			0.45	µs	
Acknowledge hold time	$T_{DUAC(MD)}$			0.45	µs	
Acknowledge setup time	$T_{SUAC(SD)}$			0.45	µs	
Acknowledge hold time	$T_{DUAC(SD)}$			0.45	µs	
I^2C clock frequency	F_{I2C}		0.4	1	MHz	
EEPROM erase/write cycles				10	times	
Write cell time	T_{WRITE}	5			ms	

Table 5 Electrical specification

***NOTE**: For best performance it is recommended to keep the supply voltage as accurate and stable as possible to 3.3V ± 0.1V*

***NOTE 2**: When a data in EEPROM cell to be changed an erase (write 0x0000) must be done prior to writing the new value. After each write at least 5ms delay is needed in order to writing process to take place.*

***NOTE 3**: Slave address 0x00 must be avoided.*

9. False pixel correction

The imager can have up to 4 defective pixels, with either no output or out of specification temperature reading. These pixels are identified in the EEPROM table of the sensor and can be read out through the I^2C. The defective pixel result can be replaced by an interpolation of its neighboring pixels.

10. Detailed General Description

10.1. Pixel position

The array consists of 768 IR sensors (also called pixels). Each pixel is identified with its row and column position as Pix(*i*,*j*) where ***i*** is its row number (from 1 to 24) and ***j*** is its column number (from 1 to 32)

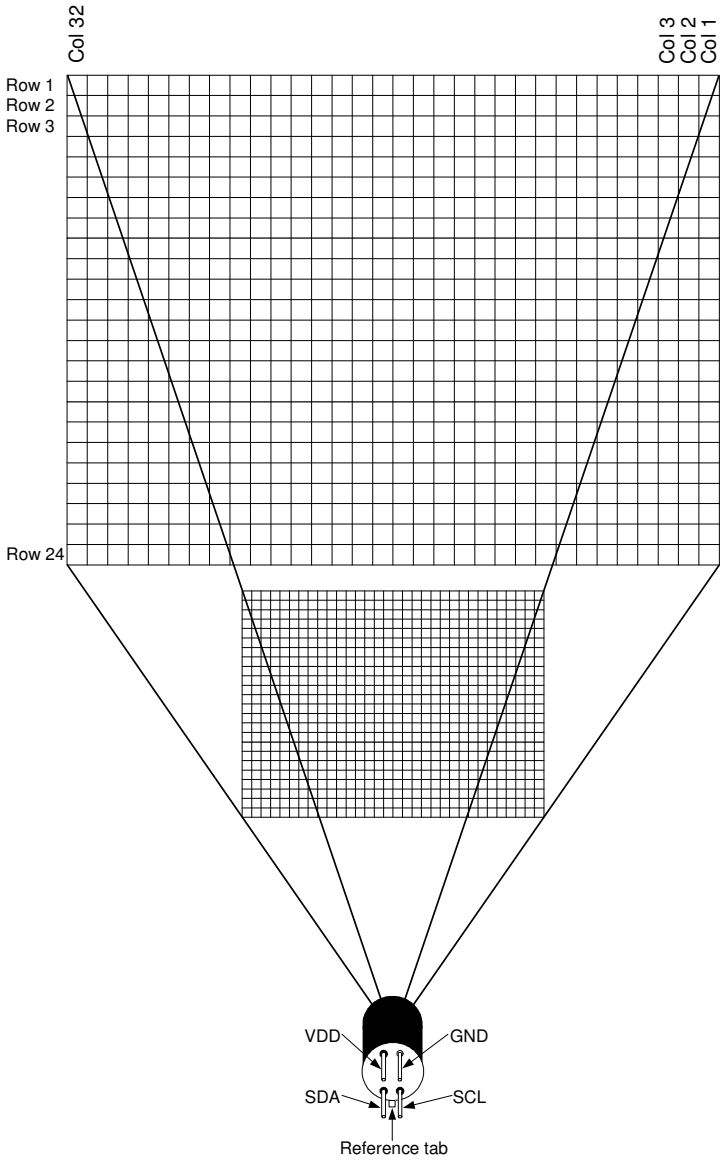


Figure 3 Pixel in the whole FOV

10.2. Communication protocol

The device use I²C protocol with support of FM+ mode (up to 1MHz clock frequency) and can be only slave on the bus.
The SDA and SCL ports are 5V tolerant and the sensor can be directly connected to a 5V I²C network.
The slave address is programmable and can have up to 127 different slave addresses.

10.2.1. Low level

10.2.1.1. Start / Stop conditions

Each communication session is initiated by a START condition and ends with a STOP condition. A START condition is initiated by a HIGH to LOW transition of the SDA while a STOP is generated by a LOW to HIGH transition. Both changes must be done while the SCL is HIGH.

10.2.1.2. Device addressing

The master is addressing the slave device by sending a 7-bit slave address after the START condition. The first seven bits are dedicated for the address and the 8th is Read/Write (R/W) bit. This bit indicates the direction of the transfer:

- Read (HIGH) means that the master will read the data from the slave
- Write (LOW) means that the master will send data to the slave

10.2.1.3. Acknowledge

During the 9th clock following every byte transfer the transmitter releases the SDA line. The receiver acknowledges (ACK) receiving the byte by pulling SDA line to low or does not acknowledge (NoACK) by letting the SDA 'HIGH'.

10.2.1.4. I²C command format

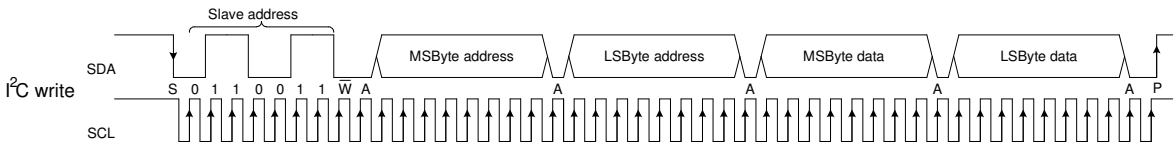


Figure 4 I²C write command format (default SA=0x33 is used)

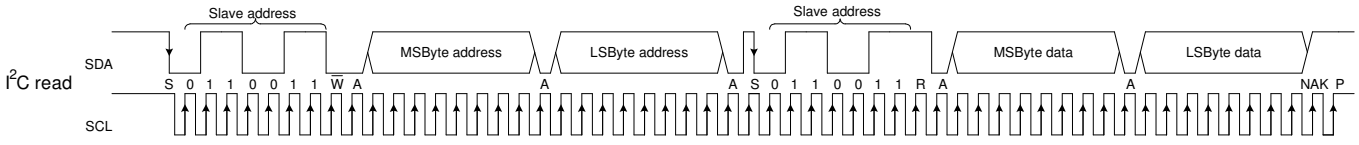


Figure 5 I²C read command format (default SA=0x33 is used)

10.3. Measurement mode

In this mode the measurements are constantly running. Depending on the selected frame rate Fps in the control register, the data for IR pixels and Ta will be updated in the RAM each $\frac{1}{F_{ps}}$ second. In this mode the external microcontroller has full access to the internal registers and memories of the device.

10.4. Refresh rate

The refresh rate is configured by "Control register 1" (0x800D) i.e. if "Refresh rate control" = 011 → 4Hz this would mean that each 250ms a new subpage data is available in the RAM.

NOTE: It is possible to program the desired refresh rate into device EEPROM eliminating the necessity to reconfigure the device every time it is powered on. The corresponding EEPROM cell is at address 0x240C (see Table 8)

Which subpage is updated is indicated by the "Last measured subpage" field.

It is important to read both subpages as the necessary information for the Ta calculations is only available by combining the data from both subpages i.e. the Ta is refreshed with an update speed twice as low as the one set in "Refresh rate control".

When a complete new data set (subpage) is available, a dedicated bit is set to indicate this – bit 3 "New data available in RAM" in "Status register" (0x8000). It is up to the customer to reset the bit once the data has been read.

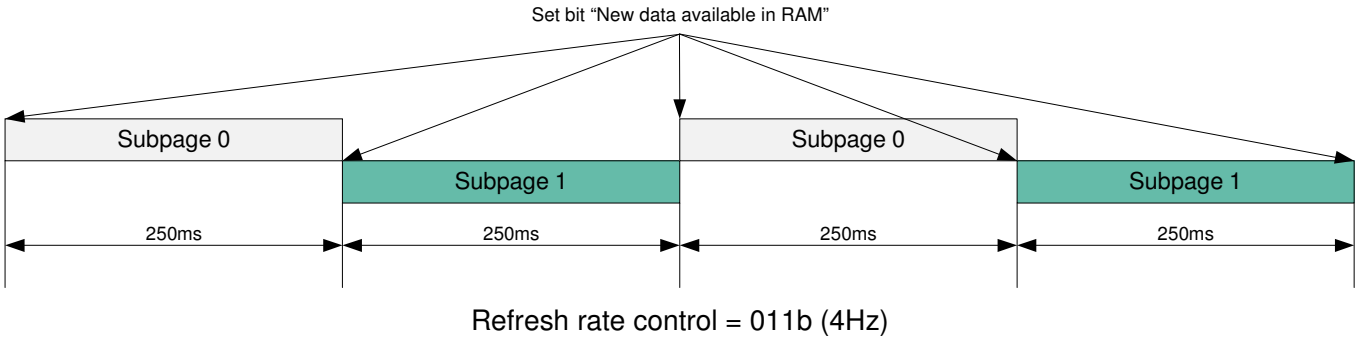


Figure 6 Refresh rate timing

10.5. Measurement flow

Following measurement flow is recommended:

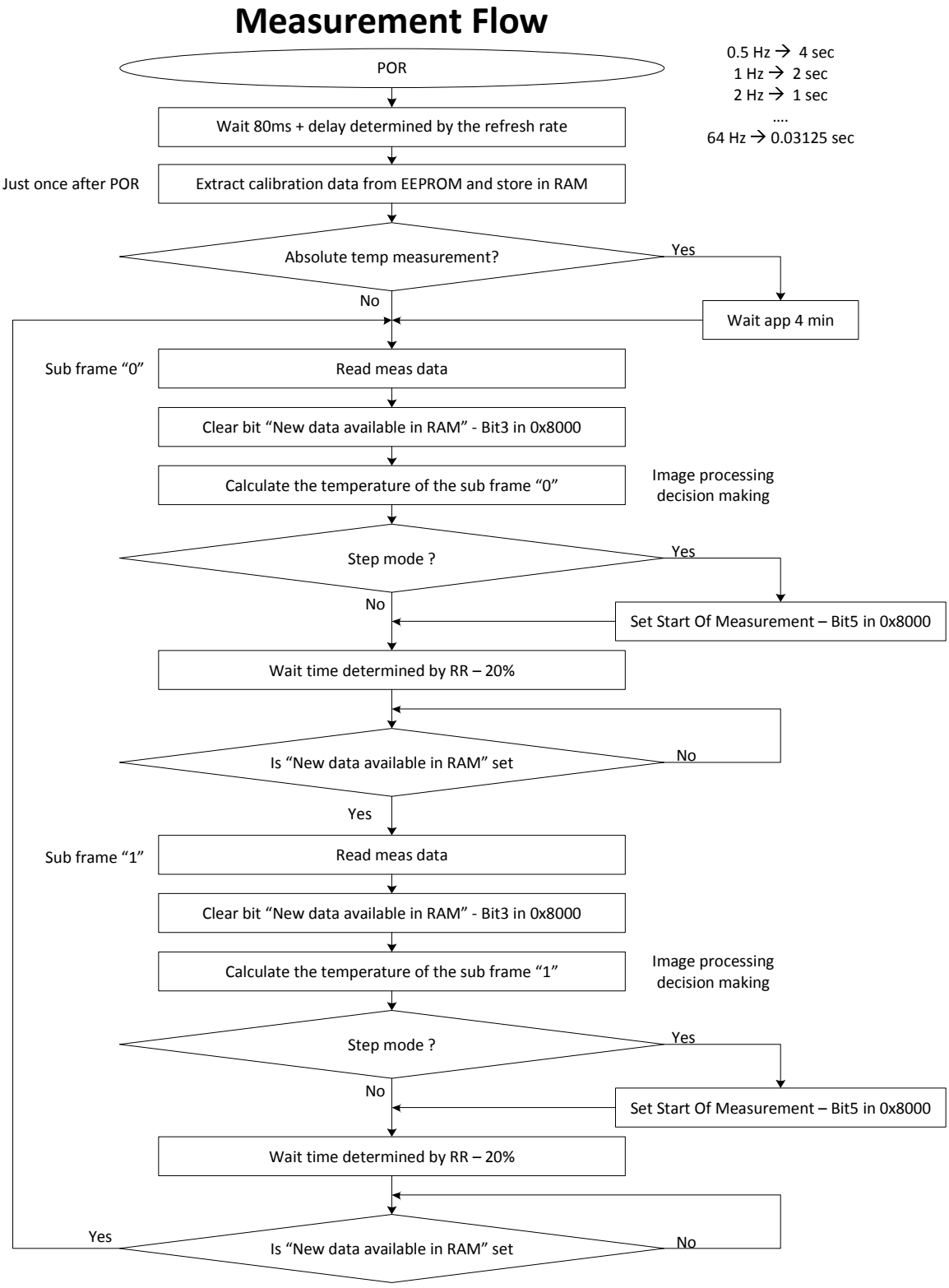


Figure 7 Recommended measurement flow

10.6. Reading patterns

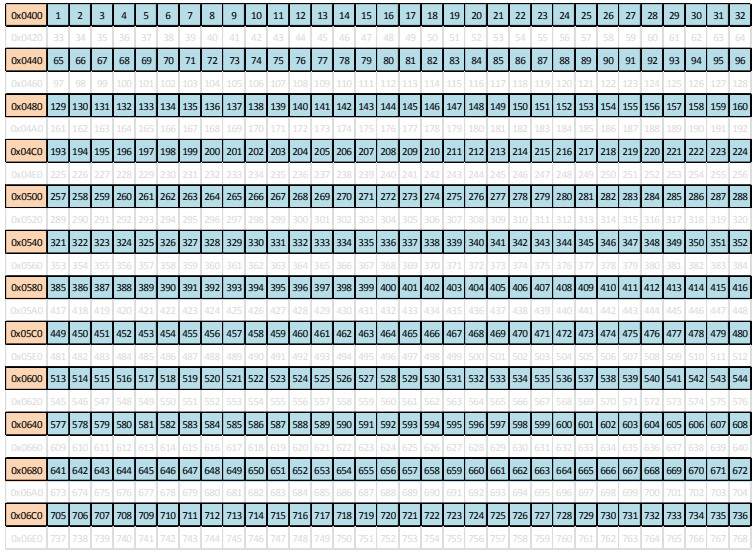
The array frame is divided in two subpages and depending of bit 12 in “Control register 1” (0x800D) – “Reading pattern” there are two modes of the pixel arrangement:

- Chess pattern mode (factory default)
- TV interleave mode

NOTE1: As a standard the MLX90640 is calibrated in Chess pattern mode, this results in better fixed pattern noise behaviour of the sensor when in chess pattern mode. For best results Melexis advices to use chess pattern mode.

NOTE2: Please make sure a proper configuration of the subpage control bit is done. See: Table 6 Priorities of subpage controls

Subpage 0 --> 0x8000 = 0xXXX8



Subpage 1 --> 0x8000 = 0xXXX9

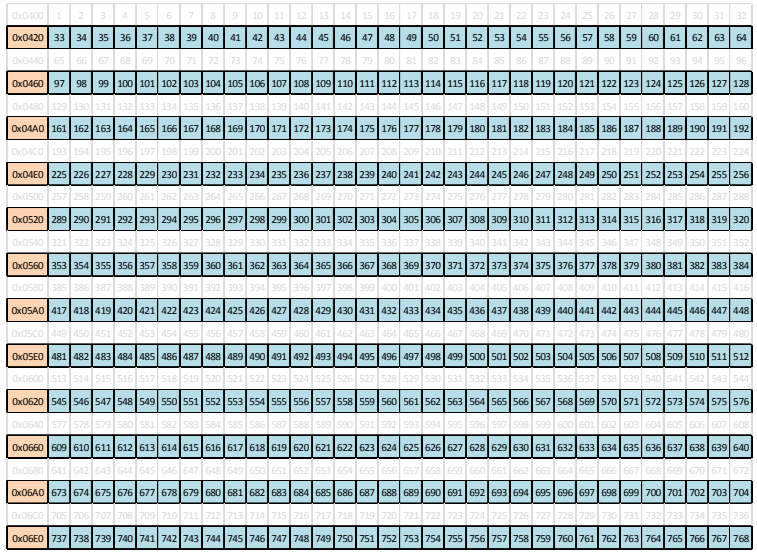
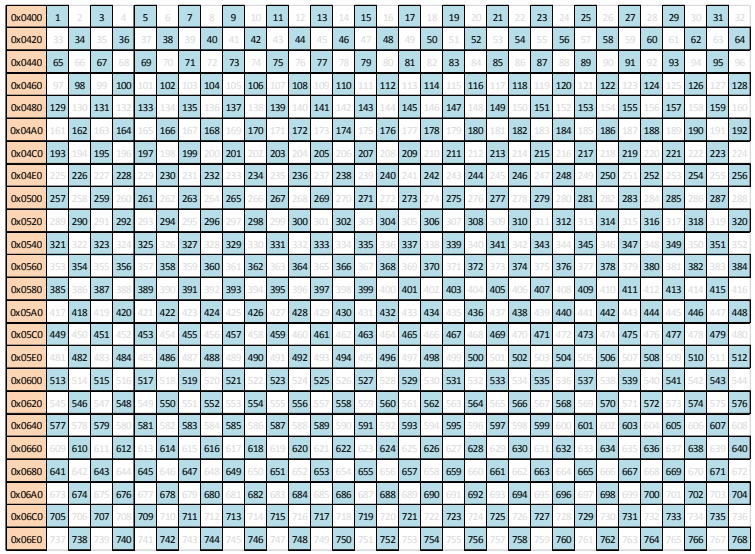


Figure 8 TV mode reading pattern (only highlighted cells are updated)

Subpage 0 --> 0x8000 = 0xXXX8



Subpage 1 --> 0x8000 = 0xXXX9

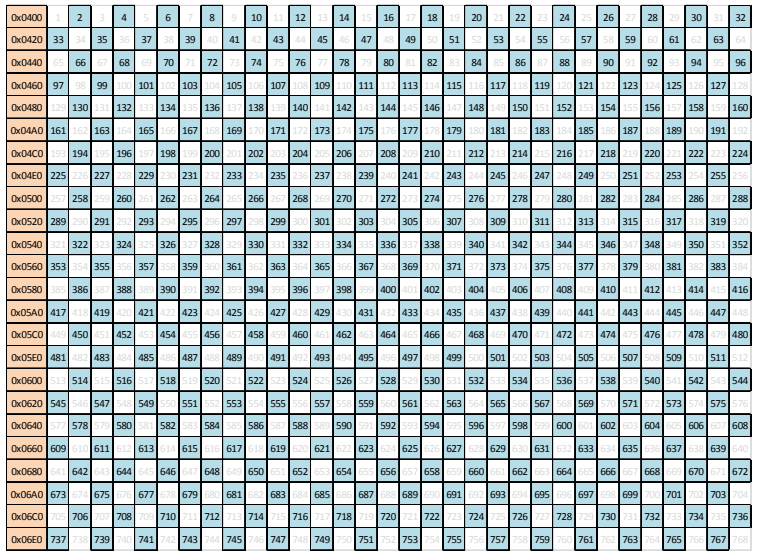


Figure 9 Chess reading pattern (only highlighted cells are updated)

10.7. Address map

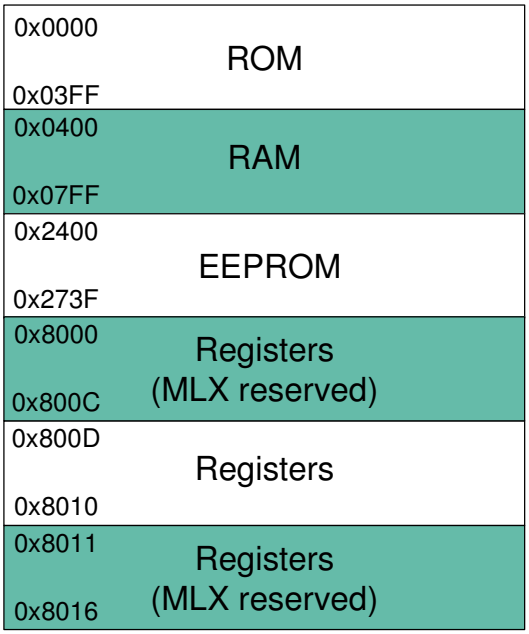


Figure 10 MXL90640 memory map

10.7.1. Internal registers

There are a few internal registers that are customer accessible through which the device performance can be customized:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	**Status register - 0x8000**
Melexis reserved											Enable overwrite	New data available in RAM	Last measured subpage controlled by MLX90641			
													0	0	0	Measurement of subpage 0 has been measured
													0	0	1	Measurement of subpage 1 has been measured
													0	1	0	Melxis reserved
													0	1	1	Melxis reserved
													1	0	0	Melxis reserved
													1	0	1	Melxis reserved
													1	1	0	Melxis reserved
													1	1	1	Melxis reserved
												0	No new data is available in RAM (must be reset be the customer)			
												1	A new data is available in RAM			
											0	Data in RAM overwrite is disabled				
											1	Data in RAM overwrite is enabled				
-	-	-	-	-	-	-	-	-	-	-	Melexis reserved					

Figure 11 Status register (0x8000) bits meaning

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Control register 1 - 0x800D
Melexis reserved			Reading pattern	Resolution control		Refresh rate control			Select subpage			Enable subpages repeat	Enable data hold	Melexis reserved	Enable subpages mode	
															0	No subpages, only one page will be measured
															1	Subpade mode is activated (default)
														0		Keep this bit = "0" (default)
													0			Transfer the data into storage RAM at each measured frame (default)
													1			Transfer the data into storage RAM only if en_overwrite = 1 (check 0x8000)
												0				Toggles between subpage "0" and subpage "1" if Enable subpages mode = "1" (default)
												1				Select subpage determines which subpage to be measured if Enable subpages mode = "1"
									0	0	0					Subpage 0 is selected (default)
									0	0	1					Subpage 1 is selected
									0	1	0					Not Applicable
									0	1	1					Not Applicable
									1	0	0					Not Applicable
									1	0	1					Not Applicable
									1	1	0					Not Applicable
									1	1	1					Not Applicable
						0	0	0								IR refresh rate = 0.5Hz
						0	0	1								IR refresh rate = 1Hz
						0	1	0								IR refresh rate = 2Hz (default)
						0	1	1								IR refresh rate = 4Hz
						1	0	0								IR refresh rate = 8Hz
						1	0	1								IR refresh rate = 16Hz
						1	1	0								IR refresh rate = 32Hz
						1	1	1								IR refresh rate = 64Hz
				0	0											ADC set to 16 bit resolution
				0	1											ADC set to 17 bit resolution
				1	0											ADC set to 18 bit resolution (default)
				1	1											ADC set to 19 bit resolution
			0													Interleaved (TV) mode
			1													Chess pattern (default)
-	-	-	Melexis reserved													

Figure 12 Control register1 (0x800D) bits meaning

Enable subpage mode (Bit 0)	Enable subpage repeat (Bit 3)	Select subpage (Bit 4)	Working mode
0	0	-	measure subpage 0 only
0	1	-	measure subpage 0 only
1	0	-	0 → 1 → 0 → 1 …
1	1	0	measure subpage 0 only
1	1	1	measure subpage 1 only

Table 6 Priorities of subpage controls (0x0800D)

B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
Melexis reserved												Melexis reserved	SDA driver current limit control	I2C threshold levels	FM+ disable	**I2C configuration register - 0x800F**
															0	FM+ mode enabled (default)
															1	FM+ mode disabled
														0		VDD reffered threshold (normal mode) (default)
														1		1.8V reffered threshold (1.8V mode)
													0			SDA driver current limit is ON (default)
													1			SDA driver current limit is OFF
												0				Melexis reserved
-	-	-	-	-	-	-	-	-	-	-	-					

Figure 13 I²C configuration register (0x800F) bits meaning

10.7.2. RAM

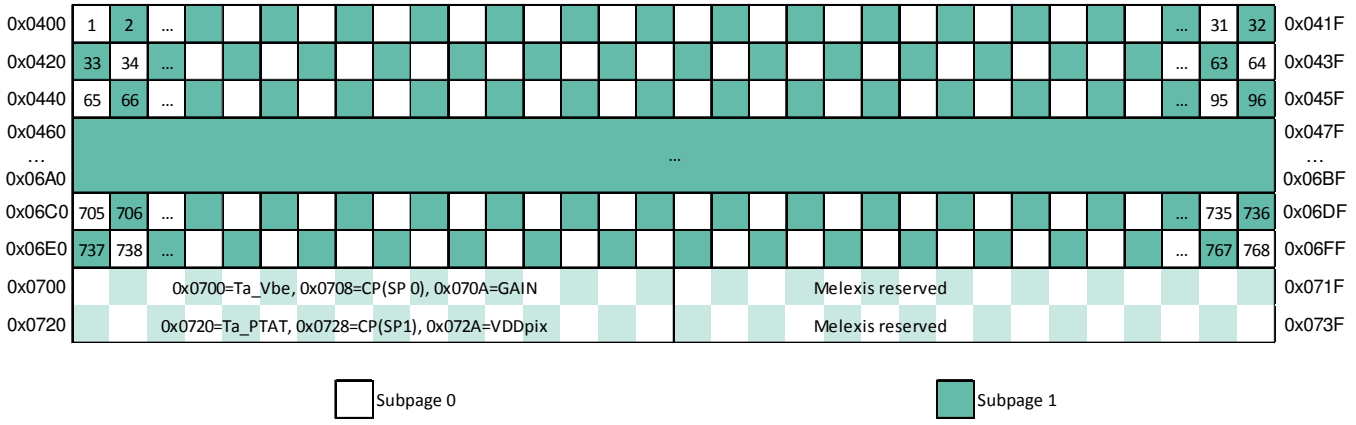


Figure 14 RAM memory map (Chess pattern mode) – factory default mode

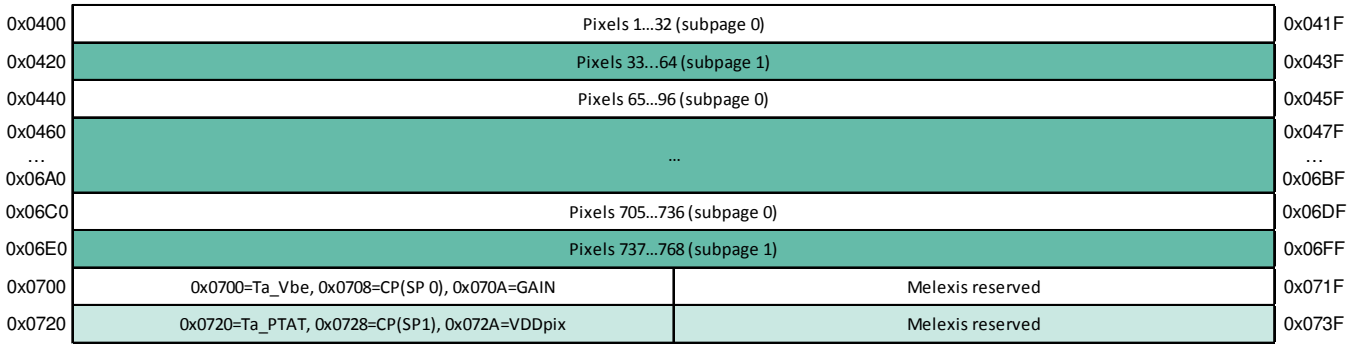


Figure 15 RAM memory map (Interleaved mode)

10.7.3. EEPROM

The EEPROM is used to store the calibration constants and the configuration parameters of the device

EEPROM address	Access	Meaning
0x2400	Melexis	Melexis reserved
0x2401	Melexis	Melexis reserved
0x2402	Melexis	Melexis reserved
0x2403	Melexis	Configuration register
0x2404	Melexis	Melexis reserved
0x2405	Melexis	Melexis reserved
0x2406	Melexis	Melexis reserved
0x2407	Melexis	Device ID1
0x2408	Melexis	Device ID2
0x2409	Melexis	Device ID3
0x240A	Melexis	Device Options
0x240B	Melexis	Melexis reserved
0x240C	Customer	Control register_1
0x240D	Customer	Control register_2
0x240E	Customer	I2CConfReg
0x240F	Customer	Melexis reserved / I2C_Address

Table 7 Configuration parameters memory

After POR the device read dedicated EEPROM cells and transfers their content to into the control and configuration register of the device. This way the device is configured and prepared for operation. The relation between EEPROM and register address is shown here after (explanation of the bit meaning can be found in section 10.7.1 Internal registers:

EEPROM address	Register address	Access	Name	Data [hex]
0x240C	0x800D	Customer	Control_register_1	1901
0x240D	0x800E	Customer	Control_register_2	0000
0x240E	0x800F	Customer	I2CConfReg	0000
0x240F	0x8010	Customer	Melexis internal use (8 bit) I2C_Address (8bit)	BE33

Table 8 EEPROM to registers mapping

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x2400	Osc Trim	Ana Trim	MLX	Conf reg	MLX	MLX	MLX	ID 1	ID 2	ID 3	MLX	MLX	Cont reg 1	Cont reg 2	I2C conf	I2C add
0x2410	Scale OCC	Pix os avg	OCC_row_01…24 (6 x 4 x 3bit+sign)						OCC_column_01…32 (8 x 4 x 3bit+sign)							
0x2420	Scale ACC	Pix α avg	ACC_row_01…24 (6 x 4 x 3bit+sign)						ACC_column_01…32 (8 x 4 x 3bit+sign)							
0x2430	GAIN	PTAT_25	Kv, Kt ptat	Kv Vdd_25	Kv_avg	MLX	Kta_avg		Kv, Kta Sca	ACP 1,2	Off - CP1,2	Kv, Kta Cp	KsTa, TGC	KsTo 4, 3	KsTo 2, 1	CT 4, 3
0x2440	768 x Offset, α, Kta, Outlier															
0x2450																
0x2460																
0x2470																
0x2480																
0x2490																
0x24A0																
0x24B0																
0x24C0																
0x24D0																
0x24E0																
0x24F0																
0x2500																
0x2510																
0x2520																
0x2530																
0x2540																
0x2550																
0x2560																
0x2570																
0x2580																
0x2590																
0x25A0																
0x25B0																
0x25C0																
0x25D0																
0x25E0																
0x25F0																
0x2600																
0x2610																
0x2620																
0x2630																
0x2640																
0x2650																
0x2660																
0x2670																
0x2680																
0x2690																
0x26A0																
0x26B0																
0x26C0																
0x26D0																
0x26E0																
0x26F0																
0x2700																
0x2710																
0x2720																
0x2730																

Table 9 EEPROM overview (words)

Address \ bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x2410	(Alpha PTAT - 8)*4				scale_Occ_row				scale_Occ_col				scale_Occ_rem			
0x2411	± Pix_os_average															
0x2412	± OCC row 4				± OCC row 3				± OCC row 2				± OCC row 1			
0x2413	± OCC row 8				± OCC row 7				± OCC row 6				± OCC row 5			
0x2414	± OCC row 12				± OCC row 11				± OCC row 10				± OCC row 9			
0x2415	± OCC row 16				± OCC row 15				± OCC row 14				± OCC row 13			
0x2416	± OCC row 20				± OCC row 19				± OCC row 18				± OCC row 17			
0x2417	± OCC row 24				± OCC row 23				± OCC row 22				± OCC row 21			
0x2418	± OCC column 4				± OCC column 3				± OCC column 2				± OCC column 1			
0x2419	± OCC column 8				± OCC column 7				± OCC column 6				± OCC column 5			
0x241A	± OCC column 12				± OCC column 11				± OCC column 10				± OCC column 9			
0x241B	± OCC column 16				± OCC column 15				± OCC column 14				± OCC column 13			
0x241C	± OCC column 20				± OCC column 19				± OCC column 18				± OCC column 17			
0x241D	± OCC column 24				± OCC column 23				± OCC column 22				± OCC column 21			
0x241E	± OCC column 28				± OCC column 27				± OCC column 26				± OCC column 25			
0x241F	± OCC column 32				± OCC column 31				± OCC column 30				± OCC column 29			
0x2420	Alpha scale - 30				Scale_ACC_row				Scale_ACC_column				Scale_ACC_remnand			
0x2421	Pix_sensitivity_average															
0x2422	± ACC row 4				± ACC row 3				± ACC row 2				± ACC row 1			
0x2423	± ACC row 8				± ACC row 7				± ACC row 6				± ACC row 5			
0x2424	± ACC row 12				± ACC row 11				± ACC row 10				± ACC row 9			
0x2425	± ACC row 16				± ACC row 15				± ACC row 14				± ACC row 13			
0x2426	± ACC row 20				± ACC row 19				± ACC row 18				± ACC row 17			
0x2427	± ACC row 24				± ACC row 23				± ACC row 22				± ACC row 21			
0x2428	± ACC column 4				± ACC column 3				± ACC column 2				± ACC column 1			
0x2429	± ACC column 8				± ACC column 7				± ACC column 6				± ACC column 5			
0x242A	± ACC column 12				± ACC column 11				± ACC column 10				± ACC column 9			
0x242B	± ACC column 16				± ACC column 15				± ACC column 14				± ACC column 13			
0x242C	± ACC column 20				± ACC column 19				± ACC column 18				± ACC column 17			
0x242D	± ACC column 24				± ACC column 23				± ACC column 22				± ACC column 21			
0x242E	± ACC column 28				± ACC column 27				± ACC column 26				± ACC column 25			
0x242F	± ACC column 32				± ACC column 31				± ACC column 30				± ACC column 29			
0x2430	± GAIN															
0x2431	± PTAT_25															
0x2432	± Kv_PTAT								± Kt_PTAT							
0x2433	± Kv_Vdd								± Vdd_25							
0x2434	± Kv_avg_RowOdd-ColumnOdd				± Kv_avg_RowEven-ColumnOdd				± Kv_avg_RowOdd-ColumnEven				± Kv_avg_RowEven-ColumnEven			
0x2435	±IL_CHESS_C3 - 5 bits						±IL_CHESS_C2 - 5 bits						±IL_CHESS_C1 - 6 bits			
0x2436	± Kta_avg_RowOdd-ColumnOdd								± Kta_avg_RowEven-ColumnOdd							
0x2437	± Kta_avg_RowOdd-ColumnEven								± Kta_avg_RowEven-ColumnEven							
0x2438	MLX		Res control calib		Kv_scale				Kta_scale_1				Kta_scale_2			
0x2439	± Alpha (CP subpage_1 / CP subpage_0 - 1)*2^7								Alpha CP subpage_0							
0x243A	± Offset (CP subpage_1 - CP subpage_0)								± Offset CP subpage_0							
0x243B	± Kv_CP								± Kta_CP							
0x243C	± KsTa*2^13								TGC (±4)*2^7							
0x243D	± KsTo range 2 (0°C…CT1°C)								± KsTo range 1 (<0°C)							
0x243E	± KsTo range 4 (CT2°C…)								± KsTo range 3 (CT1°C…CT2°C)							
0x243F	MLX		temp step x 10		CT4				CT3				KsTo Scale offset - 8			
0x2440	± Offset pixel (1, 1)								α pixel (1, 1)				± Kta (1, 1)			Outlier
0x2441	± Offset pixel (1, 2)								α pixel (1, 2)				± Kta (1, 2)			Outlier
…	…								…				…			…
0x245E	± Offset pixel (1, 31)								α pixel (1, 31)				± Kta (1, 31)			Outlier
0x245F	± Offset pixel (1, 32)								α pixel (1, 32)				± Kta (1, 32)			Outlier
0x2460	± Offset pixel (2, 1)								α pixel (2, 1)				± Kta (2, 1)			Outlier
0x2461	± Offset pixel (2, 2)								α pixel (2, 2)				± Kta (2, 2)			Outlier
…	…								…				…			…
0x273E	± Offset pixel (24, 31)								α pixel (24, 31)				± Kta (24, 31)			Outlier
0x273F	± Offset pixel (24, 32)								α pixel (24, 32)				± Kta (24, 32)			Outlier

Table 10 Calibration parameters memory (EEPROM - bits)

***NOTE 1**: EEPROM addresses from 0x2440…0x273F contain the individual pixel calibration information and may not be equal to 0x0000. In case any pixel data is equal to 0x0000 this means that this particular pixels has failed and the calculation for To should not be trusted and avoided. Depending on the application, the To value for such pixels can be replaced with a default value such as -273.15°C, can be equal to Ta or one calculate an average value from the adjacent pixels.*

***NOTE 2**: The LSB for EEPROM addresses from 0x2440…0x273F indicate if all pixel parameters are within the calibration specification. If this bit is set i.e. = "1" this would mean that at least one of the calibration parameters for this particular pixel is outside the calibration specifications and the pixel is considered as Outlier i.e. the sensor accuracy is not guaranteed by the calibration. Depending on the application one may have to choose to replace the measurement results of such pixel by an average of the temperature indicated by the adjacent pixels.*

***NOTE 3**: The maximum number of deviating pixels is 4 (please check* False pixel correction*)*

11. Calculating Object Temperature

11.1. Restoring calibration data from EERPOM

NOTE: All data in the EEPROM is coded as two's complement (unless otherwise noted)

In the example we are restoring the calibration data for pixel (12, 16)

11.1.1. Restoring the VDD sensor parameters

Following formula is used to calculate the VDD of the sensor:

$$K_{Vdd} = \frac{EE[0x2433]\ \&\ 0xFF00}{2^8}$$

If $K_{Vdd} > 127 \rightarrow K_{Vdd} = K_{Vdd} - 256$

$$K_{Vdd} = K_{Vdd} * 2^5$$

$$VDD_{25} = EE[0x2433]\ \&\ 0x00FF$$

$$VDD_{25} = (VDD_{25} - 256) * 2^5 - 2^{13}$$

11.1.2. Restoring the Ta sensor parameters

Following formula is used to calculate the Ta of the sensor:

$$T_a = \frac{\left(\frac{V_{PTAT_{art}}}{1+K_{V_{PTAT}}*\Delta V} - V_{PTAT_{25}}\right)}{K_{T_{PTAT}}} + 25,\ °C$$

Where:

$$K_{V_{PTAT}} = \frac{EE[0x2432]\ \&\ 0xFC00}{2^{10}}$$

If $K_{V_{PTAT}} > 31 \rightarrow K_{V_{PTAT}} = K_{V_{PTAT}} - 64$

$$K_{V_{PTAT}} = \frac{K_{V_{PTAT}}}{2^{12}}$$

$$K_{T_{PTAT}} = EE[0x2432]\ \&\ 0x03FF$$

If $K_{T_{PTAT}} > 511 \rightarrow K_{T_{PTAT}} = K_{T_{PTAT}} - 1024$

$$K_{T_{PTAT}} = \frac{K_{T_{PTAT}}}{2^3}$$

$$\Delta V = \frac{RAM[0x072A] - VDD_{25}}{K_V}$$

$$V_{PTAT_{25}} = EE[0x2431]$$

If $V_{PTAT_{25}} > 32767 \rightarrow V_{PTAT_{25}} = V_{PTAT_{25}} - 65536$

$$V_{PTAT_{art}} = \left(\frac{V_{PTAT}}{V_{PTAT} * Alpha_{PTAT} + V_{BE}}\right) * 2^{18}$$

Where:

$V_{PTAT} = RAM[0x0720]$

If $V_{PTAT} > 32767 \rightarrow V_{PTAT} = V_{PTAT} - 65536$

$V_{BE} = RAM[0x0700]$

If $V_{BE} > 32767 \rightarrow V_{BE} = V_{BE} - 65536$

$$Alpha_{PTAT\_EE} = \frac{EE[0x2410] \,\&\, 0xF000}{2^{12}}$$

$$Alpha_{PTAT} = \frac{Alpha_{PTAT\_EE}}{2^2} + 8$$

11.1.3. Restoring the offset

$$pix_{OS_{ref}}(i,j) = Offset_{average} + OCC_{row_i} * 2^{OCC_{scale_{row}}} + OCC_{column_j} * 2^{OCC_{scale_{column}}} + offset(i,j) * 2^{OCC_{scale_{remnant}}}$$

$Offset_{average} = EE[0x2411]$

If $Offset_{average} > 32767 \rightarrow Offset_{average} = Offset_{average} - 65536$

$OCC_{row_{12}} = \frac{EE[0x2414] \,\&\, 0xF000}{2^{12}}$ (i.e. the four most significant bits, signed)

If $OCC_{row_{12}} > 7 \rightarrow OCC_{row_{12}} = OCC_{row_{12}} - 16$

$OCC_{scale_{row}} = \frac{EE[0x2410] \,\&\, 0x0F00}{2^8}$ (unsigned)

$OCC_{column_{16}} = \frac{EE[0x241B] \,\&\, 0xF000}{2^{12}}$ (i.e. the four most significant bits, signed)

If $OCC_{column_{16}} > 7 \rightarrow OCC_{column_{16}} = OCC_{column_{16}} - 16$

$OCC_{scale_{column}} = \frac{EE[0x2410] \,\&\, 0x00F0}{2^4}$ (unsigned)

$offset(12,16) = \frac{EE[0x25AF] \,\&\, 0xFC00}{2^{10}}$ (i.e. the six most significant bits, signed)

If $offset(12,16) > 31 \rightarrow offset(12,16) = offset(12,16) - 64$

$OCC_{scale_{remnant}} = EE[0x2410] \,\&\, 0x000F$ (unsigned)

11.1.3.1. Restoring the offset in case of Interleaved reading pattern

To compensate the IR data for interleaved reading pattern following formula is used:

$$pix_{OS}(i,j) = pix_{gain}(i,j) + IL_{CHESS_{C_3}} * (2 * IL_{PATTERN} - 1) - IL_{CHESS_{C_2}} * Conversion_{pattern} - pix_{OS_{ref}} * \left(1 + K_{Ta(i,j)} * (T_a - T_{a0})\right) * \left(1 + K_{V(i,j)} * (V_{dd} - V_{dd_{V0}})\right)$$

Highlighted in yellow parameters are extracted here after.

As a default the device is factory calibrated in Chess pattern mode thus the best performance will be when a Chess pattern is used. However some customers may choose to use the device in interleaved mode which will degrade the device performance. In this case a correction can be applied to restore to some extend the performance. Once the IR data is compensated the calculation for To is done using default flow. The goal of this correction is to equalize the offset of the pixels due to the different pattern reading modes. We can achieve this by using several correction coefficients stored into the device EEPROM extracted and decoded as follows:

$$IL_{CHESS_{C1}EE} = EE[0x2435] \,\&\, 0x003\text{F}$$

If $IL_{CHESS_{C1}EE} > 31 \rightarrow IL_{CHESS_{C1}EE} = IL_{CHESS_{C1}EE} - 64$

$$IL_{CHESS_{C1}} = \frac{IL_{CHESS_{C1}EE}}{2^4}$$

$$IL_{CHESS_{C2}EE} = \frac{EE[0x2435] \,\&\, 0x07\text{C0}}{2^6}$$

If $IL_{CHESS_{C2}EE} > 15 \rightarrow IL_{CHESS_{C2}EE} = IL_{CHESS_{C2}EE} - 32$

$$L_{CHESS_{C2}} = \frac{IL_{CHESS_{C2}EE}}{2}$$

$$IL_{CHESS_{C3}EE} = \frac{EE[0x2435] \,\&\, 0x\text{F800}}{2^{11}}$$

If $IL_{CHESS_{C3}EE} > 15 \rightarrow IL_{CHESS_{C3}EE} = IL_{CHESS_{C3}EE} - 32$

$$IL_{CHESS_{C3}} = \frac{IL_{CHESS_{C3}EE}}{2^3}$$

The above calculated parameters have to be applied as a correction for the offset of each individual pixel. We do need additional patterns in order to make these calculations and the formula to calculate those patterns are as shown below depending on the pixels number:

$$IL_{PATTERN} = int\left(\frac{pixel_{number}-1}{32}\right) - int\left(\frac{int\left(\frac{pixel_{number}-1}{32}\right)}{2}\right) * 2$$

$$Conversion_{pattern} = \left(int\left(\frac{pixel_{number}-3}{4}\right) - int\left(\frac{pixel_{number}-2}{4}\right) + int\left(\frac{pixel_{number}}{4}\right) - int\left(\frac{pixel_{number}-1}{4}\right)\right) * (1 - 2 * IL_{PATTERN})$$

11.1.4. Restoring the Sensitivity $\alpha_{(i,j)}$

$$\alpha_{(i,j)} = \frac{\alpha_{reference} + ACC_{row_i} * 2^{ACC_{scale_{row}}} + ACC_{column_j} * 2^{ACC_{scale_{column}}} + \alpha_{pixel(i,j)} * 2^{ACC_{scale_{remnant}}}}{2^{\alpha_{scale}}}$$

Where (calculating for pixel (12,16)) :

$$\alpha_{reference} = EE[0x2421]$$

$$\alpha_{scale} = \frac{EE[0x2420] \,\&\, 0xF000}{2^{12}} + 30$$

$ACC_{row_{12}} = \frac{EE[0x2424] \,\&\, 0xF000}{2^{12}}$ (i.e. the four most significant bits, signed)

If $ACC_{row_{12}} > 7 \rightarrow ACC_{row_{12}} = ACC_{row_{12}} - 16$

$ACC_{scale_{row}} = \frac{EE[0x2420] \,\&\, 0x0F00}{2^{8}}$ (unsigned)

$ACC_{column_{16}} = \frac{EE[0x242B] \,\&\, 0xF000}{2^{12}}$ (i.e. the four most significant bits, signed)

If $ACC_{column_{16}} > 7 \rightarrow ACC_{column_{16}} = ACC_{column_{16}} - 16$

$ACC_{scale_{column}} = \frac{EE[0x2420] \,\&\, 0x00F0}{2^{4}}$ (unsigned)

$\alpha_{pixel}(12,16) = \frac{EE[0x258F] \,\&\, 0x03F0}{2^{4}}$

If $\alpha_{pixel}(12,16) > 31 \rightarrow \alpha_{pixel}(12,16) = \alpha_{pixel}(12,16) - 64$

$ACC_{scale_{remnant}} = EE[0x2420] \,\&\, 0x000F$ (unsigned)

11.1.5. Restoring the Kv(i,j) coefficient

$K_{V(i,j)}$ depend on the pixel position in the array i.e. if the pixel row and column is odd or even

If row number is **ODD** (1, 3, 5…23) and column number is **ODD** (1, 3, 5…31) then $K_{V(i,j)} = \frac{EE[0x2434] \,\&\, 0xF000}{2^{12}}$

If row number is **EVEN** (2, 4, 6…24) and column number is **ODD** (1, 3, 5…31) then $K_{V(i,j)} = \frac{EE[0x2434] \,\&\, 0x0F00}{2^{8}}$

If row number is **ODD** (1, 3, 5…23) and column number is **EVEN** (2, 4, 6…32) then $K_{V(i,j)} = \frac{EE[0x2434] \,\&\, 0x00F0}{2^{4}}$

If row number is **EVEN** (2, 4, 6…24) and column number is **EVEN** (2, 4, 6…32) then $K_{V(i,j)} = EE[0x2434] \,\&\, 0x000F$

If $K_{V(i,j)} > 7 \rightarrow K_{V(i,j)} = K_{V(i,j)} - 16$

$K_{V(12,16)} = \frac{K_{V(i,j)}}{2^{K_{V_{scale}}}}$ (signed)

Where:

$K_{V_{scale}} = \frac{EE[0x2438] \,\&\, 0x0F00}{2^{8}}$ (unsigned)

11.1.6. Restoring the Kta(i,j) coefficient

$K_{Ta(12,16)} = \frac{K_{Ta\_RC\_EE} + K_{Ta(12,16)\_EE} * 2^{K_{Ta_{scale\_2}}}}{2^{K_{Ta_{scale\_1}}}}$

Where:

$K_{Ta(12,16)\_EE} = \frac{EE[0x25AF] \,\&\, 0x000E}{2}$ (signed)

If $K_{Ta(12,16)\_EE} > 3 \rightarrow K_{Ta(12,16)\_EE} = K_{Ta(12,16)\_EE} - 8$