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October 1987 Revised January 2004

# MM74C164

# 8-Bit Parallel-Out Serial Shift Register

# **General Description**

The MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. A high-level input enables the other input which will then determine the state of the flip-flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

## **Features**

■ Supply voltage range: 3V to 15V

■ Tenth power TTL compatible: drive 2 LPTTL loads

■ High noise immunity: 0.45 V<sub>CC</sub> (typ.)

■ Low power: 50 nW (typ.)

■ Medium speed operation: 0.8 MHz (typ.) with 10V

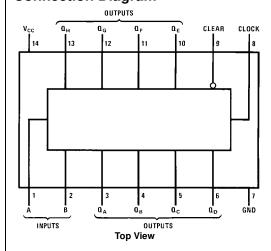
# **Applications**

- · Data terminals
- Instrumentation
- · Medical electronics
- · Alarm systems
- · Industrial electronics
- · Remote metering
- · Computers

# **Ordering Code:**

Order Number	Package Number	Package Description			
MM74C164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow			
MM74C164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

# **Connection Diagram**



# **Truth Table**

### Serial Inputs A and B

Innute

inp	Output		
t	t <sub>n+1</sub>		
Α	В	$Q_A$	
1	1	1	
0	1	0	
1	0	0	
0	0	0	

# **Block Diagram**

# **Absolute Maximum Ratings**(Note 1)

 $\begin{array}{lll} \mbox{Voltage at Any Pin} & -0.3\mbox{V to V}_{\rm CC} + 0.3\mbox{V} \\ \mbox{Operating Temperature Range} & -55\mbox{°C to +125}\mbox{°C} \\ \mbox{Storage Temperature Range} & -65\mbox{°C to +150}\mbox{°C} \\ \mbox{Absolute Maximum V}_{\rm CC} & 18\mbox{V}_{\rm CC} \end{array}$ 

Power Dissipation (P<sub>D</sub>)

Dual-In-Line 700 mW Small Outline 500 mW

Operating V<sub>CC</sub> Range 3V to 15V

Lead Temperature

(soldering, 10 seconds) 260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides

conditions for actual device operation.

# **DC Electrical Characteristics**

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	смоѕ		'			•
$V_{IN(1)}$	Logical "1" Input Voltage	V <sub>CC</sub> = 5V	3.5			V
		$V_{CC} = 10V$	8.0			v v
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 5V		1		V
		$V_{CC} = 10V$			2.0	, v
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 5V, I_{O} = -10 \mu A$	4.5			V
		$V_{CC}=10V,\ I_O=-10\ \mu A$	9.0			
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 5V, I_{O} = +10 \mu A$			0.5	V
		$V_{CC}=10V,\ I_O=+10\ \mu A$			1.0	v
I <sub>IN(1)</sub>	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μΑ
I <sub>IN(0)</sub>	Logical "0" Input Current	$V_{CC} = 15V$ , $V_{IN} = 0V$	-1.0	-0.005		μΑ
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 15V		0.05	300	μΑ
CMOS TO	LPTTL INTERFACE	•				•
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 4.75V	V <sub>CC</sub> – 1.5			V
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 4.75V			0.8	V
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 4.75V$ , $I_{O} = -360 \mu A$	2.4			V
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT D	RIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)				•
ISOURCE	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$	-1.75			mA
		$T_A = 25^{\circ}C$ , $V_{OUT} = 0V$				
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$	-8.0			mA
		$T_A = 25^{\circ}C, V_{OUT} = 0V$				
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$	1.75			mA
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$				
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$	8.0			mA
		$T_A = 25$ °C, $V_{OUT} = V_{CC}$				

# AC Electrical Characteristics (Note 2)

 $T_A=25^{\circ}C,\ C_L=50$  pF, unless otherwise noted

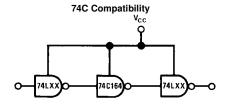
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
t <sub>pd1</sub>	Propagation Delay Time to a Logical "0" or a	$V_{CC} = 5V$		230	310		
	Logical "1" from Clock to Q	V <sub>CC</sub> = 10V		90	120	ns	
t <sub>pd0</sub>	Propagation Delay Time to a Logical "0" from	$V_{CC} = 5V$		280	380		
	Clear to Q	$V_{CC} = 10V$		110	150	ns	
t <sub>S</sub>	Time Prior to Clock Pulse that Data	$V_{CC} = 5V$	200	110			
	Must be Present	V <sub>CC</sub> = 10V	80	30		ns	
t <sub>H</sub>	Time After Clock Pulse that	$V_{CC} = 5V$	0	0		no	
	Data Must be Held	V <sub>CC</sub> = 10V	0	0		ns	
f <sub>MAX</sub>	Maximum Clock Frequency	$V_{CC} = 5V$	2.0	3		NALL-	
		V <sub>CC</sub> = 10V	5.5	8		MHz	
t <sub>W</sub>	Minimum Clear Pulse Width	$V_{CC} = 5V$		150	250	ns	
		V <sub>CC</sub> = 10V		55	90		
t <sub>r</sub> , t <sub>f</sub>	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$	15				
		$V_{CC} = 10V$	5			μs	
C <sub>IN</sub>	Input Capacitance	Any Input (Note 3)		5		pF	
C <sub>PD</sub>	Power Dissipation Capacitance	(Note 4)		140		pF	

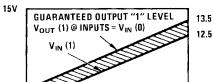
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

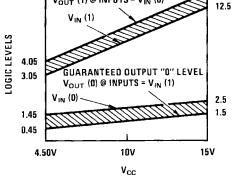
Note 4: C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note

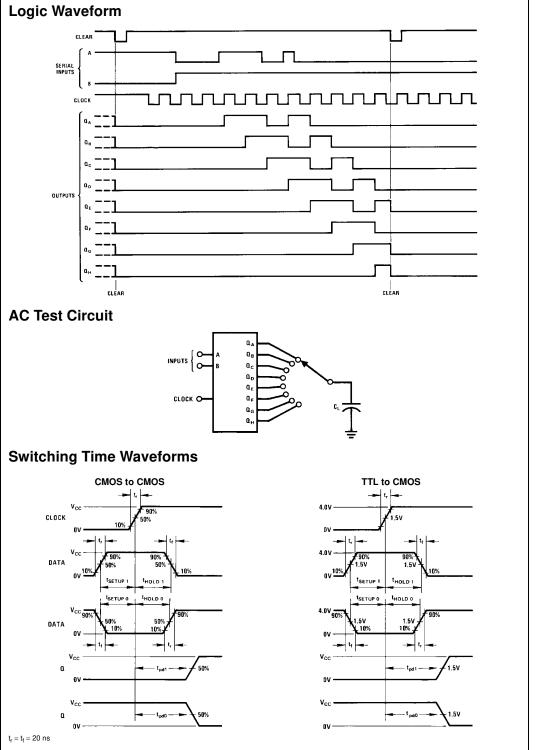
# **Typical Applications**





**Guaranteed Noise Margin** as a Function of  $V_{\mbox{\scriptsize CC}}$ 





# Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.335 - 0.344}{(8.509 - 8.738)}$ LEAD NO. 1 IDENT 0.010 MAX (0.254) $\frac{0.150 - 0.157}{(3.810 - 3.988)}$ $\frac{0.053 - 0.069}{(1.346 - 1.753)}$ $\frac{0.010 - 0.020}{(0.254 - 0.508)}$ 8° MAX TYP ALL LEADS $\frac{0.004 - 0.010}{(0.102 - 0.254)}$ SEATING PLANE 0.014 0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS 0.050 (1.270) TYP $\frac{0.014 - 0.020}{(0.356 - 0.508)} \text{ TYP}$ 0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS 0.004 (0.102) ALL LEAD TIPS 0.008 (0.203) TYP

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

M14A (REV h)

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 14 13 12 11 10 9 8 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 $0.075 \pm 0.015$ $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.023 $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ TYP (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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 $0.325 + 0.040 \\ -0.015 \\ \hline (8.255 + 1.016) \\ -0.381)$ 

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N14A (REV F)