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November 1987 Revised May 2002

MM74C221

Dual Monostable Multivibrator

General Description

The MM74C221 dual monostable multivibrator is a monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components $C_{\mbox{\footnotesize{EXT}}}$ and $R_{\mbox{\footnotesize{EXT}}}.$ The pulse width is stable over a wide range of temperature and V_{CC}.

Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} \; R_{EXT}.$ For further information and applications, see AN-138.

Features

■ Wide supply voltage range: 4.5V to 15V

■ Guaranteed noise margin: 1.0V ■ High noise immunity: 0.45 V_{CC} (typ.)

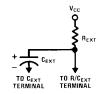
■ Low power TTL compatibility: fan out of 2 driving 74L

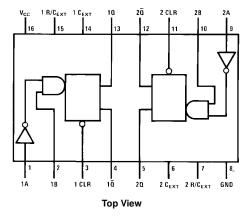
Ordering Code:

Order Number	Package Number	Package Description
74MMC221N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagrams

Timing Component





Truth Table

	Inputs			Outputs		
Clear	Α	В	Q	Q		
L	Х	Х	L	Н		
Х	Н	Х	L	Н		
Х	Х	L	L	Н		
Н	L	1	7	7		
Н	1	Н	工	ъ		

- H = HIGH Level
- L = LOW Level
- X= Irrelevant
- Transition from LOW-to-HIGH
- □ Transition from HIGH-to-LOW
 □ = One HIGH Level Pulse
 □ = One LOW Level Pulse

Absolute Maximum Ratings(Note 1)

 $\begin{array}{lll} \mbox{Voltage at Any Pin} & -0.3\mbox{V to V}_{\mbox{CC}} + 0.3\mbox{V} \\ \mbox{Operating Temperature Range} & -55\mbox{^{\circ}C to } +125\mbox{^{\circ}C} \\ \mbox{Storage Temperature Range} & -65\mbox{^{\circ}C to } +150\mbox{^{\circ}C} \\ \end{array}$

Power Dissipation

 Dual-In-Line
 700 mW

 Small Outline
 500 mW

 Operating V_{CC} Range
 4.5V to 15V

Absolute Maximum V_{CC} 18V

 $R_{EXT} \ge 80 \ V_{CC} \ (\Omega)$

Lead Temperature (Soldering, 10 seconds)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions

for actual device operation.

DC Electrical Characteristics

Max/min limits apply across temperature range, unless otherwise noted

Symbol	Parameter Parameter	Conditions	Min	Тур	Max	Units
CMOS to 0	CMOS	•		<u> </u>		
V _{IN(1)}	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
		$V_{CC} = 10V$			2.0	v
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_{O} = -10 \mu A$	4.5			V
		$V_{CC} = 10V$, $I_{O} = -10 \mu A$	9.0			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_{O} = +10 \mu A$			0.5	V
		$V_{CC} = 10V$, $I_{O} = +10 \mu A$			1	V
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μΑ
Icc	Supply Current (Standby)	V _{CC} = 15V, R _{EXT} = ∞,		0.05	300	μΑ
		Q1, Q2 = Logic "0" (Note 2)				
Icc	Supply Current	V _{CC} = 15V, Q1 = Logic "1",		15		mA
	(During Output Pulse)	Q2 = Logic "0" (Figure 4)				
		V _{CC} = 5V, Q1 = Logic "1",		2		mA
		Q2 = Logic "0" (Figure 4)				
	Leakage Current at R/C _{EXT} Pin	V _{CC} = 15V, V _{CEXT} = 5V		0.01	3.0	μΑ
CMOS/LP7	TTL Interface	·				•
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 4.75V	V _{CC} – 1.5			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 4.75V			8.0	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_{O} = -360 \mu A$	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{O} = 360 \mu A$			0.4	V
Output Dri	ive (See Family Characteristics Data	Sheet) (Short Circuit Current)				•
I _{SOURCE}	Output Source Current	V _{CC} = 5V	-1.75			mA
	(P-Channel)	$T_A = 25^{\circ}C$, $V_{OUT} = 0V$				
I _{SOURCE}	Output Source Current	V _{CC} = 10V	-8			mA
	(P-Channel)	$T_A = 25^{\circ}C$, $V_{OUT} = 0V$				
I _{SINK}	Output Sink Current	V _{CC} = 5V	1.75			mA
	(N-Channel)	$T_A = 25$ °C, $V_{OUT} = V_{CC}$				
I _{SINK}	Output Sink Current	V _{CC} = 10V	8			mA
	(N-Channel)	$T_A = 25^{\circ}C$, $V_{OUT} = V_{CC}$				

260°C

Note 2: In Standby (Q = Logic "0") the power dissipated equals the leakage current plus V_{CC}/R_{EXT} .

AC Electrical Characteristics (Note 3) Ta = 25°C, Cr. - 50 pE upless otherwise potent

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd A, B}	Propagation Delay from Trigger	V _{CC} = 5V		250	500	ns
	Input (A, B) to Output Q, Q	V _{CC} = 10V		120	250	
t _{pd CL}	Propagation Delay from Clear	V _{CC} = 5V		250	500	ns
	Input (CL) to Output Q, Q	V _{CC} = 10V		120	250	
ts	Time Prior to Trigger Input (A, B)	V _{CC} = 5V	150	50		ns
	that Clear must be Set	V _{CC} = 10V	60	20		
W(A, B)	Trigger Input (A, B) Pulse Width	V _{CC} = 5V	150	50		+
. , ,		V _{CC} = 10V	70	30		ns
t _{W(CL)}	Clear Input (CL) Pulse Width	V _{CC} = 5V	150	50		
(-)		V _{CC} = 10V	70	30		ns
tw(out)	Q or Q Output Pulse Width	V _{CC} = 5V, R _{EXT} = 10k,		900		ns
*W(OUT)	a si a saipar i also maai	$C_{EXT} = 0 \text{ pF}$		000		
		$V_{CC} = 10V, R_{EXT} = 10k,$		350		ns
		C _{EXT} = 0 pF		000		
		$V_{CC} = 15V, R_{EXT} = 10k,$		320		ns
		$C_{EXT} = 0 \text{ pF}$		020		110
		$V_{CC} = 5V, R_{EXT} = 10k,$	9.0	10.6	12.2	μS
		C _{EXT} = 1000 pF (Figure 1)	0.0	10.0		μo
		$V_{CC} = 10V, R_{EXT} = 10k,$	9.0	10	11	μs
		C _{EXT} = 1000 pF (Figure 1)				,,,,
		$V_{CC} = 15V, R_{EXT} = 10k,$	8.9	9.8	10.8	μs
		$C_{EXT} = 1000 \text{ pF (Figure 1)}$	0.0	0.0	10.0	μο
		$V_{CC} = 5V, R_{EXT} = 10k,$	900	1020	1200	μS
		$C_{EXT} = 0.1 \mu F \text{ (Figure 3)}$	000	1020	.200	μο
		$V_{CC} = 10V, R_{EXT} = 10k,$	900	1000	1100	μs
		$C_{EXT} = 0.1 \mu F \text{ (Figure 3)}$	000			μο
		V _{CC} = 15V, R _{EXT} = 10k,	900	990	1100	μS
		$C_{EXT} = 0.1 \mu F$ (Figure 3)	300	000	1100	μο
R _{ON}	ON Resistance of Transistor	V _{CC} = 5V (Note 4)		50	150	
···ON	between R/C _{EXT} to C _{EXT}	$V_{CC} = 3V \text{ (Note 4)}$ $V_{CC} = 10V \text{ (Note 4)}$		25	65	Ω
	Someon to Ext to SEXT	V _{CC} = 15V (Note 4)		16.7	45	
	Output Duty Cycle	R = 10k, C = 1000 pF	-		90	
	Salpar Bury Gyoro	$R = 10k$, $C = 0.1 \mu F$			90	%
		(Note 5)			00	
C _{IN}	Input Capacitance	R/C _{EXT} Input (Note 6)		15	25	-
CIN	input Capacitance	Any Other Input (Note 6)		5	25	pF

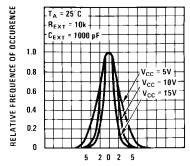
Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: See AN-138 for detailed explanation $\ensuremath{\text{R}_{\text{ON}}}.$

Note 5: Maximum output duty cycle = $R_{EXT}/R_{EXT} + 1000$.

Note 6: Capacitance is guaranteed by periodic testing.

Typical Performance Characteristics



OUTPUT PULSE WIDTH (Tw., %)

0% Point pulse width:

At $V_{CC} = 5V$, $T_W = 10.6 \,\mu s$

At $V_{CC}=10 V, T_W=10~\mu s$

At $V_{CC}=15V, T_W=9.8~\mu s$

Percentage of units within +4%:

At $V_{CC} = 5V,90\%$ of units

At $V_{CC} = 10V,95\%$ of units

At $V_{CC} = 15V,98\%$ of units

FIGURE 1. Typical Distribution of Units for Output Pulse Width

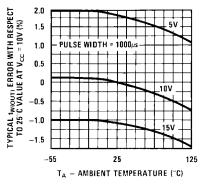
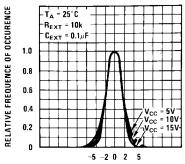


FIGURE 2. Typical Variation in Output Pulse Width vs
Temperature



OUTPUT PULSE WIDTH (Tw, %)

0% Point pulse width:

At $V_{CC} = 5V$, $T_W = 1020 \ \mu s$

At $V_{CC}=10 V, T_W=1000~\mu s$

At V_{CC} = 15V, T_W = 982 μs

Percentage of units within +4%: At $V_{CC} = 5V,95\%$ of units

At $V_{CC} = 10V,97\%$ of units

At $V_{CC} = 15V,98\%$ of units

FIGURE 3. Typical Distribution of Units for Output Pulse Width

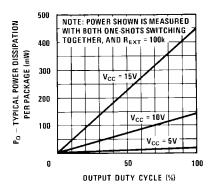


FIGURE 4. Typical Power Dissipation per Package

Typical Performance Characteristics (Continued) Switching Time Waveforms A INPUT 90% 50% 10% BINPUT CLEAR $t_r = t_f = 20 \text{ ns}$

Physical Dimensions inches (millimeters) unless otherwise noted 0.740 **-** 0.780 (18.80 **-** 19.81) (2.286)16 15 14 13 12 11 10 [6] [15] [T INDFX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 IDENT IDENT OPTION 01 OPTION 02 $\frac{0.065}{(1.651)}$ 0.130 ± 0.005 0.060 4º TYP OPTIONAL 0.300 - 0.320(3.302 ± 0.127) TYP (1.524)(7.620 - 8.128) 0.145 - 0.200 (3.683 - 5.080)95°±5° 0.008 **-** 0.016 (0.203 **-** 0.406) TYP 0.020 $\frac{0.280}{(7.112)}$ (0.508)0.125 - 0.150 $\frac{0.030 \pm 0.015}{(0.762 \pm 0.381)}$ (3.175 - 3.810)MIN 0.014 = 0.023 (0.356 = 0.584) 0.100 ± 0.010 (2.540 ± 0.254) 0.050 ± 0.010 N16E (REV F) TYP (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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