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MM74C373 • MM74C374

3-STATE Octal D-Type Latch • 3-STATE Octal D-Type Flip-Flop

General Description

The MM74C373 and MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with 3-STATE outputs. These outputs have been specially designed to drive high capacitive loads, such as one might find when driving a bus, and to have a fan out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74C373 is an 8-bit latch. When LATCH ENABLE is high, the Q outputs will follow the D inputs. When LATCH ENABLE goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until LATCH ENABLE returns high again.

The MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

Both the MM74C373 and the MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power consumption
- TTL compatibility:
 - Fan out of 1 driving standard TTL
- Bus driving capability
- 3-STATE outputs
- Eight storage elements in one package
- Single CLOCK/LATCH ENABLE and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

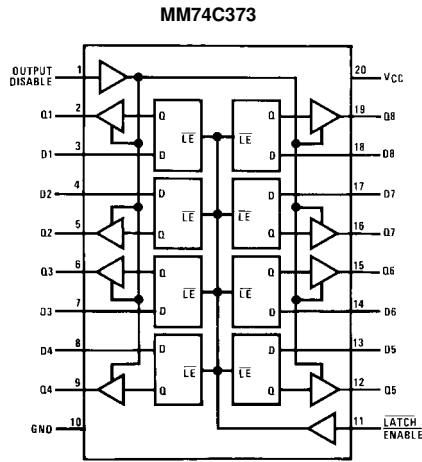
Ordering Code:

| Order Number | Package Number | Package Description |
|-----------------------|----------------|--|
| MM74C373M (Note 1) | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74C373N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| MM74C374N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

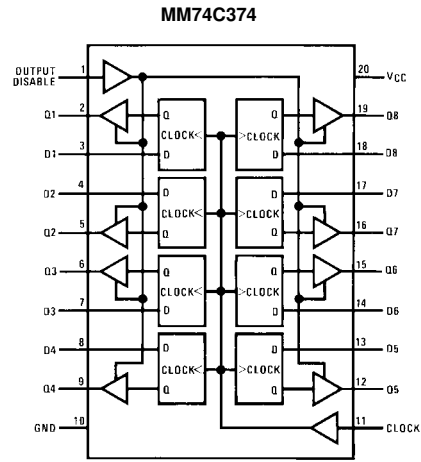
Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

MM74C373 • MM74C374 3-STATE Octal D-Type Latch • 3-STATE Octal D-Type Flip-Flop

Connection Diagrams



Top View



Top View

Truth Tables

MM74C373

| Output Disable | $\overline{\text{LATCH}} \text{ ENABLE}$ | D | Q |
|----------------|--|---|------|
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q |
| H | X | X | Hi-Z |

L = LOW logic level
 H = HIGH logic level
 X = Irrelevant

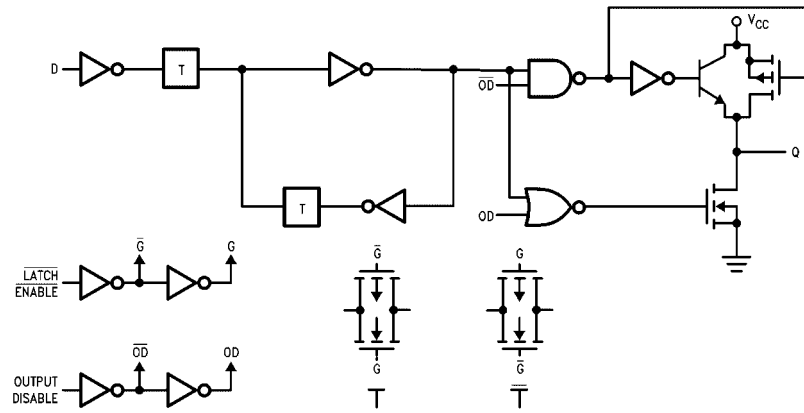
MM74C374

| Output Disable | Clock | D | Q |
|----------------|-------|---|------|
| L | ↗ | H | H |
| L | ↗ | L | L |
| L | L | X | Q |
| L | H | X | Q |
| H | X | X | Hi-Z |

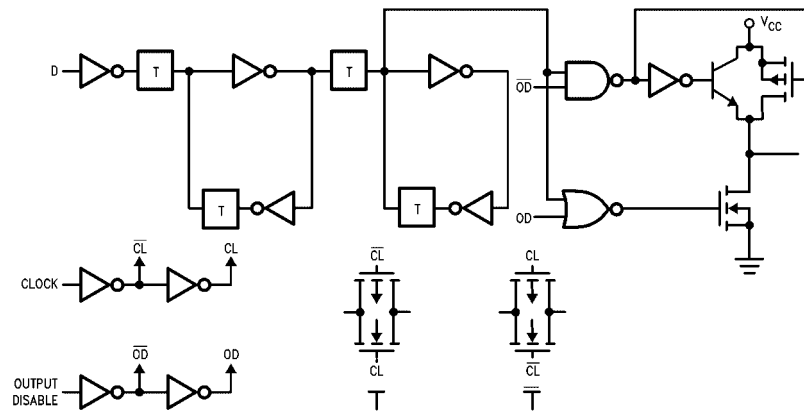
↗ = LOW-to-HIGH logic level transition
 Q = Preexisting output level
 Hi-Z = High impedance output state

Block Diagrams

MM74C373 (1 of 8 Latches)



MM74C374 (1 of 8 Flip-Flops)



Absolute Maximum Ratings(Note 2)

| | |
|---------------------------------------|--------------------------|
| Voltage at Any Pin | -0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range (T_A) | |
| MM74C373 | -55°C to +125°C |
| Storage Temperature Range (T_S) | -65°C to +150°C |
| Power Dissipation | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating V_{CC} Range | 3V to 15V |
| Absolute Maximum V_{CC} | 18V |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|------------------------------------|---|-----------------------|-----------------|------------|---------|
| CMOS TO CMOS | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5V$ $V_{CC} = 10V$ | 3.5 8.0 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5V$ $V_{CC} = 10V$ | | | 1.5 2.0 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$ | 4.5 9.0 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5V, I_O = 10 \mu A$ $V_{CC} = 10V, I_O = 10 \mu A$ | | | 0.5 1.0 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V, V_{IN} = 15V$ | | 0.005 | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V, V_{IN} = 0V$ | -1.0 | -0.005 | | μA |
| I_{OZ} | 3-STATE Leakage Current | $V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$ | -1.0 | 0.005 -0.005 | 1.0 | μA |
| I_{CC} | Supply Current | $V_{CC} = 15V$ | | 0.05 | 300 | μA |
| CMOS/LPTTL INTERFACE | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 4.75V$ | $V_{CC} - 1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 4.75V, I_O = -360 \mu A$ $V_{CC} = 4.75V, I_O = -1.6 mA$ | $V_{CC} - 0.4$ 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 4.75V, I_O = 1.6 mA$ | | | 0.4 | V |
| OUTPUT DRIVE (Short Circuit Current) | | | | | | |
| I_{SOURCE} | Output Source Current | $V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^\circ C$ (Note 3) | -12 | -24 | | mA |
| I_{SOURCE} | Output Source Current | $V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$ (Note 3) | -24 | -48 | | mA |
| I_{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$ (Note 3) | 6 | 12 | | mA |
| I_{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$ (Note 3) | 24 | 48 | | mA |

Note 3: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

| AC Electrical Characteristics (Note 4) | | | | | | |
|---|---|---|------------|------------------------|--------------------------|---------------|
| MM74C373, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $t_r = t_f = 20\text{ ns}$, unless otherwise noted | | | | | | |
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| t_{pd0} , t_{pd1} | Propagation Delay, LATCH ENABLE to Output | $V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$ | | 165 70 195 85 | 330 140 390 170 | ns |
| t_{pd0} , t_{pd1} | Propagation Delay Data In to Output | LATCH ENABLE = V_{CC} $V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$ | | 155 70 185 85 | 310 140 370 170 | ns |
| t_{SET-UP} | Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE | $t_{HOLD} = 0\text{ ns}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 70 35 | 140 70 | ns |
| f_{MAX} | Maximum LATCH ENABLE Frequency | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | 3.5 4.5 | 6.7 9.0 | | MHz |
| t_{PWH} | Minimum LATCH ENABLE Pulse Width | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 75 55 | 150 110 | ns |
| t_r , t_f | Maximum LATCH ENABLE Rise and Fall Time | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | NA NA | | μs |
| t_{1H} , t_{0H} | Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level) | $R_L = 10\text{k}$, $C_L = 5\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 105 60 | 210 120 | ns |
| t_{H1} , t_{H0} | Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State) | $R_L = 10\text{k}$, $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 105 45 | 210 90 | ns |
| t_{THL} , t_{TLH} | Transition Time | $V_{CC} = 5\text{V}$, $C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$ | | 65 35 110 70 | 130 70 220 140 | ns |
| C_{LE} | Input Capacitance | \overline{LE} Input (Note 5) | | 7.5 | 10 | pF |
| C_{OD} | Input Capacitance | OUTPUT DISABLE Input (Note 5) | | 7.5 | 10 | pF |
| C_{IN} | Input Capacitance | Any Other Input (Note 5) | | 5 | 7.5 | pF |
| C_{OUT} | Output Capacitance | High Impedance State (Note 5) | | 10 | 15 | pF |
| C_{PD} | Power Dissipation Capacitance | Per Package (Note 6) | | 200 | | pF |
| Note 4: AC Parameters are guaranteed by DC correlated testing. | | | | | | |
| Note 5: Capacitance is guaranteed by periodic testing. | | | | | | |
| Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note AN-90. | | | | | | |

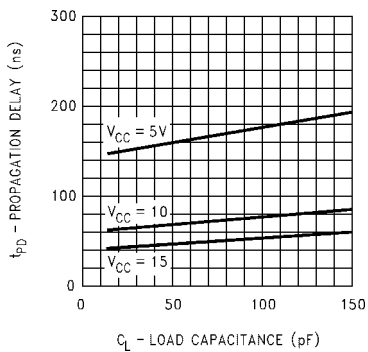
AC Electrical Characteristics (Note 7)MM74C374, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $t_r = t_f = 20\text{ ns}$, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------|---|--|----------|------------------------|--------------------------|---------------|
| t_{pd0}, t_{pd1} | Propagation Delay, CLOCK to Output | $V_{CC} = 5\text{V}, C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}, C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}, C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}, C_L = 150\text{ pF}$ | | 150 65 180 80 | 300 130 360 160 | ns |
| t_{SET-UP} | Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE | $t_{HOLD} = 0\text{ ns}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 70 35 | 140 70 | ns |
| t_{PWH}, t_{PWL} | Minimum CLOCK Pulse Width | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 70 50 | 140 100 | ns |
| f_{MAX} | Maximum CLOCK Frequency | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | 3.5 5 | 7.0 10 | | MHz |
| t_{1H}, t_{0H} | Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level) | $R_L = 10\text{k}, C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 105 60 | 210 120 | ns |
| t_{1H}, t_{H0} | Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State) | $R_L = 10\text{k}, C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | | 105 45 | 210 90 | ns |
| t_{THL}, t_{TLH} | Transition Time | $V_{CC} = 5\text{V}, C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}, C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}, C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}, C_L = 150\text{ pF}$ | | 65 35 110 70 | 130 70 220 140 | ns |
| t_r, t_f | Maximum CLOCK Rise and Fall Time | $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ | 15 5 | >2000 >2000 | | μs |
| C_{CLK} | Input Capacitance | CLOCK Input (Note 8) | | 7.5 | 10 | pF |
| C_{OD} | Input Capacitance | OUTPUT DISABLE Input (Note 8) | | 7.5 | 10 | pF |
| C_{IN} | Input Capacitance | Any Other Input (Note 8) | | 5 | 7.5 | pF |
| C_{OUT} | Output Capacitance | High Impedance State (Note 8) | | 10 | 15 | pF |
| C_{PD} | Power Dissipation Capacitance | Per Package (Note 9) | | 250 | | pF |

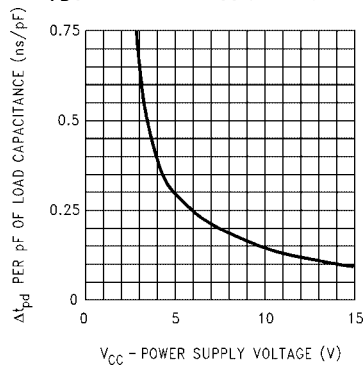
Note 7: AC Parameters are guaranteed by DC correlated testing.**Note 8:** Capacitance is guaranteed by periodic testing.**Note 9:** C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note AN-90.

Typical Performance Characteristics

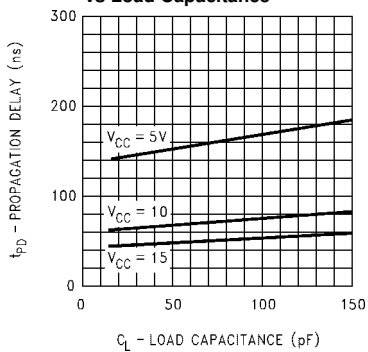
MM74C373
Propagation Delay, LATCH ENABLE to Output
vs Load Capacitance



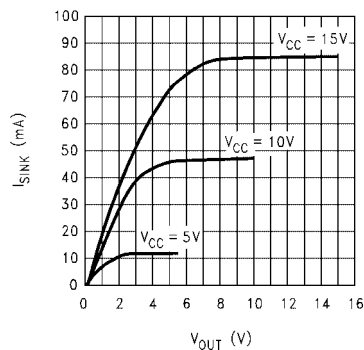
MM74C373, MM74C374
Change in Propagation Delay
per pF of Load Capacitance
($\Delta t_{pd}/pF$) vs Power Supply Voltage



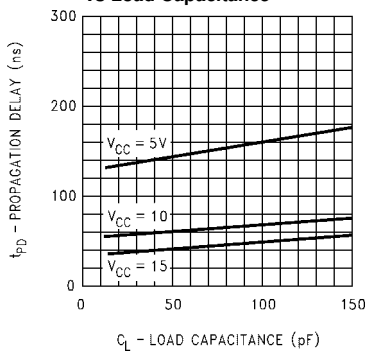
MM74C373
Propagation Delay, Data In to Output
vs Load Capacitance



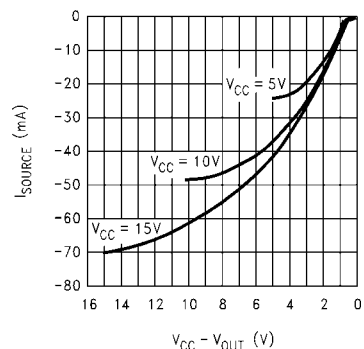
MM74C373, MM74C374
Output Sink Current vs V_{OUT}



MM74C373
Propagation Delay, CLOCK to Output
vs Load Capacitance

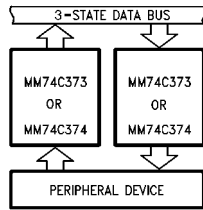


MM74C373, MM74C374
Source Current vs $V_{CC} - V_{OUT}$

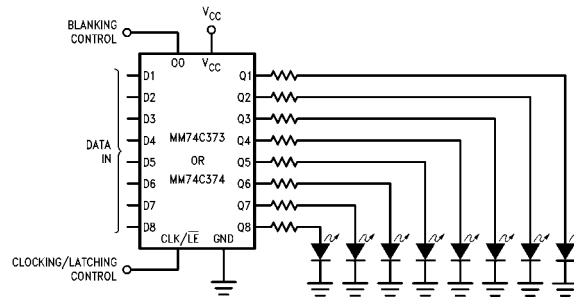


Typical Applications

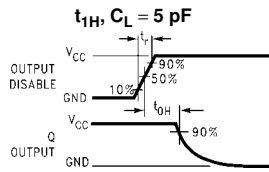
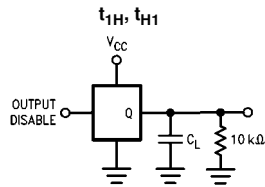
Data Bus Interfacing Element



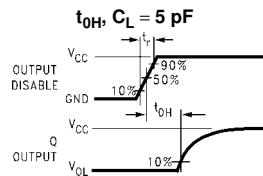
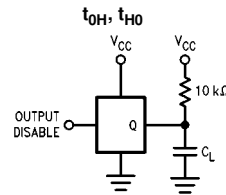
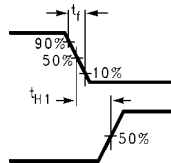
Simple, Latching, Octal, LED Indicator Driver with Blanking for Use as Data Display, Bus Monitor, μ P Front Panel Display, Etc.



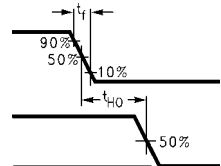
3-STATE Test Circuits and Switching Time Waveforms



t_{H1} , $C_L = 50$ pF

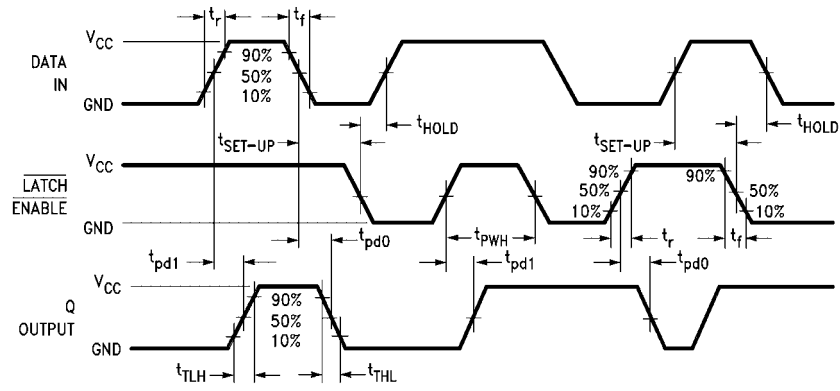


t_{H0} , $C_L = 50$ pF



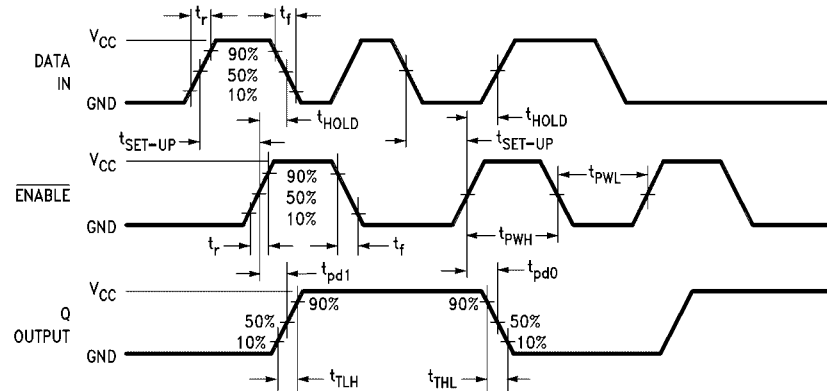
Switching Time Waveforms

MM74C373



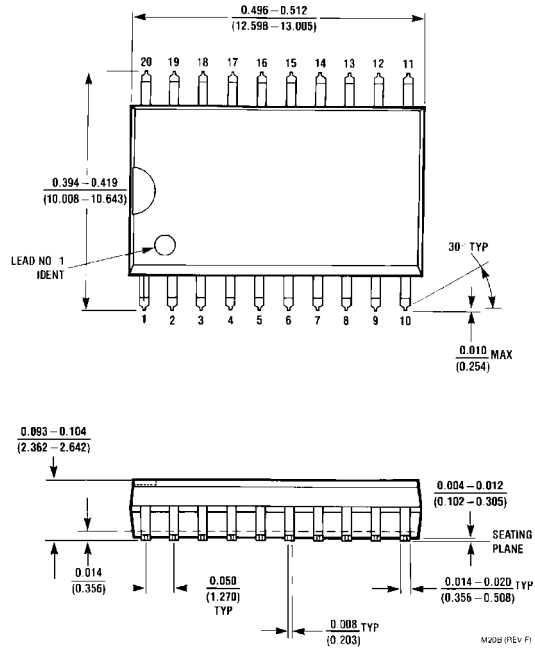
Output Disable = GND

MM74C374



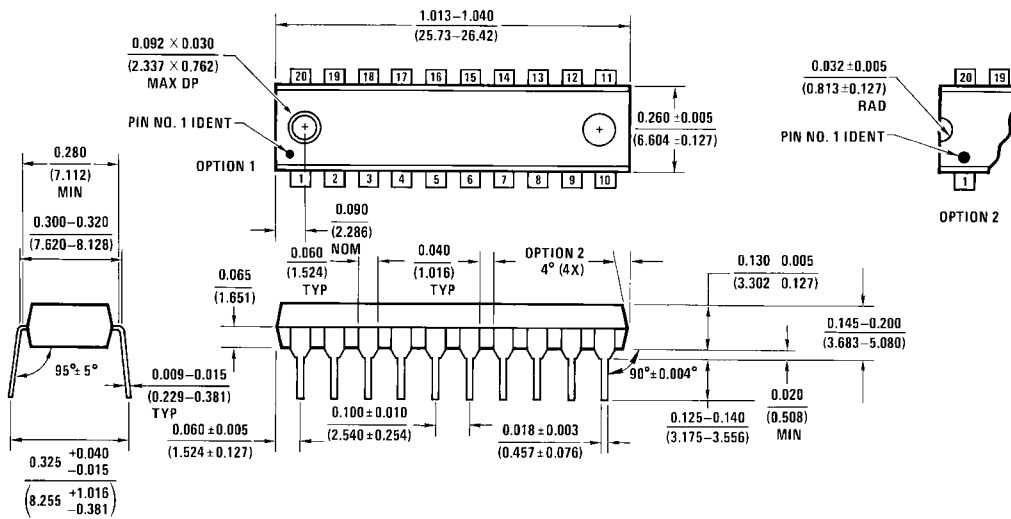
Output Disable = GND

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

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