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FAIRCHILD SEMICONDUCTOR™

September 1983
Revised December 2003

# MM74HC161 • MM74HC163
# Synchronous Binary Counter with Asynchronous Clear • Synchronous Binary Counter with Synchronous Clear

## General Description

The MM74HC161 and MM74HC163 synchronous presettable counters utilize advanced silicon-gate CMOS technology and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The HC161 and the HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the LOW-to-HIGH transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held LOW counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken HIGH before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM74HC163 counter is synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held LOW.

The MM74HC161 counter is cleared asynchronously. When the CLEAR is taken LOW the counter is cleared immediately regardless of the CLOCK.

Two active HIGH enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be HIGH to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the HIGH level portion of the $Q_A$ output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to $V_{CC}$ and ground.

## Features

- Typical operating frequency: 40 MHz
- Typical propagation delay; clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V

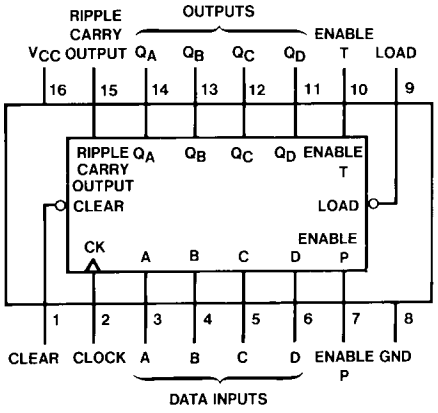
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HC161M (Note 1) | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC161SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC161MTC (Note 1) | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC161N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| MM74HC163M (Note 1) | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC163SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC163N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

**Note 1:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Truth Tables

**MM74HC161**

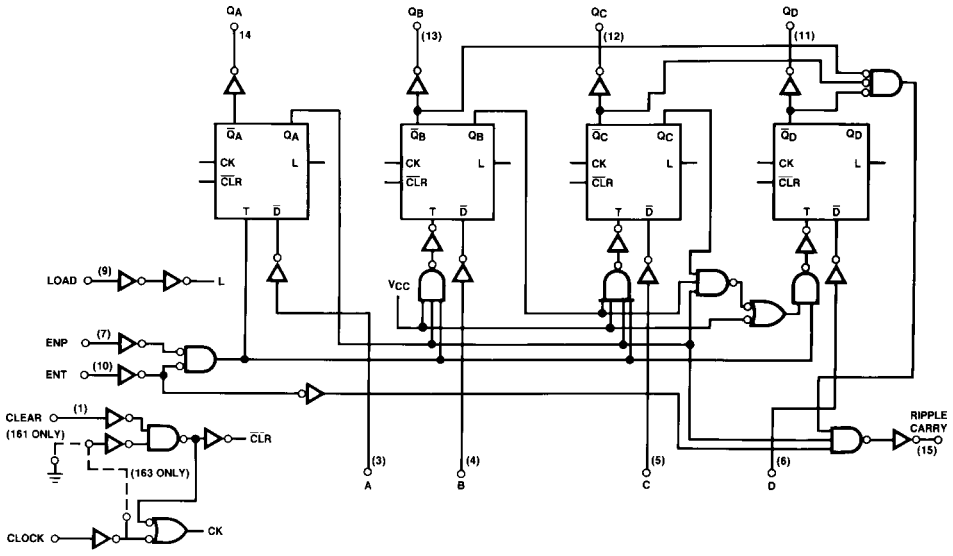
| CLK | CLR | ENP | ENT | Load | Function |
|---|---|---|---|---|---|
| X | L | X | X | X | Clear |
| X | H | H | L | H | Count & RC disabled |
| X | H | L | H | H | Count disabled |
| X | H | L | L | H | Count & RC disabled |
| ↑ | H | X | X | L | Load |
| ↑ | H | H | H | H | Increment Counter |

**MM74HC163**

| CLK | CLR | ENP | ENT | Load | Function |
|---|---|---|---|---|---|
| ↑ | L | X | X | X | Clear |
| X | H | H | L | H | Count & RC disabled |
| X | H | L | H | H | Count disabled |
| X | H | L | L | H | Count & RC disabled |
| ↑ | H | X | X | L | Load |
| ↑ | H | H | H | H | Increment Counter |

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = LOW-to-HIGH Transition

## Logic Diagram



## Absolute Maximum Ratings(Note 2)

(Note 3)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$+1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$+0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 4) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature | |
| ($T_L$) (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input or Output Voltage | 0 | $V_{CC}$ | V |
| ($V_{IN}$, $V_{OUT}$) | | | |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |
| Input Rise or Fall Times | | | |
| ($t_r$, $t_f$) $V_{CC}$ = 2.0V | | 1000 | ns |
| $V_{CC}$ = 4.5V | | 500 | ns |
| $V_{CC}$ = 6.0V | | 400 | ns |

**Note 2:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 3:** Unless otherwise specified all voltages are referenced to ground.

**Note 4:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0V | | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $\|I_{OUT}\| \le 20$ μA | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $\|I_{OUT}\| \le 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | |
| | | $\|I_{OUT}\| \le 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | V |
| | | $\|I_{OUT}\| \le 20$ μA | 2.0V | 0 | 0.1 | 0.1 | 0.1 | |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $\|I_{OUT}\| \le 4.0$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | |
| | | $\|I_{OUT}\| \le 5.2$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | 8.0 | 80 | 160 | μA |
| | | $I_{OUT}$ = 0 μA | | | | | | |

**Note 5:** For a power supply of 5V ± 10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF, $t_r = t_f$ = 6 ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | | 43 | 30 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Clock to RC | | 30 | 35 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Clock to Q | | 29 | 34 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, ENT to RC | | 18 | 32 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Clear to Q or RC | | 27 | 38 | ns |
| $t_{REM}$ | Minimum Removal Time, Clear to Clock | | 10 | 20 | ns |
| $t_S$ | Minimum Set Up Time Clear, Load, Enable or Data to Clock | | | 30 | ns |
| $t_H$ | Minimum Hold Time, Data from Clock | | | 5 | ns |
| $t_W$ | Minimum Pulse Width Clock, Clear, or Load | | | 16 | ns |

## AC Electrical Characteristics

$C_L$ = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $f_{MAX}$ | Maximum Operating Frequency | | 2.0V | 10 | 5 | 4 | 4 | MHz |
| | | | 4.5V | 40 | 27 | 21 | 18 | |
| | | | 6.0V | 45 | 32 | 25 | 21 | |
| $t_{PHL}$ | Maximum Propagation Delay, Clock to RC | | 2.0V | 100 | 215 | 271 | 320 | ns |
| | | | 4.5V | 32 | 43 | 54 | 64 | |
| | | | 6.0V | 28 | 37 | 46 | 54 | |
| $t_{PLH}$ | Maximum Propagation Delay, Clock to RC | | 2.0V | 88 | 175 | 220 | 260 | ns |
| | | | 4.5V | 18 | 35 | 44 | 52 | |
| | | | 6.0V | 15 | 30 | 37 | 44 | |
| $t_{PHL}$ | Maximum Propagation Delay, Clock to Q | | 2.0V | 95 | 205 | 258 | 305 | ns |
| | | | 4.5V | 30 | 41 | 52 | 61 | |
| | | | 6.0V | 26 | 35 | 44 | 52 | |
| $t_{PLH}$ | Maximum Propagation Delay, Clock to Q | | 2.0V | 85 | 170 | 214 | 253 | ns |
| | | | 4.5V | 17 | 34 | 43 | 51 | |
| | | | 6.0V | 14 | 29 | 36 | 43 | |
| $t_{PHL}$ | Maximum Propagation Delay, ENT to RC | | 2.0V | 90 | 195 | 246 | 291 | ns |
| | | | 4.5V | 28 | 39 | 49 | 58 | |
| | | | 6.0V | 24 | 33 | 42 | 49 | |
| $t_{PLH}$ | Maximum Propagation Delay, ENT to RC | | 2.0V | 80 | 160 | 202 | 238 | ns |
| | | | 4.5V | 16 | 32 | 40 | 48 | |
| | | | 6.0V | 14 | 27 | 34 | 41 | |
| $t_{PHL}$ | Maximum Propagation Delay, Clear to RC | | 2.0V | 100 | 220 | 275 | 325 | ns |
| | | | 4.5V | 32 | 44 | 55 | 66 | |
| | | | 6.0V | 28 | 37 | 47 | 55 | |
| $t_{PHL}$ | Maximum Propagation Delay, Clear to Q | | 2.0V | 100 | 210 | 260 | 315 | ns |
| | | | 4.5V | 32 | 42 | 52 | 63 | |
| | | | 6.0V | 28 | 36 | 45 | 54 | |
| $t_{REM}$ | Minimum Removal Time Clear to Clock | | 2.0V | | 125 | 158 | 186 | ns |
| | | | 4.5V | | 25 | 32 | 37 | |
| | | | 6.0V | | 21 | 27 | 32 | |
| $t_S$ | Minimum Setup Time Clear or Data to Clock | | 2.0V | | 150 | 190 | 225 | ns |
| | | | 4.5V | | 30 | 38 | 45 | |
| | | | 6.0V | | 26 | 32 | 38 | |
| $t_S$ | Minimum Setup Time Load to Clock | | 2.0V | | 135 | 170 | 200 | ns |
| | | | 4.5V | | 27 | 34 | 41 | |
| | | | 6.0V | | 23 | 29 | 35 | |

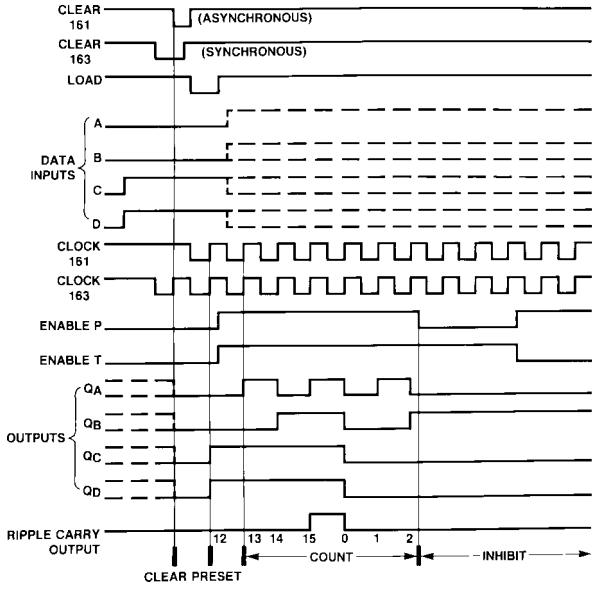
## AC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A = 25°C$ | $T_A = -40$ to $85°C$ | $T_A = -55$ to $125°C$ | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $t_S$ | Minimum Setup | | 2.0V | | 175 | 220 | 260 | |
| | Time Enable | | 4.5V | | 35 | 44 | 52 | ns |
| | to Clock | | 6.0V | | 30 | 37 | 44 | |
| $t_H$ | Minimum Hold Time | | 2.0V | | 50 | 63 | 75 | |
| | Data from Clock | | 4.5V | | 10 | 13 | 15 | ns |
| | | | 6.0V | | 9 | 11 | 13 | |
| $t_H$ | Minimum Hold Time | | 2.0V | | 0 | 0 | 0 | |
| | Enable, Load or Clear | | 4.5V | | 0 | 0 | 0 | ns |
| | to Clock | | 6.0V | | 0 | 0 | 0 | |
| $t_W$ | Minimum Pulse Width | | 2.0V | | 80 | 100 | 120 | |
| | Clock, Clear, or | | 4.5V | | 16 | 20 | 24 | ns |
| | Load | | 6.0V | | 14 | 17 | 20 | |
| $t_{TLH}$, $t_{THL}$ | Maximum | | 2.0V | 40 | 75 | 95 | 110 | |
| | Output Rise and | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | Fall Time | | 6.0V | 7 | 13 | 16 | 19 | |
| $t_r$, $t_f$ | Maximum Input Rise | | 2.0V | | 1000 | 1000 | 1000 | |
| | and Fall Time | | 4.5V | 500 | 500 | 500 | 500 | ns |
| | | | 6.0V | | 400 | 400 | 400 | |
| $C_{PD}$ | Powert Dissipation | (per package) | | 90 | | | | pF |
| | Capacitance (Note 6) | | | | | | | |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

**Note 6:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

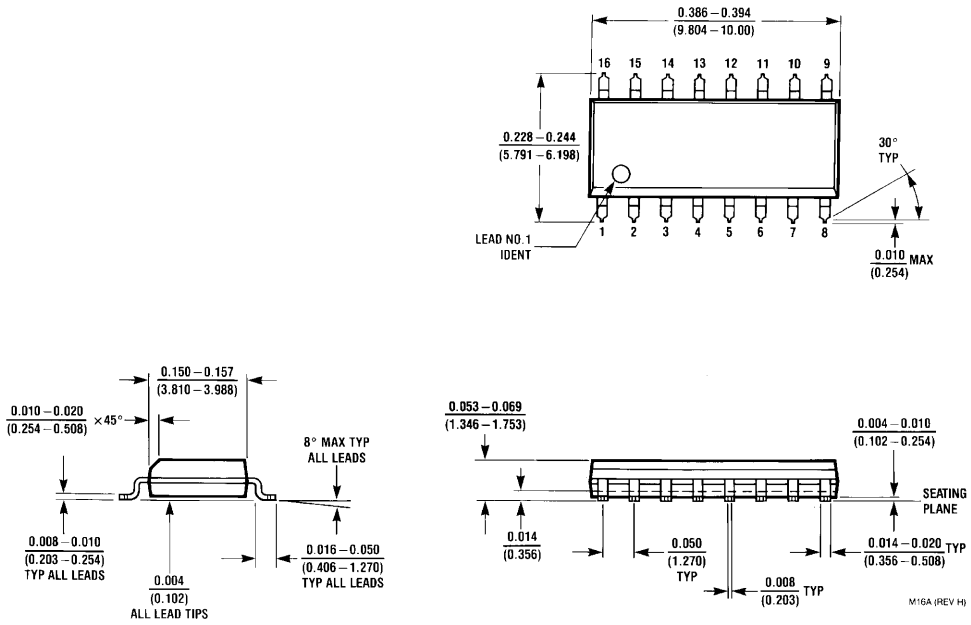
## Logic Waveforms

**Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences**



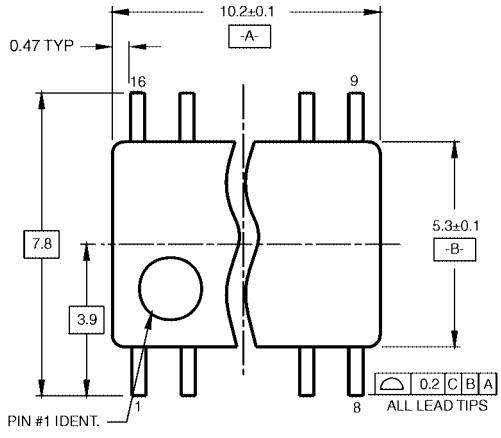

**Sequence:** (1) Clear outputs to zero (2) Preset to binary twelve (3) Count to thirteen, fourteen, fifteen, zero, one and two (4) Inhibit

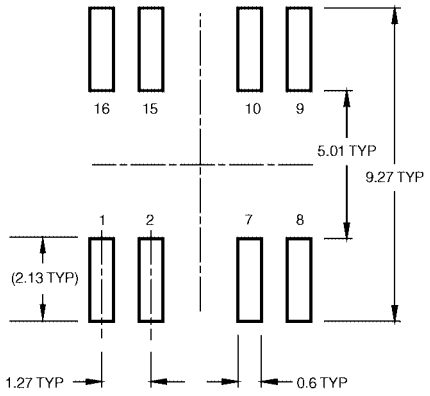
## Physical Dimensions inches (millimeters) unless otherwise noted



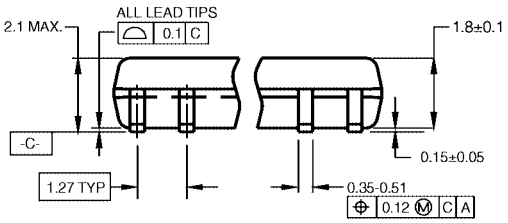

**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M16A**

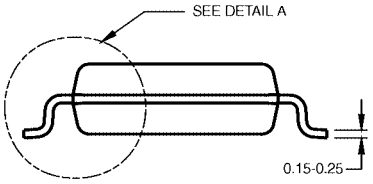
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




LAND PATTERN RECOMMENDATION




DIMENSIONS ARE IN MILLIMETERS

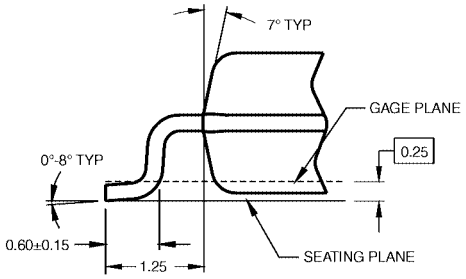
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

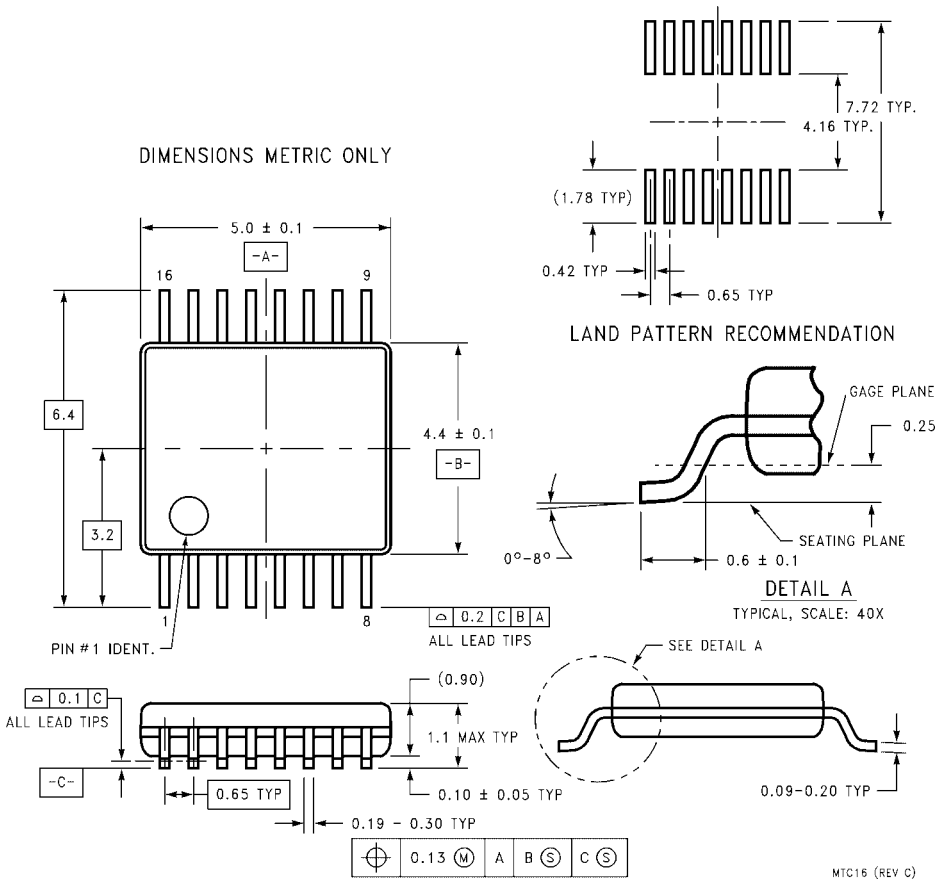
M16DRevB1




DETAIL A

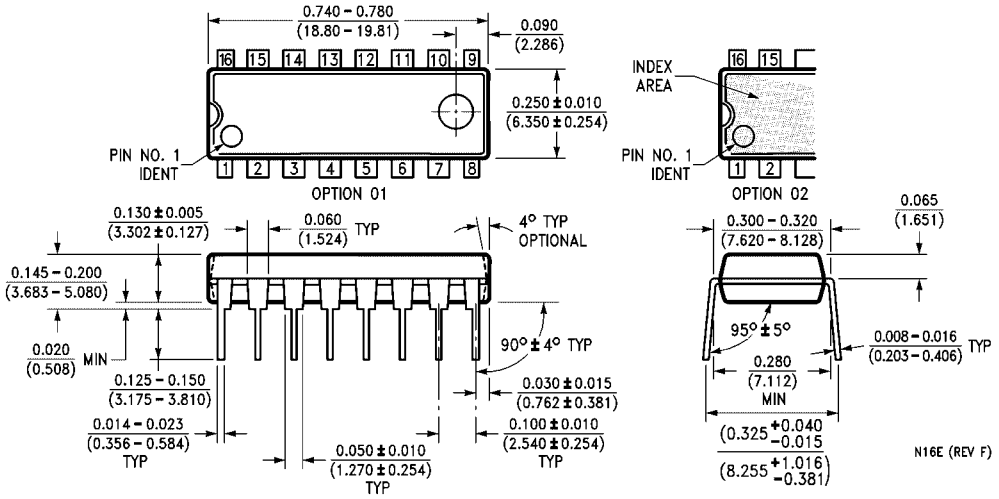
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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