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FAIRCHILD SEMICONDUCTOR®

February 2008

MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

Features

- Typical operating frequency: 50MHz
- Typical propagation delay: 19ns (clock to Q)
- Wide operating supply voltage range: 2V to 6V
- Low input current: 1µA maximum
- Low quiescent supply current: 80µA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

General Description

The MM74HC164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

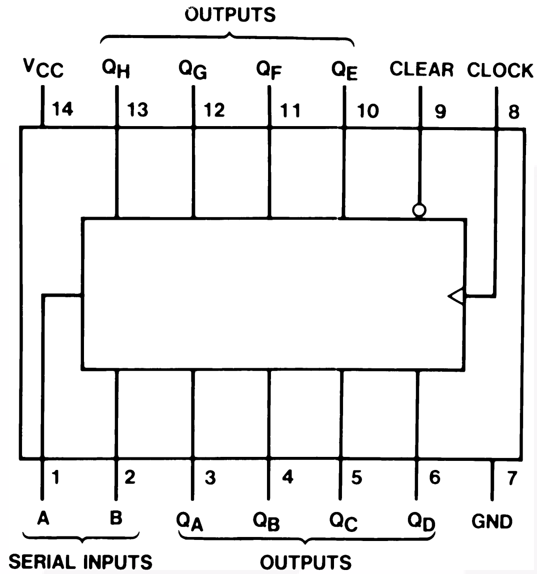
Ordering Information

Order Number	Package Number	Package Description
MM74HC164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC164MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Top View

Truth Table

Inputs				Outputs	
Clear	Clock	A	B	Q_A	Q_B … Q_H
L	X	X	X	L	L … L
H	L	X	X	Q_{AO}	Q_{BO} … Q_{HO}
H	↑	H	H	H	Q_{An} … Q_{Gn}
H	↑	L	X	L	Q_{A} … Q_{Gn}
H	↑	X	L	L	Q_{An} … Q_{Gn}

H = HIGH Level (steady state)

L = LOW Level (steady state)

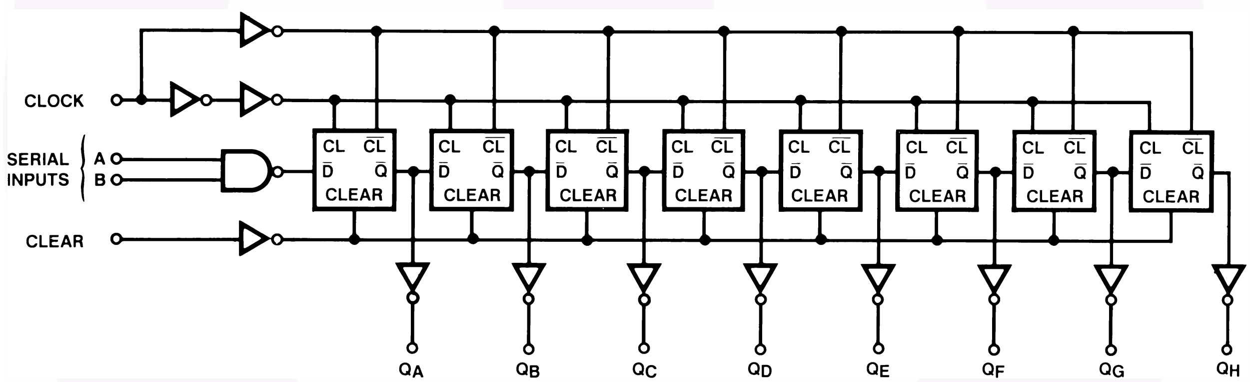
X = Irrelevant (any input, including transitions)

↑ = Transition from LOW-to-HIGH level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC}+1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic "N" package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics[3]

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$		$T_A = –40°C$ to 85°C	$T_A = –55°C$ to 125°C	Units
				Typ.	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	2.0			1.5	1.5	1.5	V
		4.5			3.15	3.15	3.15	
		6.0			4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage	2.0			0.5	0.5	0.5	V
		4.5			1.35	1.35	1.35	
		6.0			1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\mu A$	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0mA$	4.2	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 5.2mA$	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\mu A$	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0mA$	0.2	0.26	0.33	0.4	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 5.2mA$	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		8.0	80	160	µA

Note:

3. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		19	30	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		23	35	ns
t_{REM}	Minimum Removal Time, Clear to Clock		–2	0	ns
t_S	Minimum Setup Time, Data to Clock		12	20	ns
t_H	Minimum Hold Time, Clock to Data		1	5	ns
t_W	Minimum Pulse Width, Clear or Clock		10	16	ns

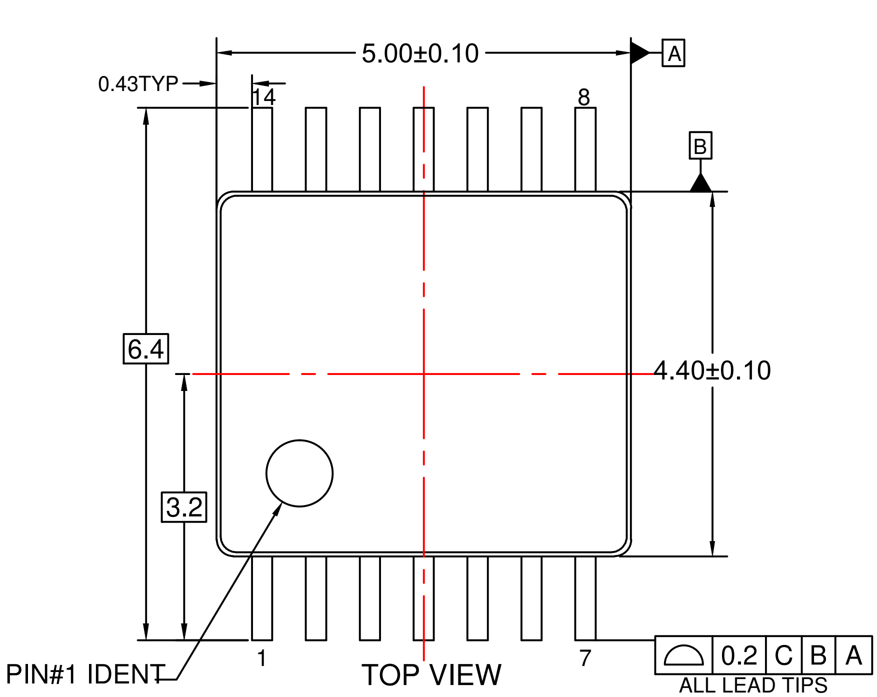
AC Electrical Characteristics

$C_L = 50pF$, $t_r = t_f = 6ns$ (unless otherwise specified)

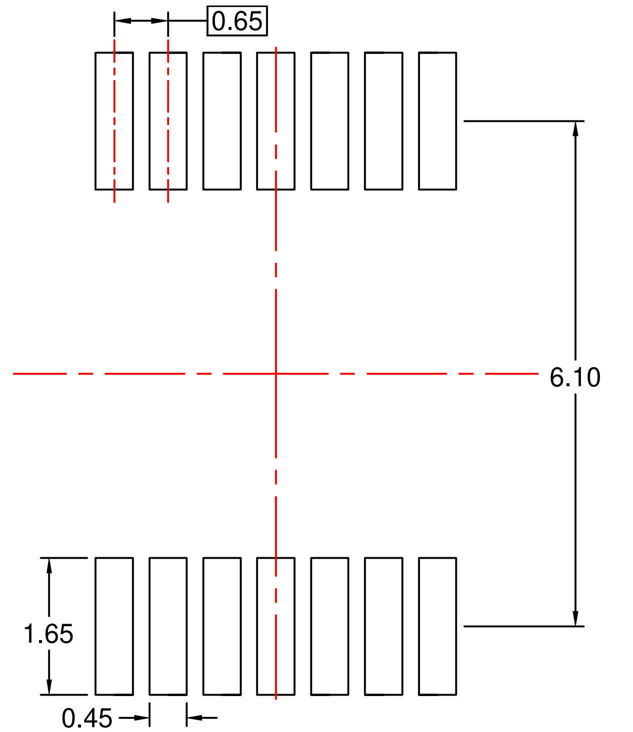
				$T_A = 25°C$		$T_A = –40°C$ to 85°C	$T_A = –55°C$ to 125°C	
Symbol	**Parameter**	**V_{CC} (V)**	**Conditions**	**Typ.**	**Guaranteed Limits**			**Units**
f_{MAX}	Maximum Operating Frequency	2.0			5	4	3	MHz
		4.5			27	21	18	
		6.0			31	24	20	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output	2.0		115	175	218	254	ns
		4.5		13	35	44	51	
		6.0		20	30	38	44	
t_{PHL}	Maximum Propagation Delay, Clear to Output	2.0		140	205	256	297	ns
		4.5		28	41	51	59	
		6.0		24	35	44	51	
t_{REM}	Minimum Removal Time, Clear to Clock	2.0		–7	0	0	0	ns
		4.5		–3	0	0	0	
		6.0		–2	0	0	0	
t_S	Minimum Setup Time, Data to Clock	2.0		25	100	125	150	ns
		4.5		14	20	25	30	
		6.0		12	17	21	25	
t_H	Minimum Hold Time, Clock to Data	2.0		–2	5	5	5	ns
		4.5		0	5	5	5	
		6.0		1	5	5	5	
t_W	Minimum Pulse Width Clear or Clock	2.0		22	80	100	120	ns
		4.5		11	16	20	24	
		6.0		10	14	18	20	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	2.0			75	95	110	ns
		4.5			15	19	22	
		6.0			13	16	19	
t_r, t_f	Maximum Input Rise and Fall Time	2.0			1000	1000	1000	ns
		4.5			500	500	500	
		6.0			400	400	400	
C_{PD}	Power Dissipation Capacitance(4)	5.0	(per package)	150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

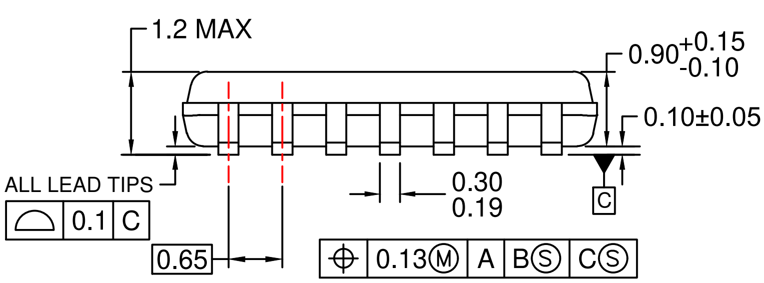
4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



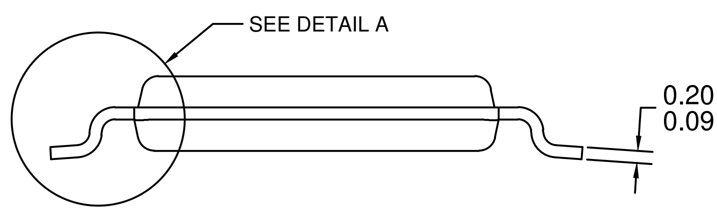
TOP VIEW

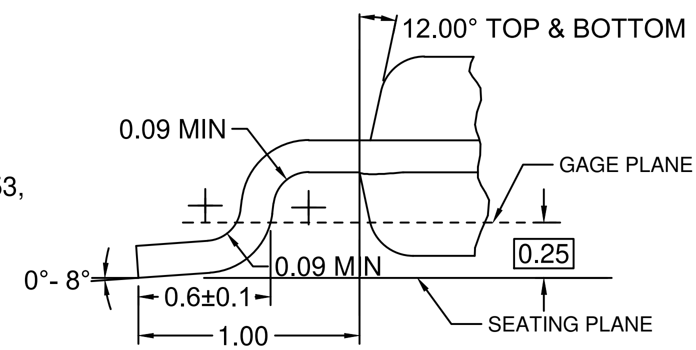


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

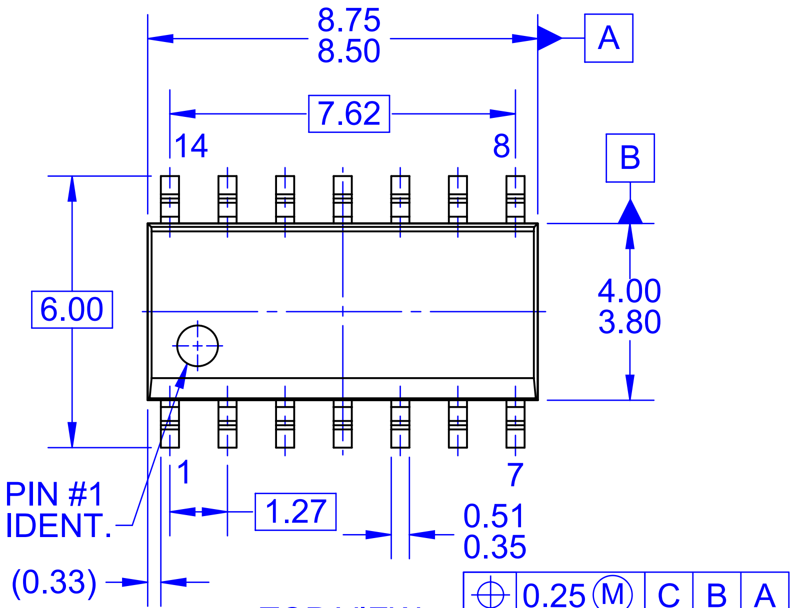
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

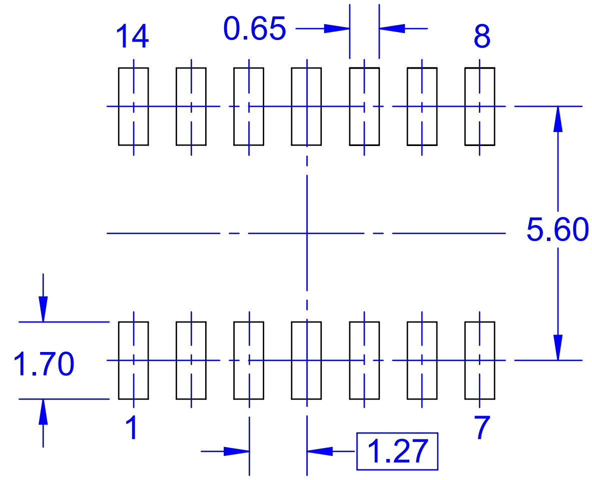
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

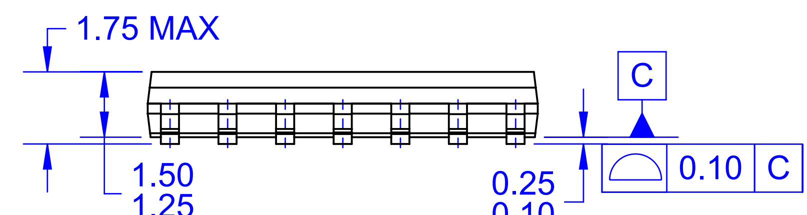
F. DRAWING FILE NAME: MKT-MTC14rev7.



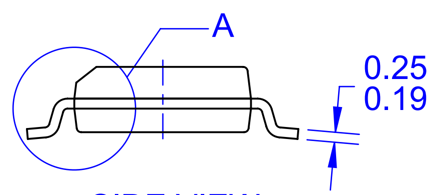
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C

B. ALL DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS

D. LAND PATTERN STANDARD: SOIC127P600X145-14M

E. CONFORMS TO ASME Y14.5M, 2009

D. DRAWING FILENAME: MKT-M14Arev14

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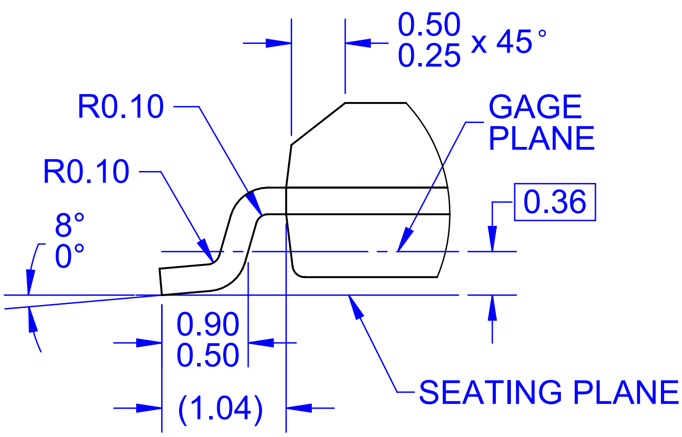

DETAIL A
SCALE 16 : 1

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