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September 1983
Revised May 2005

MM74HC373
3-STATE Octal D-Type Latch

General Description

The MM74HC373 high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

Top View
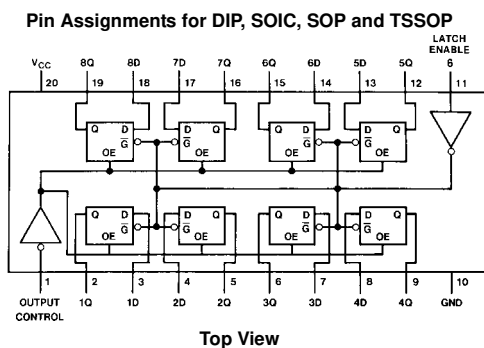
Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
Q_0 = Level of output before steady-state input conditions were established.
Z = High Impedance

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $|I_{OUT}| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL} $|I_{OUT}| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $|I_{OUT}| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $|I_{OUT}| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}, OC = V_{IH} $V_{OUT} = V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	6.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.
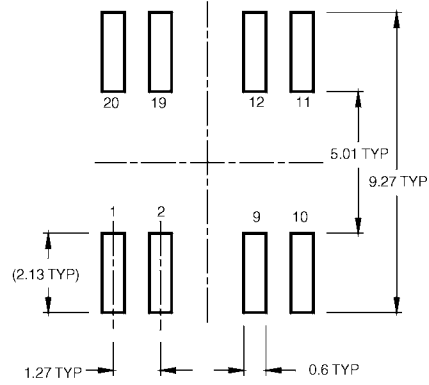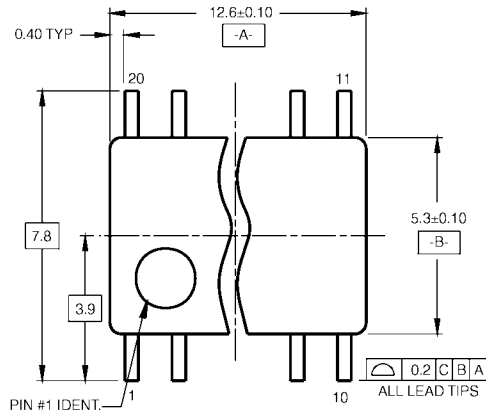
AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L = 45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L = 45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics

$V_{CC} = 2.0–6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	$T_A = -40$ to $85°C$ Guaranteed Limits	$T_A = -55$ to $125°C$ Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L = 50$ pF	2.0V	50	150	188	225	ns
		$C_L = 150$ pF	2.0V	80	200	250	300	ns
		$C_L = 50$ pF	4.5V	22	30	37	45	ns
		$C_L = 150$ pF	4.5V	30	40	50	60	ns
		$C_L = 50$ pF	6.0V	19	26	31	39	ns
		$C_L = 150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L = 50$ pF	2.0V	63	175	220	263	ns
		$C_L = 150$ pF	2.0V	110	225	280	338	ns
		$C_L = 50$ pF	4.5V	25	35	44	52	ns
		$C_L = 150$ pF	4.5V	35	45	56	68	ns
		$C_L = 50$ pF	6.0V	21	30	37	45	ns
		$C_L = 150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	50	150	188	225	ns
		$C_L = 150$ pF	2.0V	80	200	250	300	ns
		$C_L = 50$ pF	4.5V	21	30	37	45	ns
		$C_L = 150$ pF	4.5V	30	40	50	60	ns
		$C_L = 50$ pF	6.0V	19	26	31	39	ns
		$C_L = 150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ	2.0V	50	150	188	225	ns
		$C_L = 50$ pF	4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V		50	60	75	ns
			4.5V		9	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch) OC = V_{CC}		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8 9 10

30° TYP

0.010 MAX
(0.254)

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10

-A-

0.40 TYP

20

11

7.8

5.3±0.10

-B-

3.9

PIN #1 IDENT.

1

10

0.2 C B A

ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

20 19

12 11

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2

9   10

1.27 TYP

0.6 TYP

ALL LEAD TIPS

0.1 C

2.1 MAX.

1.8±0.1

-C-

0.15±0.05

1.27 TYP

0.35-0.51

0.12 M C A

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-

-0.20

20   11

-C-

6.4   4.4±0.1 -B-

3.2

PIN #1 IDENT.

1   10

⌀ 0.2 C B A
ALL LEAD TIPS

4.16   7.72

1.78

0.65   0.42

LAND PATTERN RECOMMENDATION

⌀ 0.1 C
ALL LEAD TIPS

0.90 +0.15 −0.10

1.2 max

-C-   0.1±0.05

0.65

0.19−0.30
⊕ 0.10 Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09−0.20

12.00°

R0.09min   GAGE PLANE

0 − 8°   SEATING PLANE

0.25

0.6±0.1   R0.09min

1.00
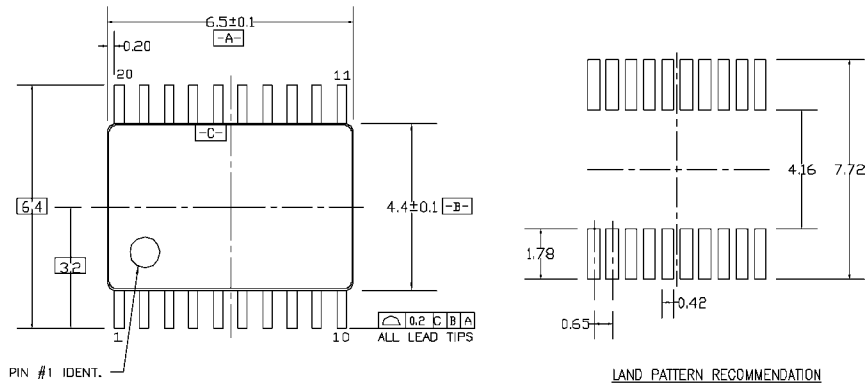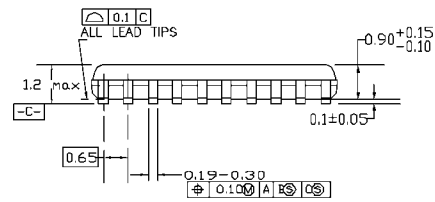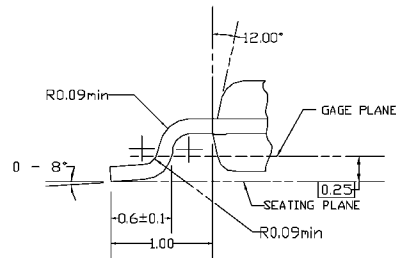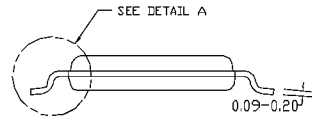
DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,
   REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,
   AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
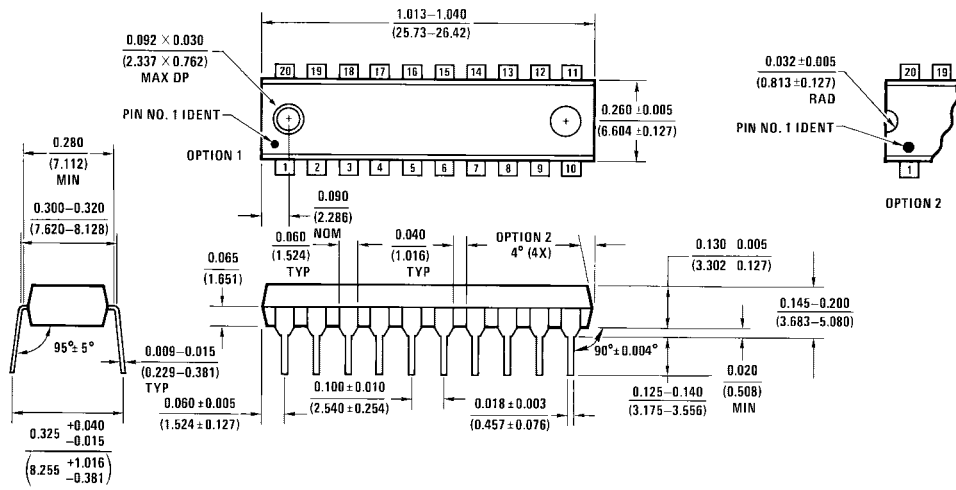
20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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