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FAIRCHILD
SEMICONDUCTOR™

September 1983
Revised January 2005

MM74HC393
Dual 4-Bit Binary Counter

General Description

The MM74HC393 counter circuits contain independent ripple carry counters and utilize advanced silicon-gate CMOS technology. The MM74HC393 contains two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the HIGH-to-LOW transition (negative edge) of the clock input, and each has an independent clear input. When clear is set HIGH all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. This counter is functionally as well as pin equivalent to the 74LS393. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

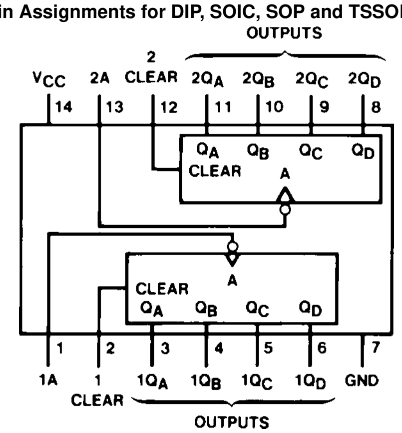
Ordering Code:

Order Number	Package Number	Package Description
MM74HC393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC393SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC393MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC393N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Absolute Maximum Ratings

(Note 2)
(Note 1)

Supply Voltage (V_{CC})	–0.5 to +7.0V
DC Input Voltage (V_{IN})	–1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	–0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	–40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic “N” package: –12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = –40 to 85°C	T_A = –55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\ \mu A$	6.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_B		19	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C		23	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_D		27	50	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		15	28	ns
t_{REM}	Minimum Removal Time		−2	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

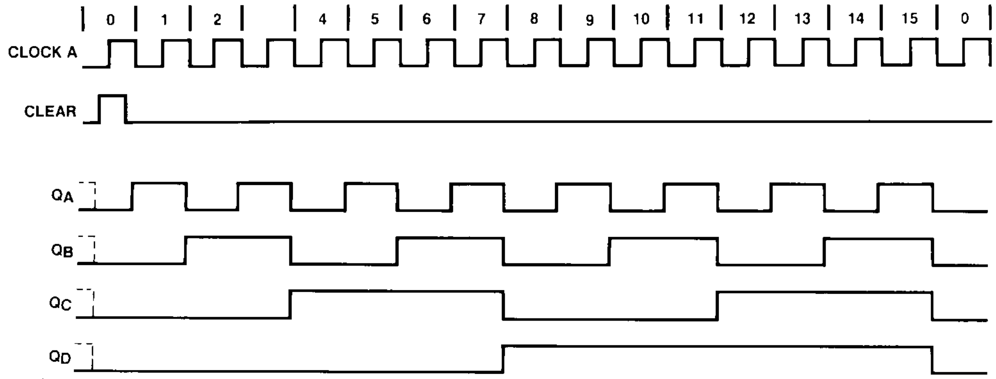
AC Electrical Characteristics

$C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

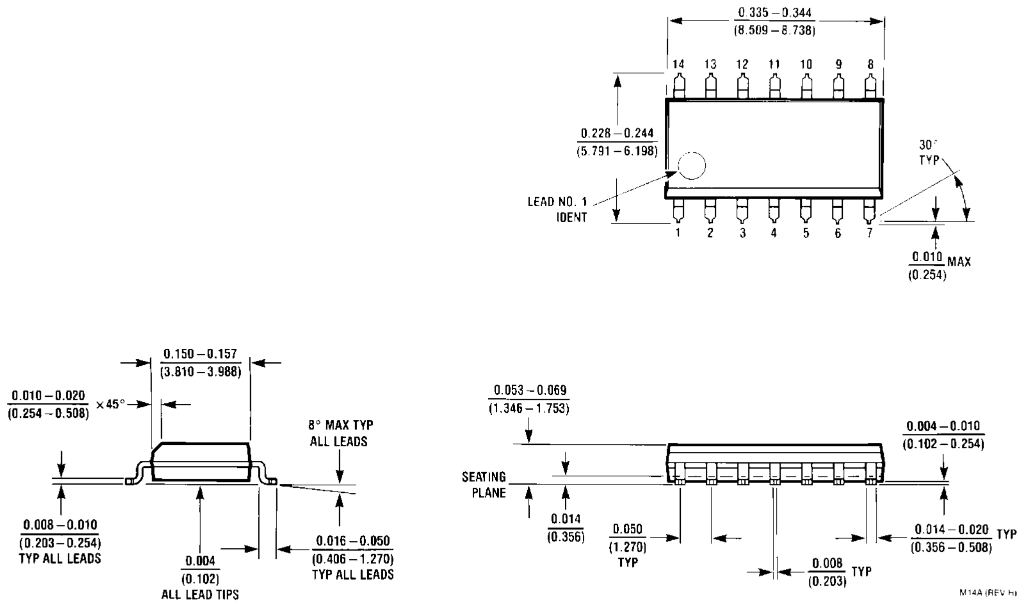
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		$T_A = -40$ to 85°C	$T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating		2.0V		5	4	3	
	Frequency		4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation		2.0V	45	120	150	180	ns
	Delay Clock A to Q_A		4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation		2.0V	68	190	240	285	ns
	Delay Clock A to Q_B		4.5V	23	38	47	57	ns
			6.0V	20	32	40	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation		2.0V	90	240	300	360	ns
	Delay Clock A to Q_C		4.5V	30	48	60	72	ns
			6.0V	26	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	100	290	360	430	ns
	Clock to Q_D		4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}	Maximum Propagation		2.0V	54	165	210	250	ns
	Delay Clear to any Q		4.5V	18	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Clear		2.0V		25	25	25	ns
	Removal Time		4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
	Clear or Clock		4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output		2.0V	30	75	95	110	ns
	Rise and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input				1000	1000	1000	ns
	Rise and Fall Time				500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation	(per counter)		42				pF
	Capacitance (Note 5)							
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2 f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC} f + I_{CC}$.

Logic Timing Waveforms

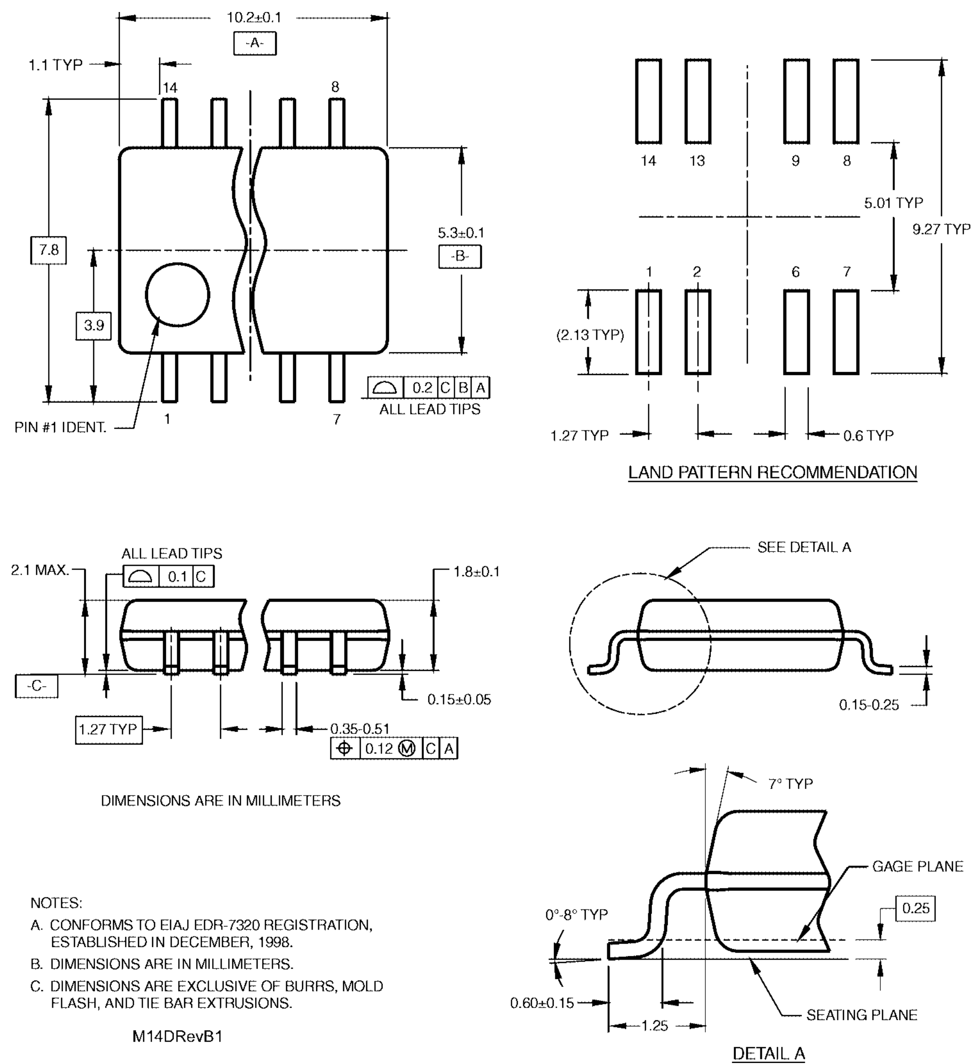


Physical Dimensions inches (millimeters) unless otherwise noted



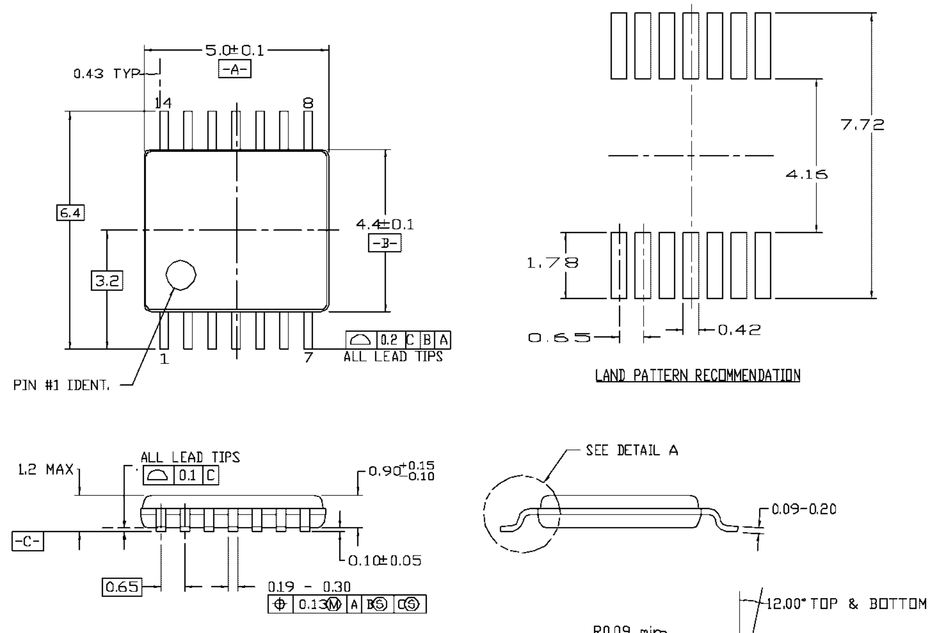
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

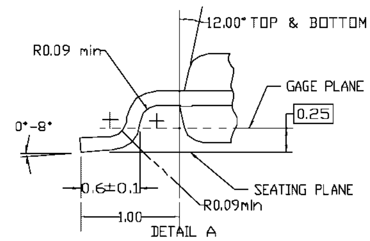
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

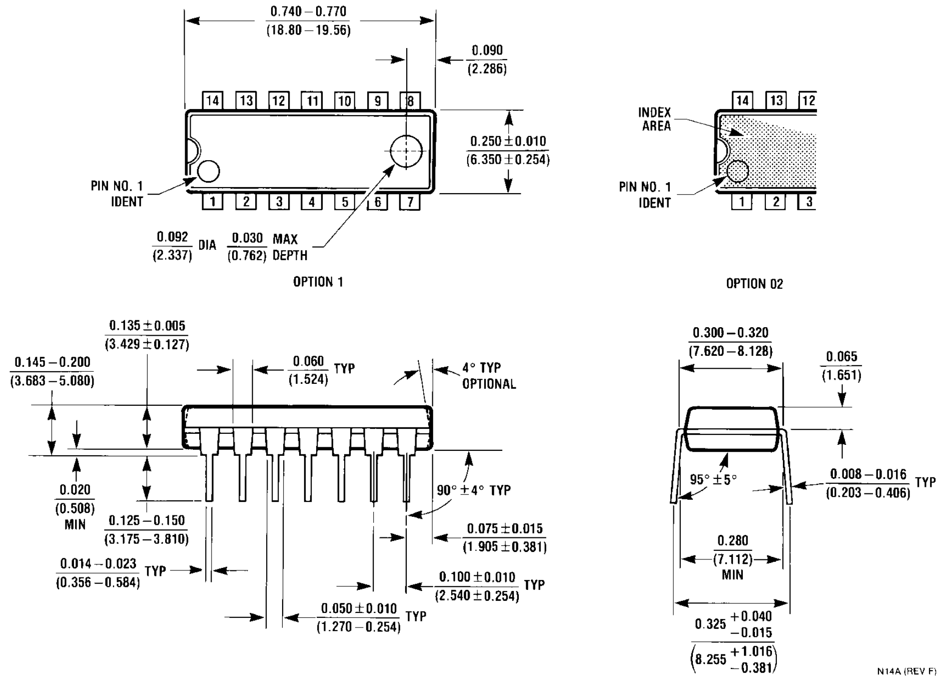
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A