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FAIRCHILD

SEMICONDUCTOR TM

February 1984 Revised December 2003

MM74HC4020 • MM74HC4040 14-Stage Binary Counter • 12-Stage Binary Counter

General Description

The MM74HC4020, MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4020 is a 14 stage counter and the MM74HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to $\rm V_{CC}$ and ground.

Features

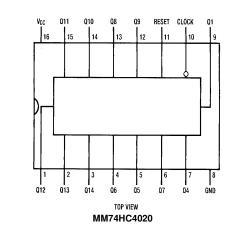
- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

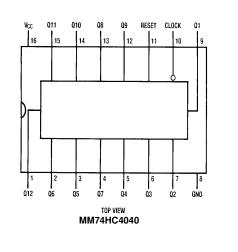
Ordering Code:

Order Number	Package Number	Package Description
MM74HC4020M (Note 1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4020SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4020N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC4040M (Note 1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4040SJ (Note 1)	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4040MTC (Note 1)	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4040N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

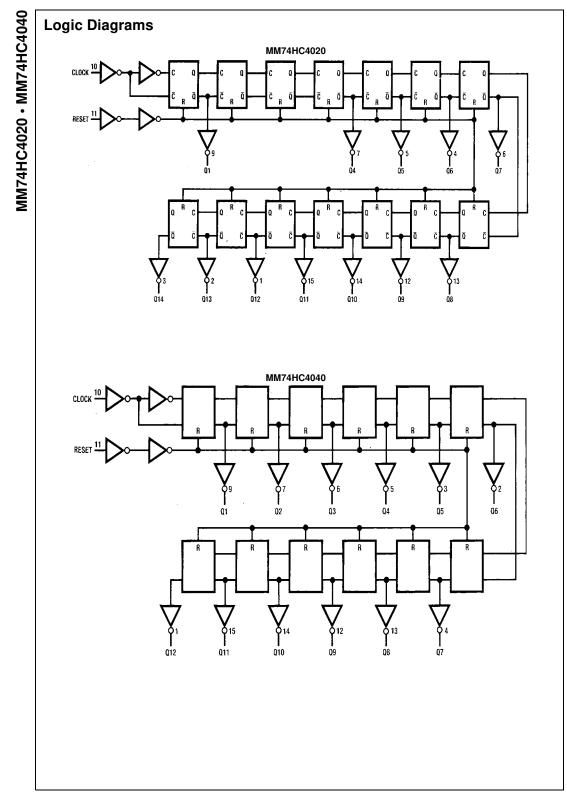
Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams





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Absolute Maximum Ratings(Note 2)

Recommended	Operating
Conditions	

	•
(Note 3)	
Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to $V_{CC}{+}1.5V$
DC Output Voltage (V _{OUT})	–0.5 to V_{CC} +0.5V
Clamp Diode Current (I _{CD})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P _D)	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature (T _L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions					
	Min	Max	Units		
Supply Voltage (V _{CC})	2	6	V		
DC Input or Output Voltage	0	V_{CC}	V	Ì	
(V _{IN} , V _{OUT})					
Operating Temperature Range (T_A)	-40	+85	°C		
Input Rise or Fall Times					
$(t_r, t_f) V_{CC} = 2.0 V$		1000	ns	1	
$V_{CC} = 4.5V$		500	ns		
$V_{CC} = 6.0V$		400	ns		
Note 2: Maximum Ratings are those values device may occur.	beyond w	/hich dama	ge to the		

Note 3: Unless otherwise specified all voltages are referenced to ground.

Note 4: Power Dissipation temperature derating - plastic "N" package: -12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	v _{cc}	$T_A = 25^{\circ}C$		$T_{A}=-40$ to $85^{\circ}C$	$T_A = -55$ to $125^{\circ}C$	Units
Symbol			• 66	Тур	Guaranteed L		imits	
VIH	Minimum HIGH Level Input		2.0V		1.5	1.5	1.5	
	Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	
VIL	Maximum LOW Level Input		2.0V		0.5	0.5	0.5	
	Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	
			4.5V	4.5	4.4	4.4	4.4	
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	
		I _{OUT} ≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	
V _{OL}	Maximum LOW Level Output	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	
			4.5V	0	0.1	0.1	0.1	
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	.26	0.33	0.4	
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	.26	0.33	0.4	
I _{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μA
	Current	$I_{OUT} = 0 \ \mu A$						

Note 5: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current value at 5.5V is 3.85V.) rent (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

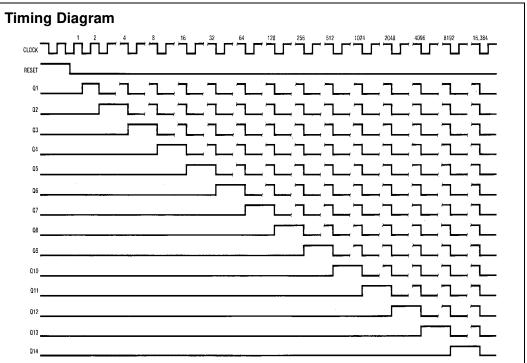
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency		50	30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to Q	(Note 6)	17	35	ns
t _{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t _{REM}	Minimum Reset Removal Time		10	20	ns
tw	Minimum Pulse Width		10	16	ns

Note 6: Typical Propagation delay time to any output can be calculated using: $t_P = 17 + 12(N-1)$ ns; where N is the number of the output, Q_W , at $V_{CC} = 5V$.

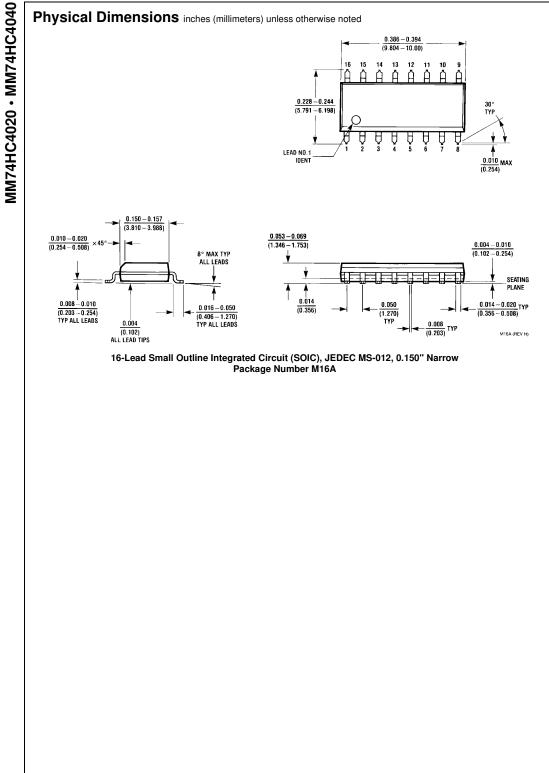
Type Guaranteed Limits f_{MAX} Maximum Operating Frequency 2.0V 10 6 5 f_{MAX} Maximum Operating Frequency 2.0V 4.5V 40 30 24 2 f_{PHL} , f_{PLH} Maximum Propagation Delay Clock to Q_1 2.0V 80 210 265 3 f_{PHL} , f_{PLH} Maximum Propagation Delay Between Stages 4.5V 21 42 53 6 f_{PHL} , f_{PLH} Maximum Propagation Delay Between Stages 4.5V 18 36 45 45 f_{PHL} , f_{PLH} Maximum Propagation Delay Reset to any Q 2.0V 72 240 302 33 f_{PHL} Maximum Propagation (4020 and 4040) 2.0V 72 240 302 33 f_{REM} Minimum Reset Removal Time 2.0V 100 126 11 f_{TLH} Minimum Pulse Width 2.0V 90 1000 11 f_{VW} Minimum Pulse Width 2.0V 30 75 95 1<	Symbol	Parameter	Conditions	V _{cc}	$T_A = 25^{\circ}C$		$T_A = -40$ to $85^{\circ}C$	$T_A = -55$ to $125^{\circ}C$	Units
Frequency Frequency 4.5V 40 30 24 24 tpHL, tpLH Maximum Propagation 2.0V 80 210 265 33 tpHL, tpLH Maximum Propagation 2.0V 80 211 42 53 60 tpHL, tpLH Maximum Propagation 2.0V 80 125 156 11 Delay Clock to Q1 4.5V 18 36 45 45 45 tpHL, tpLH Maximum Propagation 2.0V 80 125 156 11 Delay Between Stages 4.5V 18 25 31 33 33 tpHL Maximum Propagation 2.0V 72 240 302 33 Delay Reset to any Q 4.5V 24 48 60 34 36 tqHA Minimum Reset 2.0V 72 240 302 35 tqEA 6.0V 100 126 1 36 tqEA 6.0V <					Тур		Guaranteed Limits		
Image: second	мах	Maximum Operating		2.0V	10	6	5	4	
tp _{HL} , tp _{LH} Maximum Propagation Delay Clock to Q1 2.0V 80 210 265 33 tp _{HL} , tp _{LH} Delay Clock to Q1 4.5V 21 42 53 6 tp _{HL} , tp _{LH} Maximum Propagation Delay Between Stages from Qn to Qn+1 2.0V 80 125 156 1 Delay Between Stages from Qn to Qn+1 6.0V 15 21 26 31 32 tp _{HL} Maximum Propagation Delay Reset to any Q 2.0V 72 240 302 33 tq _{HL} Maximum Propagation (4020 and 4040) 2.0V 72 240 302 33 tq _{EM} Minimum Reset Removal Time 2.0V 100 126 1 tq _L Femoval Time 4.5V 20 25 9 tt Minimum Pulse Width 2.0V 90 100 1 t_TLH, tT _{HL} Maximum 2.0V 30 75 95 1 output Rise and Fall Time 6.0V 9 13 16 1		Frequency		4.5V	40	30	24	20	MHz
Internation Delay Clock to Q1 4.5V 21 42 53 60 tpHL, tpLH Maximum Propagation 2.0V 80 125 156 1 Delay Between Stages 4.5V 18 25 31 3 tpHL, tpLH Maximum Propagation 2.0V 80 125 156 1 Delay Between Stages 4.5V 18 25 31 3 3 tpHL Maximum Propagation 2.0V 72 240 302 3 Delay Reset to any Q 4.5V 24 48 60 3 (4020 and 4040) 6.0V 20 41 51 0 tqEM Minimum Reset 2.0V 100 126 1 Removal Time 4.5V 20 25 3 tw Minimum Pulse Width 2.0V 90 100 1 trut, tTLH, tTHL Maximum 2.0V 30 75 95 1 output Rise <td></td> <td></td> <td></td> <td>6.0V</td> <td>50</td> <td>35</td> <td>28</td> <td>24</td> <td></td>				6.0V	50	35	28	24	
Image:	t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	80	210	265	313	
tp _{HL} , tp _{LH} Maximum Propagation Delay Between Stages from Q _n to Q _{n+1} 2.0V 80 125 156 1 tp _{HL} , tp _{LH} Delay Between Stages from Q _n to Q _{n+1} 6.0V 15 21 26 31 32 tp _{HL} Maximum Propagation (4020 and 4040) 2.0V 72 240 302 33 tq _{EM} Minimum Reset Removal Time 2.0V 72 240 302 33 tq _{EM} Minimum Reset Removal Time 2.0V 20 41 51 60 tw Minimum Pulse Width 2.0V 200 25 90 100 126 1 true, true, true, true, true, true, true, true, true Maximum 2.0V 90 100 1 del col 2.0V 30 75 95 1 Output Rise and Fall Time 6.0V 9 13 16 1 CpD Power Dissipation (per package) 55 400 400 400		Delay Clock to Q1		4.5V	21	42	53	63	ns
Internation Delay Between Stages 4.5V 18 25 31 31 from Qn to Qn+1 6.0V 15 21 26 33 tpHL Maximum Propagation (4020 and 4040) 2.0V 72 240 302 33 tqHL Minimum Propagation (4020 and 4040) 2.0V 72 240 302 33 tqEM Minimum Reset Removal Time 2.0V 20 41 51 60 tw Minimum Pulse Width 2.0V 20 25 34 tw Minimum Pulse Width 2.0V 90 100 1 truth, tTHL Maximum 2.0V 90 100 1 doutput Rise and Fall Time 4.5V 10 15 19 2 tr, t ₁ Maximum Input Rise and Fall Time 1000 1000 1100 1000 1000 1000 t ₂ Power Dissipation (per package) 55 400 400 400 400				6.0V	18	36	45	53	
from Qn to Qn+1 6.0V 15 21 26 302 332 tpHL Maximum Propagation Delay Reset to any Q (4020 and 4040) 2.0V 72 240 302 33 tqEM Minimum Reset Removal Time 2.0V 20 41 51 60 tqEM Minimum Reset Removal Time 2.0V 100 126 1 tw Minimum Pulse Width 2.0V 20 25 2 tw Minimum Pulse Width 2.0V 90 100 1 tr_LH, t_THL Maximum 2.0V 30 75 95 1 Output Rise and Fall Time 4.5V 10 15 19 2 2 tr, t ₁ Maximum Input Rise and Fall Time 500 500 55 400 400 400 400	PHL, ^t PLH	Maximum Propagation		2.0V	80	125	156	188	
tpHL Maximum Propagation Delay Reset to any Q (4020 and 4040) 2.0V 72 240 302 332		Delay Between Stages		4.5V	18	25	31	38	ns
Internation Delay Reset to any Q (4020 and 4040) 4.5V 24 48 60 7 tREM Minimum Reset Removal Time 2.0V 100 126 1 tw Minimum Pulse Width 2.0V 20 20 25 2 tw Minimum Pulse Width 2.0V 90 100 1 true 6.0V 16 21 2 tw Minimum Pulse Width 2.0V 90 100 1 true 6.0V 14 18 2 </td <td></td> <td>from Q_n to Q_{n+1}</td> <td></td> <td>6.0V</td> <td>15</td> <td>21</td> <td>26</td> <td>31</td> <td></td>		from Q _n to Q _{n+1}		6.0V	15	21	26	31	
Delay Reset to any Q (4020 and 4040) 4.5V 24 48 60 50 tREM Minimum Reset 2.0V 100 126 1 Removal Time 4.5V 20 20 25 25 tw Minimum Pulse Width 2.0V 16 21 20 tw Minimum Pulse Width 2.0V 90 100 11 tw Minimum Pulse Width 2.0V 90 100 1 true 2.0V 90 100 1 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 25 20 20 20 25 20 20 25 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20<	t _{PHL}	Maximum Propagation		2.0V	72	240	302	358	
Minimum Reset 2.0V 100 126 1 Removal Time 4.5V 20 25 4 tw Minimum Pulse Width 2.0V 16 21 2 tw Minimum Pulse Width 2.0V 90 100 1 tw Minimum Pulse Width 2.0V 90 100 1 true 6.0V 16 20 2 2 true 6.0V 16 20 2 2 true 6.0V 14 18 2 2 2 1 2		Delay Reset to any Q		4.5V	24	48	60	72	ns
Removal Time 4.5V 20 25 90 tw Minimum Pulse Width 2.0V 90 100 1 tw Minimum Pulse Width 2.0V 90 100 1 tr_TLH, trHL Maximum 2.0V 16 20 25 90 trL+, trHL Maximum 2.0V 30 75 95 1 Output Rise 4.5V 10 15 19 20 and Fall Time 6.0V 9 13 16 100 100 100 tr, tr Maximum Input Rise and Fall Time 1000		(4020 and 4040)		6.0V	20	41	51	61	
Image: Book of two states Im	BEM	Minimum Reset		2.0V		100	126	149	
Minimum Pulse Width 2.0V 90 100 1 4.5V 16 20 2 tTLH, tTHL Maximum 2.0V 30 75 95 1 Output Rise 4.5V 10 15 19 2 and Fall Time 6.0V 9 13 16 20 tr, tr Maximum Input Rise and Fall Time 6.0V 9 13 16 100 100 100 CpD Power Dissipation (per package) 55 55 400 400 400		Removal Time		4.5V		20	25	50	ns
Maximum 4.5V 16 20 20 t _{TLH} , t _{THL} Maximum 2.0V 30 75 95 1 Output Rise and Fall Time 4.5V 10 15 19 2 t _r , t _f Maximum Input Rise and Fall Time 6.0V 9 13 16 C _{PD} Power Dissipation (per package) 55 50 50				6.0V		16	21	25	
true, true Maximum 6.0V 14 18 20 Output Rise 2.0V 30 75 95 1 Output Rise 4.5V 10 15 19 2 and Fall Time 6.0V 9 13 16 1000 1000 tr, tr Maximum Input Rise and Fall Time 1000 1000 1000 1000 1000 CpD Power Dissipation (per package) 55 55 55 55	tw	Minimum Pulse Width		2.0V		90	100	120	
true, true Maximum 2.0V 30 75 95 11 Output Rise 4.5V 10 15 19 2 and Fall Time 6.0V 9 13 16 10 tr, tr Maximum Input Rise and Fall Time 1000 1000 1000 100 CpD Power Dissipation (per package) 55 55 50 50				4.5V		16	20	24	ns
Output Rise and Fall Time 4.5V 10 15 19 2 tr, tr Maximum Input Rise and Fall Time 6.0V 9 13 16 1000				6.0V		14	18	20	
and Fall Time 6.0V 9 13 16 tr, tr Maximum Input Rise and Fall Time 1000 1000 100 C _{PD} Power Dissipation (per package) 55 50 50	t _{TLH} , t _{THL}	Maximum		2.0V	30	75	95	110	
tr, tr Maximum Input Rise and Fall Time 1000 1000 1000 C _{PD} Power Dissipation (per package) 55 50 55		Output Rise		4.5V	10	15	19	22	ns
Fall Time 500 500 55 C _{PD} Power Dissipation (per package) 55 55		and Fall Time		6.0V	9	13	16	19	
C _{PD} Power Dissipation (per package) 55 55	t _r , t _f	Maximum Input Rise and				1000	1000	1000	
C _{PD} Power Dissipation (per package) 55		Fall Time				500	500	500	ns
						400	400	400	
Capacitance (Note 7)	C _{PD}	Power Dissipation	(per package)		55				pF
		Capacitance (Note 7)							
C _{IN} Maximum Input 5 10 10	C _{IN}	Maximum Input			5	10	10	10	pF

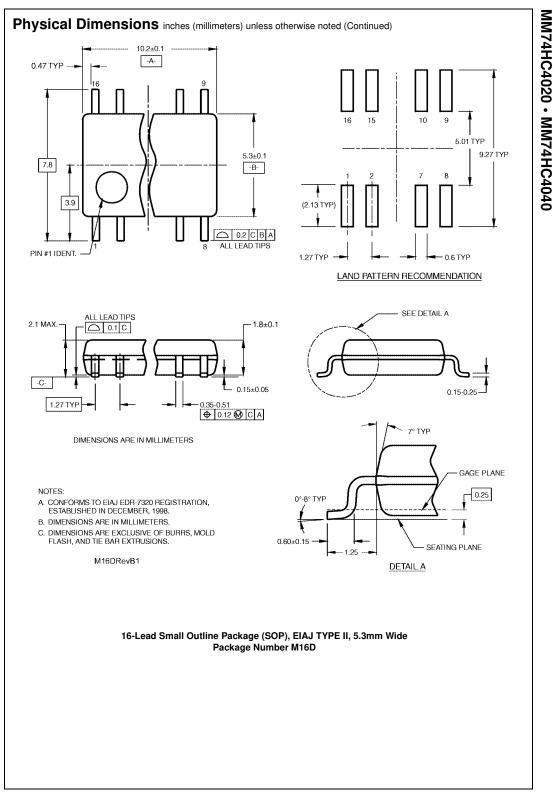
Note 7: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

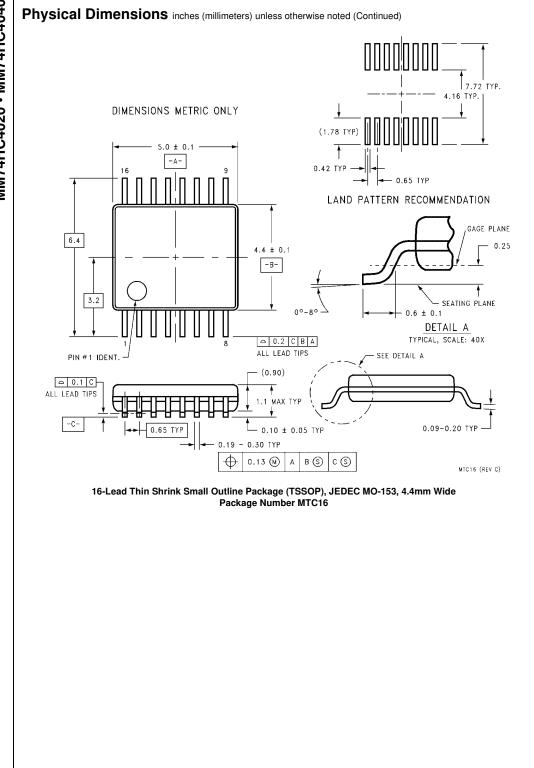
Capacitance

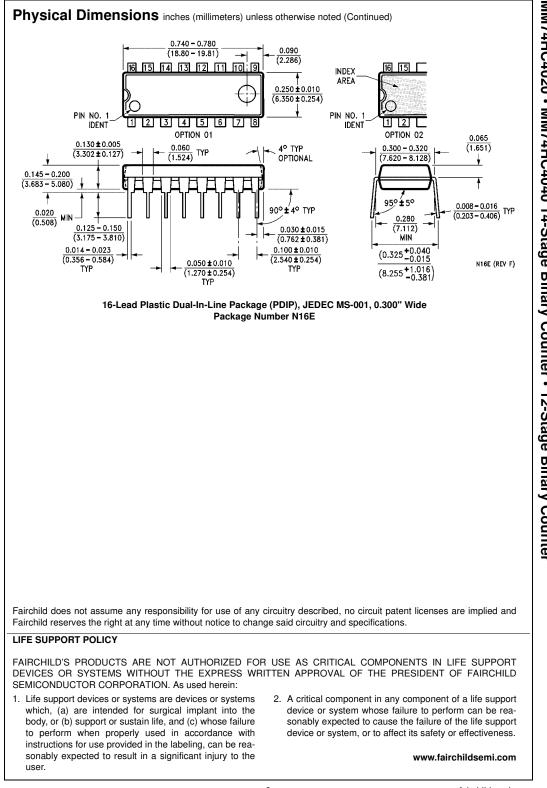


MM74HC4020 • MM74HC4040









MM74HC4020 • MM74HC4040 14-Stage Binary Counter • 12-Stage Binary Counter