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FAIRCHILD SEMICONDUCTOR™

January 1992
Revised May 1999

MM74HC594
8-Bit Shift Register with Output Registers

General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

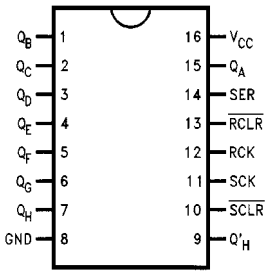
- Low quiescent current: 80 μA maximum
- Low input current: 1 μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V to 6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to30 MHz

Ordering Code:

Order Number	Package Number	Package Description
MM74HC594M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
MM74HC594N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

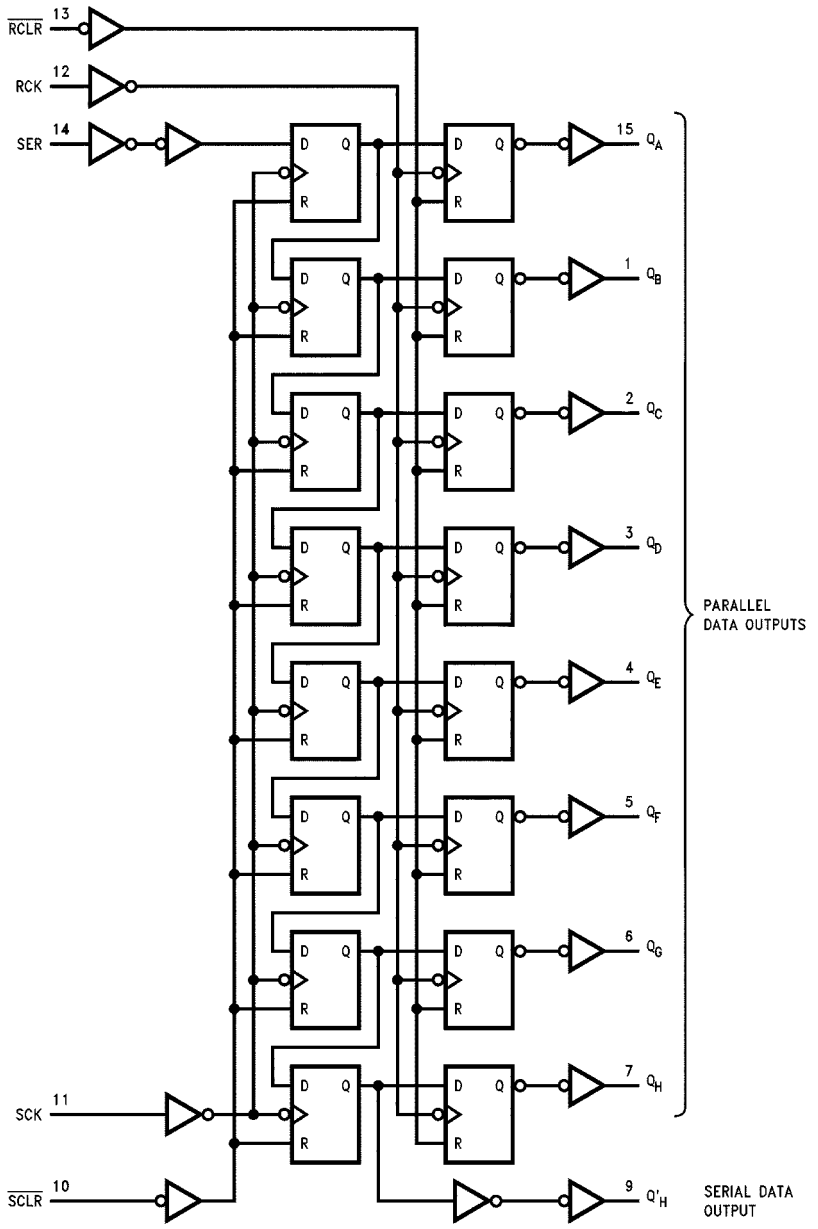
Connection Diagram



Truth Table

RCK	$\overline{SCK}$	$\overline{SCLR}$	RCLR	Function
X	X	X	L	Storage Register cleared
X	X	L	X	Shift Register cleared $Q'_H = 0$
X	↑	H	H	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	H	Contents of Shift Register transferred to output latches

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operation Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C		Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	
			6.0V		4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	
			6.0V		1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20$ µA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	
			6.0V	6.0	5.9	5.9	
	Q'_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.7	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20$ µA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	
			6.0V	0	0.1	0.1	
	Q'_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA	6.0V		8.0	80	µA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

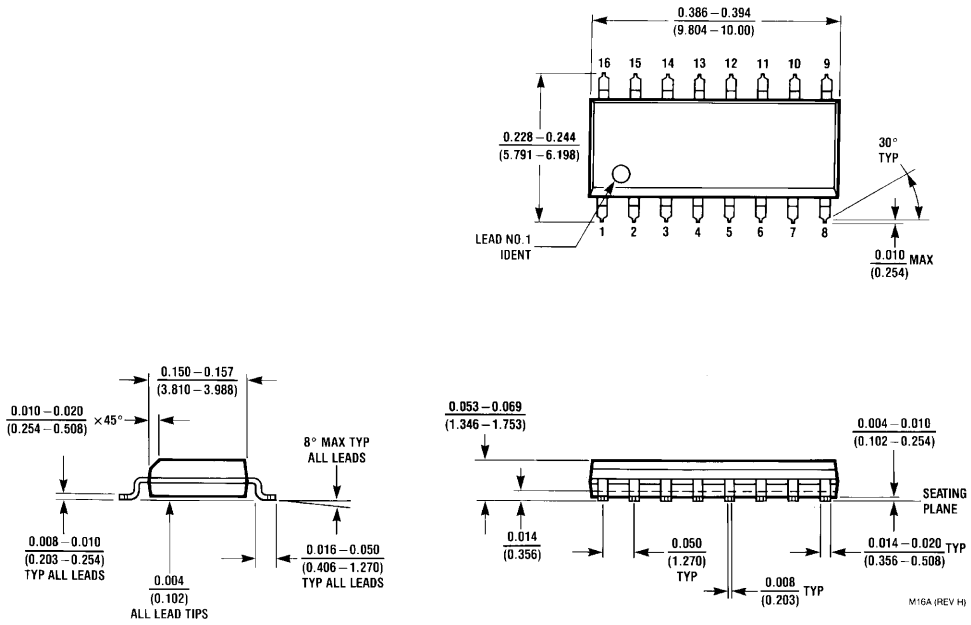
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		−40°C to +85°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	C_L = 50 pF	2.0V		6	4.8	MHz
			4.5V		30	24	
			6.0V		35	28	
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q'_H	C_L = 50 pF	2.0V		150	185	ns
			4.5V		30	37	
			6.0V		25	31	
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	C_L = 50 pF	2.0V		150	185	ns
		C_L = 150 pF	2.0V		200	250	
		C_L = 50 pF	4.5V		30	37	ns
		C_L = 150 pF	4.5V		40	50	
		C_L = 50 pF	6.0V		25	31	ns
		C_L = 150 pF	6.0V		34	43	
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SCLR}$ to Q'_H		2.0V		150	185	ns
			4.5V		30	37	
			6.0V		25	31	
t_{PHL}	Maximum Propagation Delay from $\overline{RCLR}$ to Q_A thru Q_H	C_L = 50 pF	2.0V		125	155	ns
			4.5V		25	31	
			6.0V		21	26	
		C_L = 150 pF	2.0V		200	250	ns
			4.5V		40	50	
			6.0V		34	43	
t_S	$\overline{SCLR}$ LOW to RCK		2.0V		50	63	ns
			4.5V		10	13	
			6.0V		9	11	
t_S	$\overline{RCLR}$ HIGH to SCK		2.0V		5	5	ns
			4.5V		5	5	
			6.0V		5	5	
t_S	Minimum Setup Time from SER to SCK		2.0V		90	110	ns
			4.5V		18	22	
			6.0V		15	19	
t_R	Minimum Removal Time from $\overline{SCLR}$ to SCK		2.0V		20	20	ns
			4.5V		10	10	
			6.0V		10	10	
t_S	Minimum Setup Time from SCK to RCK		2.0V		90	110	ns
			4.5V		18	22	
			6.0V		15	19	
t_H	Minimum Hold Time SER to SCK		2.0V		5	5	ns
			4.5V		5	5	
			6.0V		5	5	
t_W	Minimum Pulse Width of SCK or $\overline{SCLR}$ or RCK or $\overline{RCLR}$		2.0V		100	125	ns
			4.5V		20	25	
			6.0V		17	21	
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	ns
			4.5V		500	500	
			6.0V		400	400	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q_A - Q_H		2.0V		60	75	ns
			4.5V		12	15	
			6.0V		10	13	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q'_H		2.0V		75	95	ns
			4.5V		15	19	
			6.0V		13	16	

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		$-40°C$ to $+85°C$	Units
				Typ	Guaranteed Limits		
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 5)	$\overline{G} = V_{CC}$		90			pF
		$\overline{G} = GND$		150			
C_{IN}	Maximum Input Capacitance			5	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	pF

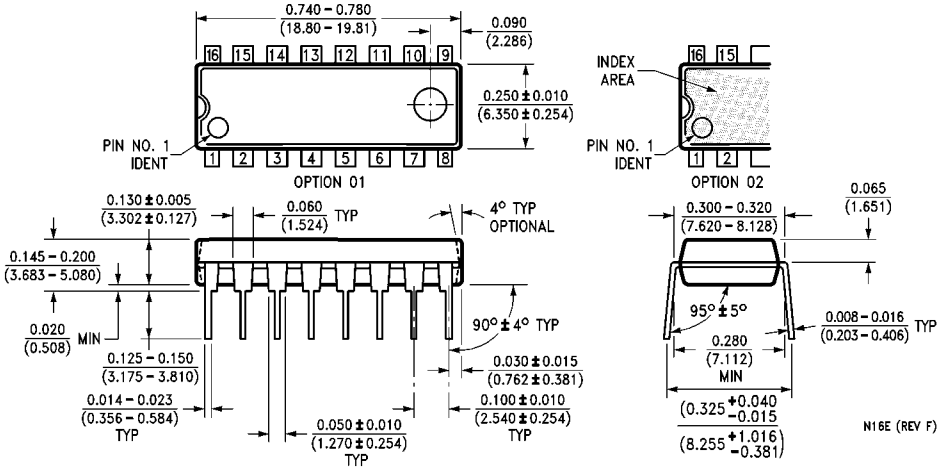
Note 5: C_{PD} determines the no load dynamic power consumption, and the no load dynamic current consumption.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E