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Future Technology Devices International Ltd.

FT900/1/2/3

(Embedded Microcontroller)

The FT90x series includes the FT900, FT901, FT902 and FT903 which are complete System-On-Chip 32-bit RISC microcontrollers for embedded applications featuring a high level of integration and low power consumption. It has the following features:

- High performance, low power 32-bit FT32 core processor, running at a frequency of 100MHz.
- 256kB on-chip Flash memory.
- 256kB on-chip shadow program memory.
- True Zero Wait States (0WS) up to 3.1 DMIPS per MHz performance
- 64kB on-chip data memory.
- EFUSE for security configuration.
- Integrated Phase-Locked Loop (PLL) supports external 12MHz crystal and direct external clock source input.
- 32.768 kHz real time clock support.
- One USB2.0 EHCI compatible host controller supports high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s).
- One USB2.0 peripheral controller supports high-speed (480 Mbit/s) and full-speed (12 Mbit/s).
- USB2.0 host and peripheral controllers support the Isochronous, Interrupt, Control, and Bulk transfers.
- 10/100 Mbps Ethernet that is compliant with the IEEE 802.3/802.3u standards. (FT900 and FT901 only)
- Supports One-Wire debugger for downloading firmware to Flash memory or shadow program memory, and supports a software debugger.
- Two CAN controllers support CAN protocol 2.0 parts A & B, data rate is up to 1 Mbit/s. (FT900 and FT902 only)
- One SPI master supports single / dual / quad modes of data transfer. Clock rate is up to 25 MHz
- Two SPI slaves support single data transfer with 25MHz clock.
- Two I^2C bus interfaces can be configured as master or slave, which support standard / fast / fast plus / high speed mode data transfers. Max data transfer rate up to 3.4 Mbit/s. Clock stretching is supported.
- I^2S bus interface can be configured as master or slave. Two clock input options (24.576 MHz and 22.5792 MHz) to support I^2S master mode for different audio sample rates.
- UART interface can be configured as one full programmable UART0 or two simple interfaces, UART0 and UART1 with CTS / RTS control function.
- Four user timers with pre-scaling and a watchdog function.
- 8-bit parallel data interface supports camera data capturing.
- Support 7 independent PWM channels. Channel 0 and 1 can be configured as PCM 8-bit/16-bit stereo audio output.
- SD host controller is compatible to standard specification V3.0, it supports up to 25 MHz SD clock speed and software supports SD card format in SD/SDHC/SDXC.
- Support two 10-bit DAC 0/1 channels output, sample rate at ~1 MS/s.
- Support seven 10-bit ADC 1/7 channels input, sample rate is up to ~960 kS/s.
- Single 3.3 volt power supply, built-in 1.2 V regulators.
- 3.3 volt I/O power supply.
- Support USB Battery Charging Specification Rev 1.2. Downstream port can be configured as SDP, CDP or DCP. Upstream port can perform BCD mode detection.
- Support VBUS power switching and over current control.
- Power-On Reset (POR).
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 100-Pin packages (all RoHS compliant).

1 Typical Applications

- Home security system
- Home Automation
- Embedded audio application
- Motor drive and application control
- E-meter
- CCTV monitor
- Industrial automation
- Medical appliances
- Instrumentation
- DAQ System

1.1 Part Numbers

Part Number	Package
FT900Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, support both CAN Bus and Ethernet features.
FT900L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, support both CAN Bus and Ethernet features.
FT901Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, support Ethernet, doesn't support CAN Bus.
FT901L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, support Ethernet, doesn't support CAN Bus.
FT902Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, support CAN Bus, doesn't support Ethernet.
FT902L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, support CAN Bus, doesn't support Ethernet.
FT903Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, doesn't support both CAN Bus and Ethernet features.
FT903L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, doesn't support both CAN Bus and Ethernet features.

Table 1-1 FT90x series Part Numbers

Common Interfaces on all packages include: USB Host, USB Peripheral, SPI, UART, ADC, DAC, I2S, PWM, RTC, Timers/Watchdog, Interrupt Controller.

Note: Packaging codes for X is:

-R: Tape and Reel (Qty per reel is 1000)

-T: Tray packing (Qty per tray for LQFP is 90, qty per tray for QFN is 152)

1.2 USB2.0 Compliant

The FT90x series contains a USB2.0 host controller and peripheral controller that both are compliant with USB2.0 specification.

2 FT900 Block Diagram

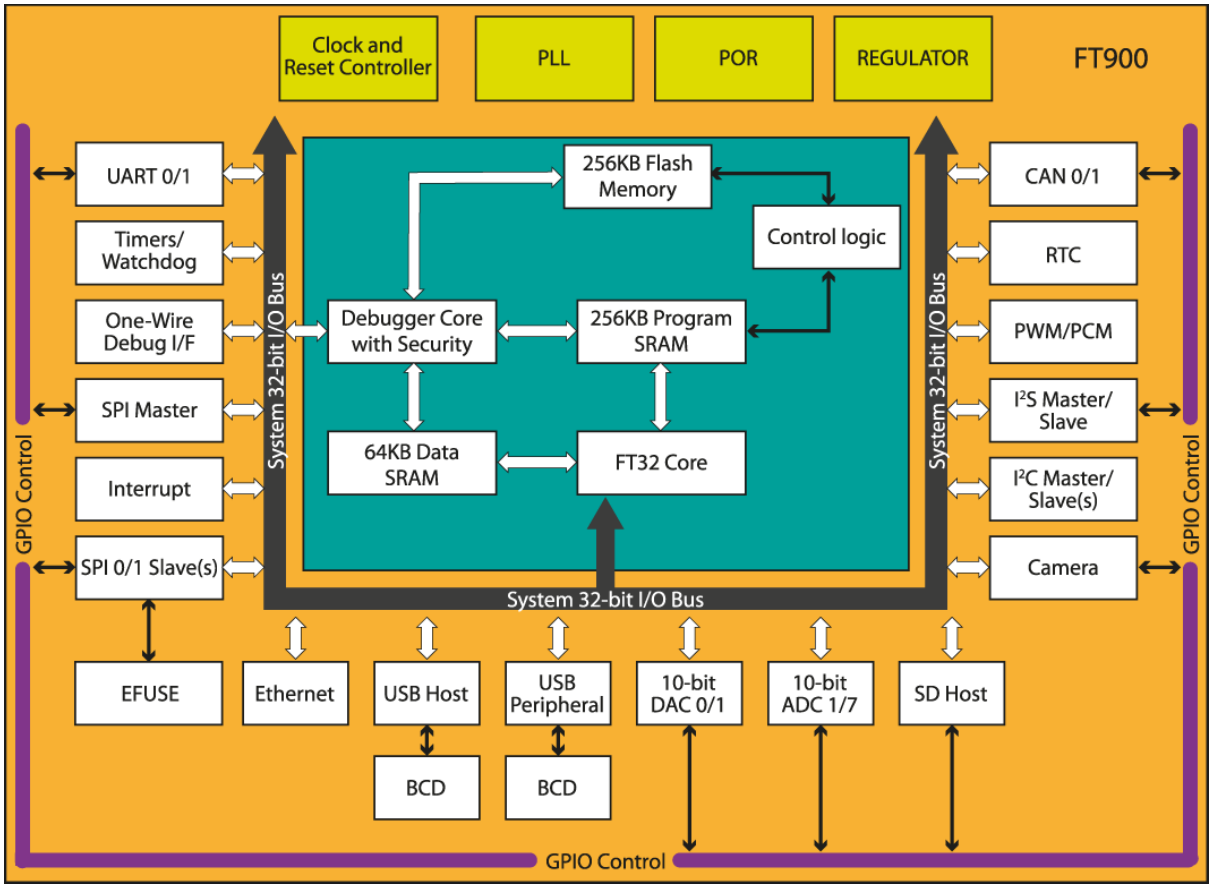

Figure 2-1 FT900 Block Diagram

For a description of each function please refer to Section 5.

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3 Device Pin Out and Signal Description

3.1 Pin Out – FT900 QFN-100

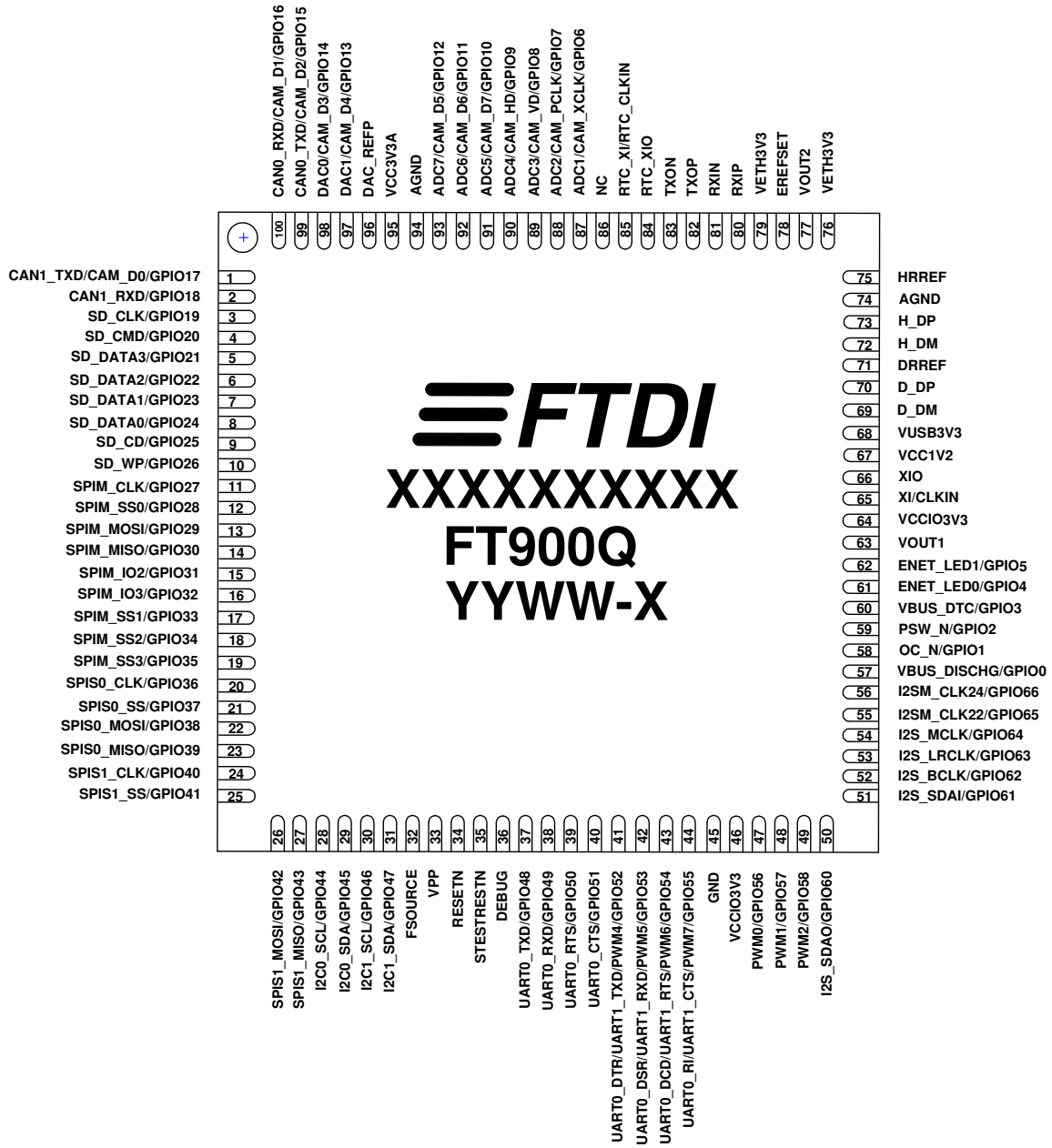

Figure 3-1 Pin Configuration FT900Q (top-down view)

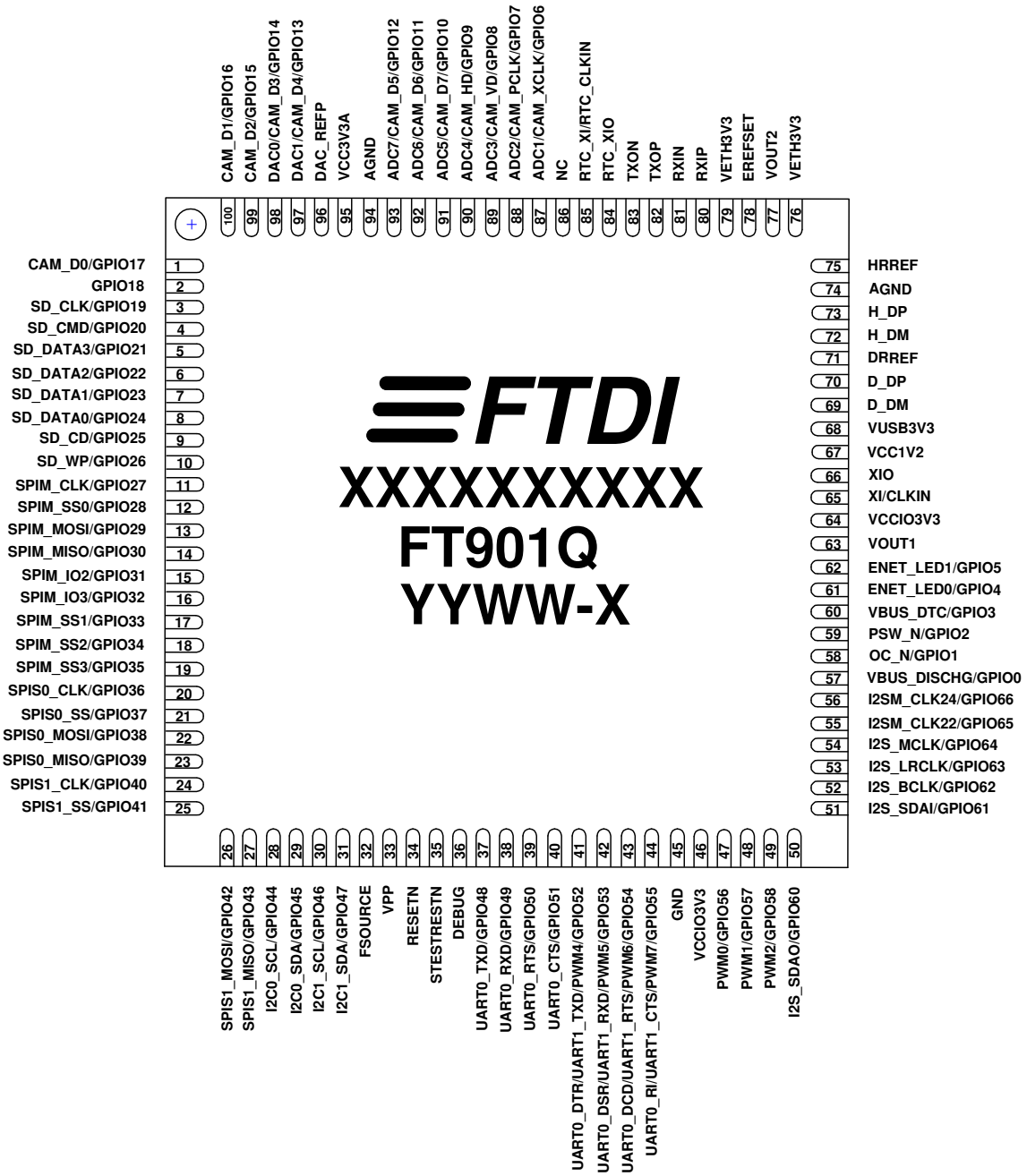

Figure 3-2 Pin Configuration FT901Q (top-down view)

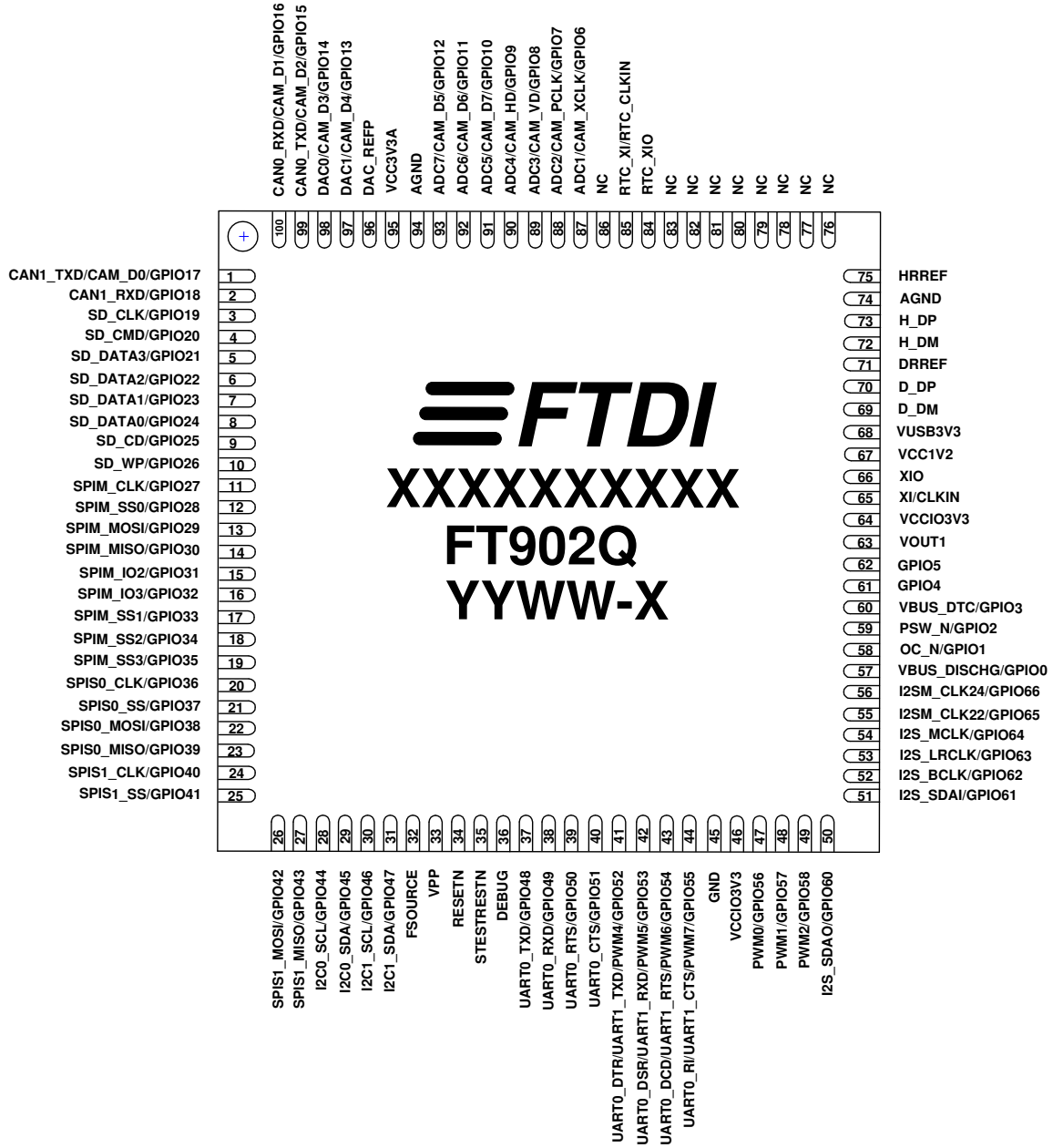

Figure 3-3 Pin Configuration FT902Q (top-down view)

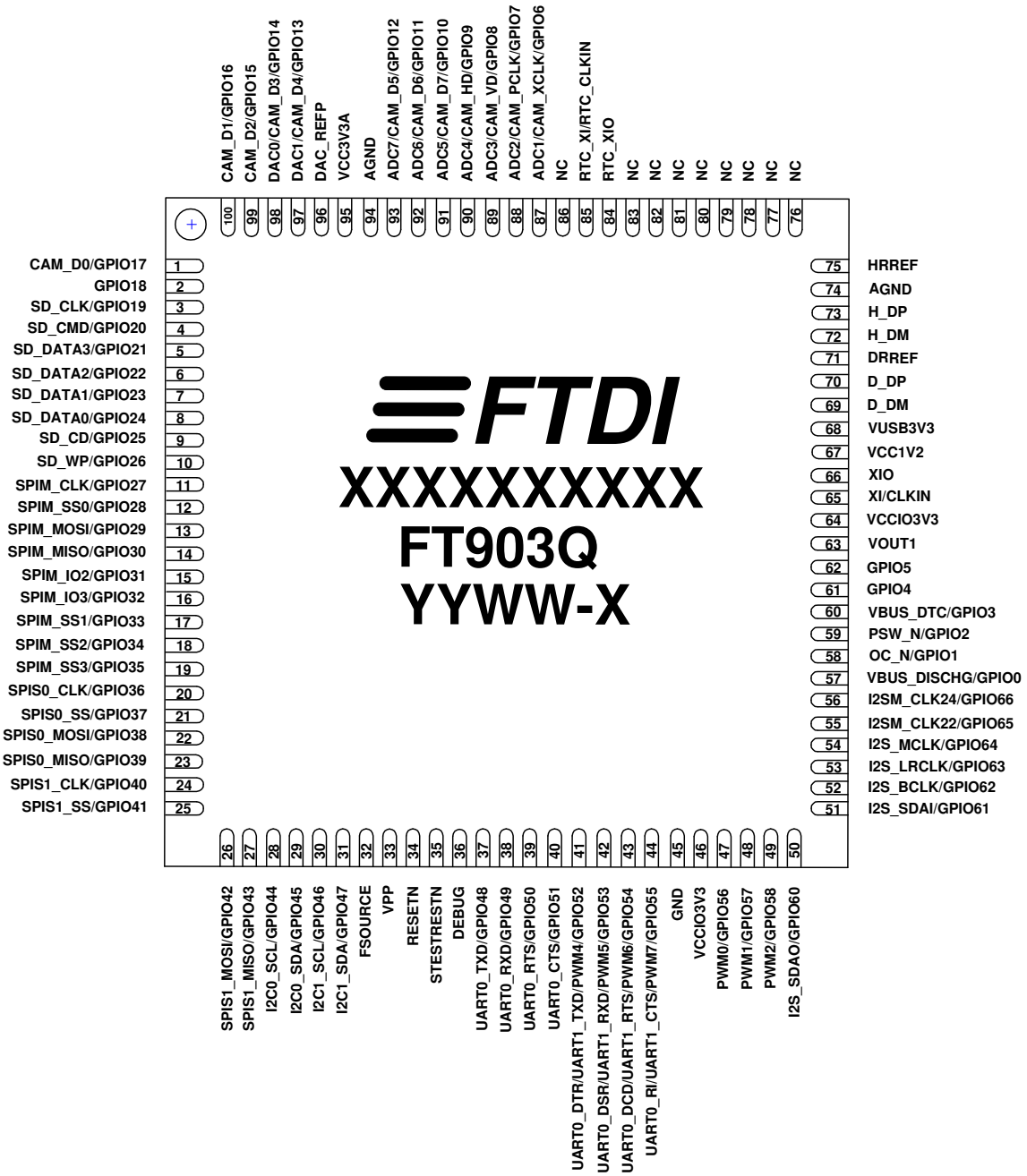

Figure 3-4 Pin Configuration FT903Q (top-down view)

3.2 Pin Out – FT900 LQFP-100

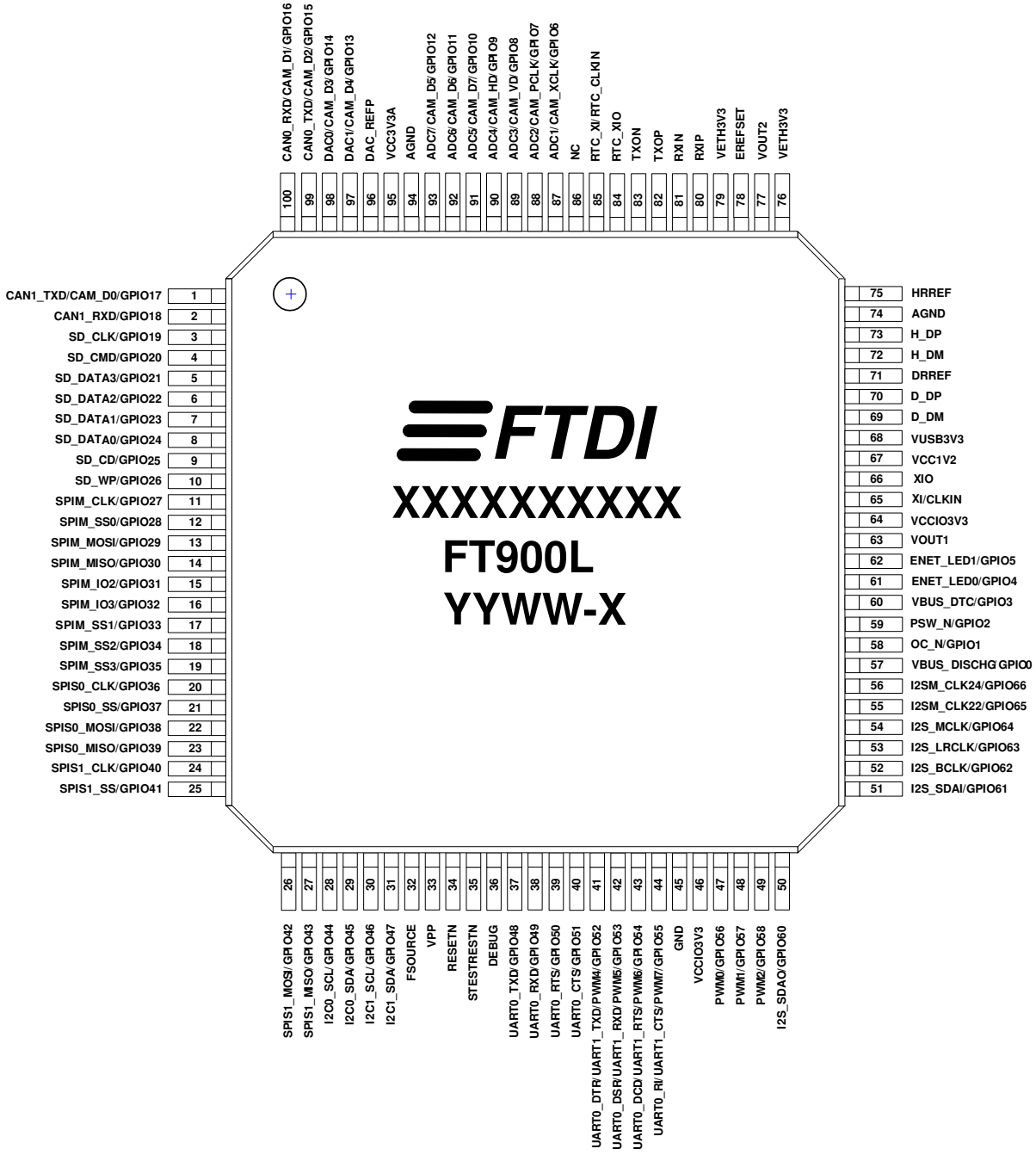

Figure 3-5 Pin Configuration FT900L (top-down view)

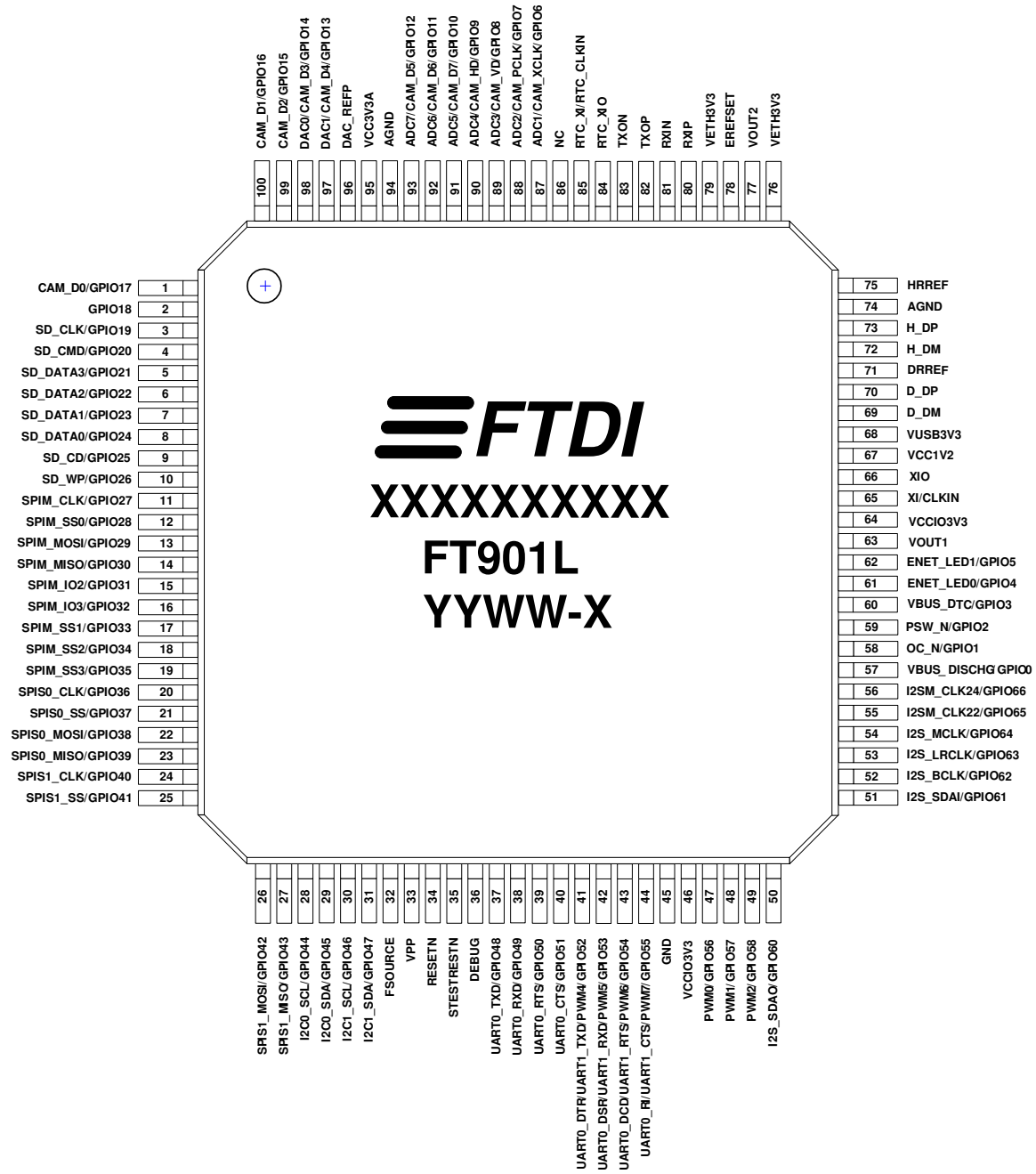

Figure 3-6 Pin Configuration FT901L (top-down view)

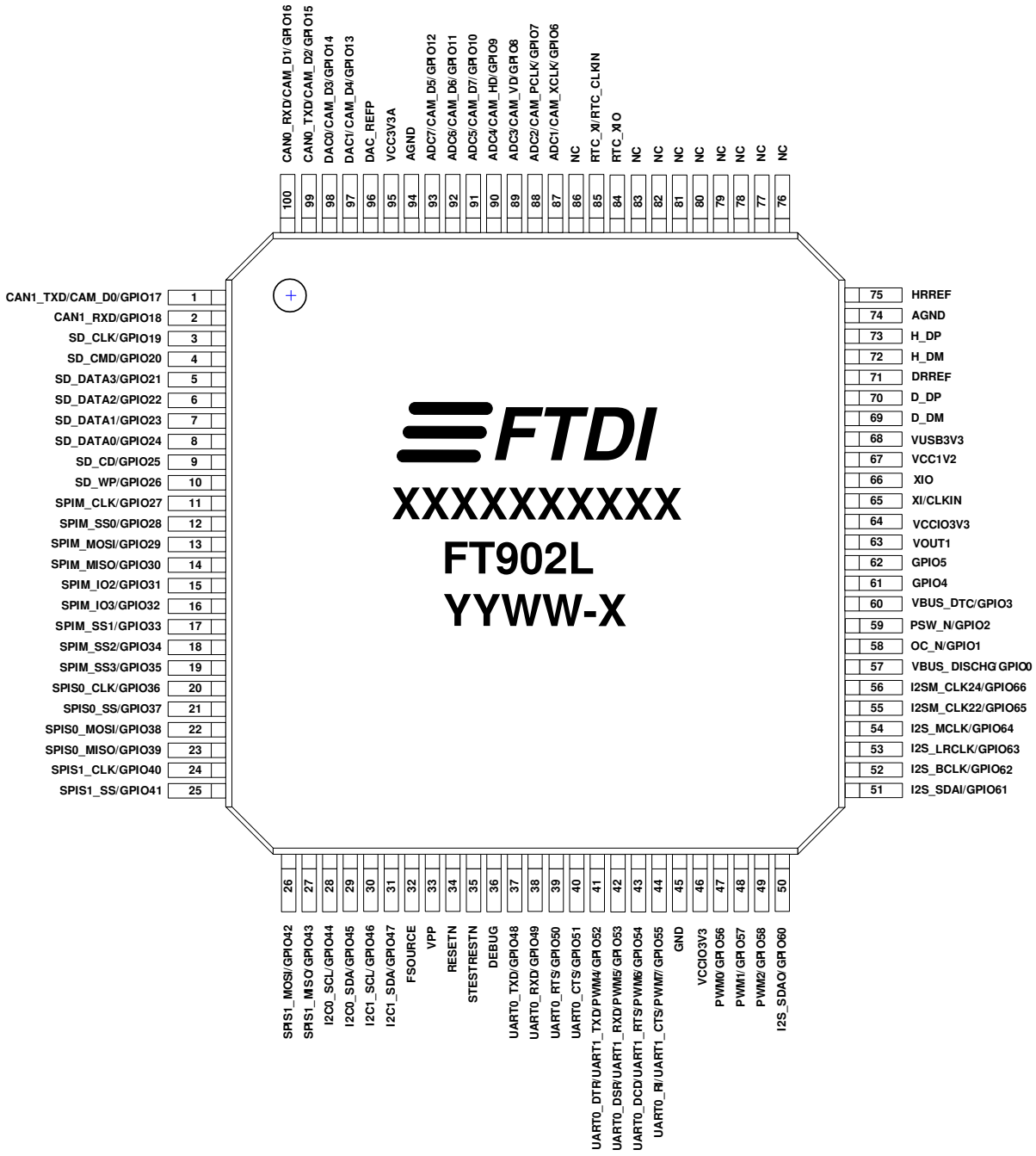

Figure 3-7 Pin Configuration FT902L (top-down view)

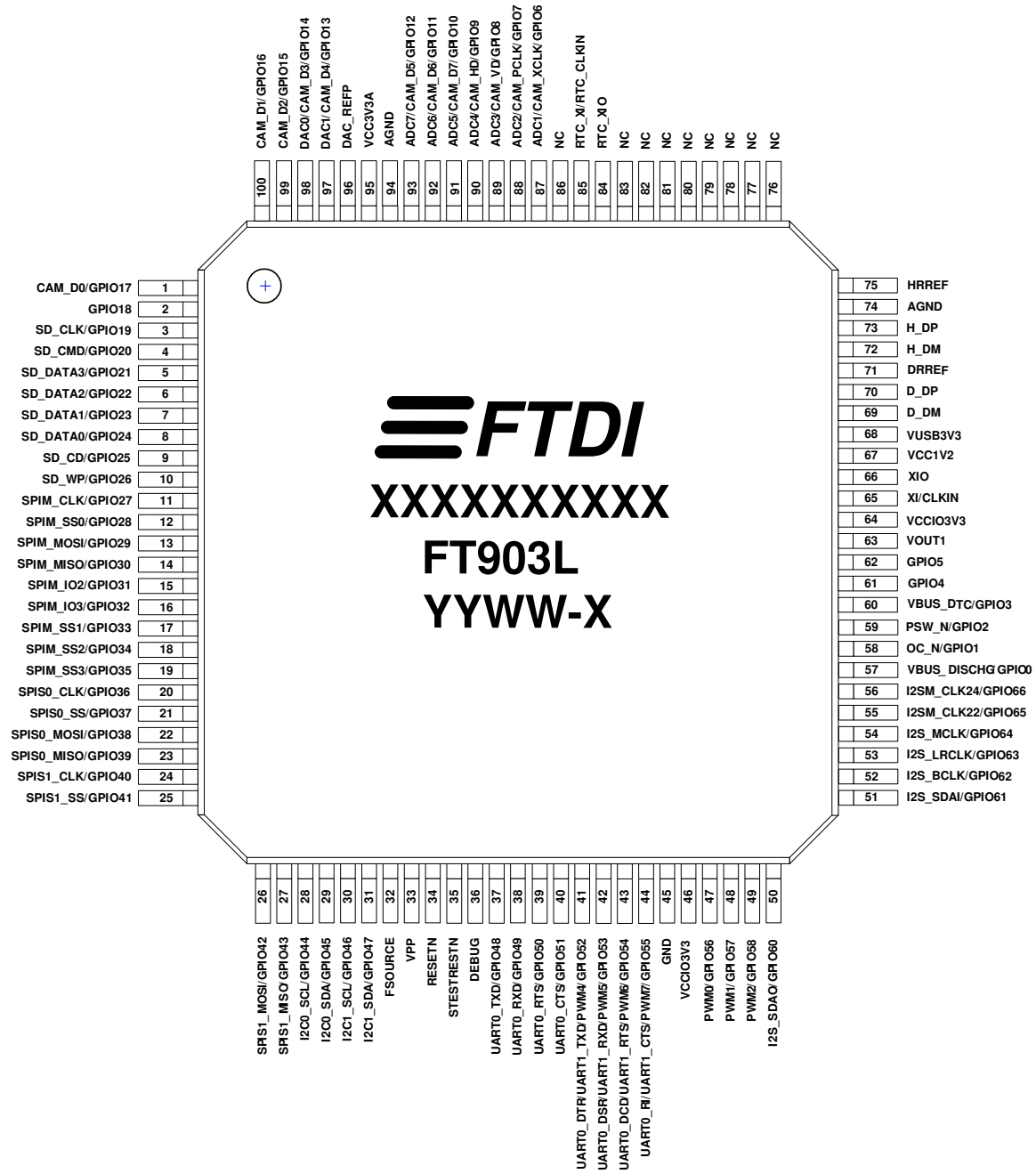

Figure 3-8 Pin Configuration FT903L (top-down view)

3.3 Pin Description

Pin No.	Name	Type	Description
1	CAN1_TXD/CAM_D0/GPIO17	I/O	GPIO17 input/output. (By default is GPIO input, internal pull-low) Camera data 0 input. CAN1 transmitter output. [1]
2	CAN1_RXD/GPIO18	I/O	GPIO18 input/output. (By default is GPIO input, internal pull-low) CAN1 receiver input.[1]
3	SD_CLK/GPIO19	I/O	GPIO19 input/output. (By default is GPIO input, internal pull-low) SD card serial clock output.
4	SD_CMD/GPIO20	I/O	GPIO20 input/output. (By default is GPIO input, internal pull-low) SD card command signal input/output.
5	SD_DATA3/GPIO21	I/O	GPIO21 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 3 input/output.
6	SD_DATA2/GPIO22	I/O	GPIO22 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 2 input/output.
7	SD_DATA1/GPIO23	I/O	GPIO23 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 1 input/output.
8	SD_DATA0/GPIO24	I/O	GPIO24 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 0 input/output.
9	SD_CD/GPIO25	I/O	GPIO25 input/output. (By default is GPIO input, internal pull-low) SD card detect input.
10	SD_WP/GPIO26	I/O	GPIO26 input/output. (By default is GPIO input, internal pull-low) SD card write protection input.
11	SPIM_CLK/GPIO27	I/O	GPIO27 input/output. (By default is GPIO input, internal pull-low) Serial clock output for SPI master.
12	SPIM_SS0/GPIO28	I/O	GPIO28 input/output. (By default is GPIO input, internal pull-low) Slave select 0 output for SPI master.
13	SPIM_MOSI/GPIO29	I/O	GPIO29 input/output. (By default is GPIO input, internal

Pin No.	Name	Type	Description
			pull-low) Master out slave in for SPI master. Data line 0 input/output for SPI master dual & quad mode.
14	SPIM_MISO/GPIO30	I/O	GPIO30 input/output. (By default is GPIO input, internal pull-low) Master in slave out for SPI master. Data line 1 input/output for SPI master dual & quad mode.
15	SPIM_IO2/GPIO31	I/O	GPIO31 input/output. (By default is GPIO input, internal pull-low) Data line 2 input/output for SPI master quad mode.
16	SPIM_IO3/GPIO32	I/O	GPIO32 input/output. (By default is GPIO input, internal pull-low) Data line 3 input/output for SPI master quad mode.
17	SPIM_SS1/GPIO33	I/O	GPIO33 input/output. (By default is GPIO input, internal pull-low) Slave select 1 output for SPI master.
18	SPIM_SS2/GPIO34	I/O	GPIO34 input/output. (By default is GPIO input, internal pull-low) Slave select 2 output for SPI master.
19	SPIM_SS3/GPIO35	I/O	GPIO35 input/output. (By default is GPIO input, internal pull-low) Slave select 3 output for SPI master.
20	SPIS0_CLK/GPIO36	I/O	GPIO36 input/output. (By default is GPIO input, internal pull-low) Serial clock input for SPI slave 0.
21	SPIS0_SS/GPIO37	I/O	GPIO37 input/output. (By default is GPIO input, internal pull-low) Slave select input for SPI slave 0.
22	SPIS0_MOSI/GPIO38	I/O	GPIO38 input/output. (By default is GPIO input, internal pull-low) Master out slave in for SPI slave 0.
23	SPIS0_MISO/GPIO39	I/O	GPIO39 input/output. (By default is GPIO input, internal pull-low) Master in slave out for SPI slave 0.
24	SPIS1_CLK/GPIO40	I/O	GPIO40 input/output. (By default is GPIO input, internal pull-low) Serial clock input for SPI slave 1.
25	SPIS1_SS/GPIO41	I/O	GPIO41 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			Slave select input for SPI slave 1.
26	SPIS1_MOSI/GPIO42	I/O	GPIO42 input/output. (By default is GPIO input, internal pull-low) Master out slave in for SPI slave 1.
27	SPIS1_MISO/GPIO43	I/O	GPIO43 input/output. (By default is GPIO input, internal pull-low) Master in slave out for SPI slave 1.
28	I2C0_SCL/GPIO44	I/O	GPIO44 input/output. (By default is GPIO input, internal pull-low) I^2C 0 serial clock input/output. (By default is I^2C 0 master)
29	I2C0_SDA/GPIO45	I/O	GPIO45 input/output. (By default is GPIO input, internal pull-low) I^2C 0 data line input/output. (By default is I^2C 0 master)
30	I2C1_SCL/GPIO46	I/O	GPIO46 input/output. (By default is GPIO input, internal pull-low) I^2C 1 serial clock input/output. (By default is I^2C 1 slave)
31	I2C1_SDA/GPIO47	I/O	GPIO47 input/output. (By default is GPIO input, internal pull-low) I^2C 1 data line input/output. (By default is I^2C 1 slave)
32	FSOURCE	I	EFUSE Program source input (3.6V-3.8V). If not used for EFUSE programming, leave this pin floating or short to Ground.
33	VPP	I	EFUSE Program source input (1.8V-1.9V). If not used for EFUSE programming, leave this pin floating.
34	RESETN	I	Chip reset input for normal operation. Active low. Connect external 10k pull-up to VCC3V3 for safe operation.
35	STESTRESETN	I	Chip reset input for test mode. Short to Ground for normal operation.
36	DEBUG	I/O	One-wire debugger interface input/output.
37	UART0_TXD/GPIO48	I/O	GPIO48 input/output. (By default is GPIO input, internal pull-low) Transmitter output for UART0.
38	UART0_RXD/GPIO49	I/O	GPIO49 input/output. (By default is GPIO input, internal pull-low) Receiver input for UART0.
39	UART0_RTS/GPIO50	I/O	GPIO50 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			Request to send output for UART0.
40	UART0_CTS/GPIO51	I/O	GPIO51 input/output. (By default is GPIO input, internal pull-low) Clear to send input for UART0.
41	UART0_DTR/UART1_TXD/ PWM4/GPIO52	I/O	GPIO52 input/output. (By default is GPIO input, internal pull-low) PWM channel 4, output. Transmitter output for UART1. Data terminal ready output for UART0.
42	UART0_DSR/UART1_RXD/ PWM5/GPIO53	I/O	GPIO53 input/output. (By default is GPIO input, internal pull-low) PWM channel 5, output. Receiver input for UART1. Data set ready input for UART0.
43	UART0_DCD/UART1_RTS/ PWM6/GPIO54	I/O	GPIO54 input/output. (By default is GPIO input, internal pull-low) PWM channel 6, output. Request to send output for UART1. Data carrier detection input for UART0.
44	UART0_RI/UART1_CTS/ PWM7/GPIO55	I/O	GPIO55 input/output. (By default is GPIO input, internal pull-low) PWM channel 7, output. Clear to send input for UART1. Ring indicator input for UART0.
45	GND	P	Ground
46	VCCIO3V3	P	+3.3V supply voltage. This is the supply voltage for all the I/O ports. Connect 10uF and 0.1uF decoupling capacitors to GND. This pin must be connected to pin 64.
47	PWM0/GPIO56	I/O	GPIO56 input/output. (By default is GPIO input, internal pull-low) PWM channel 0, output. A stereo 16/8-bit PCM audio data channel output.
48	PWM1/GPIO57	I/O	GPIO57 input/output. (By default is GPIO input, internal pull-low) PWM channel 1, output. A stereo 16/8-bit PCM audio data channel output.
49	PWM2/GPIO58	I/O	GPIO58 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			PWM channel 2, output.
50	I2S_SDAO/GPIO60	I/O	GPIO60 input/output. (By default is GPIO input, internal pull-low) Serial data line output for I2S master or slave.
51	I2S_SDAI/GPIO61	I/O	GPIO61 input/output. (By default is GPIO input, internal pull-low) Serial data line input for I2S master or slave.
52	I2S_BCLK/GPIO62	I/O	GPIO62 input/output. (By default is GPIO input, internal pull-low) Bit clock line output for I2S master transmitter or input for I2S slave receiver.
53	I2S_LRCLK/GPIO63	I/O	GPIO63 input/output. (By default is GPIO input, internal pull-low) Left / Right clock line output for I2S master transmitter or input for I2S slave receiver.
54	I2S_MCLK/GPIO64	I/O	GPIO64 input/output. (By default is GPIO input, internal pull-low) I2S master transmitter clock output.
55	I2SM_CLK22/GPIO65	I/O	GPIO65 input/output. (By default is GPIO input, internal pull-low) I2S master external 22.5792MHz clock input.
56	I2SM_CLK24/GPIO66	I/O	GPIO66 input/output. (By default is GPIO input, internal pull-low) I2S master external 24.576MHz clock input.
57	VBUS_DISCHG/GPIO0	I/O	GPIO0 input/output. (By default is GPIO input, internal pull-high) USB host VBUS discharge.
58	OC_N/GPIO1	I/O	GPIO1 input/output. (By default is GPIO input, internal pull-high) USB host port over current status output. Active low.
59	PSW_N/GPIO2	I/O	GPIO2 input/output. (By default is GPIO input, internal pull-high) USB host port external VBUS power switcher. Active low.
60	VBUS_DTC/GPIO3	I/O	GPIO3 input/output. (By default is GPIO input, internal pull-low) USB peripheral VBUS detection.
61	ENET_LED0/GPIO4	I/O	GPIO4 input/output. (By default is GPIO input, internal pull-low) Ethernet activity indicator LED 0.[2]

Pin No.	Name	Type	Description
62	ENET_LED1/GPIO5	I/O	GPIO5 input/output. (By default is GPIO input, internal pull-low) Ethernet activity indicator LED 1.[2]
63	VOUT1	P	+1.2V Regulator power output. This is internal regulator output. Connect 4.7uF and 0.1uF decoupling capacitors to GND. This pin must be connected to pin 67.
64	VCCIO3V3	P	+3.3V supply voltage. This is the supply voltage for all the I/O ports. Connect a 0.1uF decoupling capacitor. This pin must be connected to pin 46.
65	XI/CLKIN	AI	12MHz clock frequency input to the Oscillator circuit or to internal clock generator circuit.
66	XIO	AO	Output from the Oscillator amplifier.
67	VCC1V2	P	+1.2V Regulator power supply for USB. Provide +1.2V power to this pin. This pin must be connected to pin 63. Connect 0.1uF decoupling capacitor.
68	VUSB3V3	P	+3.3V supply voltage. This is the supply voltage for USB peripheral and host I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor.
69	D_DM	AI/O	USB peripheral bidirectional DM line.
70	D_DP	AI/O	USB peripheral bidirectional DP line.
71	DRREF	AI	USB peripheral reference voltage input. Connect 12Kohm +/- 1% resistor to GND.
72	H_DM	AI/O	USB host bidirectional DM line.
73	H_DP	AI/O	USB host bidirectional DP line.
74	AGND	P	Analog Ground
75	HRREF	AI	USB host reference voltage input. Connect 12Kohm +/- 1% resistor to GND.
76	VETH3V3	P	+3.3V supply voltage. This is the supply voltage for Ethernet I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor.
77	VOUT2	P	+1.2V Regulator power supply.[2] This is an internal regulator output. Connect 0.1uF

Pin No.	Name	Type	Description
			decoupling capacitors.
78	EREFSET	AI	Ethernet reference voltage input.[2] Connect 12.3Kohm +/- 1% resistor to GND.
79	VETH3V3	P	+3.3V supply voltage. This is the supply voltage for Ethernet I/O ports. Connect a 0.1uF decoupling capacitor. This pin must be connected to pin 76.
80	RXIP	I	Ethernet receive data positive input.[2] Differential receive signal pair.
81	RXIN	I	Ethernet receive data negative input.[2] Differential receive signal pair.
82	TXOP	O	Ethernet transmit data positive output.[2] Differential transmit signal pair.
83	TXON	O	Ethernet transmit data negative output.[2] Differential transmit signal pair.
84	RTC_XIO	AO	Output from the RTC Oscillator amplifier.
85	RTC_XI/RTC_CLKIN	AI	32.768KHz clock frequency input to the RTC Oscillator circuit or to internal RTC clock generator circuit.
86	NC	-	Not connected.
87	ADC1/CAM_XCLK/GPIO6	I/O	GPIO6 input/output. (By default is GPIO input, internal pull-low) Camera external clock output. 10-bit A/D converter 1, input.
88	ADC2/CAM_PCLK/GPIO7	I/O	GPIO7 input/output. (By default is GPIO input, internal pull-low) Camera pixel clock input. 10-bit A/D converter 2, input.
89	ADC3/CAM_VD/GPIO8	I/O	GPIO8 input/output. (By default is GPIO input, internal pull-low) Camera vertical sync input. 10-bit A/D converter 3, input.
90	ADC4/CAM_HD/GPIO9	I/O	GPIO9 input/output. (By default is GPIO input, internal pull-low) Camera horizontal reference input. 10-bit A/D converter 4, input.
91	ADC5/CAM_D7/GPIO10	I/O	GPIO10 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			Camera data 7 input. 10-bit A/D converter 5, input.
92	ADC6/CAM_D6/GPIO11	I/O	GPIO11 input/output. (By default is GPIO input, internal pull-low) Camera data 6 input. 10-bit A/D converter 6, input.
93	ADC7/CAM_D5/GPIO12	I/O	GPIO12 input/output. (By default is GPIO input, internal pull-low) Camera data 5 input. 10-bit A/D converter 7, input.
94	AGND	P	Analog Ground
95	VCC3V3A	P	+3.3V supply voltage. This is the supply voltage for Analog I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all VCC3V3 pins without 10uF capacitor.
96	DAC_REFP	I	10-bit DAC positive reference voltage.
97	DAC1/CAM_D4/GPIO13	I/O	GPIO13 input/output. (By default is GPIO input, internal pull-low) Camera data 4 input. 10-bit D/A converter 1, output.
98	DAC0/CAM_D3/GPIO14	I/O	GPIO14 input/output. (By default is GPIO input, internal pull-low) Camera data 3 input. 10-bit D/A converter 0, output.
99	CAN0_TXD/CAM_D2/GPIO15	I/O	GPIO15 input/output. (By default is GPIO input, internal pull-low) CAN0 transmitter output. [1] Camera data 2 input.
100	CAN0_RXD/CAM_D1/GPIO16	I/O	GPIO16 input/output. (By default is GPIO input, internal pull-low) CAN0 receiver input. [1] Camera data 1 input.

Table 3-1 FT900 pin description

[1] CAN Bus 0/1 only are featured on both FT900 and FT902 packages.

[2] Ethernet pins are available on FT900 and FT901 only. For FT902 and FT903, shall leave all Ethernet pins as NC pin floating except for pin61 and pin62 as GPIO by default.

Notes:

P : Power or ground I : Input

O	: Output	AI	: Analog Input
OD	: Open drain output	AO	: Analog Output
I/O	: Bi-direction Input and Output	AI/O	: Analog Input / Output

4 Function Description

4.1 Architectural Overview

The FT90x series embedded microcontrollers include a high performance 32-bit FT32 RISC core processor and 256kB hi-speed Flash memory for software program downloading with a One-Wire debugger interface. The core processor uses a 32-bit I/O system bus to connect to all of the peripherals.

- USB2.0 host controller
- USB2.0 peripheral controller
- 10/100Mbps Ethernet controller *(FT900 and FT901 only)*
- Two CAN bus interfaces *(FT900 and FT902 only)*
- Real Time Clock
- One-Wire debugger interface
- One SPI master interface and two SPI slave interfaces
- Two I^2C bus interfaces
- One I^2S bus interface
- UART interface
- Four timers and a 32-bit watchdog timer
- Camera parallel interface
- SD host controller
- PWM motor controller
- 10-bit DAC0/1 channel
- 10-bit ADC1-7 channel
- General purpose I/O interface

The functions for each controller / interface are briefly described in the following subsections.

4.2 FT32 Core Processor

The FT32 core processor is running at frequencies of up to 100MHz. The processor contains the CPU itself with control logic and its 256kB program memory and 64kB data memory. The outside connections for the core processor are the memory-mapped I/O interface, the interrupt interface, asynchronous reset and the system clock.

4.3 256kB Flash Memory

The internal 256kB Flash memory is used to store a boot loader or user application of the FT90x series. It is a high performance and low power consumption memory that supports upto 80MHz serial clock. The system will perform memory copy from Flash memory to CPU program memory automatically after system power on.

4.4 Boot Sequence

After the initial memory copy completes, the CPU jumps to program memory location zero. This may be the start of the user application which is stored in advance in Flash memory, or a boot loader only which allows program memory to perform modification via (e.g.) UART or USB.

The option of a boot loader is a special purpose routine in the FT90x series embedded microcontroller. It is a small routine stored in the Flash memory. Typically the boot loader is 1-4kbytes in size, and is loaded at the top of the available memory.