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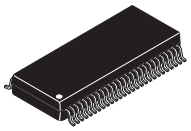
Document Number: MM908E621
Rev. 6.0, 4/2012

RoHS

Integrated Quad Half-bridge and Triple High Side with Embedded MCU and LIN for High End Mirror

908E621

QUAD HALF-BRIDGE AND TRIPLE HIGH SIDE SWITCH WITH EMBEDDED MCU AND LIN



EK (Pb-Free)
98ASA10712D
54-PIN SOICW-EP

The 908E621 is an integrated single package solution that includes a high performance HC08 microcontroller with a SMARTMOS analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), a 10 bit analog-to-digital converter (ADC), internal serial peripheral interface (SPI), and an internal clock generator module (ICG). The analog control die provides four half-bridge and three high side outputs with diagnostic functions, a Hall effect sensor input, analog inputs, voltage regulator, window watchdog, and local interconnect network (LIN) physical layer.

The single package solution, together with LIN, provides optimal application performance adjustments and space saving PCB design. It is well-suited for the control of automotive high end mirrors.

Features

- High performance M68HC908EY16 core
- 16 KB of on-chip flash memory, 512 B of RAM
- Two 16-bit, two-channel timers
- LIN physical layer interface
- Autonomous MCU watchdog / MCU supervision
- One analog input with switchable current source
- Four low $R_{DS(ON)}$ half-bridge outputs
- Three low $R_{DS(ON)}$ high side outputs
- Wake-up and 2 or 3-pin Hall effect sensor input
- 12 microcontroller I/Os
- Pb-free packaging designated by suffix codes EK

ORDERING INFORMATION		
Device (Add an R2 suffix for Tape and reel orders)	**Temperature Range (T_A)**	**Package**
MM908E621ACPEK	-40 to 85°C	54 SOICW-EP

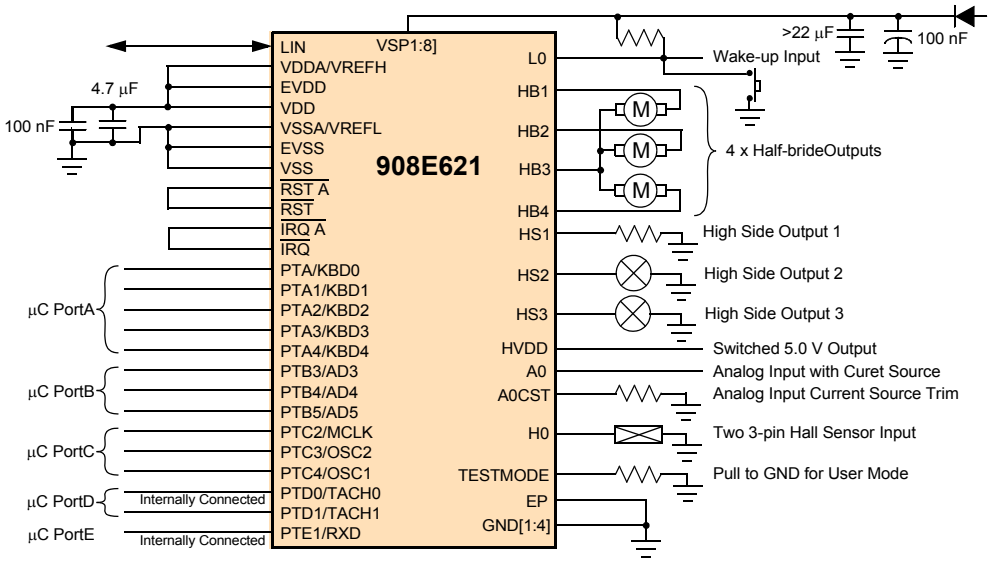


Figure 1. 908E621 Simplified Application Diagram

freescale

INTERNAL BLOCK DIAGRAM

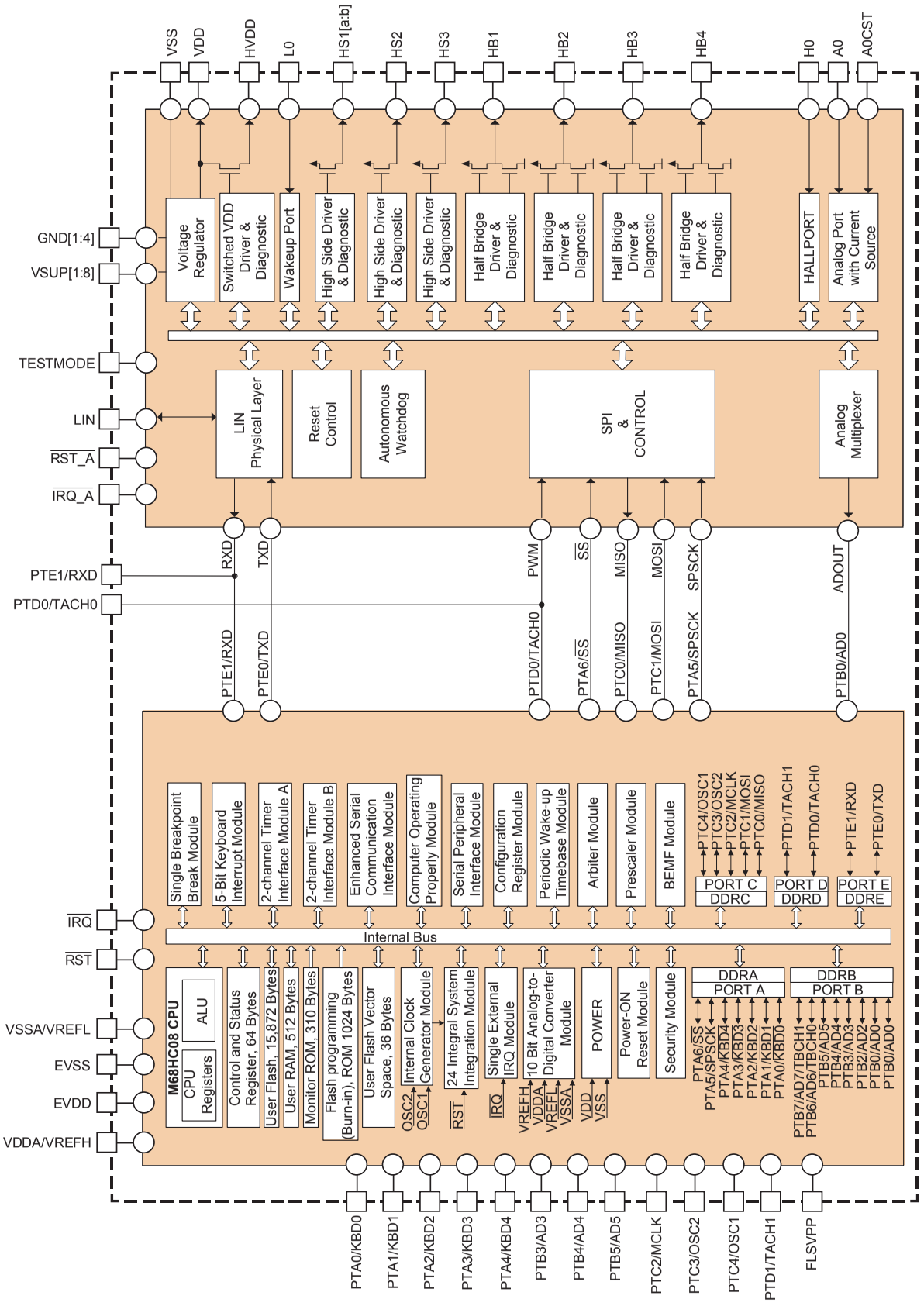


Figure 2. 908E621 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

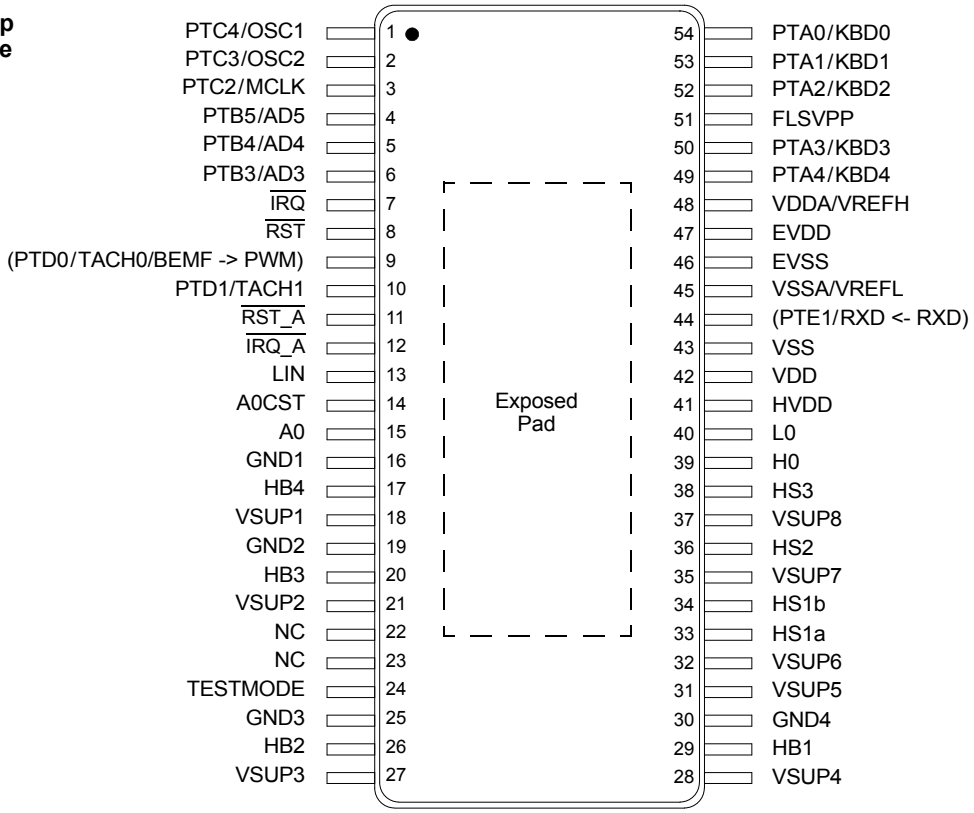


Figure 3. Pin Connections

Table 1. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 3	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	4 5 6	PTB5/AD5 PTB4/AD4 PTB3/AD3	Port B I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	7	$\overline{\text{IRQ}}$	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	8	$\overline{\text{RST}}$	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU / Analog	9	(PTD0/TACH0/BEMF -> PWM)	PWM signal	This pin is the PWM signal test pin. It internally connects the MCU PTD0/TACH0 pin with the Analog die PWM input. Note: Do not connect in the application.
MCU	10	PTD1/TACH1	Port D I/Os	This pin is a special function, bidirectional I/O port pin that is shared with other functional modules in the MCU.
MCU / Analog	44	(PTE1/RXD <- RXD)	LIN Transceiver Output	This pin is the LIN Transceiver output test pin. It internally connects the MCU PTE1/RXD pin with the Analog die LIN transceiver output pin RXD. Note: Do not connect in the application.

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Die	Pin	Pin Name	Formal Name	Definition
MCU	45 48	VSSA/VREFL VDDA/VREFH	ADC Supply and Reference Pins	These pins are the power supply and voltage reference pins for the analog-to-digital converter (ADC).
MCU	46 47	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	11	$\overline{\text{RST\_A}}$	Internal Reset	This pin is the bidirectional reset pin of the analog die.
Analog	12	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	13	LIN	LIN Bus	This pin represents the single wire bus transmitter and receiver.
Analog	14	A0CST	Analog Input Trim Pin	This is the analog input trim pin for the A0 input. This is to connect a known fixed resistor value to trim the current source measurement.
Analog	15	A0	Analog Input Pin	This pin is an analog input port with selectable source values.
Analog	16 19 25 30	GND1 GND2 GND3 GND4	Power Ground Pins	These pins are device power ground connections.
Analog	29 26 20 17	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for DC motor drivers, or as high side and low side switches. Note: The HB3 and HB4 have a lower $R_{DS(ON)}$ then HB1 and HB2.
Analog	18 21 27 28 31 32 35	VSUP1 VSUP2 VSUP3 VSUP4 VSUP5 VSUP6 VSUP7	Power Supply Pins	These pins are device power supply pins.
–	22 23	NC NC	No Connect	These pins are not connected.
Analog	24	TESTMODE	TESTMODE Input	Pin for test purpose only. In application this pin needs to be tied GND.
Analog	34 35	HS1a HS1b	High Side HS1 Output	This output pin is a low $R_{DS(ON)}$ high side switch.
Analog	36 38	HS2 HS3	High Side HS2 Output High Side HS3 Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	39	H0	Hall-Effect Sensor / General Purpose Input	This pin provides an input for a Hall-effect sensor or general purpose input.
Analog	40	L0	Wake-up Input	This pin provides an high voltage input, which is wake-up capable.
Analog	41	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g. potentiometers.
Analog	42	VDD	Voltage Regulator Output	The +5. V voltage regulator output pin is intended to supply the embedded microcontroller.

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 19.

Die	Pin	Pin Name	Formal Name	Definition
Analog	43	VSS	Voltage Regulator Ground	Ground pin for the connection of all non-power ground connections (microcontroller and sensors).
–	EP	Exposed Pad	Exposed Pad	The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-state) Analog Chip Supply Voltage under Transient Conditions(1) MCU Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 5.5	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins except VDD, VSS, PTA0:PTA4 PTA0:PTA4	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-state) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 16)	 $V_{BUS(SS)}$ $V_{BUS(PK)}$	 -18 to 40 -150 to 100	V
ESD Voltage(2) Human Body Model H0 pin Human Body Model all other pins Machine Model Charge Device Model	 V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3}	 ±1000 ±2000 ±200 ±750	V

Notes
1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Ambient Temperature[3]	T_A	-40 to 85	°C
Operating Junction Temperature[4]	T_J	-40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Reflow[5], [6]	T_{PPRT}	Note 6	°C

Notes

3. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
4. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150 °C under these conditions.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal Operating Voltage	V_{SUP1}	9.0	—	16	V
Extended Operating Voltage (LIN only 8…18 V)(8)	V_{SUP2}	7.5	—	20	V
SUPPLY CURRENT RANGE					
Normal Mode(8) V_{SUP} = 12 V, Analog Chip in Normal Mode (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	25	—	mA
Stop Mode(8), (9) V_{SUP} = 12 V, Voltage Regulator with limited current capability	I_{STOP}	—	40	50	µA
Sleep Mode(8), (9) V_{SUP} = 12 V, Voltage Regulator off	I_{SLEEP}	—	12	20	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output pins $\overline{RST\_A}$, $\overline{IRQ\_A}$, RXD (MISO probe only)					V
Low-state Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High-state Output Voltage (I_{OUT} = 250 µA)	V_{OH}	3.85	–	–	
Output pin RXD - Capacitance(10)	C_{OUT}	–	4.0	–	pF
Input pins $\overline{RST\_A}$, PWM ($\overline{SS}$, MOSI, TXD probe only)					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input pins - Capacitance(10)	C_{IN}	–	4.0	–	pF
Pins $\overline{IRQ\_A}$, $\overline{RST\_A}$ - Pull-up Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Pins $\overline{SS}$ - Pull-up Resistor	$R_{PULLUP2}$	–	100	–	kΩ
Pins MOSI, SPSCK, PWM - Pull-down Resistor	$R_{PULLDOWN}$	–	100	–	kΩ
Pin TXD - Pull-up Current Source	I_{PULLUP}	–	35	–	µA

Notes

7. Device is fully functional, but some of the parameters might be out of spec.
8. Total current measured at GND pins.
9. Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
10. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low Voltage Reset (LVR)					
Threshold	V_{LVRON}	3.8	4.2	4.65	V
Hysteresis	V_{LVR_HYS}	50	–	300	mV
Low Voltage Interrupt (LVI)					V
Threshold	V_{LVION}	6.0	–	7.5	
Hysteresis	V_{LVI_HYS}	0.3	–	0.8	
High Voltage Interrupt (HVI)					V
Threshold	V_{HVION}	20	–	24	
Hysteresis	V_{HVI_HYS}	0.5	–	1.5	
High Temperature Interrupt (HTI)[11]					°C
Threshold T_J	T_{ION}	125	–	150	
Hysteresis	T_{IH}	5.0	–	10.0	
High Temperature Reset (HTR)[11]					°C
Threshold T_J	T_{RON}	155	–	180	
Hysteresis	T_{IH}	5.0	–	10.0	
VOLTAGE REGULATOR[12]					
Normal Mode Output Voltage[13]					V
I_{OUT} = 60 mA, 7.5 V < V_{SUP} < 20 V	V_{DDRUN1}	4.75	5.0	5.25	
I_{OUT} = 60 mA, V_{SUP} < 7.5 V and V_{SUP} > 20 V	V_{DDRUN2}	4.75	5.0	5.25	
Normal Mode Total Output Current	I_{OUTRUN}	–	120	150	mA
Load Regulation - I_{OUT} = 60 mA, V_{SUP} = 9.0 V, T_J = 125 °C	V_{LR}	–	–	100	mV
STOP Mode Output Voltage[13]	V_{DDSTOP}	4.75	5.0	5.25	V
STOP Mode Total Output Current	$I_{OUTSTOP}$	150	500	1100	µA

Notes

11. This parameter is guaranteed by process monitoring but is not production tested.
12. Specification with external low ESR ceramic capacitor 1.0 µF< C < 4.7 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Its not recommended to use capacitor values above 4.7 µF
13. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pull-up Resistor to VSUP	R_{PU}	20	30	47	kΩ
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	20	—	µA
Output Current Shutdown Threshold	I_{BLIM}	100	230	280	mA
Output Current Shutdown Timing	I_{BLS}	5.0	–	40	µs
Leakage Current to GND					
V_{SUP} Disconnected, V_{BUS} at 18 V	I_{BUS}	–	1.0	10	µA
Recessive state, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V ≤ V_{BUS} ≤ 18 V, V_{BUS} ≥ V_{SUP}	$I_{BUS\text{-}PAS\text{-}REC}$	0.0	3.0	20	µA
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V	$I_{BUS\text{-}NOGND}$	-1.0	–	1.0	mA
LIN Receiver					VSUP
Receiver Threshold Dominant	V_{BUS_DOM}	–	–	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	–	–	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	–	–	0.175	
HIGH SIDE OUTPUT HS1					
Switch On Resistance					mΩ
T_J = 25 °C, I_{LOAD} = 1.0 A	$R_{DS(ON)\text{-}HS1}$	–	185	225	
Over-current Shutdown	I_{HSOC1}	6.0	–	9.0	A
Over-current Shutdown blanking time[14]	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio[15]	$CR_{RATIOHS1}$	0.84	1.2	1.56	V/A
V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2.0 A)					
High Side Switching Frequency[14]	f_{PWMHS}	–	–	25	kHz
High Side Freewheeling Diode Forward Voltage	V_{HSF}	–	0.9	–	V
T_J = 25 °C, I_{LOAD} = 1.0 A					
Leakage Current	I_{LeakHS}	–	<0.2	10	µA

Notes
14. This parameter is guaranteed by process monitoring but is not production tested.
15. This parameter is guaranteed only if correct trimming was applied.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUTS HS2 AND HS3(18)					
Switch On Resistance T_J = 25 °C, I_{LOAD} = 1.0 A	$R_{DS(ON)-HS23}$	–	440	500	mΩ
Over-current Shutdown	I_{HSOC23}	3.6	–	5.6	A
Over-current Shutdown blanking time(16)	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio(17) V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2.0 A)	$CR_{RATIOHS23}$	1.16	1.66	2.16	V/A
High Side Switching Frequency(16)	f_{PWMHS}	–	–	25	kHz
High Side Freewheeling Diode Forward Voltage T_J = 25 °C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	V
Leakage Current	I_{LEAKHS}	–	<0.2	10	µA
HALF-BRIDGE OUTPUTS HB1 AND HB2					
Switch On Resistance High Side, T_J = 25°C, I_{LOAD} = 1.0A Low Side, T_J = 25°C, I_{LOAD} = 1.0A	$R_{DS(ON)-HB12}$	 – –	 750 750	 900 900	mΩ
Over-current Shutdown High Side Low Side	I_{HBOC12}	 1.0 1.0	 – –	 1.5 1.5	A
Over-current Shutdown blanking time(19)	t_{OCB}	–	4-8	–	µs
Switching Frequency(19)	f_{PWM}	–	–	25	kHz
Freewheeling Diode Forward Voltage High Side, T_J = 25 °C, I_{LOAD} = 1.0 A Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A	 V_{HSF} V_{LSF}	 – –	 0.9 0.9	 – –	V
Leakage Current	I_{LEAKHB}	–	<0.2	10	µA
Low Side Current to Voltage Ratio(20) V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HB} = 200 mA) V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HB} = 500 mA)	$CR_{RATIOHB12}$	 17.5 3.5	 25.0 5.0	 32.5 6.5	V/A

Notes
16. This parameter is guaranteed by process monitoring but is not production tested.
17. This parameter is guaranteed only if correct trimming was applied.
18. The high side HS3 can be only used for resistive loads.
19. This parameter is guaranteed by process monitoring but is not production tested.
20. This parameter is guaranteed only if correct trimming was applied

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALF-BRIDGE OUTPUTS HB3 AND HB4					
Switch On Resistance	$R_{DS(ON)-HB34}$				mΩ
High Side, T_J = 25 °C, I_{LOAD} = 1.0 A		–	275	325	
Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A		–	275	325	
Over-current Shutdown	I_{HBOC34}				A
High Side		4.8	–	7.2	
Low Side		4.8	–	7.2	
Over-current Shutdown blanking time(21)	t_{OCB}	–	4-8	–	µs
Switching Frequency(21)	f_{PWM}	–	–	25	kHz
Freewheeling Diode Forward Voltage					V
High Side, T_J = 25 °C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	
Low Side, T_J = 25 °C, I_{LOAD} = 1.0 A	V_{LSF}	–	0.9	–	
Leakage Current	I_{LEAKHB}	–	<0.2	10	µA
Low Side Current to Voltage Ratio(22)	$CR_{RATIOHB34}$				V/A
V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HB} = 500 mA)		3.5	5.0	6.5	
V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HB} = 2.0 A)		0.7	1.0	1.3	
SWITCHABLE V_{DD} OUTPUT HVDD					
Over-current Shutdown	I_{HVDDOC}	25	35	50	mA
Over-current Shutdown Blanking Time(23)	$t_{HVDDOCB}$				µs
HVDDT1:0 = 00		–	950	–	
HVDDT1:0 = 01		–	536	–	
HVDDT1:0 = 10		–	234	–	
HVDDT1:0 = 11		–	78	–	
Over-current Flag Delay(23)	$t_{HVDDOCFD}$	–	0.5	–	ms
Dropout Voltage @ I_{LOAD} = 20 mA	$V_{HVDDDROP}$	–	110	300	mV
V_{SUP} DOWN SCALER(24)					
Voltage Ratio (RATIO $_{VSUP}$ = V_{SUP} / V_{ADOUT})	$RATIO_{VSUP}$	4.75	5.0	5.25	–
INTERNAL DIE TEMPERATURE SENSOR(24)					
Voltage / Temperature Slope(23)	S_{TTOV}	–	26	–	mV/°C
Output Voltage @25°C	V_{T25}	1.7	1.9	2.1	V

Notes
21. This parameter is guaranteed by process monitoring but is not production tested.
22. This parameter is guaranteed only if correct trimming was applied
23. This parameter is guaranteed by process monitoring but is not production tested.
24. This parameter is guaranteed only if correct trimming was applied

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALL-EFFECT SENSOR INPUT H0 - GENERAL PURPOSE INPUT MODE (H0MS = 0)					
Input Voltage Low Threshold	V_{LT}	–	–	1.5	V
Input Voltage High Threshold	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{HH}	100	–	500	mV
Pull-up resistor	R_{PH}	7.0	10	13	kΩ
HALL-EFFECT SENSOR INPUT H0 - 2PIN HALL SENSOR INPUT MODE (H0MS = 1)					
Output Voltage V_{SUP} < 17 V V_{SUP} >17 V	 V_{HALL1} V_{HALL2}	 – –	 V_{SUP}-1.2 –	 – 15.8	V
Output Drop @ I_{OUT} = 15 mA	V_{H0D}	–	–	2.5	V
Sense Current Threshold	I_{HSCT}	6.0	7.9	10	mA
Sense Current Hysteresis	I_{HSCH}	650	–	1650	µA
Sense Current Limitation	V_{HSCLIM}	20	40	70	mA
ANALOG INPUT A0, A0CST					
Current Source A0, A0CST[25], [26] CSSEL1:0 = 00 CSSEL1:0 = 01 CSSEL1:0 = 10 CSSEL1:0 = 11	 I_{CS1} I_{CS2} I_{CS3} I_{CS4}	 – – – –	 40 120 320 800	 – – – –	µA
WAKE-UP INPUT L0					
Input Voltage Threshold Low	V_{LT}	–	–	1.5	V
Input Voltage Threshold High	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{LH}	0.5	–	–	V
Input Current	I_N	-10	–	10	µA
Wake-up Filter Time[27]	t_{WUP}	–	20	–	µs

Notes
25. This parameter is guaranteed only if correct trimming was applied
26. The current values are optimized to read a NTC temperature sensor, e.g. EPCOS type B57861 (R25 = 3000Ω, R/T characteristic 8016)
27. This parameter is guaranteed by process monitoring but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate(28), (29)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Duty Cycle 1: D1 = $t_{BUS\_REC(MIN)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.0 V…18 V	D1	0.396	–	–	
Duty Cycle 2: D2 = $t_{BUS\_REC(MAX)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.6 V…18 V	D2	–	–	0.581	
Driver Characteristics for Slow Slew Rate(28), (30)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Duty Cycle 3: D3 = $t_{BUS\_REC(MIN)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.0 V…18 V	D3	0.417	–	–	
Duty Cycle4: D4 = $t_{BUS\_REC(MAX)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.6 V…18 V	D4	–	–	0.590	
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	20	—	V/µs
Receiver Characteristics and Wake-up Timings					
Receiver Dominant Propagation Delay(31)	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay(31)	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-up Deglitcher	t_{PROPWL}	30	50	150	µs
Bus Wake-up Event Reported(32)	t_{WAKE}	—	20	—	µs

Notes

28. V_{SUP} from 7.0 to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
29. See Figure 6, page 16.
30. See Figure 7, page 17.
31. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
32. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 9 and Figure 8, page 17. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD pin.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency(33)	f_{SPIOP}	0.25	—	4.0	MHz
State Machine					
Reset Low Level Duration after V_{DD} High	t_{RST}	0.8	1.25	1.94	ms
Normal Request Timeout	$t_{NORMREQ}$	51	80	150	ms
Window Watchdog Timer(34)					
Watchdog Period (WDP1:0 = 00)	t_{WD80}	52	80	124	ms
Watchdog Period (WDP1:0 = 01)	t_{WD40}	26	40	62	ms
Watchdog Period (WDP1:0 = 10)	t_{WD20}	13	20	31	ms
Watchdog Period (WDP1:0 = 11)	t_{WD10}	6.5	10	15.5	ms

Notes

33. This parameter is guaranteed by process monitoring but is not production tested.
34. This parameter is guaranteed only if correct trimming was applied. Additionally See Watchdog Period Range Value (AWD Trim) on page 46

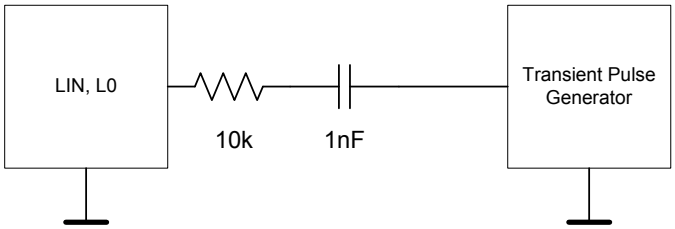
MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 k Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud Rate Adjustment
ICG	Internal Clock Generation Module

TIMING DIAGRAMS



Note: Waveform in accordance to ISO7637 part 1, test pulses 1, 2, 3a and 3b.

Figure 4. Test Circuit for Transient Test Pulses

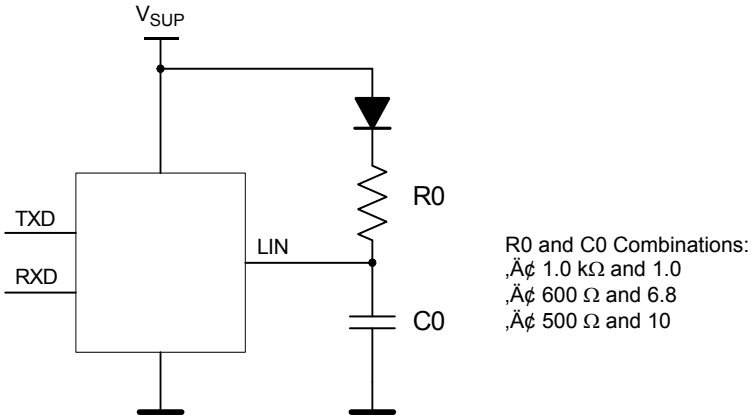


Figure 5. Test Circuit for LIN Timing Measurements

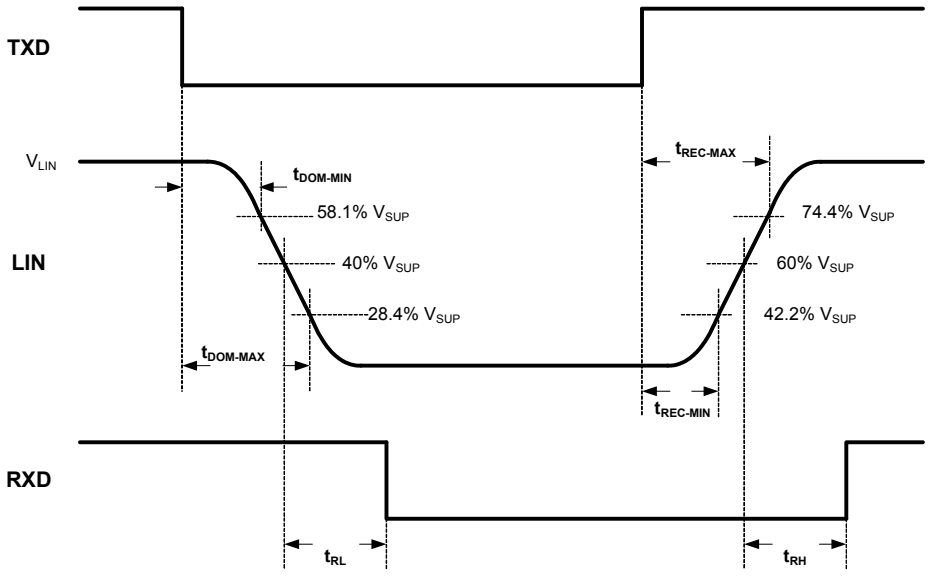


Figure 6. LIN Timing Measurements for Normal Slew Rate

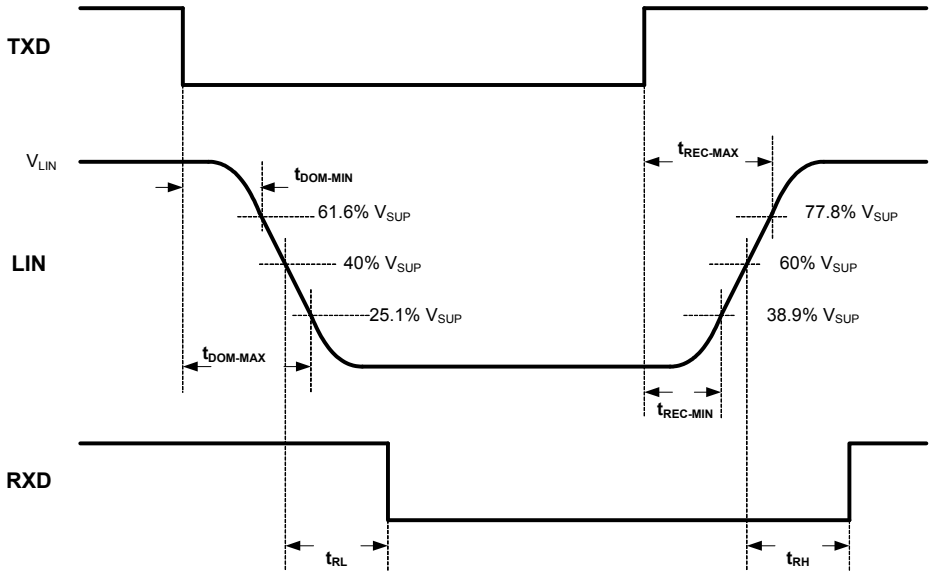


Figure 7. LIN Timing Measurements for Slow Slew Rate

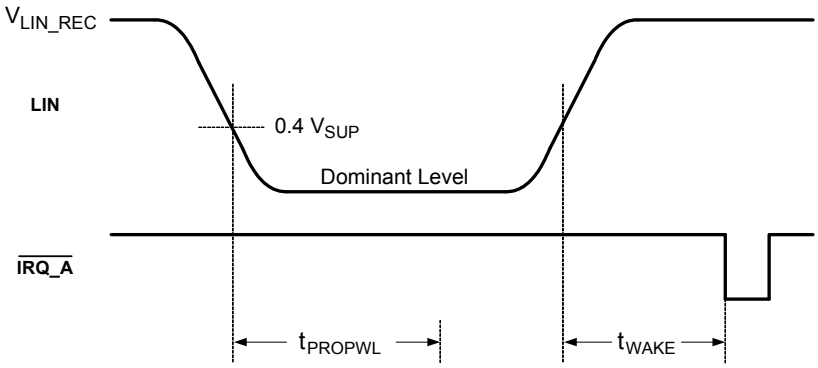


Figure 8. Wake-up Stop Mode Timing

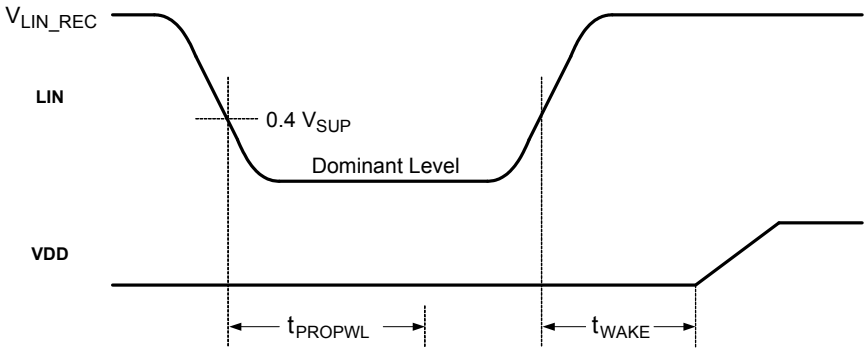


Figure 9. Wake-up Sleep Mode Timing

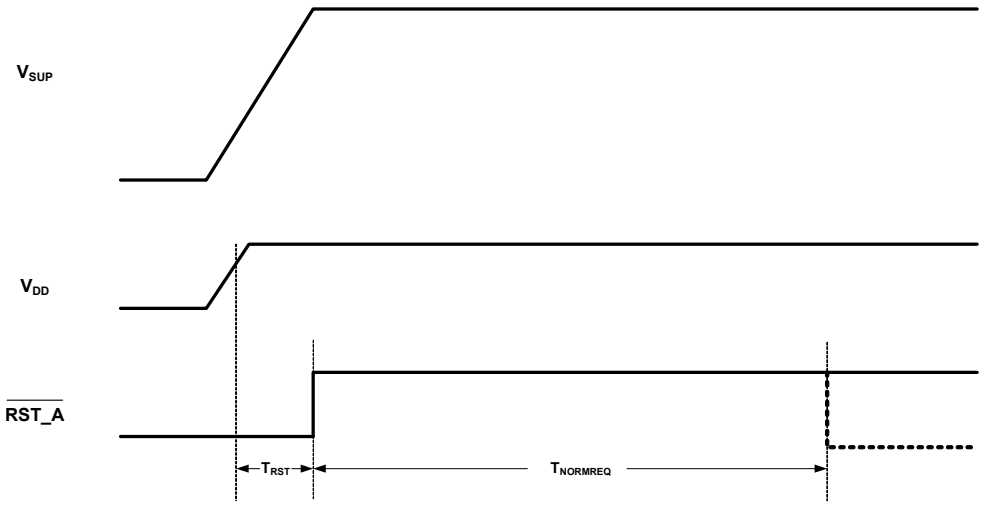


Figure 10. Power On Reset and Normal Request Timeout Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E621 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E621 is well suited to perform complete mirror control via a three wire LIN bus.

This device combines an HC908EY16 MCU core with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as half-bridge outputs and three high side switches. Other ports are also provided, which include one Hall-effect sensor input port, one analog input port with a switched current source, one wake-up pin, and a selectable HVDD pin. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See Figure 2, 908E621 Simplified Internal Block Diagram, page 2, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 3 for a depiction of the pin locations on the package.

PORT A I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die.

The PTA6/$\overline{SS}$ pin is not accessible in this device and is internally connected to the SPI slave select input of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated (e.g., current recopy, V_{SUP}, etc.).

The PTB1/AD1, PTB2/AD2, PTB6/AD6/TBCH0, PTB7/AD7/TBCH1 pins are not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O PINS

PTD0/TACH0/BEMF and PTD1/TACH1 are special function, bi-directional I/O port pins that can also be programmed to be timer pins.

PTD0/TACH0 pin is internally connected to the PWM input of the analog die and only accessible for test purposes (can not be used in the application).

For details refer to the 68HC908EY16 datasheet.

PORT E I/O PIN

PTE0/TXD and PTE1/RXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

PTE1/RXD is internally connected to the RXD pin of the analog die and only accessible for test purposes (can not be used in the application).

For details refer to the 68HC908EY16 datasheet.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET PIN ($\overline{\text{RST}}$)

A logic [0] on the $\overline{\text{RST}}$ pin forces the MCU to a known startup state. $\overline{\text{RST}}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

POWER SUPPLY PINS (VSUP1:VSUP8)

VSUP1:VSUP8 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1:GND4)

GND1:GND4 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E621 device includes power MOSFETs configured as four half-bridge driver outputs. The HB3:HB4 have a lower $R_{DS(ON)}$, to run higher currents (e.g. fold motor), than the HB1:B2 outputs.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy. Over-current protection is done on both high side and low side FET's. The current recopy are done on the low side MOSFETs.

HIGH SIDE OUTPUT PINS (HS1:HS3)

The HS output pins are a low $R_{DS(ON)}$ high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM or feature a real PWM capability using the PWM input.

The HS1 has a lower $R_{DS(ON)}$, to run higher currents (e.g. heater), than the HS2 and HS3 outputs.

For the HS1 two pins (HS1a:HS1b) are necessary for the current capability and have to be connected externally.

Important: The HS3 can be only used to drive resistive loads.

HALL-EFFECT SENSOR INPUT PIN (H0)

The Hall-effect sensor input pin H0 provides an input for Hall-effect sensors (2-pin or 3-pin) or a switch.

ANALOG INPUT PINS (A0, A0CST)

These pins are analog inputs with selectable current source values. The A0CST intent is to trim the A0 input.

WAKE-UP INPUT PIN (L0)

This pin is 40 V rated input. It can be used as wake-up source for a system wake-up. The input is falling or rising edge sensitive.

Important: If unused this pin should be connected to VSUP or GND to avoid parasitic transitions. In Low Power mode this could lead to random wake-up events.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply (e.g., 3 pin Hall-effect sensors or potentiometers). The output is short-circuit protected.

LIN BUS PIN (LIN)

The LIN pin represents the single wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important: The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD and VDDA/VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors). **Important**: VSS, EVSS and VSSA/VREFL pins must be connected together.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pullup resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pullup resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

ADC SUPPLY/REFERENCE PINS (VDDA/VREFH AND VSSA/VREFL)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC).

VREFH and VREFL are the reference voltage pins for the ADC.

The supply and reference signals are internally connected.

It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

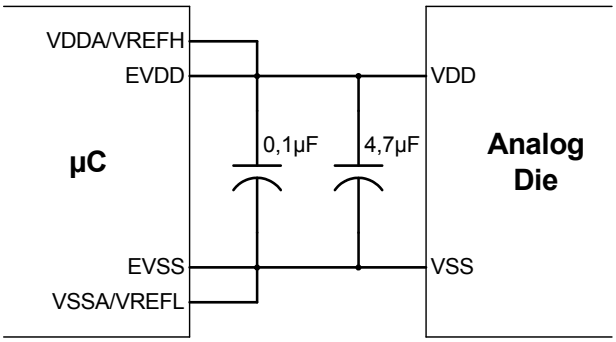
For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.



TEST MODE PIN (TESTMODE)

This pin is for test purpose only. In the application this pin has to be forced to GND.

For Programming/Test this pin has to be forced to V_{DD} to bring the analog die into Test mode. In Test mode the Reset Timeout (80 ms) is disabled and the LIN receiver is disabled

NOTE: After detecting a RESET (internal or external), the PSON bit needs to be set within 80 ms. If not, the device will automatically enter sleep mode.

MCU TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should either be left open (not connected) or can be connected to GND.

NO CONNECT PINS (NC)

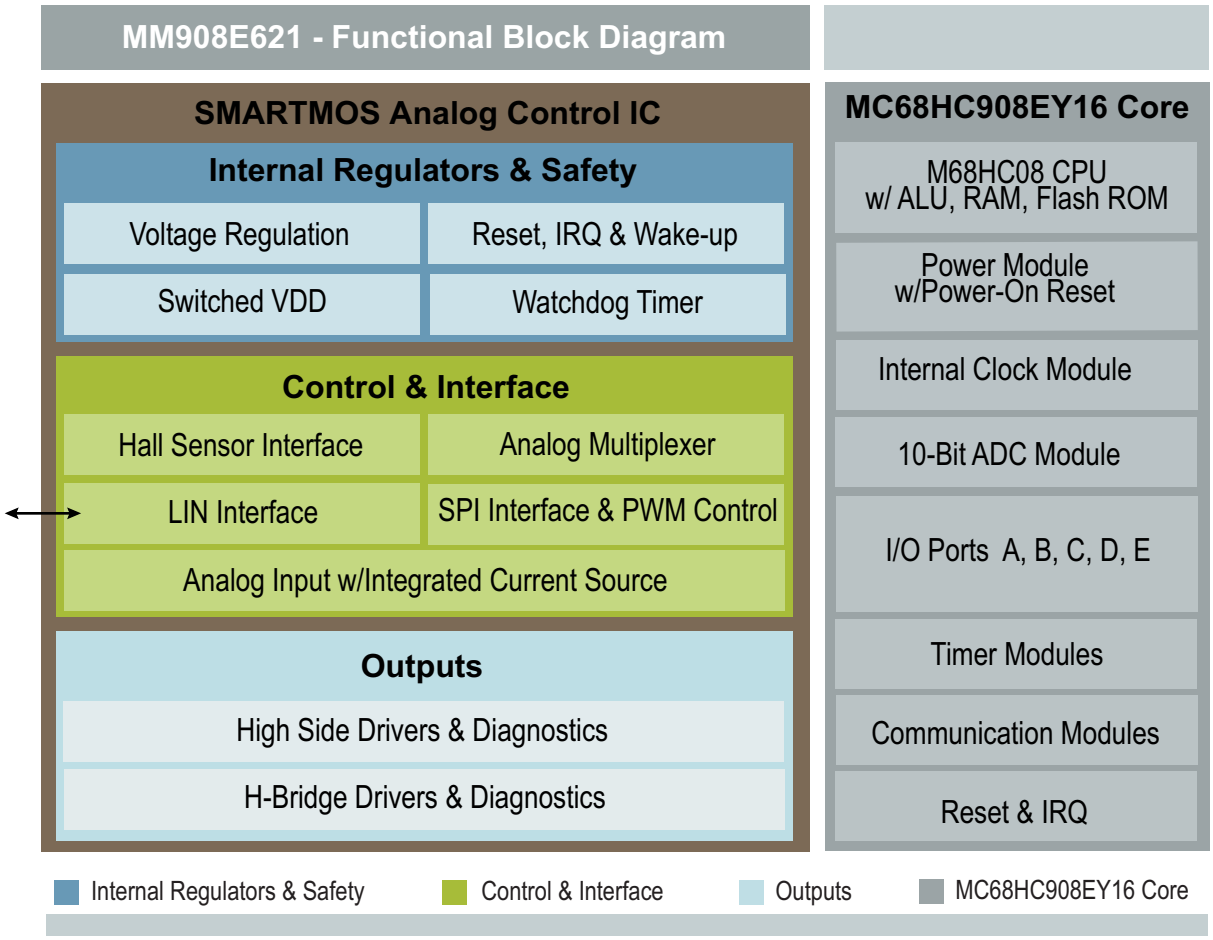
The NC pins are not connected internally.

Note: Each of the NC pins can be left open or connected to ground (recommended).

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance, the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



SMARTMOS ANALOG CONTROL IC

INTERNAL REGULATORS & SAFETY:

VOLTAGE REGULATION

The voltage regulator circuitry provides the regulated voltage for the Analog IC as well as the VDD/VSS rails for the core IC. The on-chip regulator consists of two elements, the main regulator, and the low voltage reset circuit. The V_{DD} regulator accepts an unregulated input supply, and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin, to provide the 5.0 V to the microcontroller.

SWITCHED VDD

This function provides a switchable +5.0 V V_{DD} rail for an external load.

WATCHDOG TIMER

The watchdog timer module generates a reset, in case of a watchdog timeout or wrong watchdog timer reset. A watchdog reset event will reset all registers in the SPI, excluding the RSR.

RESET, IRQ & WAKE-UP

There are several functions on the Analog IC that can generate a reset or wake-up signal to the core IC. There is a pin that is used to detect an external wake-up event. The Reset signal has many possible sources in the Analog IC circuitry. The IRQ function on the Analog IC, will notify the core IC of pending system critical conditions.

CONTROL & INTERFACE:

HALL SENSOR INTERFACE

This interface can be configured to support an input pin as a general purpose input, or as a hall-effect sensor input, to be able to read 3-pin / 2-pin hall sensors or switches.

SPI INTERFACE & PWM CONTROL

The SPI and PWM interfaces are mastered by the core IC (CPU), and are used to control the output functions of the Analog IC, as well as to report status and failure information of the Analog IC.

LIN INTERFACE

The LIN interface function supports the single wire bus transmit and receive capabilities. It is suited for automotive bus systems and is based on the LIN bus/physical layer specification. The LIN driver is a low side MOSFET with slope control, internal current limitation, and thermal shutdown.

ANALOG MULTIPLEXER

To be able to have different sources for the MCU with one single signal, an analog multiplexer is integrated in the analog IC. This multiplexer has eleven different sources on the Analog IC, which can be selected with the SS[3:0] bits (through SPI communication) in the A0MUCTL register.

ANALOG INPUT W/INTEGRATED CURRENT SOURCE

The terminal A0 provides a switchable current source, to allow the reading of switches, NTC, etc., without the need for an additional supply line for the sensor (single wire). There are four different selectable current source values.

OUTPUTS:

HIGH SIDE DRIVERS & DIAGNOSTICS

The HS outputs are low RDS(ON) high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM, or feature a real PWM capability using the PWM input.

H-BRIDGE DRIVERS & DIAGNOSTICS

The device includes power MOSFETs configured as four half-bridge driver outputs. These outputs are short-circuit and over-temperature protected. Over-current protection is done on both high side and low side MOSFETs.

MM68HC908EY16 CORE IC

M68HC08 CPU W/ALU, RAM, FLASH ROM

This possesses the functionality of the CPU08 architecture, along with 512 bytes of RAM and 15,872 bytes of FLASH memory, with in-circuit programming.

POWER MODULE W/P0WER-ON-RESET

This block of circuitry manages the power supplied to the core IC, as well as providing POR, LVI, Watchdog timer, and MCU supervision circuitry (COP).

INTERNAL CLOCK MODULE

This module provides the clocks needed by the core IC functions, without the need for external components. Software selectable bus frequencies are available. It also provides a clock monitor function.

10-BIT ADC MODULE

This module provides an 8-channel, 10-bit successive approximation analog-to-digital converter (ADC).

I/O PORTS A, B, C, D, E

There are many I/O pins that are controlled by the CPU through the several I/O ports of the core IC.

TIMER MODULES

There are two 16-bit, 2 channel timer interface modules with selectable input capture, output compare, and PWM capabilities, for each channel.

COMMUNICATION MODULES

There are several communication functions supported by the core IC, including an enhanced serial communication interface module (ESCI) for the LIN communication, and an SPI module for inter-IC communication.

RESET & IRQ

There are interrupt and reset connections between the Analog IC and the core IC, for concise control and error/ exception management.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E621 ANALOG DIE MODES OF OPERATION

The 908E621 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities.

The different modes can be selected by the STOP and SLEEP bits in the System Control Register.

Figure 11 describes how transitions are done between the different operating modes and Table 6, page 26, gives an overview of the operating modes.

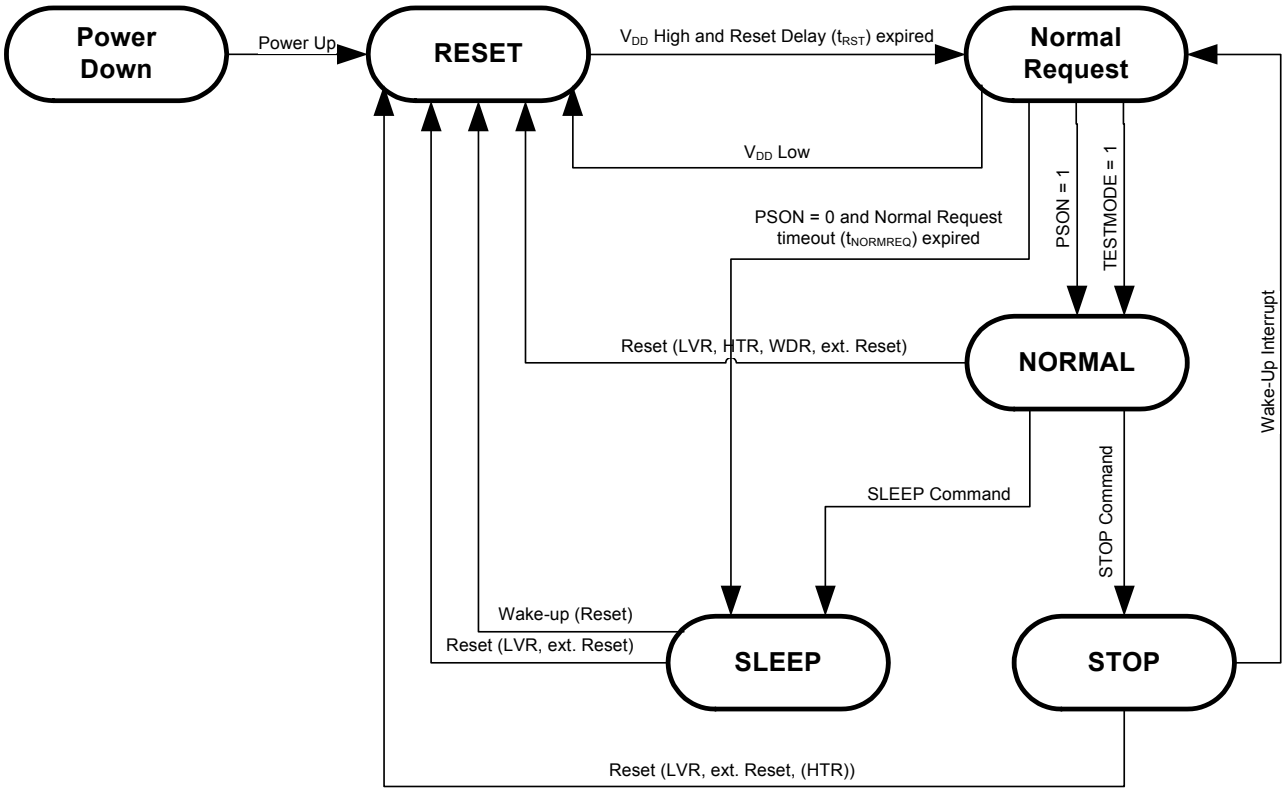


Figure 11. Operating Modes and Transitions

Normal Mode

This Mode is the normal operating mode of the device, all functions and power stages are active and can be enabled/ disabled. The voltage regulator provides the +5.0 V V_{DD} to the MCU.

After a reset (e.g. Power-On-Reset, Wake-up from Sleep), the MCU has to set the PSON bit in the System Control Register within 80 ms typical ($t_{NORMREQ}$). This is to ensure the MCU has started up and is operating correctly. If the PSON bit is not set within the required time frame, the device enters SLEEP mode to reduce power consumption (fail safe).

This MCU monitoring can be disabled (e.g. for programming) by applying V_{DD} on the TESTMODE pin.

Stop Mode

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability). To enter the Stop mode, the STOP bit in the System Control Register must be set, and the MCU has to be stopped also (see 908EY16 datasheet for details).

Wake-up from this mode is possible by the LIN bus activity or the wake-up input L0. It is maskable with the LINIE and/or L0IE bits in the Interrupt Mask Register. The analog die is generating an interrupt on $\overline{IRQ\_A}$ pin to wake-up the MCU. The wake-up / interrupt source can be evaluated with the L0IF and LINIF bits in the Interrupt Flag Register.

Stop mode has a higher current consumption than Sleep mode, but allows a quicker wake-up. Additionally the wake-

up sources can be selected (maskable), which is not possible in Sleep mode.

Figure 12 show the procedure to enter the Stop mode and how the system is waking up.

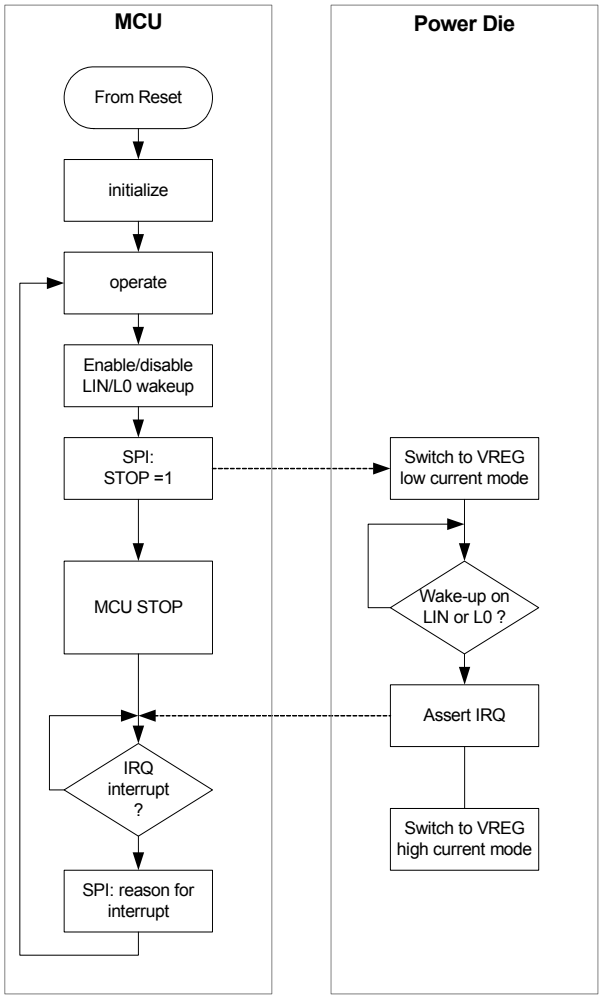


Figure 12. STOP Mode Wake-up Procedure

Sleep Mode

In Sleep mode, the voltage regulator is turned off and the MCU is not supplied (V_{DD} = 0 V), also the $\overline{RST\_A}$ pin is pulled low.

To enter the Sleep mode, the Sleep bit in the System Control Register has to be set.

Wake-up from this mode is possible by LIN bus activity or the wake-up input L0, and is not maskable. The wake-up behaves like a power on reset. The wake-up / reset source can be evaluated by the L0WF and/or LINWF bits in the Reset Status Register.

Sleep mode has a lower current consumption than Stop mode, but requires a longer time to wake-up. The wake-up sources can not be selected (not maskable).

Figure 13 show the procedure to enter the Sleep mode and how a wake-up is performed.

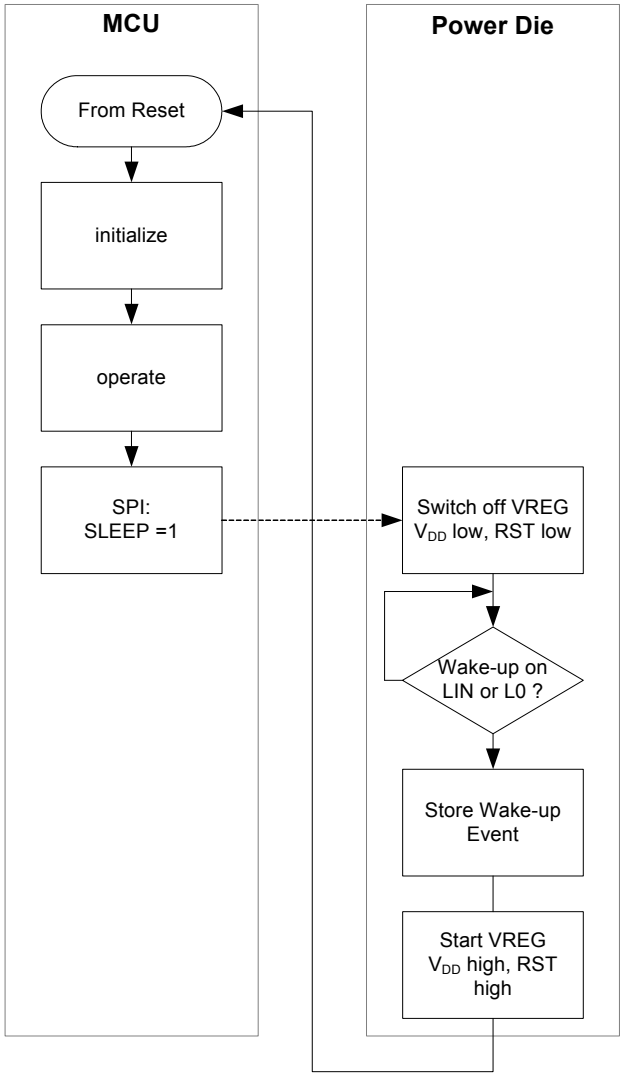


Figure 13. SLEEP Mode Wake-up Procedure

Table 6 summarized the Operating modes.