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Integrated Triple High Side Switch with Embedded MCU and LIN Serial Communication for Relay Drivers

The 908E624 is an integrated single-package solution that includes a high performance HC08 microcontroller with a SMARTMOS analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), internal serial peripheral interface (SPI), and an internal clock generator module. The analog control die provides three high side outputs with diagnostic functions, voltage regulator, watchdog, current sense operational amplifier, and local interconnect network (LIN) physical layer.

The single package solution, together with LIN, provides optimal application performance adjustments and space saving PCB design. It is well-suited for the control of automotive high current motors applications using relays (e.g., window lifts, fans, and sun roofs).

Features

- High performance M68HC908EY16 core
- 16 KB of on-chip flash memory, 512 B of RAM
- Internal clock generator module
- Two 16-bit, two-channel timers
- 10-bit ADC
- LIN physical layer interface
- Low dropout voltage regulator
- Three high side outputs
- Two wake-up inputs
- 16 microcontroller I/Os

908E624

HIGH SIDE SWITCH



ORDERING INFORMATION		
Device (Add an R2 suffix for Tape and reel orders)	Temperature Range (T _A)	Package
MM908E624ACPEW	-40°C to 85°C	54 SOICW
MM908E624AYPEW	-40°C to 125°C	

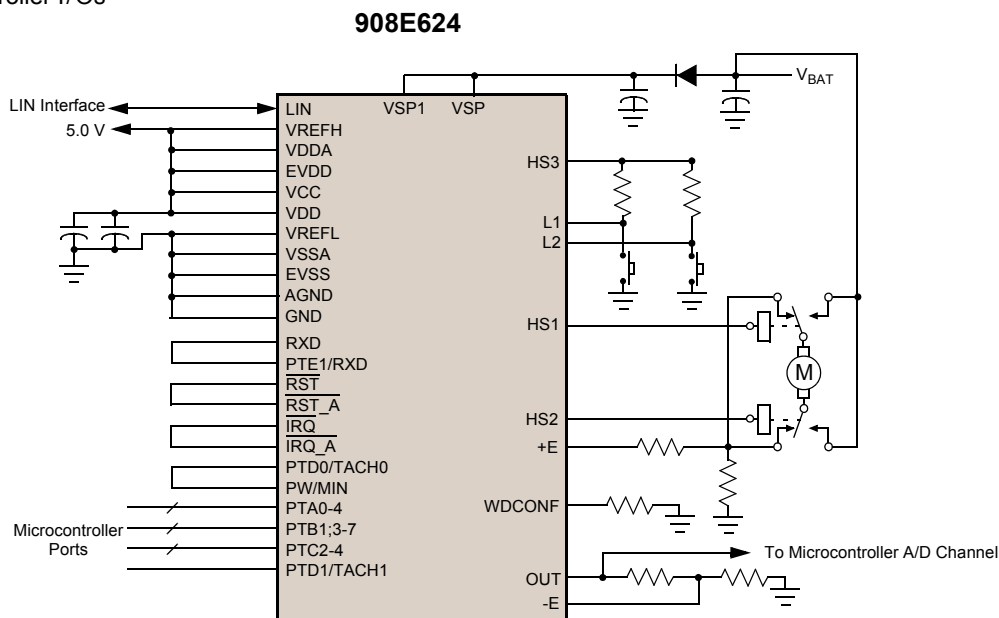


Figure 1. 908E624 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM

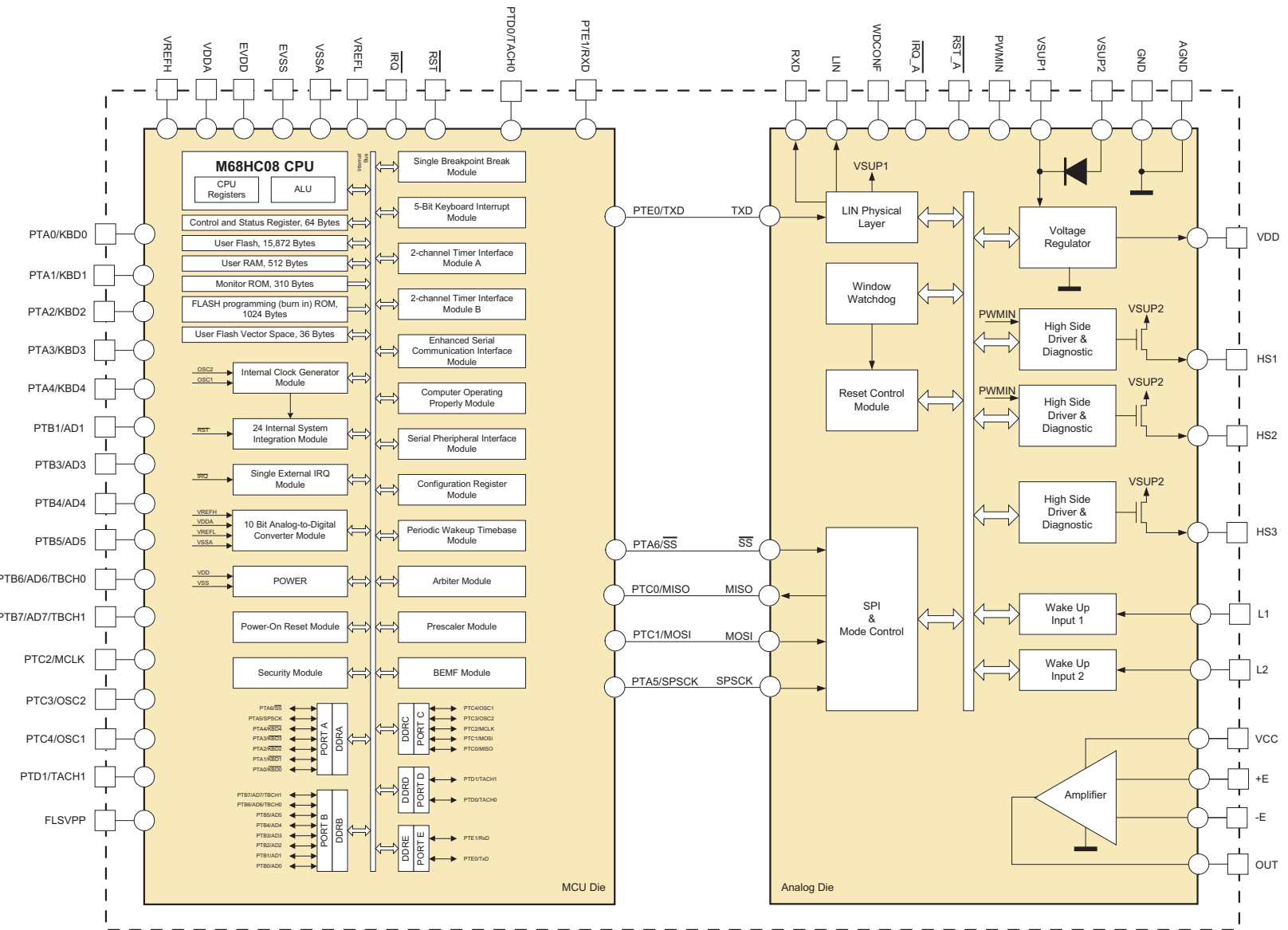


Figure 2. 908E624 Simplified Internal Block Diagram

PIN CONNECTIONS

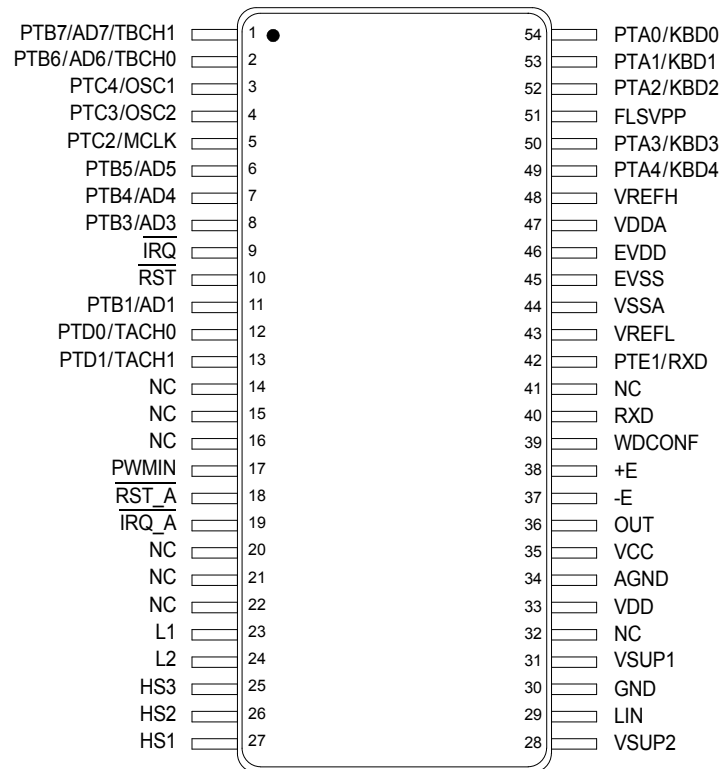


Figure 3. Pin Connections

Table 1. Pin Definitions

A functional description of each pin can be found in the [Functional Pin Description](#) section beginning on page 16.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	10	RST	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0 PTD1/TACH1	Port D I/Os	These pins are special function, bidirectional I/O port pins, that are shared with other functional modules in the MCU.
—	14, 15, 16, 20, 21, 22, 32, 41	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bidirectional I/O port pin, that can be shared with other functional modules in the MCU.

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the [Functional Pin Description](#) section beginning on page [16](#).

Die	Pin	Pin Name	Formal Name	Definition
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	17	PWMIN	Direct High Side Control Input	This pin allows the enabling and PWM control of the high side HS1 and HS2 pins.
Analog	18	RST_A	Internal Reset Output	This pin is the reset output pin of the analog die.
Analog	19	IRQ_A	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	23 24	L1 L2	Wake-Up Inputs	These pins are the wake-up inputs of the analog chip.
Analog	25 26 27	HS3 HS2 HS1	High Side Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	31 28	VSUP1 VSUP2	Power Supply Pins	These pins are device power supply pins.
Analog	29	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	30 34	GND AGND	Power Ground Pins	These pins are device power ground connections.
Analog	33	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	35	VCC	Amplifier Power Supply	This pin is the single +5.0 V power supply for the current sense operational amplifier.
Analog	36	OUT	Amplifier Output	This pin is the output of the current sense operational amplifier.
Analog	37 38	-E +E	Amplifier Inputs	These pins are the current sense operational amplifier inverted and non-inverted inputs.
Analog	39	WDCONF	Window Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
Analog	40	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-state)	$V_{SUP(SS)}$	-0.3 to 27	
Analog Chip Supply Voltage under Transient Conditions	$V_{SUP(PK)}$	-0.3 to 40	
MCU Chip Supply Voltage	V_{DD}	-0.3 to 5.5	
Input Pin Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to $V_{DD}+0.3$	
Microcontroller Chip	$V_{IN(MCU)}$	$V_{SS}-0.3$ to $V_{DD}+0.3$	
Maximum Microcontroller Current per Pin			mA
All Pins except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
PTA0:PTA6, PTC0:PTC1 Pins	$I_{PIN(2)}$	±25	
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
Current Sense Operational Amplifier			
Maximum Input Voltage, +E, -E Pins	V_{+E-E}	-0.3 to 7.0	V
Maximum Input Current, +E, -E Pins	I_{+E-E}	±20	mA
Maximum Output Voltage, OUT Pin	V_{OUT}	-0.3 to $V_{CC}+0.3$	V
Maximum Output Current, OUT Pin	I_{OUT}	±20	mA
LIN Supply Voltage			V
Normal Operation (Steady-state)	$V_{BUS(SS)}$	-18 to 40	
Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4 , page 13)	$V_{BUS(PK)}$	-150 to 100	
L1 and L2 Pin Voltage			V
Normal Operation with a 33 kΩ resistor (Steady-state)	$V_{WAKE(SS)}$	-18 to 40	
Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4 , page 13)	$V_{WAKE(PK)}$	-100 to 100	
ESD Voltage			V
Human Body Model ⁽¹⁾	V_{ESD1}	±2000	
Machine Model ⁽¹⁾	V_{ESD2}	±100	
Charge Device Model ⁽¹⁾	V_{ESD3}	±500	

Notes

- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), the Machine Model ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0$ Ω), and the Charge Device Model, Robotic ($C_{ZAP} = 4.0$ pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Package Operating Ambient Temperature ⁽⁴⁾ MM908E624ACPEW MM908E624AYPEW	T_A	-40 to 85 -40 to 125	°C
Operating Junction Temperature ⁽²⁾⁽⁴⁾ MM908E624ACPEW MM908E624AYPEW	T_J	-40 to 125 -40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Reflow ⁽³⁾⁽⁵⁾	T_{PPRT}	Note 5	°C

Notes

- The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation of the analog die. The analog die junction temperature must not exceed 150°C under these conditions.
- Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Independent of T_A , device parametrics are only guaranteed for $-40 < T_J < 125$ °C. Please see note 2. T_J is a factor of power dissipation, package thermal resistance, and available heat sinking.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_{\text{J}} \leq 125\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal Operating Voltage	V_{SUP}	5.5	—	18	V
Functional Operating Voltage ⁽⁶⁾	V_{SUPOP}	—	—	27	V
SUPPLY CURRENT RANGE					
Normal Mode ⁽⁷⁾ $V_{\text{SUP}} = 13.5\text{ V}$, Analog Chip in Normal Mode, MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	20	—	mA
Stop Mode ^{(7), (8)} $V_{\text{SUP}} = 13.5\text{ V}$, LIN in recessive state	I_{STOP}	—	60	75	μA
Sleep Mode ^{(7), (8)} $V_{\text{SUP}} = 13.5\text{ V}$, LIN in recessive state	I_{SLEEP}	—	35	45	μA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Pin $\overline{\text{RST_A}}$ Low-state Output Voltage ($I_{\text{OUT}} = -1.5\text{ mA}$) High-state Output Current ($V_{\text{OUT}} > 3.5\text{ V}$) Pull-down Current Limitation	V_{OL} I_{OH} $I_{\text{OL_MAX}}$	— — -1.5	— 250 —	0.4 — -8.0	V μA mA
Output Pin $\overline{\text{IRQ_A}}$ Low-state Output Voltage ($I_{\text{OUT}} = -1.5\text{ mA}$) High-state Output Voltage ($I_{\text{OUT}} = 250\text{ }\mu\text{A}$)	V_{OL} V_{OH}	— 3.85	— —	0.4 —	V
Output Pin RXD Low-state Output Voltage ($I_{\text{OUT}} = -1.5\text{ mA}$) High-state Output Voltage ($I_{\text{OUT}} = 250\text{ }\mu\text{A}$) Capacitance ⁽⁹⁾	V_{OL} V_{OH} C_{IN}	— 3.85 —	— — 4.0	0.4 — —	V V pF
Input Pin PWMIN Input Logic Low Voltage Input Logic High Voltage Input Current Capacitance ⁽⁹⁾	V_{IL} V_{IH} I_{IN} C_{IN}	— 3.5 -10 —	— — — 4.0	1.5 — 10 —	V V μA pF
Pin TXD, $\overline{\text{SS}}$ —Pull-up Current	I_{PU}	—	40	—	μA

Notes

- Device is fully functional. All functions are operating. Over-temperature may occur.
- Total current ($I_{\text{VSUP1}} + I_{\text{VSUP2}}$) measured at GND pin.
- Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
- This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_{\text{J}} \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low-voltage Reset (LVR) Threshold	V_{LVRON}	3.6	4.0	4.4	V
Low-voltage Interrupt (LVI) Threshold	V_{LVI}	5.7	6.0	6.6	V
LVI Hysteresis	$V_{\text{LVI_HYS}}$	—	1.0	—	
High-voltage Interrupt (HVI) Threshold	V_{HVI}	18	19.25	20.5	V
HVI Hysteresis	$V_{\text{HVI_HYS}}$	—	220	—	mV

VOLTAGE REGULATOR ⁽¹⁰⁾

Normal Mode Output Voltage $2.0\text{ mA} < I_{\text{DD}} < 50\text{ mA}$, $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{DDRUN}	4.75	5.0	5.25	V
Normal Mode Output Current Limitation ⁽¹¹⁾	I_{DDRUN}	50	110	200	mA
Dropout Voltage $V_{\text{SUP}} = 4.9\text{ V}$, $I_{\text{DD}} = 50\text{ mA}$	V_{DDDROP}	—	0.1	0.2	V
Stop Mode Output Voltage ⁽¹²⁾	V_{DDSTOP}	4.75	5.0	5.25	V
Stop Mode Regulator Current Limitation	I_{DDSTOP}	4.0	8.0	14	mA
Line Regulation Normal Mode, $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$, $I_{\text{DD}} = 10\text{ mA}$ Stop Mode, $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$, $I_{\text{DD}} = 2.0\text{ mA}$	V_{LRRUN} V_{LRSTOP}	— —	20 10	150 100	mV
Load Regulation Normal Mode, $1.0\text{ mA} < I_{\text{DD}} < 50\text{ mA}$, $V_{\text{SUP}} = 18\text{ V}$ Stop Mode, $1.0\text{ mA} < I_{\text{DD}} < 5.0\text{ mA}$, $V_{\text{SUP}} = 18\text{ V}$	V_{LRRUN} V_{LDSTOP}	— —	40 40	150 150	mV
Over-temperature Prewarning (Junction) ⁽¹³⁾	T_{PRE}	120	135	160	$^{\circ}\text{C}$
Thermal Shutdown Temperature (Junction) ⁽¹³⁾	T_{SD}	155	170	—	$^{\circ}\text{C}$
Temperature Threshold Difference $T_{\text{SD}} - T_{\text{PRE}}$	$\Delta T_{\text{SD}} - T_{\text{PRE}}$	20	30	45	$^{\circ}\text{C}$

Notes

- Specification with external capacitor $2.0\text{ }\mu\text{F} < C < 10\text{ }\mu\text{F}$ and $200\text{ m}\Omega \leq \text{ESR} \leq 10\text{ }\Omega$. Capacitor value up to $47\text{ }\mu\text{F}$ can be used.
- Total V_{DD} regulator current. A 5.0 mA current for current sense operational amplifier is included. Digital output supplied from V_{DD} .
- When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.
- This parameter is guaranteed by process monitoring but not production tested

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_{\text{J}} \leq 125\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
External Resistor Range	R_{EXT}	10	—	100	$\text{k}\Omega$
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) ⁽¹⁴⁾	WD_{CACC}	-15	—	15	%
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage Recessive State, TXD HIGH, $I_{\text{OUT}} = 1.0\text{ }\mu\text{A}$ Dominant State, TXD LOW, $500\text{ }\Omega$ External Pull-up Resistor	$V_{\text{LIN_REC}}$ $V_{\text{LIN_DOM}}$	$V_{\text{SUP}}-1$ —	— —	— 1.4	V
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	60	$\text{k}\Omega$
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	2.0	—	μA
Output Current Shutdown Threshold	$I_{\text{OV-CUR}}$	50	75	150	mA
Leakage Current to GND VSUP Disconnected, V_{BUS} at 18 V Recessive State, $8.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $8.0\text{ V} \leq V_{\text{BUS}} \leq 18\text{ V}$, $V_{\text{BUS}} \geq V_{\text{SUP}}$ GND Disconnected, $V_{\text{GND}} = V_{\text{SUP}}$, V_{BUS} at -18 V	I_{BUS}	— 0.0 -1.0	1.0 3.0 —	10 20 1.0	μA
LIN Receiver Receiver Threshold Dominant Receiver Threshold Recessive Receiver Threshold Center Receiver Threshold Hysteresis	$V_{\text{BUS_DOM}}$ $V_{\text{BUS_REC}}$ $V_{\text{BUS_CNT}}$ $V_{\text{BUS_HYS}}$	— 0.6 0.475 —	— — 0.5 —	0.4 — 0.525 0.175	V_{SUP}
HIGH SIDE OUTPUTS HS1 AND HS2					
Switch On Resistance $T_{\text{J}} = 25\text{ }^\circ\text{C}$, $I_{\text{LOAD}} = 150\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_{\text{J}} = 125\text{ }^\circ\text{C}$, $I_{\text{LOAD}} = 150\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_{\text{J}} = 125\text{ }^\circ\text{C}$, $I_{\text{LOAD}} = 120\text{ mA}$, $5.5\text{ V} < V_{\text{SUP}} > 9.0\text{ V}$	$R_{\text{DS(ON)}}$	— — —	2.0 — 3.0	2.5 4.5 —	Ω
Output Current Limit	I_{LIM}	300	—	600	mA
Over-temperature Shutdown ^{(15), (16)}	T_{HSSD}	155	—	190	$^\circ\text{C}$
Leakage Current	I_{LEAK}	—	—	10	μA
Output Clamp Voltage $I_{\text{OUT}} = -100\text{ mA}$	V_{CL}	-6.0	—	—	V

Notes

14. Watchdog timing period calculation formula: $P_{\text{WD}} = 0.991 * R_{\text{EXT}} + 0.648$ (R_{EXT} in $\text{k}\Omega$ and P_{WD} in ms).
15. This parameter is guaranteed by process monitoring but it is not production tested
16. When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH SIDE OUTPUT HS3					
Switch On Resistance $T_J = 25\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 125\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$, $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 125\text{ }^{\circ}\text{C}$, $I_{\text{LOAD}} = 30\text{ mA}$, $5.5\text{ V} < V_{\text{SUP}} > 9.0\text{ V}$	$R_{\text{DS(ON)}}$	—	—	7.0 10 14	Ω
Output Current Limitation	I_{LIM}	60	100	200	mA
Over-temperature Shutdown (17), (18)	T_{HSSD}	155	—	190	$^{\circ}\text{C}$
Leakage Current	I_{LEAK}	—	—	10	μA

CURRENT SENSE OPERATIONAL AMPLIFIER

Rail-to-Rail Input Voltage	V_{IMC}	-0.1	—	$V_{\text{CC}}+0.1$	V
Output Voltage Range Output Current $\pm 1.0\text{ mA}$ Output Current $\pm 5.0\text{ mA}$	V_{OUT1} V_{OUT2}	0.1 0.3	— —	$V_{\text{CC}}-0.1$ $V_{\text{CC}}-0.3$	V
Input Bias Current	I_{B}	—	—	250	nA
Input Offset Current	I_{O}	-100	—	100	nA
Input Offset Voltage	V_{IO}	-25	—	25	mV

L1 AND L2 INPUTS

Low Detection Threshold $5.5\text{ V} < V_{\text{SUP}} < 6.0\text{ V}$ $6.0\text{ V} < V_{\text{SUP}} < 18\text{ V}$ $18\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{THL}	2.0 2.5 2.7	2.5 3.0 3.2	3.0 3.5 3.7	V
High Detection Threshold $5.5\text{ V} < V_{\text{SUP}} < 6.0\text{ V}$ $6.0\text{ V} < V_{\text{SUP}} < 18\text{ V}$ $18\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{THH}	2.7 3.0 3.5	3.3 4.0 4.2	3.8 4.5 4.7	V
Hysteresis $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$	V_{HYS}	0.5	—	1.3	V
Input Current $-0.2\text{ V} < V_{\text{IN}} < 40\text{ V}$	I_{IN}	-10	—	10	μA

Notes

- This parameter is guaranteed by process monitoring but it is not production tested
- When over-temperature occurs, switch is turned off and latched off. Flag is set in SPI.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_{\text{J}} \leq 125\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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LIN PHYSICAL LAYER

 Driver Characteristics for Normal Slew Rate ^{(19), (20)}

Dominant Propagation Delay TXD to LIN	$t_{\text{DOM-MIN}}$	—	—	50	μs
Dominant Propagation Delay TXD to LIN	$t_{\text{DOM-MAX}}$	—	—	50	μs
Recessive Propagation Delay TXD to LIN	$t_{\text{REC-MIN}}$	—	—	50	μs
Recessive Propagation Delay TXD to LIN	$t_{\text{REC-MAX}}$	—	—	50	μs
Propagation Delay Symmetry: $t_{\text{DOM-MIN}} - t_{\text{REC-MAX}}$	DT1	-10.44	—	—	μs
Propagation Delay Symmetry: $t_{\text{DOM-MAX}} - t_{\text{REC-MIN}}$	DT2	—	—	11	μs

 Driver Characteristics for Slow Slew Rate ^{(19), (21)}

Dominant Propagation Delay TXD to LIN	$t_{\text{DOM-MIN}}$	—	—	100	μs
Dominant Propagation Delay TXD to LIN	$t_{\text{DOM-MAX}}$	—	—	100	μs
Recessive Propagation Delay TXD to LIN	$t_{\text{REC-MIN}}$	—	—	100	μs
Recessive Propagation Delay TXD to LIN	$t_{\text{REC-MAX}}$	—	—	100	μs
Propagation Delay Symmetry: $t_{\text{DOM-MIN}} - t_{\text{REC-MAX}}$	DT1S	-22	—	—	μs
Propagation Delay Symmetry: $t_{\text{DOM-MAX}} - t_{\text{REC-MIN}}$	DT2S	—	—	23	μs

Driver Characteristics for Fast Slew Rate

LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	15	—	$\text{V}/\mu\text{s}$
---------------------------------------	---------------------------	---	----	---	------------------------

Receiver Characteristics and Wake-Up Timings

Receiver Dominant Propagation Delay ⁽²²⁾	t_{RL}	—	3.5	6.0	μs
Receiver Recessive Propagation Delay ⁽²²⁾	t_{RH}	—	3.5	6.0	μs
Receiver Propagation Delay Symmetry	$t_{\text{R-SYM}}$	-2.0	—	2.0	μs
Bus Wake-up Deglitcher	t_{PROPWL}	35	—	150	μs
Bus Wake-up Event Reported ⁽²³⁾	t_{WAKE}	—	20	—	μs

Notes

19. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 k Ω , 6.8 nF/660 Ω , 10 nF/500 Ω . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
20. See [Figure 6](#), page 14.
21. See [Figure 7](#), page 14.
22. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
23. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See [Figure 8](#) and [Figure 9](#), page 15. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD pin.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^\circ\text{C} \leq T_{\text{J}} \leq 125\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER (CONTINUED)					
Output Current Shutdown Delay	$t_{\text{OV-DELAY}}$	—	10	—	μs
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency	$f_{\text{SPIO P}}$	0.25	—	4.0	MHz
L1 AND L2 INPUTS					
Wake-up Filter Time ⁽²⁴⁾	t_{WUF}	8.0	20	38	μs
WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)					
Watchdog Period	t_{PWD}				ms
External Resistor $R_{\text{EXT}} = 10\text{ k}\Omega$ (1%)		—	10.558	—	
External Resistor $R_{\text{EXT}} = 100\text{ k}\Omega$ (1%)		—	99.748	—	
Without External Resistor R_{EXT} (WDCONF Pin Open)		97	150	205	
STATE MACHINE TIMING					
Reset Low Level Duration after V_{DD} High ⁽²⁸⁾	t_{RST}	0.65	1.0	1.35	ms
Interrupt Low Level Duration	t_{INT}	7.0	10	13	μs
Normal Request Mode Timeout ⁽²⁸⁾	$t_{\text{NRTOU T}}$	97	150	205	ms
Delay Between SPI Command and HS1/HS2/HS3 Turn On ^{(25), (26)}	$t_{\text{S-HSON}}$	—	3.0	10	μs
Delay Between SPI Command and HS1/HS2/HS3 Turn Off ^{(25), (26)}	$t_{\text{S-HSOFF}}$	—	3.0	10	μs
Delay Between Normal Request and Normal Mode After W/D Trigger Command ⁽²⁷⁾	$t_{\text{S-NR2N}}$	6.0	35	70	μs
Delay Between $\overline{\text{SS}}$ Wake-Up ($\overline{\text{SS}}$ LOW to HIGH) and Normal Request Mode (VDD On and Reset High)	$t_{\text{W-SS}}$	15	40	80	μs
Delay Between $\overline{\text{SS}}$ Wake-Up ($\overline{\text{SS}}$ LOW to HIGH) and First Accepted SPI Command	$t_{\text{W-SPI}}$	90	—	N/A	μs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{\text{S-1STSPI}}$	30	—	N/A	μs
Minimum Time Between Two Rising Edges on $\overline{\text{SS}}$	t_{2SS}	15	—	—	μs

Notes

- 24. This parameter is guaranteed by process monitoring but is not production tested.
- 25. Delay between turn-on or turn-off command and high side on or high side off, excluding rise or fall time due to external load.
- 26. Delay between the end of the SPI command (rising edge of the $\overline{\text{SS}}$) and start of device activation/deactivation.
- 27. This parameter is guaranteed by process monitoring but it is not production tested.
- 28. Also see [Figure 10](#) on page [15](#)

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\text{ V} \leq V_{\text{SUP}} \leq 16\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_{\text{J}} \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE OPERATIONAL AMPLIFIER					
Supply Voltage Rejection Ratio ⁽²⁹⁾	SVR	60	—	—	dB
Common Mode Rejection Ratio ⁽²⁹⁾	CMR	70	—	—	dB
Gain Bandwidth ⁽²⁹⁾	GBP	1.0	—	—	MHz
Slew Rate	SR	0.5	—	—	V/ μ s
Phase Margin (for Gain = 1, Load 100 pF / 5.0 k Ω) ⁽²⁹⁾	PHMO	40	—	—	$^{\circ}$
Open Loop Gain	OLG	—	85	—	dB

Notes

29. This parameter is guaranteed by process monitoring but it is not production tested.

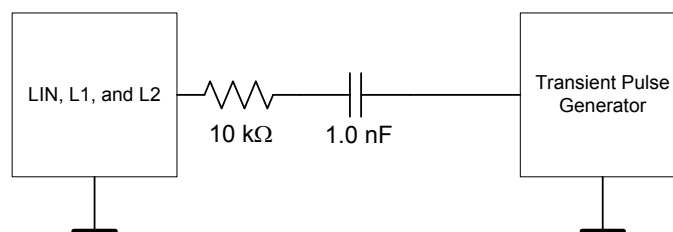
MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 data sheet.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module

TIMING DIAGRAMS



Note Waveform in accordance with ISO7637 Part 1, Test Pulses 1, 2, 3a, and 3b.

Figure 4. Test Circuit for Transient Test Pulses

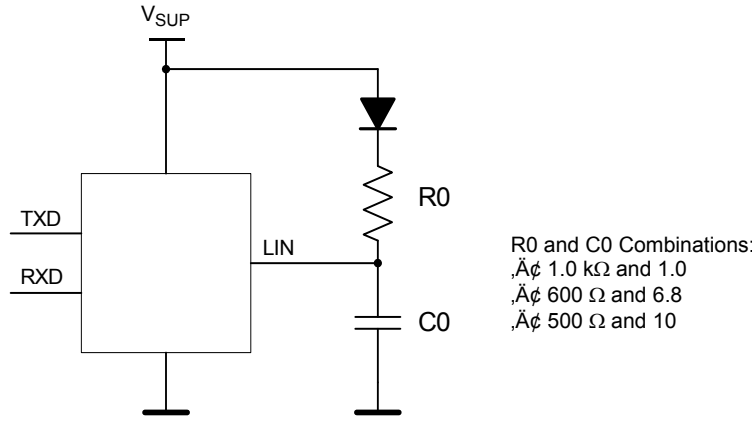


Figure 5. Test Circuit for LIN Timing Measurements

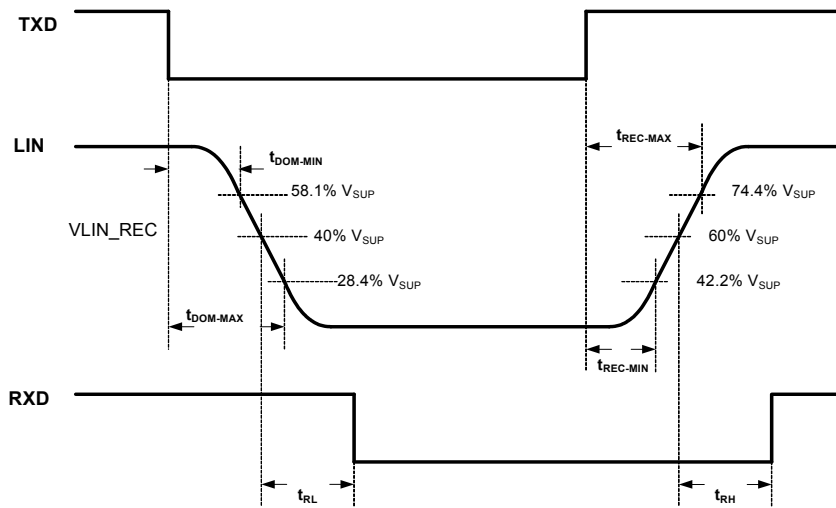


Figure 6. LIN Timing Measurements for Normal Slew Rate

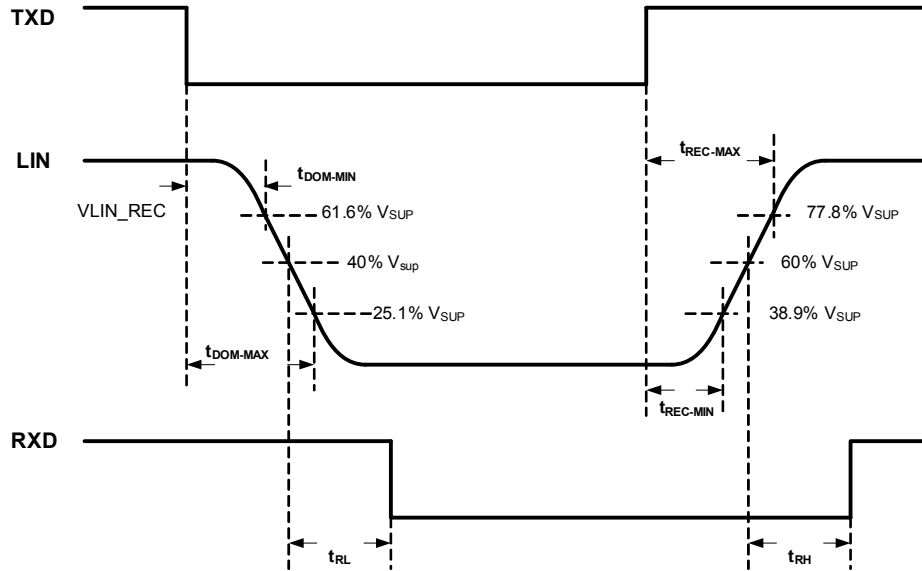


Figure 7. LIN Timing Measurements for Slow Slew Rate

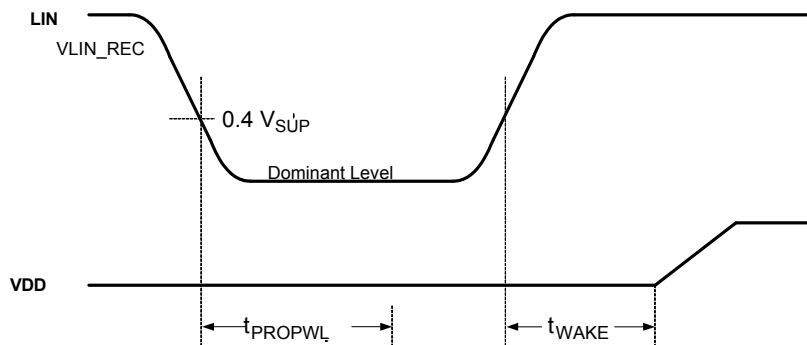


Figure 8. Wake-up Sleep Mode Timing

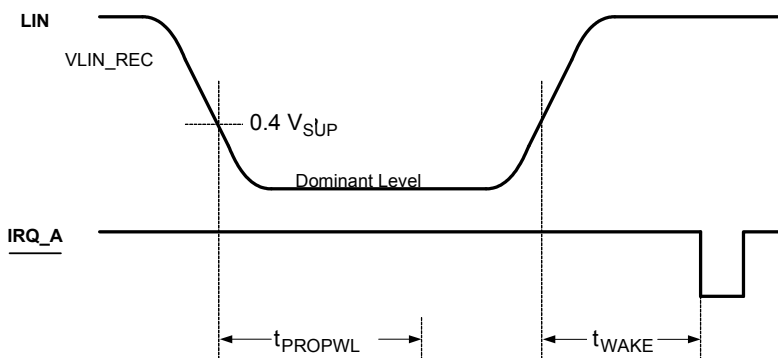


Figure 9. Wake-up Stop Mode Timing

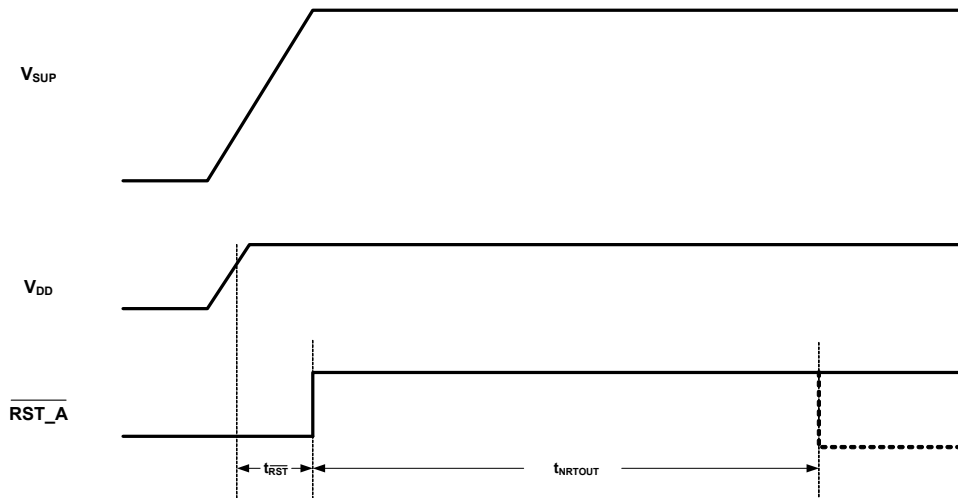


Figure 10. Power On Reset and Normal Request Timeout Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E624 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E624 is well suited to perform relay control in applications like window lift, sunroof, etc., via a three-wire LIN bus.

The device combines an HC908EY16 MCU core with flash memory together with a *SmartMOS* IC chip. The *SmartMOS* IC chip combines power and control in one chip. Power switches are provided on the *SmartMOS* IC configured as

high side outputs. Other ports are also provided, which include a current sense operational amplifier port and two wake-up pins. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See [Figure 1. 908E624 Simplified Application Diagram](#), page 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on [page 3](#) for a depiction of the pin locations on the package.

PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/ \overline{SS} pin is likewise not accessible.

For details, refer to the 68HC908EY16 data sheet.

PORT B I/O PINS (PTB1:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

The PTB0/AD0 and PTB2/AD2 pins are not accessible in this device.

For details, refer to the 68HC908EY16 data sheet.

PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details, refer to the 68HC908EY16 data sheet.

PORT D I/O PINS (PTD0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

For details, refer to the 68HC908EY16 data sheet.

PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL INTERRUPT PIN (\overline{IRQ})

The \overline{IRQ} pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the \overline{IRQ} pin is pulled LOW.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL RESET PIN (\overline{RST})

A logic [0] on the \overline{RST} pin forces the MCU to a known startup state. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

Important To ensure proper operation, do not add any external pull-up resistor.

For details, refer to the 68HC908EY16 data sheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins, respectively. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details, refer to the 68HC908EY16 data sheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details, refer to the 68HC908EY16 data sheet.

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSSA via separate traces.

For details, refer to the 68HC908EY16 data sheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. Do not connect in the application or connect to GND.

PWMIN PIN (PWMIN)

This pin is the direct PWM input for high side outputs 1 and 2 (HS1 and HS2). If no PWM control is required, PWMIN must be connected to VDD to enable the HS1 and HS2 outputs.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

RESET PIN ($\overline{\text{RST_A}}$)

$\overline{\text{RST_A}}$ is the reset output pin of the analog die and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

Important To ensure proper operation, do not add any external pull-up resistor.

INTERRUPT PIN ($\overline{\text{IRQ_A}}$)

$\overline{\text{IRQ_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. This pin must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)

This pin is the configuration pin for the internal watchdog. A resistor is connected to this pin. The resistor value defines

the watchdog period. If the pin is open, the watchdog period is fixed to its default value.

The watchdog can be disabled (e.g., for flash programming or software debugging) by connecting this pin to GND.

POWER SUPPLY PINS (VSUP1 AND VSUP2)

This VSUP1 power supply pin supplies the voltage regulator, the internal logic, and LIN transceiver.

This VSUP2 power supply pin is the positive supply for the high side switches.

POWER GROUND PIN (GND)

This pin is the device ground connection.

HIGH SIDE OUTPUT PINS (HS1 AND HS2)

These pins are high side switch outputs to drive loads such as relays or lamps. Each switch is protected with over-temperature and current limit (over-current). The output has an internal clamp circuitry for inductive load. The HS1 and HS2 outputs are controlled by the SPI and have a direct enabled input (PWMIN) for PWM capability.

HIGH SIDE OUTPUT PIN (HS3)

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. The switch is protected with over-temperature and current limit (over-current). The output is controlled only by the SPI.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

WAKE-UP PINS (L1 AND L2)

These pins are high-voltage capable inputs used to sense external switches and to wake-up the device from Sleep or Stop mode. During Normal mode the state of these pins can be read through the SPI.

Important If unused, these pins should be connected to VSUP or GND to avoid parasitic transitions. In Low Power Mode, this could lead to random wake-up events.

CURRENT SENSE OPERATIONAL AMPLIFIER PINS (E+, E-, OUT, VCC)

These are the pins of the single supply current sense operational amplifier.

- The E+ and E- input pins are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT pin is the output pin of the current sense operational amplifier.
- The VCC pin is the +5.0 V single supply connection.

Note If the operational amplifier is not used, it is possible to connect all pins (E+, E-, OUT and VCC) to GND. In this case, all of the four pins must be grounded.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller. The pin is protected against shorts to GND with an integrated current limit (temperature shutdown could occur).

Important The VDD, EVDD, VDDA, and VREFH pins must be connected together.

VOLTAGE REGULATOR AND CURRENT SENSE AMPLIFIER GROUND PIN (AGND)

The AGND pin is the ground pin of the voltage regulator and the current sense operational amplifier.

Important GND, AGND, VSS, EVSS, VSSA, and VREFL pins must be connected together.

NO CONNECT PINS (NC)

The NC pins are not connected internally.

Note Each of the NC pins can be left open or connected to ground (recommended).

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E624 ANALOG DIE MODES OF OPERATION

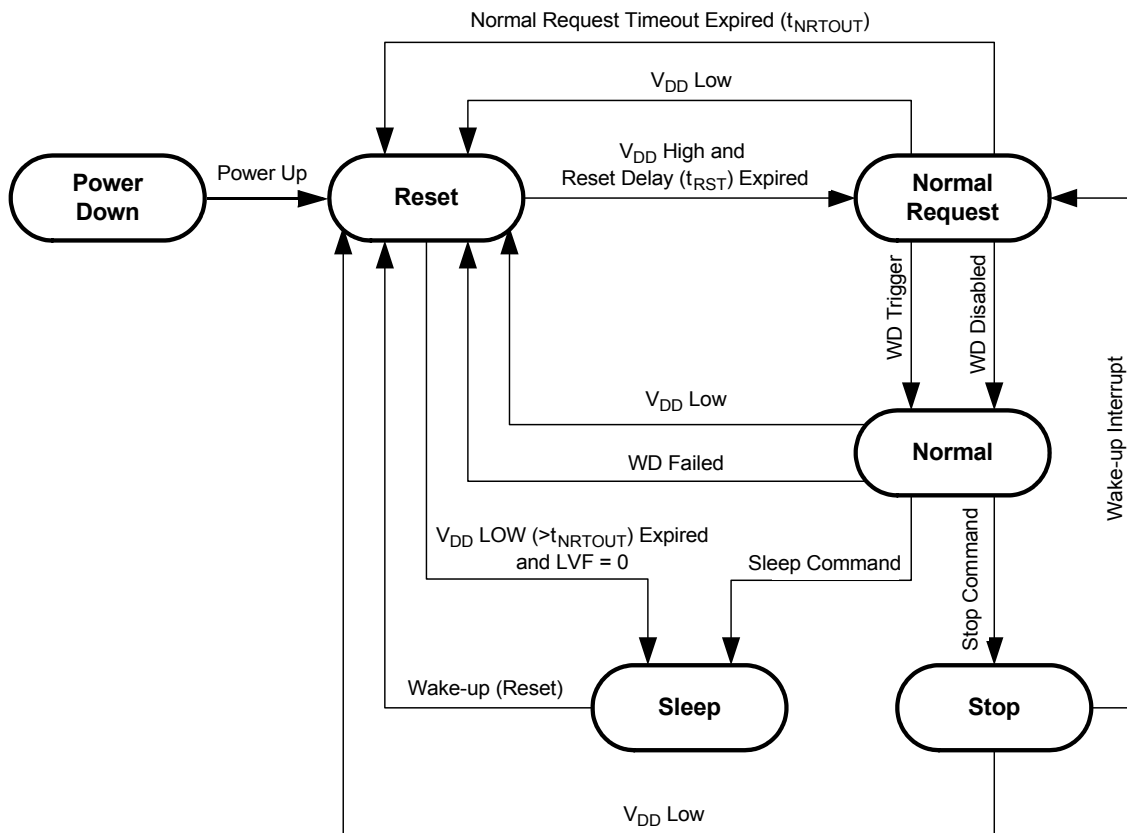
The 908E624 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode the device is active and is operating under normal application conditions. The Stop and Sleep modes are low-power modes with wake-up capabilities.

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability), and in Sleep mode the voltage regulator is turned off ($V_{DD} = 0$ V).

Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MODE1:2 bits in the SPI Control register.

[Figure 11](#) describes how transitions are done between the different operating modes and [Table 6](#), page 20, gives an overview of the operating mode.



Legend

- WD: Watchdog
- WD Disabled: Watchdog disabled (WDCONF pin connected to GND)
- WD Trigger: Watchdog is triggered by SPI command
- WD Failed: No watchdog trigger or trigger occurs in closed window
- Stop Command: Stop command sent via SPI
- Sleep Command: Sleep command sent via SPI
- Wake-up: L1 or L2 state change or LIN bus wake-up or \overline{SS} rising edge

Figure 11. Operating Modes and Transitions

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	RST_A Output	Watchdog Function	HS1, HS2, and HS3	LIN Interface	Sense Amplifier
Reset	V _{DD} ON	N/A	LOW	Disabled	Disabled	Recessive only	Not active
Normal Request	V _{DD} ON	N/A	HIGH	150 ms time out if WD enabled	Enabled	Transmit and receive	Not active
Normal (Run)	V _{DD} ON	N/A	HIGH	Window WD if enabled	Enabled	Transmit and receive	Active
Stop	V _{DD} ON with limited current capability	LIN wake-up, L1, L2 state change, SS rising edge	HIGH	Disabled	Disabled	Recessive state with wake-up capability	Not active
Sleep	V _{DD} OFF	LIN wake-up L1, L2 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability	Not active

INTERRUPTS

In Normal (Run) mode the 908E624 has four different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ_A}}$ pin is generated to report a fault to the MCU. All interrupts are not maskable and cannot be disabled.

After an Interrupt the INTSRC bit in the SPI Status register is set, indicating the source of the event. This interrupt source information is only transferred once, and the INTSRC bit is cleared automatically.

Low-Voltage Interrupt

Low-voltage interrupt (LVI) is related to external supply voltage VSUP1. If this voltage falls below the LVI threshold, it will set the LVF bit in the SPI Status register and an interrupt will be initiated. The LVF bit remains set as long as the Low-voltage condition is present.

During Sleep and Stop mode the low-voltage interrupt circuitry is disabled.

High-voltage Interrupt

High-voltage interrupt (HVI) is related to external supply voltage VSUP1. If this voltage rises above the HVI threshold, it will set the HVF bit in the SPI Status register and an interrupt will be initiated. The HVF bit remains set as long as the high-voltage condition is present.

During Sleep and Stop mode the high-voltage interrupt circuitry is disabled.

Wake-up Interrupts

In Stop mode the $\overline{\text{IRQ_A}}$ pin reports wake-up events on the L1, L2, or the LIN bus to the MCU. All wake-up interrupts are not maskable and cannot be disabled.

After a wake-up interrupt, the INTSRC bit in the Serial Peripheral Interface (SPI) Status register is set, indicating the source of the event. This wake-up source information is only transferred once, and the INTSRC bit is cleared automatically.

[Figure 12](#), page 21, describes the Stop/Wake-up procedure.

Voltage Regulator Temperature Prewarning (VDDT)

Voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Status register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop mode the voltage regulator temperature prewarning circuitry is disabled.

High Side Switch Thermal Shutdown (HSST)

The high side switch thermal shutdown HSST is generated if one of the high side switches HS1:HS3 is above the HSST threshold, it will shutdown all high side switches, set the HSST flag in the SPI Status register and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present.

During Sleep and Stop mode the high side switch thermal shutdown circuitry is disabled.

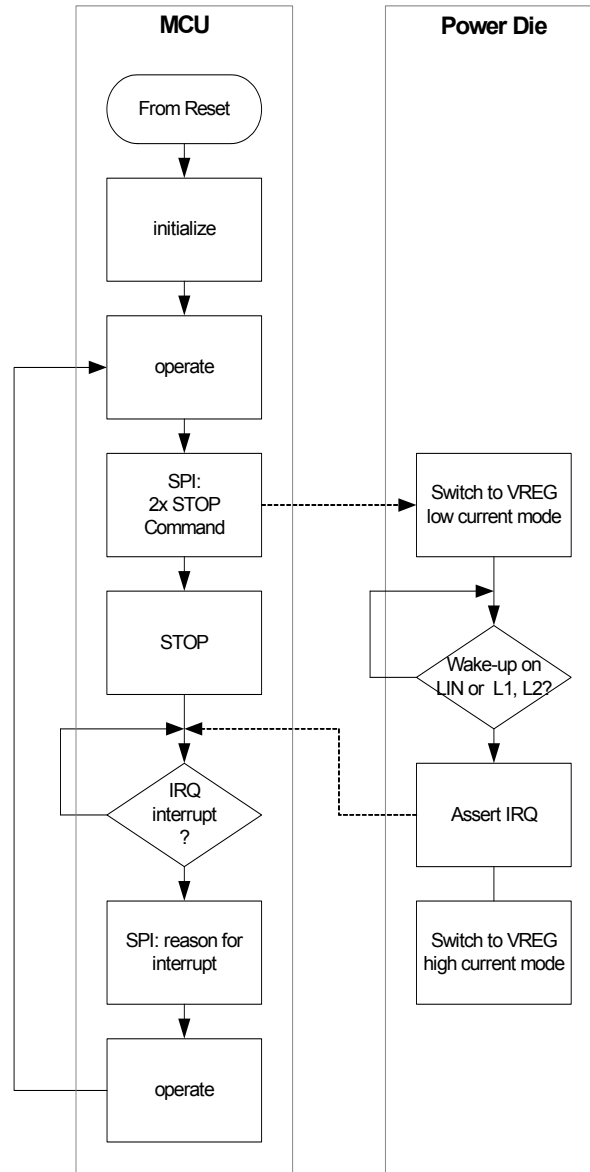


Figure 12. Stop Mode/Wake-up Procedure

ANALOG DIE INPUTS/OUTPUTS

High Side Output Pins HS1 and HS2

These are two high side switches used to drive loads such as relays or lamps. They are protected with over-temperature and current limit (over-current) and include an active internal clamp circuitry for inductive load drive. Control is done using the SPI Control register. PWM capability is offered through the PWMIN input pin.

The high side switch is turned on if both the HSxON bit in the SPI Control register is set and the PWMIN input is HIGH (refer to [Figure 13](#), page 22). In order to have HS1 on, the PWMIN must be HIGH and bit HS1ON must be set. The same applies to the HS2 output.

If no PWM control is required, PWMIN must be connected to the VDD pin.

Current Limit (Over-current) Protection

These high side switches feature current limit to protect them against over-current and short circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop modes the high sides are disabled.

High Side Output HS3

This high side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. Control is done using the SPI Control register. No direct PWM control is possible on this pin (refer to [Figure 14](#), page 22).

Current Limit (Over-current) Protection

This high side feature switch feature current limit to protect it against over-current and short-circuit conditions.

Over-temperature Protection

If an over-temperature condition occurs on any of the three high side switches, all high side switches (HS1, HS2, and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop mode the high side is disabled.

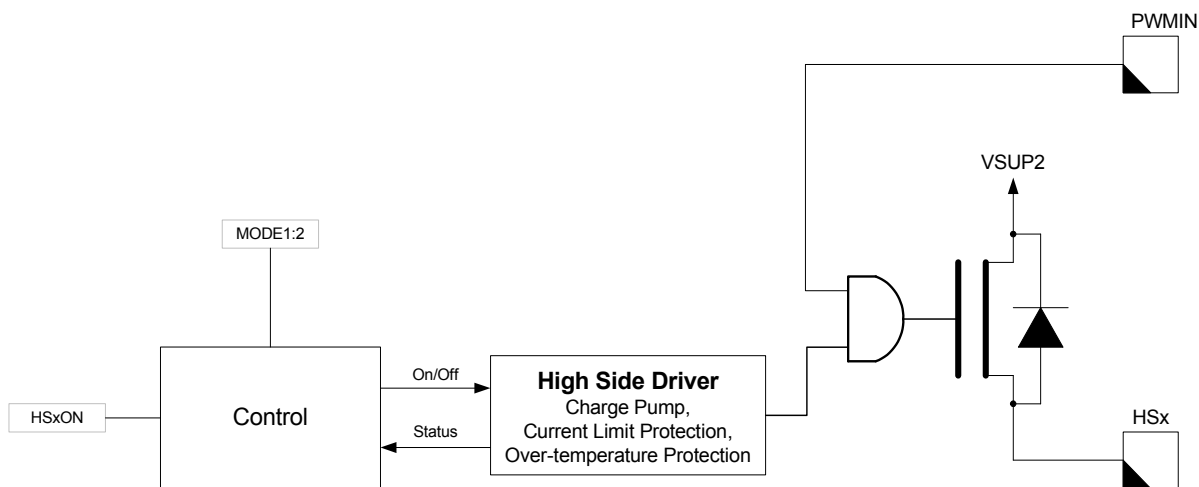


Figure 13. High Side HS1 and HS2 Circuitry

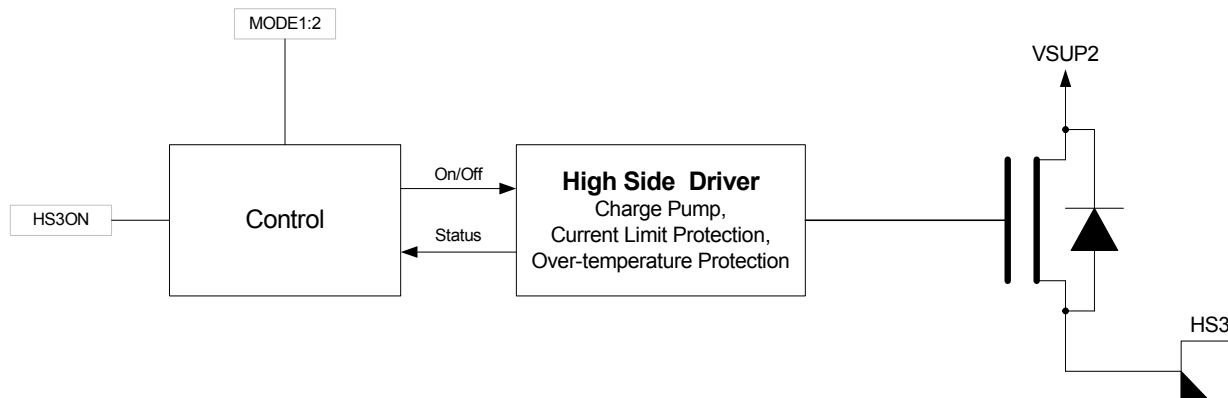


Figure 14. High Side HS3 Circuitry

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with over-current protection and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave

node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LINS2:1 in the SPI Control Register. The initial slew rate is optimized for 20 kBit/s.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled in Normal and Normal Request mode.

An over-current condition (e.g. LIN bus short to V_{BAT}) or a over-temperature in the output low side FET will shutdown

the transmitter and set the LINFAIL flag in the SPI Status Register.

For improved performance and safe behavior in case of LIN bus short to Ground or LIN bus leakage during low power mode the internal pull-up resistor on the LIN pin can be disconnected, with the LIN-PU bit in the SPI Control Register, and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

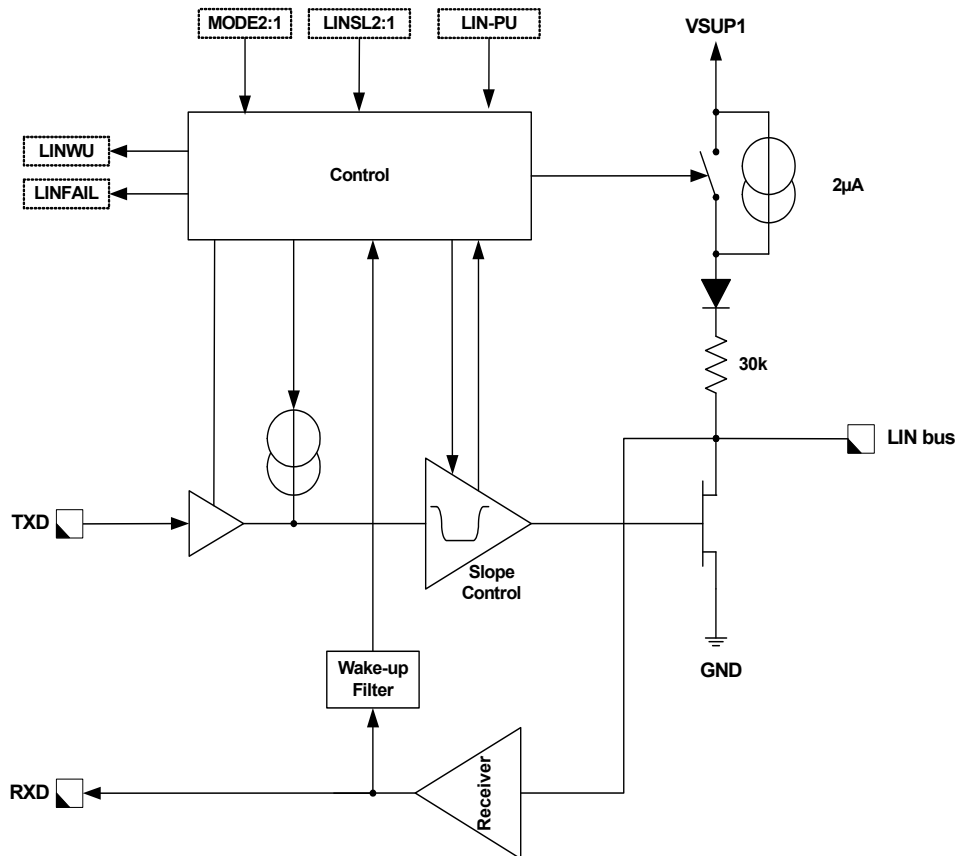


Figure 15. LIN Interface

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see [Figure 2](#), page 2). When TXD is LOW, the LIN pin is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD pin has an internal pull-up current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a wake-up interrupt and set the LINWF flag in the SPI Status Register. Also see [Figure 9](#), page 15.

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep mode sequence the internal pull-up resistor is

disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the SPI Status Register. Also see [Figure 8](#), page [15](#).

WINDOW WATCHDOG

The window watchdog is configurable using an external resistor at the WDCONF pin. The watchdog is cleared through by the MODE1:2 bits in the SPI Control register (refer to [Table 8](#), page [26](#)).

A watchdog clear is only allowed in the open window. If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST_A}$ pin and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

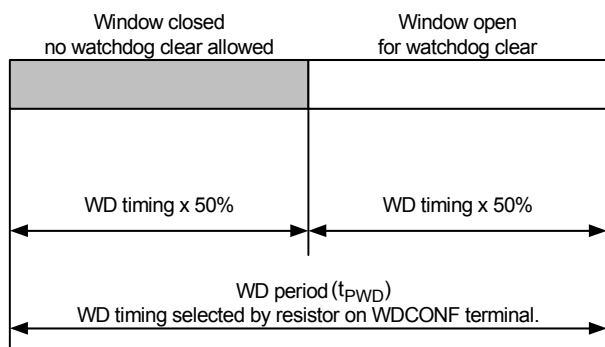


Figure 16. Window Watchdog Operation

Watchdog Configuration

If the WDCONF pin is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF pin must be connected to GND.

The watchdog period is calculated using the following formula:

$$t_{PWD} [\text{ms}] = 0.991 * R_{EXT} [\text{k}\Omega] + 0.648$$

VOLTAGE REGULATOR

The 908E624 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

Current Limit (Over-current) Protection

The voltage regulator has current limit to protect the device against over-current and short-circuit conditions.

Over-temperature Protection

The voltage regulator also features an over-temperature protection having an over-temperature warning (Interrupt - VDDT) and an over-temperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode the voltage regulator external V_{DD} is turned off.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease of use of the 908E624, various parameters (e.g., ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values, located in the flash memory, is explained in the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as $\pm 25\%$, due to process, temperature, and voltage dependencies. To compensate for these dependencies, an ICG trim value is located at the address \$FDC2. After trimming the ICG, a range of typ. $\pm 2\%$ ($\pm 3\%$ max.) at nominal conditions (filtered (100 nF) and stabilized (4.7 μF) $V_{DD} = 5.0 \text{ V}$, $T_{Ambient} \sim 23 \text{ }^\circ\text{C}$) and will vary over-temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 data sheet.

To trim the ICG, these values must be copied to the ICG Trim Register ICGTR at address \$38 of the MCU.

Important The value has to be copied after every reset.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 data sheet.

LOGIC COMMANDS AND REGISTERS

908E624 SPI INTERFACE AND CONFIGURATION

The serial peripheral interface creates the communication link between the microcontroller and the analog die of the 908E624.

The interface consists of four pins (see [Figure 17](#)):

- \overline{SS} —Slave Select

- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCCK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 8 bits of control information and the slave replies with 8 bits of status data.

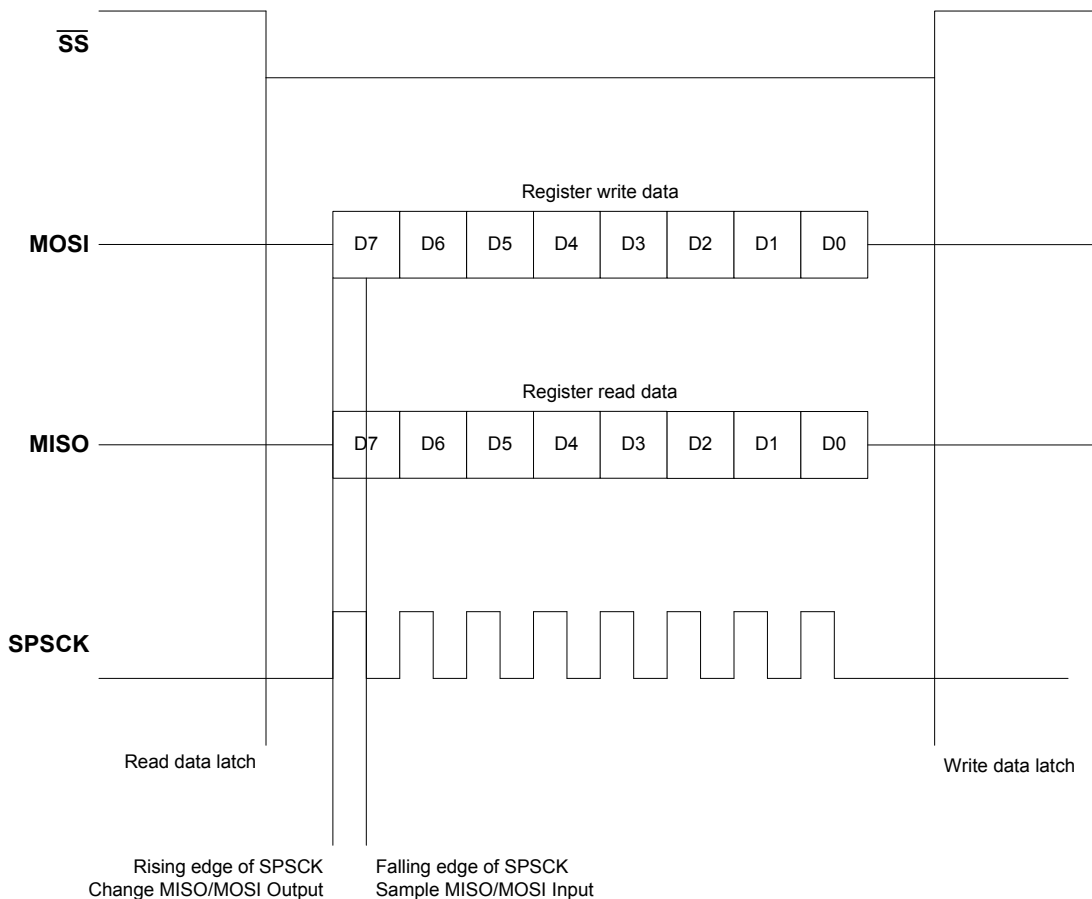


Figure 17. SPI Protocol

During the inactive phase of the \overline{SS} (HIGH), the new data transfer is prepared.

The falling edge of the \overline{SS} indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data).

With the rising edge of the SPI clock, SPSCCK the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock SPSCCK the data is sampled by the Receiver.

The data transfer is only valid if exactly 8 sample clock edges are present in the active (low) phase of \overline{SS} .

The rising edge of the slave select \overline{SS} indicates the end of the transfer and latches the write data (MOSI) into the register. The \overline{SS} high forces MISO to the high-impedance state.

SPI REGISTER OVERVIEW

[Table 7](#) summarizes the SPI Register bit meaning, reset value, and bit reset condition.