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Rev. 11.0, 2/2013

RoHS

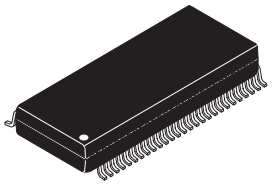
Integrated Stepper Motor Driver with Embedded MCU and LIN Serial Communication

908E626

STEPPER MOTOR DRIVER WITH EMBEDDED MCU AND LIN

The 908E626 is an integrated single package solution that includes a high performance HC08 microcontroller with a SMARTMOS analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), internal serial peripheral interface (SPI), and an internal clock generator (ICG) module. The analog control die provides fully protected H-Bridge outputs, voltage regulator, autonomous watchdog, and local interconnect network (LIN) physical layer.

The single package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is well-suited for the control of automotive stepper applications like climate control and light-leveling.



EK SUFFIX (PB-FREE)
98ARL10519D
54-PIN SOICW-EP

Features

- High performance M68HC08EY16 core
- 16 KB of on-chip flash memory
- 512 B of RAM
- Internal clock generation module
- Two 16-bit, two-channel timers
- 10-bit analog-to-digital converter
- Four low $R_{DS(ON)}$ half-bridge outputs
- 13 microcontroller I/Os

ORDERING INFORMATION		
Device (Add an R2 suffix for Tape and reel orders)	**Temperature Range (T_A)**	**Package**
MM908E626AVPEK	-40 to 115 °C	54 SOICW EP

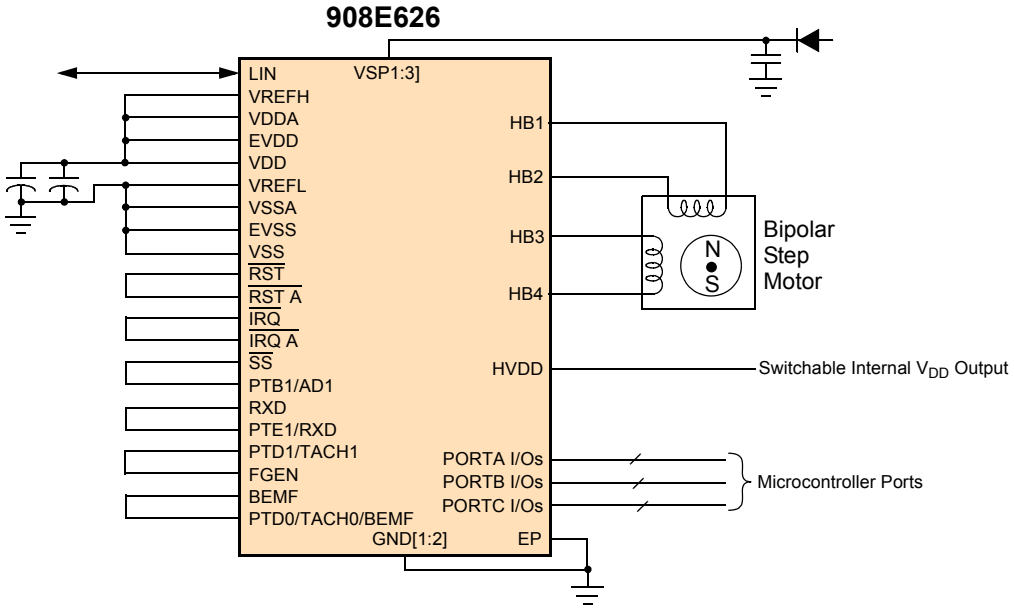


Figure 1. 908E626 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale

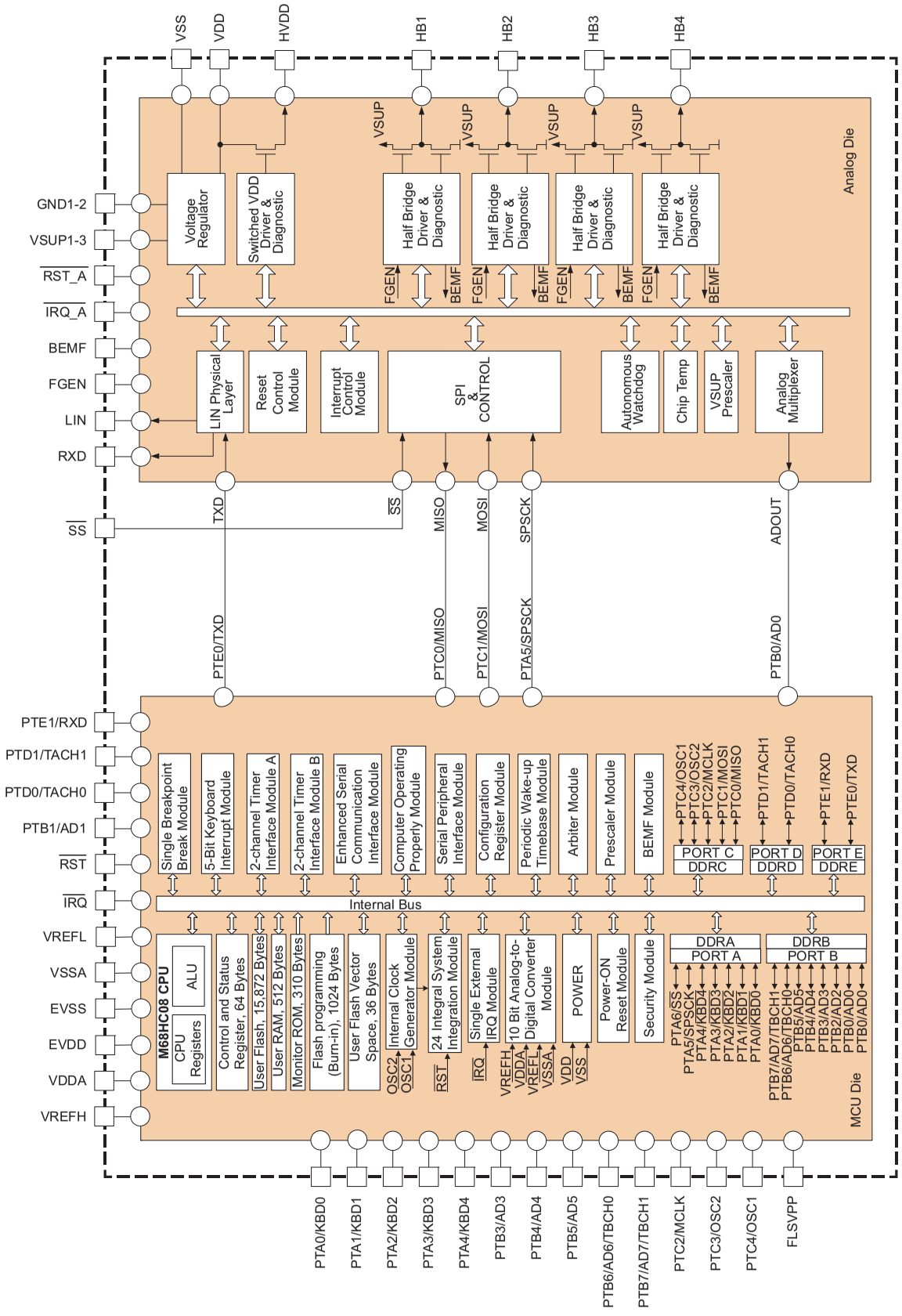


Figure 2. 908E626 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

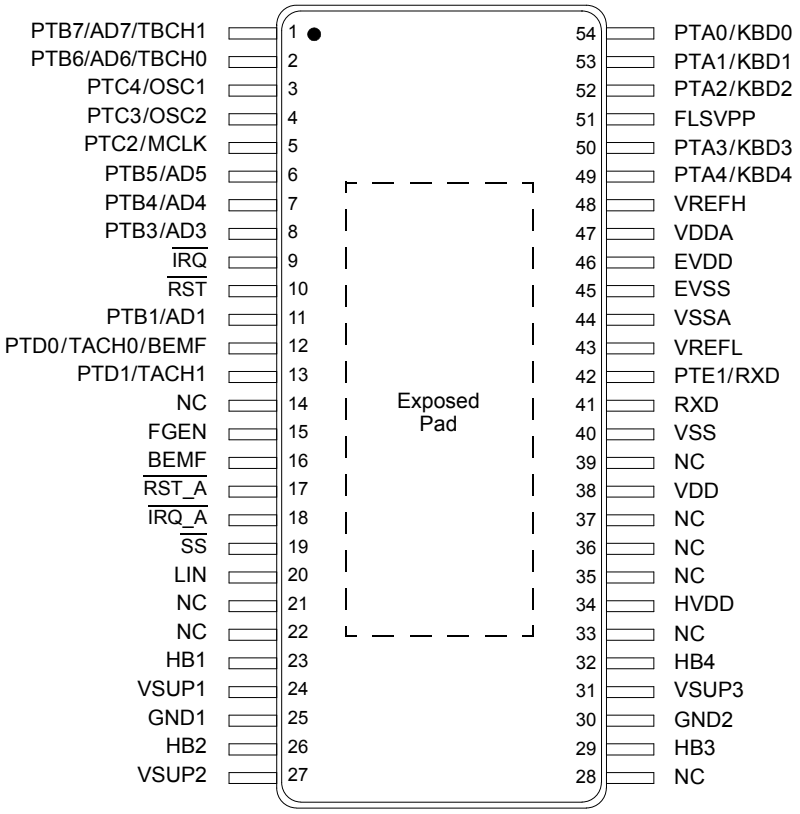


Figure 3. 908E626 Pin Connections

Table 1. 908E626 PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	10	RST	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0/BEMF PTD1/TACH1	Port D I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.

Table 1. 908E626 PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Die	Pin	Pin Name	Formal Name	Definition
–	14, 21, 22, 28, 33, 35, 36, 37, 39	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bidirectional I/O port pin that can is shared with other functional modules in the MCU.
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	15	FGEN	Current Limitation Frequency Input	This is the input pin for the half-bridge current limitation PWM frequency.
Analog	16	BEMF	Back Electromagnetic Force Output	This pin gives the user information about back electromagnetic force (BEMF).
Analog	17	$\overline{\text{RST\_A}}$	Internal Reset	This pin is the bidirectional reset pin of the analog die.
Analog	18	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	19	$\overline{\text{SS}}$	Slave Select	This pin is the SPI slave select pin for the analog chip.
Analog	20	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	23 26 29 32	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.
Analog	24 27 31	VSUP1 VSUP2 VSUP3	Power Supply Pins	These pins are device power supply pins.
Analog	25 30	GND1 GND2	Power Ground Pins	These pins are device power ground connections.
Analog	34	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3 pin Hall-effect sensors.
Analog	38	VDD	Voltage Regulator Output	The 5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	40	VSS	Voltage Regulator Ground	Ground pin for the connection of all non-power ground connections (microcontroller and sensors).
Analog	41	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.
–	EP	Exposed Pad	Exposed Pad	The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-state)	$V_{SUP(SS)}$	-0.3 to 28	
Analog Chip Supply Voltage under Transient Conditions (1)	$V_{SUP(PK)}$	-0.3 to 40	
Microcontroller Chip Supply Voltage	V_{DD}	-0.3 to 6.0	
Input Pin Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to 5.5	
Microcontroller Chip	$V_{IN(MCU)}$	V_{SS}-0.3 to V_{DD}+0.3	
Maximum Microcontroller Current per Pin			mA
All Pins Except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
Pins PTA0:PTA6, PTC0:PTC1	$I_{PIN(2)}$	±25	
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage			V
Normal Operation (Steady-state)	$V_{BUS(SS)}$	-18 to 28	
Transient Conditions (1)	$V_{BUS(DYNAMIC)}$	40	
ESD Voltage			V
Human Body Model (2)	V_{ESD1}	±3000	
Machine Model (3)	V_{ESD2}	±150	
Charge Device Model (4)	V_{ESD3}	±500	

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0 pF).

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Case Temperature (5)	T_C	-40 to 115	°C
Operating Junction Temperature(6)	T_J	-40 to 135	°C
Peak Package Reflow Temperature During Solder Mounting (7)(8)	T_{PPRT}	Note 8	°C

Notes

5. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
6. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150 °C under these conditions
7. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT					
NORMAL Mode V_{SUP} = 12 V, Power Die ON (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	–	20	–	mA
STOP Mode (9) V_{SUP} = 12 V, Cyclic Wake-up Disabled	I_{STOP}	–	–	75	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$					V
Low State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.0 µA)	V_{OH}	3.85	–	–	
Output Pins BEMF, RXD					V
Low State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.5 mA)	V_{OH}	3.85	–	–	
Output Pin RXD– Capacitance (10)	C_{IN}	–	4.0	–	pF
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$–Capacitance (10)	C_{IN}	–	4.0	–	pF
Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$–Pull-up Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Pin $\overline{SS}$–Pull-up Resistor	$R_{PULLUP2}$	–	60	–	kΩ
Pins FGEN, MOSI, SPSCK–Pull-down Resistor	$R_{PULLDOWN}$	–	60	–	kΩ
Pin TXD–Pull-up Current Source	I_{PULLUP}	–	35	–	µA

Notes

9. STOP mode current will increase if V_{SUP} exceeds 15 V.
10. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
High Voltage Reset					V
Threshold	V_{HVRON}	27	30	33	
Hysteresis	V_{HVRH}	–	1.5	–	
Low Voltage Reset					
Threshold	V_{LVRON}	3.6	4.0	4.7	V
Hysteresis	V_{LVRH}	–	100	–	mV
High Voltage Interrupt					V
Threshold	V_{HVION}	17.5	21	23	
Hysteresis	V_{HVIH}	–	1.0	–	
Low Voltage Interrupt					V
Threshold	V_{LVION}	6.5	–	8.0	
Hysteresis	V_{LVIH}	–	0.4	–	
High Temperature Reset (12)					°C
Threshold	T_{RON}	–	170	–	
Hysteresis	T_{RH}	5.0	–	–	
High Temperature Interrupt (13)					°C
Threshold	T_{ION}	–	160	–	
Hysteresis	T_{IH}	5.0	–	–	
VOLTAGE REGULATOR					
Normal Mode Output Voltage I_{OUT} = 60 mA, 6.0 V < V_{SUP} < 18 V	V_{DDRUN}	4.75	5.0	5.25	V
Load Regulation I_{OUT} = 80 mA, V_{SUP} = 9.0 V	V_{LR}	–	–	100	mV
STOP Mode Output Voltage (Maximum Output Current 100 μA)(11)	V_{DDSTOP}	4.45	4.7	5.0	V

Notes

11. Tested to be VLVRON < VDDSTOP
12. This parameter is guaranteed by process monitoring but is not production tested.
13. High Temperature Interrupt (HTI) threshold is linked to High Temperature Reset (HTR) threshold (HTR = HTI + 10 °C).

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Output Low Level TXD LOW, 500 Ω Pull-up to V_{SUP}	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level TXD HIGH, I_{OUT} = 1.0 µA	$V_{LIN-HIGH}$	V_{SUP}-1.0	–	–	V
Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Leakage Current to GND Recessive State (-0.5 V < V_{LIN} < V_{SUP})	$I_{BUS\_PAS\_REC}$	0.0	–	20	µA
Leakage Current to GND (V_{SUP} Disconnected) Including Internal Pull-up Resistor, V_{LIN} @ -18 V Including Internal Pull-up Resistor, V_{LIN} @ +18 V	 $I_{BUS\_NO\_GND}$ I_{BUS}	 – –	 -600 25	 – –	µA
LIN Receiver Recessive Dominant Threshold Input Hysteresis	 V_{IH} V_{IL} V_{ITH} V_{IHY}	 0.6V_{LIN} 0 – 0.01V_{SUP}	 – – V_{SUP}/2 –	 V_{SUP} 0.4V_{LIN} – 0.1V_{SUP}	V
LIN Wake-up Threshold	V_{WTH}	–	V_{SUP}/2	–	V
HALF-BRIDGE OUTPUTS (HB1:HB4)					
Switch ON Resistance @ T_J = 25 °C with I_{LOAD} = 1.0 A High Side Low Side	 $R_{DS(ON)HB\_HS}$ $R_{DS(ON)HB\_LS}$	 – –	 425 400	 500 500	mΩ
High Side Overcurrent Shutdown	I_{HBHSOC}	3.0	–	7.5	A
Low Side Overcurrent Shutdown	I_{HBLSOC}	2.5	–	7.5	A
Low Side Current Limitation @ T_J = 25 °C Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1) Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0) Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1) Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0) Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	 I_{CL1} I_{CL2} I_{CL3} I_{CL4} I_{CL5}	 – 210 300 450 600	 55 260 370 550 740	 – 315 440 650 880	mA
Half-bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	-30	0.0	V
Half-bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A]) CSA = 1 CSA = 0	 $RATIO_H$ $RATIO_L$	 7.0 1.0	 12.0 2.0	 14.0 3.0	V/A

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHABLE V_{DD} OUTPUT (HVDD)					
Overcurrent Shutdown Threshold	$I_{HVDDOCT}$	24	30	40	mA
V_{SUP} DOWN-SCALER					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} /V_{ADOUT})	$RATIO_{VSUP}$	4.8	5.1	5.35	–
INTERNAL DIE TEMPERATURE SENSOR					
Voltage/Temperature Slope	S_{TTOV}	–	19	–	mV/°C
Output Voltage @ 25 °C	V_{T25}	1.7	2.1	2.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 135 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Propagation Delay (14), (15)					µs
TXD LOW to LIN LOW	$t_{TXD-LIN-LOW}$	–	–	6.0	
TXD HIGH to LIN HIGH	$t_{TXD-LIN-HIGH}$	–	–	6.0	
LIN LOW to RXD LOW	$t_{LIN-RXD-LOW}$	–	4.0	8.0	
LIN HIGH to RXD HIGH	$t_{LIN-RXD-HIGH}$	–	4.0	8.0	
TXD Symmetry	$t_{TXD-SYM}$	-2.0	–	2.0	
RXD Symmetry	$t_{RXD-SYM}$	-2.0	–	2.0	
Output Falling Edge Slew Rate (14), (16)	SR_F				V/µs
80% to 20%		-1.0	-2.0	-3.0	
Output Rising Edge Slew Rate (14), (16)	SR_R				V/µs
20% to 80%, R_{BUS} > 1.0 kΩ, C_{BUS} < 10 nF		1.0	2.0	3.0	
LIN Rise/Fall Slew Rate Symmetry (14), (16)	SR_S	-2.0	–	2.0	µs
AUTONOMOUS WATCHDOG (AWD)					
AWD Oscillator Period	t_{OSC}	–	40	–	µs
AWD Period Low = 512 t_{OSC}	t_{AWDPH}				ms
TJ < 25 °C		16	27	34	
TJ ≥ 25 °C		16	22	28	
AWD Period High = 256 t_{OSC}	t_{AWDPL}				ms
TJ < 25 °C		8.0	13.5	17	
TJ ≥ 25 °C		8.0	11	14	
AWD Cyclic Wake-up On Time	$t_{AWDHPON}$	–	90	–	µs

Notes
14. All LIN characteristics are for initial LIN slew rate selection (20 kbaud) (SRS0:SRS1= 00).
15. See Figure 4, page 12.
16. See Figure 5, page 13.

MICROCONTROLLER PARAMETRICS

Table 5. MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with Two Channels (TIM A and TIM B)
Flash	16 k Bytes
RAM	512 Bytes

Table 5. MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
ADC	10 Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud Rate Adjustment
ICG	Internal Clock Generation Module
BEMF Counter	Special Counter for *SMARTMOS* BEMF Output

TIMING DIAGRAMS

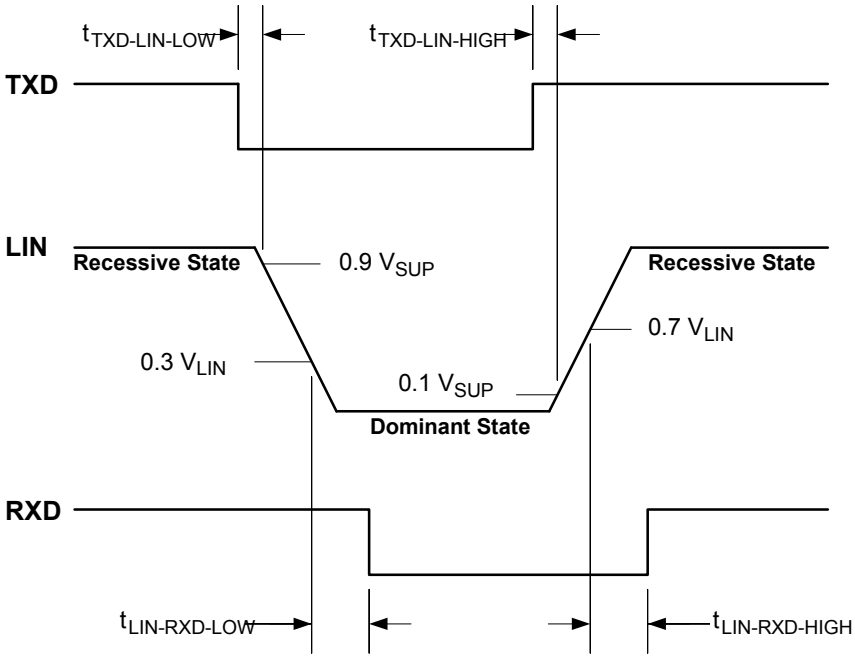
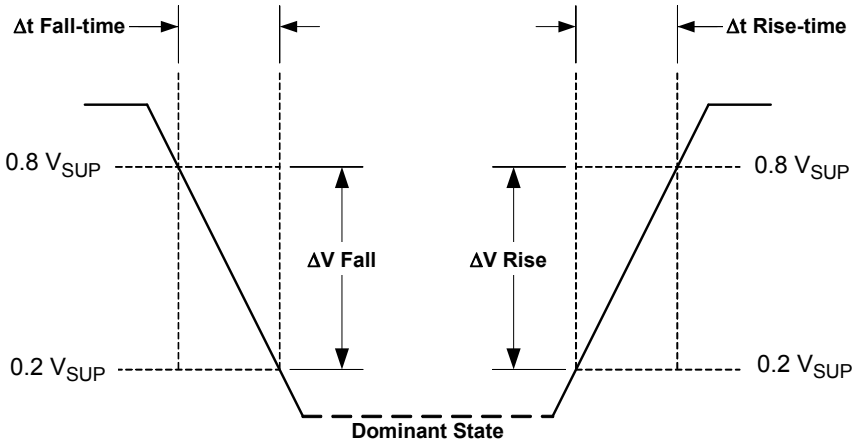


Figure 4. LIN Timing Description



$$SR_F = \frac{\Delta V\ Fall}{\Delta t\ Fall\text{-}time} \qquad SR_R = \frac{\Delta V\ Rise}{\Delta t\ Rise\text{-}time}$$

Figure 5. LIN Slew Rate Description

FUNCTIONAL DIAGRAMS

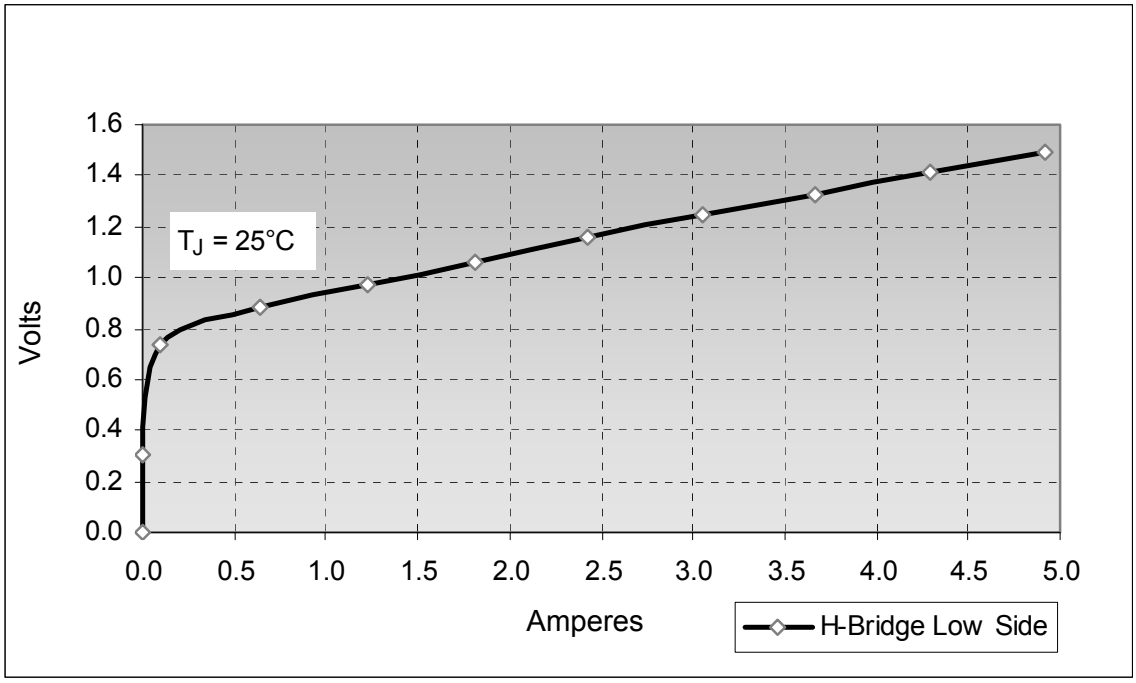


Figure 6. Free Wheel Diode Forward Voltage

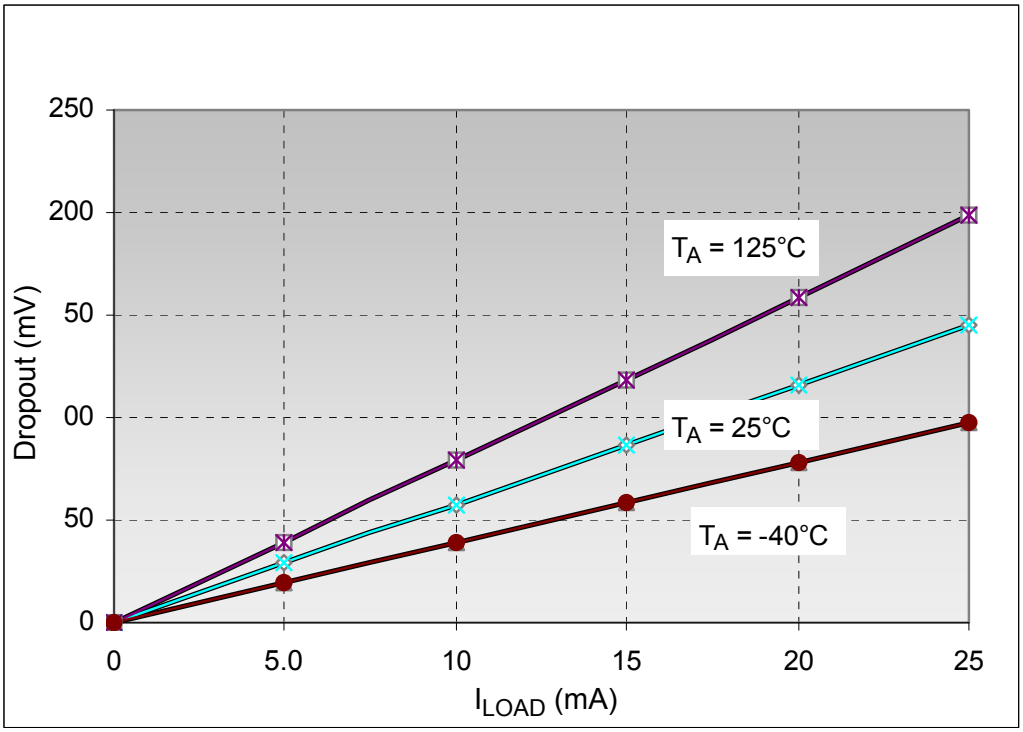


Figure 7. Dropout Voltage on HVDD

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E626 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E626 is well suited to perform stepper motor control, e.g. for climate or light-levelling control via a 3-wire LIN bus.

This device combines an standard HC08 MCU core (68HC908EY16) with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as four half-bridge outputs. Other ports are also provided including a selectable HVDD pin. An internal voltage regulator is provided on the *SMARTMOS* IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables the device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

FUNCTIONAL PIN DESCRIPTION

See Figures 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on Figures 3 for a depiction of the pin locations on the package.

PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/$\overline{SS}$ pin is likewise not accessible.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O PINS (PTB1, PTB3:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc. The PTB2/AD2 pin is not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O PINS (PTD0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

In step motor applications, the PTD0 pin should be connected to the BEMF output of the analog die, to evaluate the BEMF signal with a special BEMF module of the MCU.

PTD1 pin is recommended for use as an output pin for generating the FGEN signal (PWM signal), if required by the application.

PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die.The connection for the receiver must be done externally.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

CURRENT LIMITATION FREQUENCY INPUT PIN (FGEN)

Input pin for the half-bridge current limitation PWM frequency. This input is not a real PWM input pin; it should just supply the period of the PWM. The duty cycle will be generated automatically.

Important The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

BACK ELECTROMAGNETIC FORCE OUTPUT PIN (BEMF)

This pin gives the user information about back electromagnetic force (BEMF). This feature allows stall detection and coil failures in step motor applications. In order to evaluate this signal the pin must be directly connected to pin PTD0/TACH0/BEMF.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

SLAVE SELECT PIN ($\overline{\text{SS}}$)

This pin is the SPI Slave Select pin for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E626 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.

The HB1:HB4 outputs are short-circuit and overtemperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low side MOSFETs.

POWER SUPPLY PINS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; The output is short-circuit protected.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD, VDDA, and VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL pins must be connected together.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces.

VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INTERRUPTS

The 908E626 has six different interrupt sources as described in the following paragraphs. The interrupts can be disabled or enabled via the SPI. After reset all interrupts are automatically disabled.

LOW VOLTAGE INTERRUPT

The Low Voltage Interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. If the Low Voltage Interrupt is enabled, an interrupt will be initiated.

With LVI the H-Bridges (high side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

During STOP mode the LVI circuitry is disabled.

HIGH VOLTAGE INTERRUPT

The High Voltage Interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVI flag. If the High Voltage Interrupt is enabled, an interrupt will be initiated.

With HVI the H-Bridges (high side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

During STOP mode the HVI circuitry is disabled.

HIGH TEMPERATURE INTERRUPT

The High Temperature Interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. If the High Temperature Interrupt is enabled, an interrupt will be initiated.

During STOP mode the HTI circuitry is disabled.

AUTONOMOUS WATCHDOG INTERRUPT (AWD)

Refer to Autonomous Watchdog (AWD) on page 30.

LIN INTERRUPT

If the LINIE bit is set, a falling edge on the LIN pin will generate an interrupt. During STOP mode this interrupt will initiate a system wake-up.

OVERCURRENT INTERRUPT

If an overcurrent condition on a half-bridge or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

SYSTEM WAKE-UP

System wake-up can be initiated by any of four events:

- A falling edge on the LIN pin
- A wake-up signal from the AWD
- An LVR condition

If one of these wake-up events occurs and the interrupt mask bit for this event is set, the interrupt will wake-up the microcontroller as well as the main voltage regulator (MREG) Figures 8.

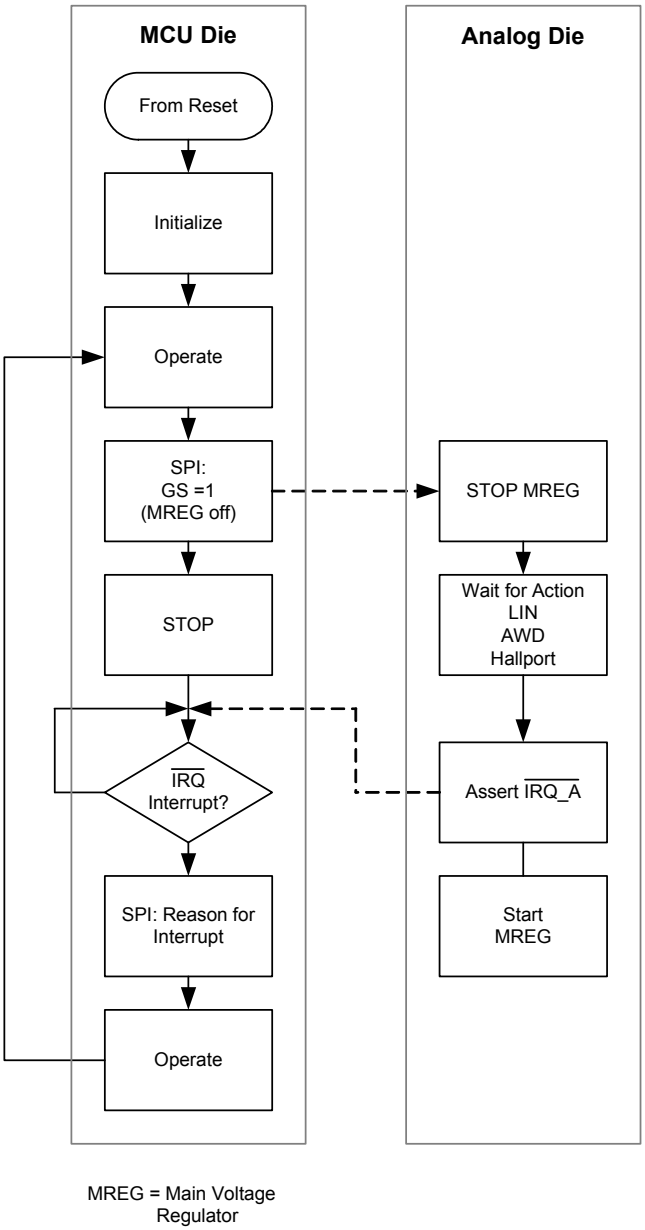


Figure 8. STOP Mode/Wake-up Procedure

INTERRUPT FLAG REGISTER (IFR)

Register Name and Address: IFR - $05

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	LINF	HTF	LVF	HVF	OCF	0
Write								
Reset	0	0	0	0	0	0	0	0

LINF—LIN FLAG BIT

This read/write flag is set on the falling edge at the LIN data line. Clear LINF by writing a logic [1] to LINF. Reset clears the LINF bit. Writing a logic [0] to LINF has no effect.

- 1 = Falling edge on LIN data line has occurred.
- 0 = Falling edge on LIN data line has not occurred since last clear.

HTF—HIGH TEMPERATURE FLAG BIT

This read/write flag is set on a high temperature condition. Clear HTF by writing a logic [1] to HTF. If a high temperature condition is still present while writing a logic [1] to HTF, the writing has no effect. Therefore, a high temperature interrupt cannot be lost due to inadvertent clearing of HTF. Reset clears the HTF bit. Writing a logic [0] to HTF has no effect.

- 1 = High temperature condition has occurred.

- 0 = High temperature condition has not occurred.

LVF—LOW VOLTAGE FLAG BIT

This read/write flag is set on a low voltage condition. Clear LVF by writing a logic [1] to LVF. If a low voltage condition is still present while writing a logic [1] to LVF, the writing has no effect. Therefore, a low voltage interrupt cannot be lost due to inadvertent clearing of LVF. Reset clears the LVF bit. Writing a logic [0] to LVF has no effect.

- 1 = Low voltage condition has occurred.
- 0 = Low voltage condition has not occurred.

HVF—HIGH VOLTAGE FLAG BIT

This read/write flag is set on a high voltage condition. Clear HVF by writing a logic [1] to HVF. If high voltage condition is still present while writing a logic [1] to HVF, the writing has no effect. Therefore, a high voltage interrupt cannot be lost due to inadvertent clearing of HVF. Reset clears the HVF bit. Writing a logic [0] to HVF has no effect.

- 1 = High voltage condition has occurred.
- 0 = High voltage condition has not occurred.

OCF—OVERCURRENT FLAG BIT

This read-only flag is set on an overcurrent condition. Reset clears the OCF bit. To clear this flag, write a logic [1] to the appropriate overcurrent flag in the SYSSTAT Register. See Figure 9, which shows the two signals triggering the OCF.

- 1 = High current condition has occurred.
- 0 = High current condition has not occurred.

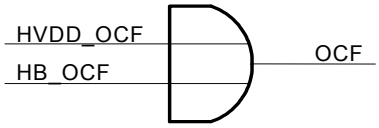


Figure 9. Principal Implementation for OCF

INTERRUPT MASK REGISTER (IMR)

Register Name and Address: IMR - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
Write								
Reset	0	0	0	0	0	0	0	0

LINIE—LIN LINE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the LIN flag, LINF. Reset clears the LINIE bit.

- 1 = Interrupt requests from LINF flag enabled.
- 0 = Interrupt requests from LINF flag disabled.

HTIE—HIGH TEMPERATURE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high temperature flag, HTF. Reset clears the HTIE bit.

- 1 = Interrupt requests from HTF flag enabled.
- 0 = Interrupt requests from HTF flag disabled.

LVIE—LOW VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the low voltage flag, LVF. Reset clears the LVIE bit.

- 1 = Interrupt requests from LVF flag enabled.
- 0 = Interrupt requests from LVF flag disabled.

HVIE—HIGH VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high voltage flag, HVF. Reset clears the HVIE bit.

- 1 = Interrupt requests from HVF flag enabled.
- 0 = Interrupt requests from HVF flag disabled.

OCIE—OVERCURRENT INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the overcurrent flag, OCF. Reset clears the OCIE bit.

- 1 = Interrupt requests from OCF flag enabled.
- 0 = Interrupt requests from OCF flag disabled.

RESET

The 908E626 chip has four internal reset sources and one external reset source, as explained in the paragraphs below. Figure 10 depicts the internal reset sources.

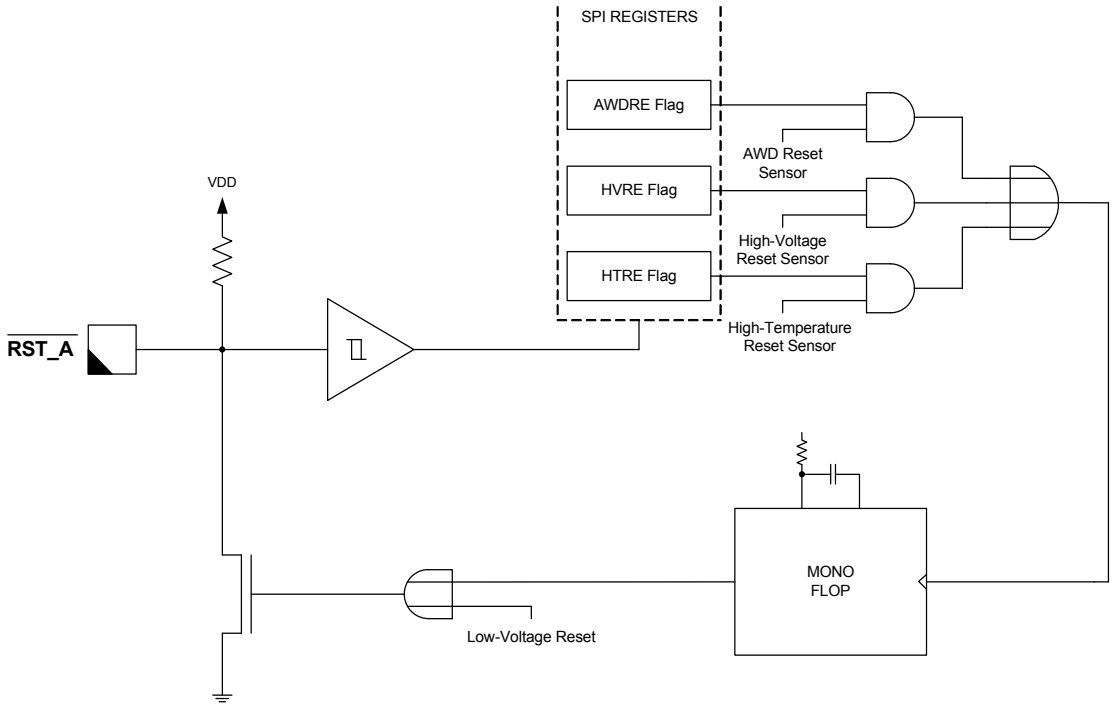


Figure 10. Internal Reset Routing

RESET INTERNAL SOURCES

Autonomous Watchdog

AWD modules generates a reset because of a timeout (watchdog function).

High Temperature Reset

To prevent damage to the device, a reset will be initiated if the temperature rises above a certain value. The reset is maskable with bit HTRE in the Reset Mask Register. After a reset the high temperature reset is disabled.

Low Voltage Reset

The LVR is related to the internal V_{DD}. In case the voltage falls below a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ pin.

High Voltage Reset

The HVR is related to the external V_{SUP} voltage. In case the voltage is above a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ pin. The reset is maskable with bit HVRE in the Reset Mask Register. After a reset the high voltage reset is disabled.

RESET EXTERNAL SOURCE

External Reset Pin

The microcontroller has the capability of resetting the *SMARTMOS* device by pulling down the $\overline{\text{RST}}$ pin.

Reset Mask Register (RMR)

Register Name and Address: RMR - $06

	Bit7	6	5	4	3	2	1	Bit0
Read	TTEST	0	0	0	0	0	HVRE	HTRE
Write								
Reset	0	0	0	0	0	0	0	0

TTEST—High Temperature Reset Test

This read/write bit is for test purposes only. It decreases the overtemperature shutdown limit for final test. Reset clears the HTRE bit.

- 1 = Low temperature threshold enabled.
- 0 = Low temperature threshold disabled.

HVRE—High Voltage Reset Enable Bit

This read/write bit enables resets on high voltage conditions. Reset clears the HVRE bit.

- 1 = High voltage reset enabled.
- 0 = High voltage reset disabled.

HTRE—High Temperature Reset Enable Bit

This read/write bit enables resets on high temperature conditions. Reset clears the HTRE bit.

- 1 = High temperature reset enabled.
- 0 = High temperature reset disabled.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E626.

The interface consists of four pins (see Figure 11):

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock (maximum frequency 4.0 MHz)

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.

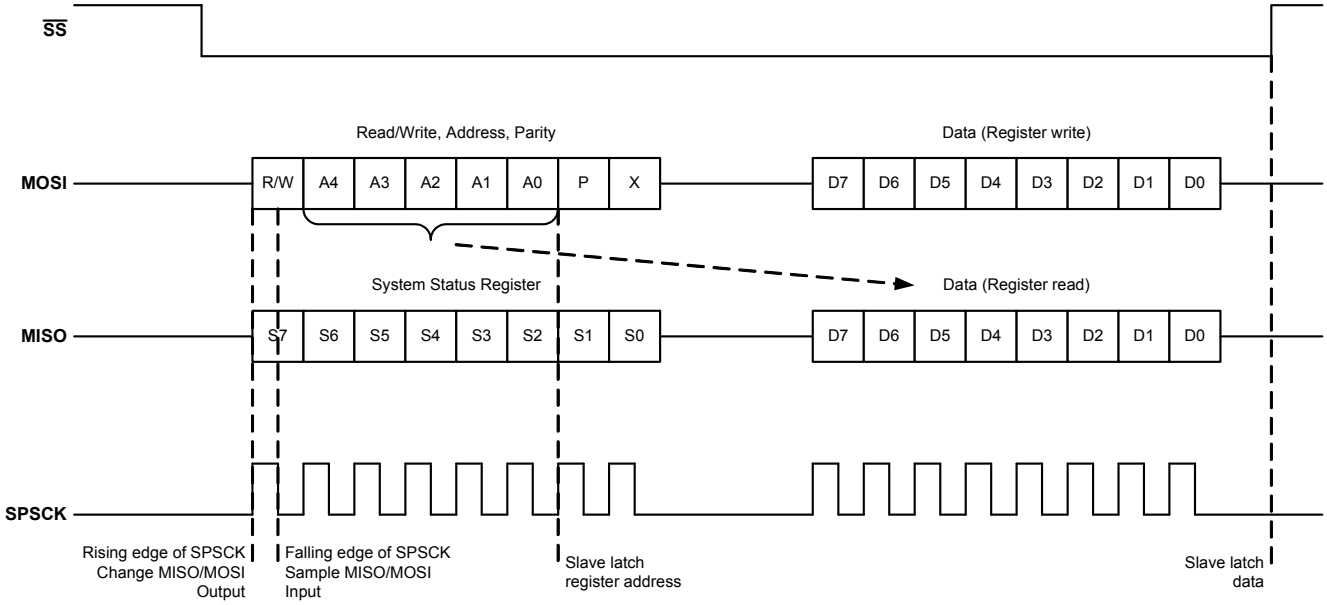


Figure 11. SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer is prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high-impedance.

MASTER ADDRESS BYTE

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

Parity P

The parity bit is equal to “0” if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals “1”. For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals “0.”

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

Contains data to be written or no valid data during a read operation.

Table 6. List of Registers

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$01	H-bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	H-bridge Control (HBCTL)	R	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
		W								
$03	System Control (SYSCTL)	R	PSON	SRS1	SRS0	0	0	0	0	0
		W								GS
$04	Interrupt Mask (IMR)	R	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
		W								
$05	Interrupt Flag (IFR)	R	0	0	LINF	HTF	LVF	HVF	OCF	0
		W								
$06	Reset Mask (RMR)	R	TTEST	0	0	0	0	0	HVRE	HTRE
		W								
$07	Analog Multiplexer Configuration (ADMUX)	R	0	0	0	0	SS3	SS2	SS1	SS0
		W								
$08	Reserved	R	0	0	0	0	0	0	0	0
		W								
$09	Reserved	R	0	0	0	0	0	0	0	0
		W								
$0a	AWD Control (AWDCTL)	R	0	0	0	AWDRE	AWDIE	0	AWDF	AWDR
		W			AWDRST					
$0b	Power Output (POUT)	R	0	0	0	0	0	0	HVDDON	0
		W								
$0c	System Status (SYSSTAT)	R	0	LINCL	HVDD_OCF	0	LVF	HVF	HB_OCF	HTF
		W								

Slave Status Byte

Contains the contents of the System Status Register ($0c) independent of whether it is a write or read operation or which register was selected.

Slave Data Byte

Contains the contents of selected register. During a write operation it includes the register content prior to a write operation.

SPI Register Overview

Table 6 summarizes the SPI Register addresses and the bit names of each register.

ANALOG DIE I/OS

LIN Physical Layer

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with internal current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled by setting the PSON bit in the System Control Register (SYSCTL). If the transmitter works in the current limitation region, the LINCL bit in the System Status Register (SYSSTAT) is set. Due to excessive power dissipation in the transmitter, software is advised to monitor this bit and turn the transmitter off immediately.

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see Figure 2). When TXD is LOW, LIN output is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off. The TXD pin has an internal pull-up current source in order to set the LIN bus in recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode/Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. The receiver pin is still active and able to detect wake-up events on the LIN bus line.If LIN interrupt is enabled (LINIE bit in the Interrupt Mask Register is set), a falling edge on the LIN line causes an interrupt. This interrupt switches on the main voltage regulator and generates a system wake-up.

Analog Multiplexer/ADOUT Pin

The ADOUT pin is the analog output interface to the ADC of the MCU (see Figure 2). An analog multiplexer is used to read six internal diagnostic analog voltages.

Current Recopy

The analog multiplexer is connected to the four low side current sense circuits of the half-bridges. These sense circuits offer a voltage proportional to the current through the low side MOSFET. High or low resolution is selectable: 5.0 V/2.5 A or 5.0 V/500 mA, respectively. (Refer to Half-bridge Current Recopy on page 27.)

Temperature Sensor

The 908E626 includes an on-chip temperature sensor. This sensor offers a voltage that is proportional to the actual chip junction temperature.

V_{SUP} Prescaler

The V_{SUP} prescaler permits the reading or measurement of the external supply voltage. The output of this voltage is $V_{SUP}/RATIO_{VSUP}$.

The different internal diagnostic analog voltages can be selected with the ADMUX Register.

Analog Multiplexer Configuration Register (ADMUX)

Register Name and Address: ADMUX - $07

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	SS3	SS2	SS1	SS0
Write								
Reset	0	0	0	0	0	0	0	0

SS3, SS2, SS1, and SS0—A/D Input Select Bits

These read/write bits select the input to the ADC in the microcontroller according to Table 7. Reset clears SS3, SS2, SS1, and SS0 bits.

Table 7. Analog Multiplexer Configuration Register

SS3	SS2	SS1	SS0	Channel
0	0	0	0	Current Recopy HB1
0	0	0	1	Current Recopy HB2
0	0	1	0	Current Recopy HB3
0	0	1	1	Current Recopy HB4
0	1	0	0	V_{SUP} Prescaler
0	1	0	1	Temperature Sensor
0	1	1	0	Not Used
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Power Output Register (POUT)

Register Name and Address: P_{OUT} - $0b

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0 (17)	0 (17)	0 (17)	0 (17)	HVDD ON	0 (17)
Write								
Reset	0	0	0	0	0	0	0	0

Notes

17. This bit must always be set to 0.

HVDDON—HVDD On Bit

This read/write bit enables HVDD output. Reset clears the HVDDON bit.

- 1 = HVDD enabled.
- 0 = HVDD disabled.

HALF-BRIDGES

Outputs HB1:HB4 provide four low resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high side, or low side configurations.

Reset clears all bits in the H-Bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short-circuit (overcurrent) protection on high side and low side MOSFETs.
- Current recopy feature (low side MOSFET).
- Overtemperature protection.
- Overvoltage and undervoltage protection.
- Current limitation feature (low side MOSFET).

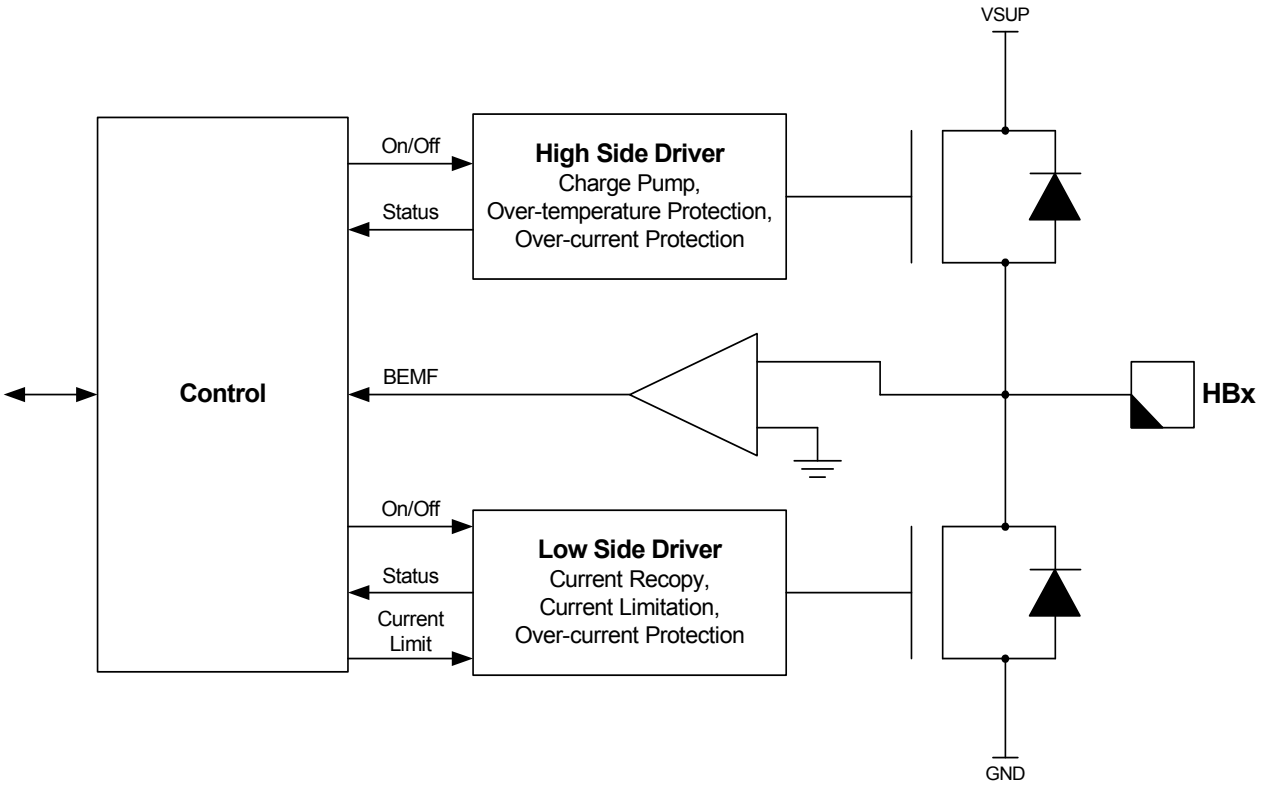


Figure 12. Half-bridge Push-Pull Output Driver

Half-bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists.Switching the high side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low side MOSFET on is blocked as long as the potential between gate and source of the high side MOSFET did not fall below a certain threshold.

Half-bridge Output Register (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_L—Low Side On/Off Bits

These read/write bits turn on the low side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low side MOSFET turned on for half-bridge output x.
- 0 = Low side MOSFET turned off for half-bridge output x.