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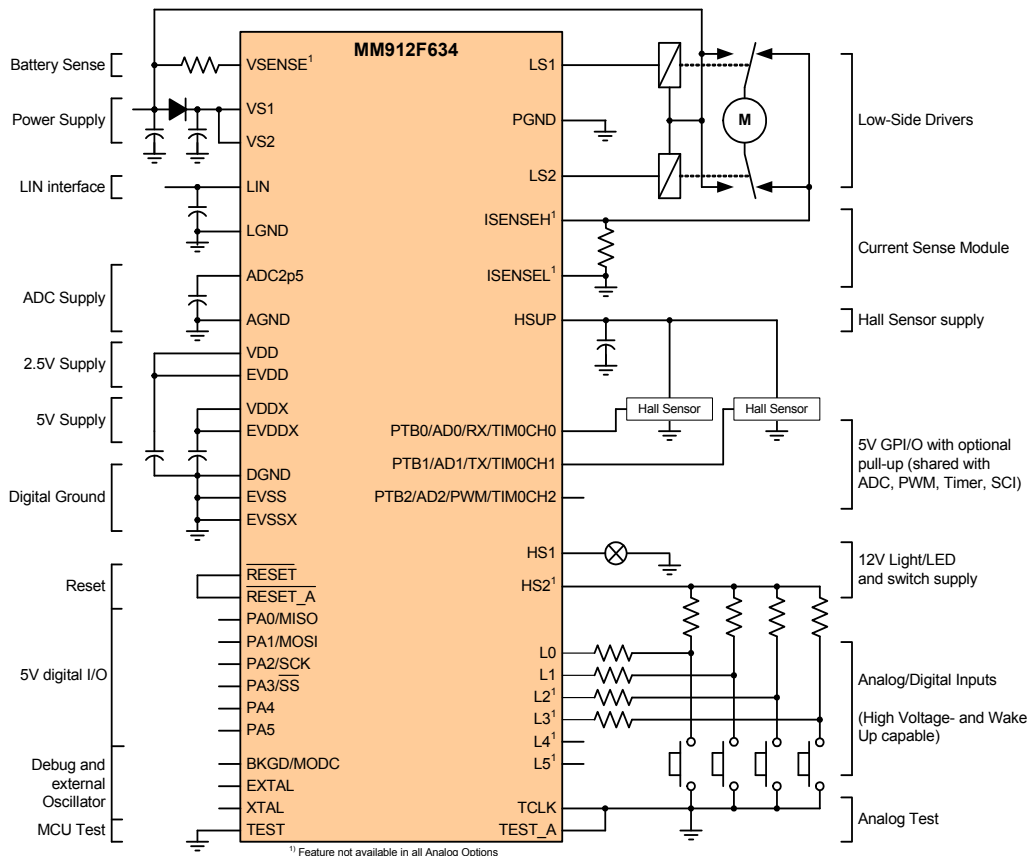
# Integrated S12 Based Relay Driver with LIN

The MM912F634 is an integrated single package solution that integrates an HCS12 microcontroller with a SMARTMOS analog control IC. The Die to Die Interface (D2D) controlled analog die combines system base chip and application specific functions, including a LIN transceiver.

## Features

- 16-Bit S12 CPU, 32 kByte FLASH, 2.0 kByte RAM
- Background Debug (BDM) & Debug Module (DBG)
- Die to Die bus interface for transparent memory mapping
- On-chip oscillator & two independent watchdogs
- LIN 2.1 Physical Layer Interface with integrated SCI
- Six digital MCU GPIOs shared with SPI (PA5...0)
- 10-Bit, 15 Channel - Analog to Digital Converter (ADC)
- 16-Bit, 4 Channel - Timer Module (TIM16B4C)
- 8-Bit, 2 Channel - Pulse width modulation module (PWM)
- Six high voltage / Wake-up inputs (L5.0)
- Three low voltage GPIOs (PB2.0)
- Low Power Modes with cyclic sense & forced wake-up
- Current Sense Module with selectable gain
- Reverse Battery protected Voltage Sense Module
- Two protected low side outputs to drive inductive loads
- Two protected high side outputs
- Chip temperature sensor
- Hall sensor supply
- Integrated voltage regulator(s)

<b>MM912F634</b>	
	48-PIN LQFP-EP, 7.0 mm x 7.0 mm AE SUFFIX: Exposed Pad Option
	48-PIN LQFP, 7.0 mm x 7.0 mm AP SUFFIX: Non-exposed Pad Option
<b>ORDERING INFORMATION</b>	
See Page 2.	



**Figure 1. Simplified Application Diagram**

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.



## Ordering Information

# 1 Ordering Information

**Table 1. Ordering Information**

Device (Add an R2 for Tape and Reel orders)	Temperature Range (T <sub>A</sub> )	Package	Max. Bus Frequency (MHz) (f <sub>BUSMAX</sub> )	Flash (kB)	RAM (kB)	Analog Option <sup>(1)</sup>	Stop mode wake-up
MM912F634CV1AE	-40 to 105 °C	98ASA00173D 48-PIN LQFP-EP	20	32	2	1	(2)
MM912F634DV1AE							Enhanced
MM912F634CV2AE						(2)	Enhanced
MM912F634DV2AE							
MM912F634CV2AP		2	(2)				
MM912F634DV2AP			Enhanced				
		98ASH00962A 48-PIN LQFP	16	32			

Note:

- See [Table 2](#).
- Refer to MM912F634, Silicon Analog Mask (M91W) / Digital Mask (M33G) Errata

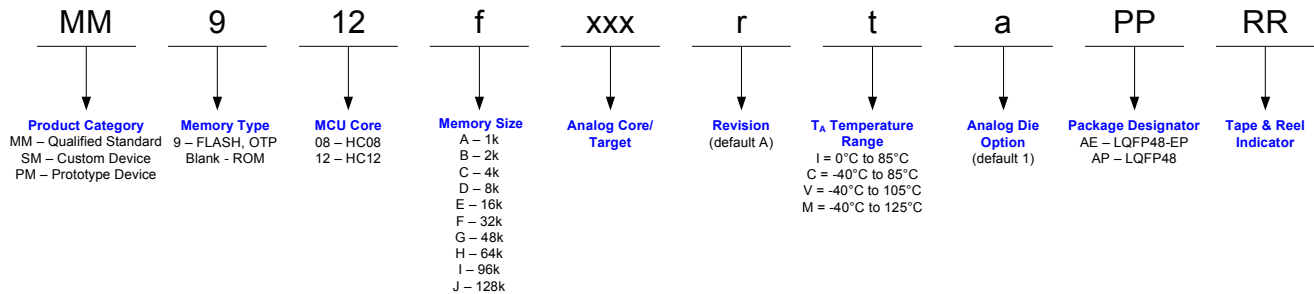
**Table 2. Analog Options<sup>(3)</sup>**

Feature	Option 1	Option 2
Current Sense Module	YES	NO
Wake-up Inputs (Lx)	L0...L5	L0...L3

Note:

- This table only highlights the analog die differences between the derivatives. See [Section 4.2.3, "Analog Die Options"](#) for detailed information.

The device part number is following the standard scheme below:



**Figure 2. Part Number Scheme**

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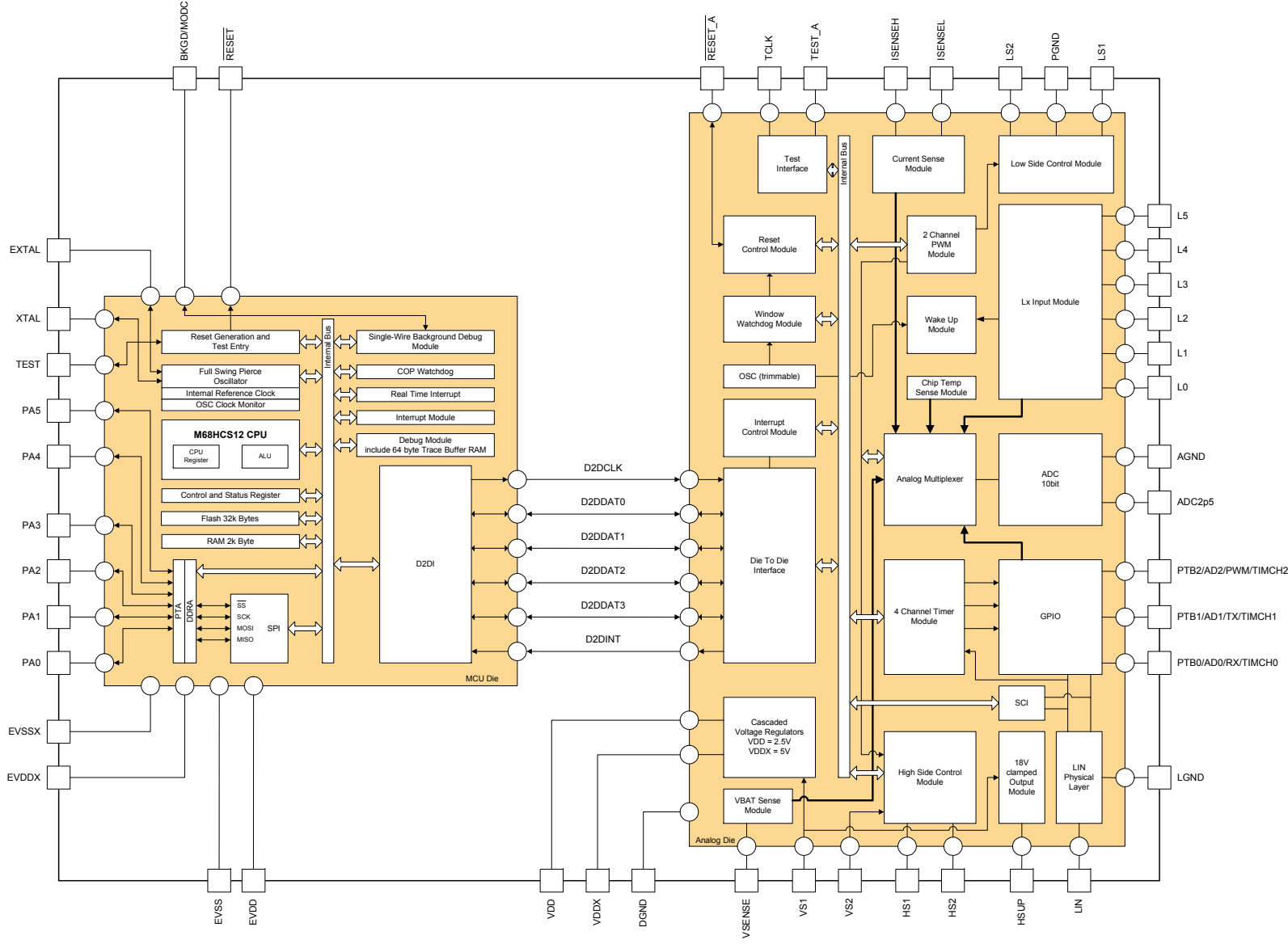


Figure 3. Device Block Diagram

## 2 Pin Assignment

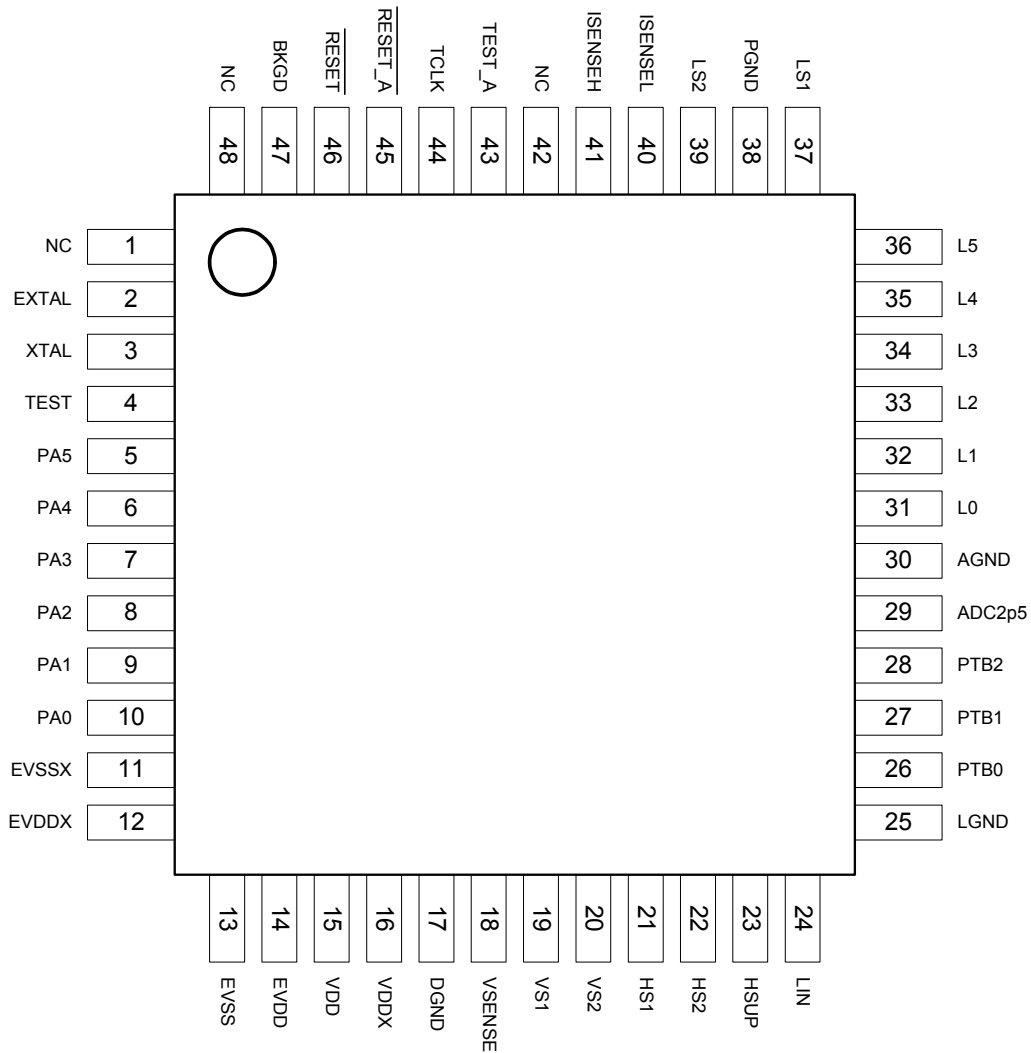


Figure 4. MM912F634 Pin Out

### NOTE

The device exposed pad (package option AE only) is recommended to be connected to GND.

Not all pins are available for analog die option 2. See [Section 4.2.3, "Analog Die Options"](#) for details.

## 2.1 MM912F634 Pin Description

The following table gives a brief description of all available pins on the MM912F634 package. Refer to the highlighted chapter for detailed information.

**Table 3. MM912F634 Pin Description**

Pin #	Pin Name	Formal Name	Description
1	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.
2	EXTAL	MCU Oscillator Pin	EXTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock. See <a href="#">Section 4.33, "External Oscillator (S12SS12SCRGV1)"</a> .
3	XTAL	MCU Oscillator Pin	XTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock. See <a href="#">Section 4.33, "External Oscillator (S12SS12SCRGV1)"</a> .
4	TEST	MCU Test Pin	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to EVSS in user mode.
5	PA5	MCU PA5 Pin	General purpose port A input or output pin 5. See <a href="#">Section 4.27, "Port Integration Module (9S12I32PIMV1)"</a>
6	PA4	MCU PA4 Pin	General purpose port A input or output pin 4. See <a href="#">Section 4.27, "Port Integration Module (9S12I32PIMV1)"</a> .
7	PA3	MCU PA3 / $\overline{SS}$ Pin	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI Interface. See <a href="#">Section 4.27, "Port Integration Module (9S12I32PIMV1)"</a> .
8	PA2	MCU PA2 / SCK Pin	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI Interface. See <a href="#">Section 4.27, "Port Integration Module (9S12I32PIMV1)"</a> .
9	PA1	MCU PA1 / MOSI Pin	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI Interface. See <a href="#">Section 4.27, "Port Integration Module (9S12I32PIMV1)"</a> .
10	PA0	MCU PA0 / MISO Pin	General-purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI Interface. See <a href="#">Section 4.27, "Port Integration Module (9S12I32PIMV1)"</a> .
11	EVSSX	MCU 5.0 V Ground Pin	Ground for the MCU 5.0 V power supply.
12	EVDDX	MCU 5.0 V Supply Pin	MCU 5.0 V - I/O buffer supply. See <a href="#">Section 4.26, "MM912F634 - MCU Die Overview"</a> .
13	EVSS	MCU 2.5 V Ground Pin	Ground for the MCU 2.5 V power supply.
14	EVDD	MCU 2.5 V Supply Pin	MCU 2.5 V - MCU Core- and Flash power supply. See <a href="#">Section 4.26, "MM912F634 - MCU Die Overview"</a> .
15	VDD	Voltage Regulator Output 2.5 V	+2.5 V main voltage regulator output pin. External capacitor ( $C_{VDD}$ ) needed. See <a href="#">Section 4.4, "Power Supply"</a> .
16	VDDX	Voltage Regulator Output 5.0 V	+5.0 V main voltage regulator output pin. External capacitor ( $C_{VDDX}$ ) needed. See <a href="#">Section 4.4, "Power Supply"</a> .
17	DGND	Digital Ground Pin	This pin is the device digital ground connection for the 5.0 V and 2.5 V logic. DGND, LGND, and AGND are internally connected to PGND via a back to back diode.
18	VSENSE	Voltage Sense Pin	Battery voltage sense input. This pin can be connected directly to the battery line for voltage measurements. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC via the analog multiplexer. The pin is self-protected against reverse battery connections. An external resistor ( $R_{VSENSE}$ ) is needed for protection <sup>(4)</sup> . See <a href="#">Section 4.22, "Supply Voltage Sense - VSENSE"</a> .

Table 3. MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
19	VS1	Power Supply Pin 1	This pin is the device power supply pin 1. VS1 is primarily supplying the VDDX Voltage regulator and the Hall Sensor Supply Regulator (HSUP). VS1 can be sensed via a voltage divider through the AD converter. Reverse battery protection diode is required. See <a href="#">Section 4.4, "Power Supply"</a>
20	VS2	Power Supply Pin 2	This pin is the device power supply pin 2. VS2 supplies the High Side Drivers (HSx). Reverse battery protection diode required. See <a href="#">Section 4.4, "Power Supply"</a>
21	HS1	High Side Output 1	This pin is the first High Side output. It is supplied through the VS2 pin. It is designed to drive small resistive loads with optional PWM. In cyclic sense mode, this output will activate periodically during low power mode. See <a href="#">Section 4.11, "High Side Drivers - HS"</a> .
22	HS2	High Side Output 2	This pin is the second High Side output. It is supplied through the VS2 pin. It is designed to drive small resistive loads with optional PWM. In cyclic sense mode, this output will activate periodically during low power mode. See <a href="#">Section 4.11, "High Side Drivers - HS"</a> .
23	HSUP	Hall Sensor Supply Output	This pin is designed as an 18 V Regulator to drive Hall Sensor Elements. It is supplied through the VS1 pin. An external capacitor (C <sub>HSUP</sub> ) is needed. See <a href="#">Section 4.10, "Hall Sensor Supply Output - HSUP"</a> .
24	LIN	LIN Bus I/O	This pin represents the single-wire bus transmitter and receiver. See <a href="#">Section 4.14, "LIN Physical Layer Interface - LIN"</a> .
25	LGND	LIN Ground Pin	This pin is the device LIN Ground connection. DGND, LGND, and AGND are internally connected to PGND via a back to back diode.
26	PTB0	General Purpose I/O 0	This is the General Purpose I/O pin 0 based on VDDX with the following shared functions: <ul style="list-style-type: none"> <li>• PTB0 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor.</li> <li>• AD0 - Analog Input Channel 0, 0...2.5 V (ADC2p5) analog input</li> <li>• TIM0CH0 - Timer Channel 0 Input/Output</li> <li>• Rx - Selectable connection to LIN / SCI</li> </ul> See <a href="#">Section 4.17, "General Purpose I/O - PTB[0...2]"</a> .
27	PTB1	General Purpose I/O 1	This is the General Purpose I/O pin 1 based on VDDX with the following shared functions: <ul style="list-style-type: none"> <li>• PTB1 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor.</li> <li>• AD1 - Analog Input Channel 1, 0...2.5 V (ADC2p5) analog input</li> <li>• TIM0CH1 - Timer Channel 1 Input/Output</li> <li>• Tx - Selectable connection to LIN / SCI</li> </ul> See <a href="#">Section 4.17, "General Purpose I/O - PTB[0...2]"</a> .
28	PTB2	General Purpose I/O 2	This is the General Purpose I/O pin 2 based on VDDX with the following shared functions: <ul style="list-style-type: none"> <li>• PTB2 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor.</li> <li>• AD2 - Analog Input Channel 2, 0...2.5 V (ADC2p5) analog input</li> <li>• TIM0CH2 - Timer Channel 2 Input/Output</li> <li>• PWM - Selectable connection to PWM Channel 0 or 1</li> </ul> See <a href="#">Section 4.17, "General Purpose I/O - PTB[0...2]"</a> .
29	ADC2p5	ADC Reference Voltage	This pin represents the ADC reference voltage and has to be connected to a filter capacitor. See <a href="#">Section 4.19, "Analog Digital Converter - ADC"</a>
30	AGND	Analog Ground Pin	This pin is the device Analog to Digital Converter ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.



Table 3. MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
31	L0	High Voltage Input 0	This pins is the High Voltage Input 0 with the following shared functions: <ul style="list-style-type: none"> <li>L0 - Digital High Voltage Input 0. When used as digital input, a series resistor (<math>R_{Lx}</math>) must be used to protect against automotive transients.<sup>(5)</sup></li> <li>AD3 - Analog Input 3 with selectable divider for 0...5.0 V and 0...18 V measurement range.</li> <li>WU0 - Selectable Wake-up input 0 for wake up and cyclic sense during low power mode.</li> </ul> See Section 4.16, "High Voltage Inputs - Lx"
32	L1	High Voltage Input 1	This pins is the High Voltage Input 1 with the following shared functions: <ul style="list-style-type: none"> <li>L1 - Digital High Voltage Input 1. When used as digital input, a series resistor (<math>R_{Lx}</math>) must be used to protect against automotive transients.<sup>(5)</sup></li> <li>AD4 - Analog Input 4 with selectable divider for 0...5.0 V and 0...18 V measurement range.</li> <li>WU1 - Selectable Wake-up input 1 for wake-up and cyclic sense during low power mode.</li> </ul> See Section 4.16, "High Voltage Inputs - Lx"
33	L2	High Voltage Input 2	This pins is the High Voltage Input 2 with the following shared functions: <ul style="list-style-type: none"> <li>L2 - Digital High Voltage Input 2. When used as digital input, a series resistor (<math>R_{Lx}</math>) must be used to protect against automotive transients.<sup>(5)</sup></li> <li>AD5 - Analog Input 5 with selectable divider for 0...5.0 V and 0...18 V measurement range.</li> <li>WU2 - Selectable Wake-up input 2 for wake-up and cyclic sense during low power mode.</li> </ul> See Section 4.16, "High Voltage Inputs - Lx".
34	L3	High Voltage Input 3	This pins is the High Voltage Input 3 with the following shared functions: <ul style="list-style-type: none"> <li>L3 - Digital High Voltage Input 3. When used as digital input, a series resistor (<math>R_{Lx}</math>) must be used to protect against automotive transients.<sup>(5)</sup></li> <li>AD6 - Analog Input 6 with selectable divider for 0...5.0 V and 0...18 V measurement range.</li> <li>WU3 - Selectable Wake-up input 3 for wake-up and cyclic sense during low power mode.</li> </ul> See Section 4.16, "High Voltage Inputs - Lx".
35	L4	High Voltage Input 4	This pins is the High Voltage Input 4 with the following shared functions: <ul style="list-style-type: none"> <li>L4 - Digital High Voltage Input 4. When used as digital input, a series resistor (<math>R_{Lx}</math>) must be used to protect against automotive transients.<sup>(5)</sup></li> <li>AD7 - Analog Input 7 with selectable divider for 0...5.0 V and 0...18 V measurement range.</li> <li>WU4 - Selectable Wake-up input 4 for wake-up and cyclic sense during low power mode.</li> </ul> See Section 4.16, "High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
36	L5	High Voltage Input 5	This pins is the High Voltage Input 5 with the following shared functions: <ul style="list-style-type: none"> <li>L5 - Digital High Voltage Input 5. When used as digital input, a series resistor (<math>R_{Lx}</math>) must be used to protect against automotive transients.<sup>(5)</sup></li> <li>AD8 - Analog Input 8 with selectable divider for 0...5.0 V and 0...18 V measurement range.</li> <li>WU5 - Selectable Wake-up input 5 for wake-up and cyclic sense during low power mode.</li> </ul> See Section 4.16, "High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
37	LS1	Low Side Output 1	Low Side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, "Low Side Drivers - LSx"
38	PGND	Power Ground Pin	This pin is the device Low Side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.

Table 3. MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
39	LS2	Low Side Output 2	Low Side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, "Low Side Drivers - LSx"
40	ISENSEL	Current Sense Pins L	Current Sense differential input "Low". This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 4.20, "Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pins H	Current Sense differential input "High". This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. See Section 4.20, "Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode Pin	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 4.9, "Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. $V_{DDX}$ based. See Section 4.7, "Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset Pin	The $\overline{\text{RESET}}$ pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to EVDDX.
47	BKGD	MCU Background Debug and Mode Pin	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$ . The BKGD pin has a pull-up device.
48	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.

## Note:

- An optional filter capacitor  $C_{VSENSE}$  is recommended to be placed between the board connector and  $R_{VSENSE}$  to GND for increased ESD performance.
- An optional filter capacitor  $C_{Lx}$  is recommended to be placed between the board connector and  $R_{Lx}$  to GND for increased ESD performance.

## 2.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

**Table 4. Signal Properties Summary**

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
EXTAL	—	V <sub>DD</sub>	NA	NA	Oscillator pins
XTAL	—	V <sub>DD</sub>	NA	NA	
$\overline{\text{RESET}}$	—	V <sub>DDX</sub>	Pull-up		External reset
TEST	—	N.A.	$\overline{\text{RESET}}$ pin	Down	Test input
BKGD	MODC	V <sub>DDX</sub>	Always on	UP	Background debug
PA5	—	V <sub>DDX</sub>	NA	NA	Port A I/O
PA4	—	V <sub>DDX</sub>	NA	NA	Port A I/O
PA3	SS	V <sub>DDX</sub>	NA	NA	Port A I/O, SPI
PA2	SCK	V <sub>DDX</sub>	NA	NA	Port A I/O, SPI
PA1	MOSI	V <sub>DDX</sub>	NA	NA	Port A I/O, SPI
PA0	MISO	V <sub>DDX</sub>	NA	NA	Port A I/O, SPI

### 3 Electrical Characteristics

#### 3.1 General

This supplement contains electrical information for the embedded MC9S12132 microcontroller die, as well as the MM912F634 analog die.

#### 3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level. All voltages are with respect to ground unless otherwise noted.

**Table 5. Absolute Maximum Electrical Ratings - Analog Die**

Ratings	Symbol	Value	Unit
Supply Voltage at VS1 and VS2 Normal Operation (DC) Transient Conditions (load dump) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	$V_{SUP(SS)}$ $V_{SUP(PK)}$ $V_{SUP(TR)}$	-0.3 to 27 -0.3 to 40 see Section 3.9, "Additional Test Information ISO7637-2"	V
L0...L5 - Pin Voltage Normal Operation with a series $R_{LX}$ resistor (DC) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	$V_{LXDC}$ $V_{LXTR}$	-27 to 40 see Section 3.9, "Additional Test Information ISO7637-2"	V
LIN Pin Voltage Normal Operation (DC) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	$V_{BUSDC}$ $V_{BUSTR}$	-33 to 40 see Section 3.9, "Additional Test Information ISO7637-2"	V
Supply Voltage at VDDX	$V_{DDX}$	-0.3 to 5.5	V
Supply Voltage at VDD <sup>(6)</sup>	$V_{DD}$	-0.3 to 2.75	V
VDD output current	$I_{VDD}$	Internally Limited	A
VDDX output current	$I_{VDDX}$	Internally Limited	A
TCLK Pin Voltage	$V_{TCLK}$	-0.3 to 10	V
RESET_A Pin Voltage	$V_{IN}$	-0.3 to $V_{DDX}+0.3$	V
Input / Output Pins PTB[0:2] Voltage	$V_{IN}$	-0.3 to $V_{DDX}+0.3$	V
HS1 and HS2 Pin Voltage (DC)	$V_{HS}$	-0.3 to $VS2+0.3$	V
LS1 and LS2 Pin Voltage (DC)	$V_{LS}$	-0.3 to 45	V
ISENSEH and ISENSEL Pin Voltage (DC)	$V_{ISENSE}$	-0.3 to 40	V
HSUP Pin Voltage (DC)	$V_{HSUP}$	-0.3 to $VS1+0.3$	V
VSENSE Pin Voltage (DC)	$V_{VSENSE}$	-27 to 40	V

Note:

- Caution: As this pin is adjacent to the VDDX pin, care should be taken to avoid a short between VDD and VDDX, for example, during the soldering process. A short-circuit between these pins might lead to permanent damage.

**Table 6. Maximum Electrical Ratings - MCU Die**

Ratings	Symbol	Value	Unit
5.0 V Supply Voltage	$V_{EDDX}$	-0.3 to 6.0	V
2.5 V Supply Voltage	$V_{EDD}$	-0.3 to 2.75	V
Digital I/O input voltage (PA0...PA7, PE0, PE1)	$V_{IN}$	-0.3 to 6.0	V
EXTAL, XTAL	$V_{ILV}$	-0.3 to 2.16	V
TEST input	$V_{TEST}$	-0.3 to 10.0	V
Instantaneous maximum current Single pin limit for all digital I/O pins	$I_D$	-25 to 25	mA
Instantaneous maximum current Single pin limit for EXTAL, XTAL	$I_{DL}$	-25 to 25	mA

**Table 7. Maximum Thermal Ratings**

Ratings	Symbol	Value	Unit
Storage Temperature	$T_{STG}$	-55 to 150	°C
Package Thermal Resistance - LQFP48-EP	$R_{\theta JA}$	max. 39	°C/W
Package Thermal Resistance - LQFP48	$R_{\theta JA}$	max. 62	°C/W
Peak Package Reflow Temperature During Reflow <sup>(7),(8)</sup>	$T_{PPRT}$	300	°C

## Notes

- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC34xxxD enter 34xxx), and review parametrics.

### 3.3 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

**Table 8. Operating Conditions**

Ratings	Symbol	Value	Unit
Analog Die Nominal Operating Voltage	$V_{SUP}$	5.5 to 18	V
Analog Die Functional Operating Voltage - Device is fully functional. All features are operating.	$V_{SUPOP}$	5.5 to 27	V
MCU I/O and supply voltage <sup>(9)</sup>	$V_{EDDX}$	4.5 to 5.5	V
MCU Digital logic supply voltage <sup>(9)</sup>	$V_{EDD}$	2.25 to 2.75	V
MCU External Oscillator	$f_{OSC}$	4.0 to 16	MHz
MCU Bus frequency	$f_{BUS}$	$f_{BUSMAX}$ <sup>(10)</sup>	MHz
Operating Ambient Temperature MM912x634xVxxx	$T_A$	-40 to 105	°C
Operating Junction Temperature - Analog Die	$T_{J\_A}$	-40 to 150	°C
Operating Junction Temperature - MCU Die	$T_{J\_M}$	-40 to 140	°C

## Note:

- During power up and power down sequence always  $V_{DD} < V_{DDX}$
- $f_{BUSMAX}$  frequency ratings differ by device and is specified in [Table 1](#)

### 3.4 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

#### 3.4.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted, the currents are measured in MCU special single chip mode and the CPU code is executed from RAM.

**Table 9. Supply Currents**

Ratings	Symbol	Min	Typ <sup>(11)</sup>	Max	Unit
Normal Mode analog die only, excluding external loads, LIN Recessive State ( $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ , $2.25\text{ V} \leq E_{\text{VDD}} \leq 2.75\text{ V}$ , $4.5\text{ V} \leq E_{\text{VDDX}} \leq 5.5\text{ V}$ , $-40\text{ }^\circ\text{C} \leq T_{\text{J}_A} \leq 150\text{ }^\circ\text{C}$ ).	$I_{\text{RUN}_A}$	-	5.0	8.0	mA
Normal Mode MCU die only ( $T_{\text{J}_M} = 140\text{ }^\circ\text{C}$ ; $V_{\text{DD}} = 2.75\text{ V}$ , $V_{\text{DDX}} = 5.5\text{ V}$ , $f_{\text{OSC}} = 4.0\text{ MHz}$ , $f_{\text{BUS}} = f_{\text{BUSMAX}}$ <sup>(15)(12)</sup> )	$I_{\text{RUN}_M}$	-	12.5	15	mA
Stop Mode internal analog die only, excluding external loads, LIN Recessive State, Lx enabled, measured at VS1+VS2 ( $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ , $2.25\text{ V} \leq E_{\text{VDD}} \leq 2.75\text{ V}$ , $4.5\text{ V} \leq E_{\text{VDDX}} \leq 5.5\text{ V}$ ) $-40\text{ }^\circ\text{C} \leq T_{\text{J}_A} \leq 125\text{ }^\circ\text{C}$ $125\text{ }^\circ\text{C} < T_{\text{J}_A} \leq 140\text{ }^\circ\text{C}$	$I_{\text{STOP}_A}$	- -	20 -	40 50	$\mu\text{A}$
Stop Mode MCU die only ( $V_{\text{DD}} = 2.75\text{ V}$ , $V_{\text{DDX}} = 5.5\text{ V}$ , $f_{\text{OSC}} = 4.0\text{ MHz}$ , $f_{\text{BUS}} = f_{\text{BUSMAX}}$ <sup>(15)</sup> ; MCU in STOP; RTI and COP off) <sup>(13)</sup> $T_{\text{J}_M} = 140\text{ }^\circ\text{C}$ $T_{\text{J}_M} = 105\text{ }^\circ\text{C}$ $T_{\text{J}_M} = 25\text{ }^\circ\text{C}$	$I_{\text{STOP}_M}$	- - -	0.135 0.035 0.010	0.400 0.200 0.030	mA
Stop Mode MCU die only ( $V_{\text{DD}} = 2.75\text{ V}$ , $V_{\text{DDX}} = 5.5\text{ V}$ , $f_{\text{OSC}} = 4.0\text{ MHz}$ , $f_{\text{BUS}} = f_{\text{BUSMAX}}$ <sup>(15)</sup> ; MCU in STOP; RTI and COP on) <sup>(13)</sup> $T_{\text{J}_M} = 140\text{ }^\circ\text{C}$ $T_{\text{J}_M} = 105\text{ }^\circ\text{C}$ $T_{\text{J}_M} = 25\text{ }^\circ\text{C}$	$I_{\text{STOP}_M}$	- - -	0.205 0.104 0.079	0.500 0.300 0.110	mA
Wait Mode MCU die only ( $T_{\text{J}_M} = 140\text{ }^\circ\text{C}$ ; $V_{\text{DD}} = 2.75\text{ V}$ , $V_{\text{DDX}} = 5.5\text{ V}$ , $f_{\text{OSC}} = 4.0\text{ MHz}$ , $f_{\text{BUS}} = f_{\text{BUSMAX}}$ <sup>(15)</sup> ; All modules except RTI disabled) <sup>(14)</sup>	$I_{\text{WAIT}_M}$	-	7.0	12	mA
Sleep Mode ( $V_{\text{DD}} = V_{\text{DDX}} = \text{OFF}$ ; $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ ; $-40\text{ }^\circ\text{C} \leq T_{\text{J}_A} \leq 150\text{ }^\circ\text{C}$ ; $3.0\text{ V} < L_X < 1.0\text{ V}$ ).	$I_{\text{SLEEP}}$	-	15	28	$\mu\text{A}$
Cyclic Sense Supply Current Adder (5.0 ms Cycle)	$I_{\text{CS}}$	-	15	20	$\mu\text{A}$

Note:

- Typical values noted reflect the approximate parameter mean at  $T_A = 25\text{ }^\circ\text{C}$
- $I_{\text{RUN}_M}$  denotes the sum of the currents flowing into VDD and VDDX.
- $I_{\text{STOP}_M}$  denotes the sum of the currents flowing into VDD and VDDX.
- $I_{\text{WAIT}_M}$  denotes the sum of the currents flowing into VDD and VDDX.
- $f_{\text{BUSMAX}}$  frequency ratings differ by device and is specified in [Table 1](#).

### 3.5 Static Electrical Characteristics

Static electrical characteristics noted under conditions  $5.5V \leq V_{SUP} \leq 18V$ ,  $-40^\circ C \leq T_A \leq 105^\circ C$ , unless otherwise noted. Typical values noted reflect the approximate parameter mean at  $T_A = 25^\circ C$  under nominal conditions unless otherwise noted.

#### 3.5.1 Static Electrical Characteristics Analog Die

**Table 10. Static Electrical Characteristics - Power Supply**

Ratings	Symbol	Min	Typ	Max	Unit
Power-On Reset (POR) Threshold (measured on VS1)	V <sub>POR</sub>	1.5	-	3.5	V
Low Voltage Warning (LVI) Threshold (measured on VS1, falling edge) Hysteresis (measured on VS1)	V <sub>LVI</sub> V <sub>LVI_H</sub>	5.55 -	6.0 1.0	6.6 -	V
High Voltage Warning (HVI) Threshold (measured on VS2, rising edge) Hysteresis (measured on VS2)	V <sub>HVI</sub> V <sub>HVI_H</sub>	18 -	19.25 1.0	20.5 -	V
Low Battery Warning (LBI) Threshold (measured on VSENSE, falling edge) Hysteresis (measured on VSENSE)	V <sub>LBI</sub> V <sub>LBI_H</sub>	5.55 -	6.0 1.0	6.6 -	V
J2602 Under-voltage threshold	V <sub>J2602UV</sub>	5.5	5.7	6.2	V
Low VDDX Voltage (LVRX) Threshold	V <sub>LVRX</sub>	2.7	3.0	3.3	V
Low VDD Voltage Reset (LVR) Threshold Normal Mode	V <sub>LVR</sub>	2.30	2.35	2.4	V
Low VDD Voltage Reset (LVR) Threshold Stop Mode <sup>(16)</sup>	V <sub>LVR_S</sub>	1.6	1.85	2.1	V
VDD Over-voltage Threshold (VROV)	V <sub>VDDOV</sub>	2.575	2.7875	3.0	V
VDDX Over-voltage Threshold (VROVX)	V <sub>VDDXOV</sub>	5.25	5.675	6.1	V

Note:

16. See MM912F634ER, MM912F634, Silicon Analog Mask (M91W) / Digital Mask (M33G) Errata

**Table 11. Static Electrical Characteristics - Resets**

Ratings	Symbol	Min	Typ	Max	Unit
Low-state Output Voltage I <sub>OUT</sub> = 2.0 mA	V <sub>OL</sub>	-	-	0.8	V
Pull-up Resistor	R <sub>RPU</sub>	25	-	50	kOhm
Low-state Input Voltage	V <sub>IL</sub>	-	-	0.3V <sub>DXX</sub>	V
High-state Input Voltage	V <sub>IH</sub>	0.7V <sub>DXX</sub>	-	-	V
Reset Release Voltage (VDDX)	V <sub>RSTRV</sub>	-	1.5	-	V
RESET_A pin Current Limitation		5.0	7.5	10	mA

**Table 12. Static Electrical Characteristics - Window Watchdog**

Ratings	Symbol	Min	Typ	Max	Unit
Watchdog Disable Voltage (fixed voltage)	V <sub>TST</sub>	7.0	-	10	V
Watchdog Enable Voltage (fixed voltage)	V <sub>TSTEN</sub>	-	-	5.5	V

**Table 13. Static Electrical Characteristics - Voltage Regulator 5V (VDDX)**

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I <sub>VDDX</sub> + I <sub>VDDXINTERNAL</sub> < 80 mA; 5.5 V < V <sub>SUP</sub> < 27 V <sup>(17)</sup>	V <sub>DXXRUN</sub>	4.75	5.00	5.25	V
Normal Mode Output Current Limitation (I <sub>VDDX</sub> )	I <sub>VDDXLIMRUN</sub>	80	130	200	mA

Table 13. Static Electrical Characteristics - Voltage Regulator 5V (VDDX) (continued)

Ratings	Symbol	Min	Typ	Max	Unit
Stop Mode Output Voltage ( $I_{VDDX} + I_{VDDXINTERNAL} < 500 \mu A$ for $T_J \geq 25^\circ C$ ; $I_{VDDX} + I_{VDDXINTERNAL} < 400 \mu A$ for $T_J < 25^\circ C$ ) (17)	$V_{DDXSTOP}$	-	5.0	5.5	V
Stop Mode Output Current Limitation ( $I_{VDDX}$ )	$I_{VDDXLIMITSTOP}$	-	-	20	mA
Line Regulation Normal Mode, $I_{VDDX} = 80$ mA Stop Mode, $I_{VDDX} = 500 \mu A$	$LR_{XRUN}$ $LR_{XSTOP}$	- -	20 -	25 200	mV
Load Regulation Normal Mode, $1.0$ mA $< I_{VDDX} < 80$ mA Normal Mode, $V_{SUP} = 3.6$ V, $1.0$ mA $< I_{VDDX} < 40$ mA Stop Mode, $100 \mu A < I_{VDDX} < 500 \mu A$	$LD_{XRUN}$ $LD_{XCRK}$ $LD_{XSTOP}$	- - -	15 - -	80 200 250	mV
External Capacitor	$C_{VDDX}$	1.0	-	10	$\mu F$
External Capacitor ESR	$C_{VDDX\_R}$	-	-	10	Ohm

Note:

17.  $I_{VDDXINTERNAL}$  includes internal consumption from both analog and MCU die.

Table 14. Static Electrical Characteristics - Voltage Regulator 2.5 V (VDD)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage $1.0$ mA $< I_{VDD} + I_{VDDINTERNAL} \leq 45$ mA; $5.5$ V $< V_{SUP} < 27$ V (18)	$V_{DDRUN}$	2,425	2.5	2,575	V
Normal Mode Output Current Limitation ( $I_{VDD}$ ) $T_J < 25^\circ C$ $T_J \geq 25^\circ C$	$I_{VDDLIMRUN}$	- -	80 80	120 143	mA
Stop Mode Output Voltage ( $I_{VDD} + I_{VDDINTERNAL} < 500 \mu A$ for $T_J \geq 25^\circ C$ ; $I_{VDD} + I_{VDDINTERNAL} < 400 \mu A$ for $T_J < 25^\circ C$ ) (18)	$V_{DDSTOP}$	2.25	2.5	2.75	V
Stop Mode Output Current Limitation ( $I_{VDD}$ )	$I_{VDDLIMSTOP}$	-	-	10	mA
Line Regulation Normal Mode, $I_{VDD} = 45$ mA Stop Mode, $I_{VDD} = 1.0$ mA	$LR_{RUN}$ $LR_{STOP}$	- -	10 -	12.5 200	mV
Load Regulation Normal Mode, $1.0$ mA $< I_{VDD} < 45$ mA Normal Mode, $V_{SUP} = 3.6$ V, $1.0$ mA $< I_{VDD} < 30$ mA Stop Mode, $100 \mu A < I_{VDD} < 500 \mu A$	$LD_{RUN}$ $LD_{CRK}$ $LD_{STOP}$	- - -	7.5 - -	40 40 200	mV
External Capacitor	$C_{VDD}$	1.0	-	10	$\mu F$
External Capacitor ESR	$C_{VDD\_R}$	-	-	10	Ohm

Note:

18.  $I_{VDDINTERNAL}$  includes internal consumption from both analog and MCU die.

Table 15. Static Electrical Characteristics - Hall Sensor Supply Output - HSUP

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation ( $3.7$ V $\leq V_{SUP} \leq 18$ V)	$I_{HSUP}$	40	70	90	mA
Output Drain-to-Source On resistance $T_J = 150^\circ C$ , $I_{LOAD} = 30$ mA; $5.5$ V $\leq V_{SUP} \leq 16$ V $T_J = 150^\circ C$ , $I_{LOAD} = 30$ mA; $3.7$ V $\leq V_{SUP} < 5.5$ V	$R_{DS(ON)}$	- -	- -	10 12	Ohm
Output Voltage: ( $18$ V $\leq V_{SUP} \leq 27$ V)	$V_{HSUPmax}$	16	17.5	18	V
Load Regulation ( $1.0$ mA $< I_{HSUP} < 30$ mA; $V_{SUP} > 18$ V)	$LD_{HSUP}$	-	-	500	mV



Table 15. Static Electrical Characteristics - Hall Sensor Supply Output - HSUP (continued)

Ratings	Symbol	Min	Typ	Max	Unit
Hall Supply Capacitor Range	$C_{HSUP}$	0.22	-	10	$\mu\text{F}$
External Capacitor ESR	$C_{HSUP\_R}$	-	-	10	Ohm

(continued)

Table 16. Static Electrical Characteristics - High Side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance $T_J = 25\text{ }^\circ\text{C}$ , $I_{LOAD} = 50\text{ mA}$ ; $V_{SUP} > 9.0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ , $I_{LOAD} = 50\text{ mA}$ ; $V_{SUP} > 9.0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ , $I_{LOAD} = 30\text{ mA}$ ; $5.5\text{ V} < V_{SUP} < 9.0\text{ V}$	$R_{DS(ON)}$	-	-	7.0 10 14	Ohm
Output Current Limitation ( $0\text{ V} < V_{OUT} < V_{SUP} - 2.0\text{ V}$ )	$I_{LIMHSX}$	60	110	250	mA
Open Load Current Detection	$I_{OLHSX}$	-	5.0	7.5	mA
Leakage Current ( $-0.2\text{ V} < V_{HSX} < V_{S2} + 0.2\text{ V}$ )	$I_{LEAK}$	-	-	10	$\mu\text{A}$
Current Limitation Flag Threshold ( $5.5\text{ V} < V_{SUP} < 27\text{ V}$ )	$V_{THSC}$	$V_{SUP} - 2$	-	-	V

Table 17. Static Electrical Characteristics - Low Side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance $T_J = 25\text{ }^\circ\text{C}$ , $I_{LOAD} = 150\text{ mA}$ , $V_{SUP} > 9.0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ , $I_{LOAD} = 150\text{ mA}$ , $V_{SUP} > 9.0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ , $I_{LOAD} = 120\text{ mA}$ , $5.5\text{ V} < V_{SUP} < 9.0\text{ V}$	$R_{DS(ON)}$	-	-	2.5 4.5 10	Ohm
Output Current Limitation ( $2.0\text{ V} < V_{OUT} < V_{SUP}$ )	$I_{LIMLSX}$	180	275	380	mA
Open Load Current Detection	$I_{OLLSX}$	-	8.0	12	mA
Leakage Current ( $-0.2\text{ V} < V_{OUT} < VS1$ )	$I_{LEAK}$	-	-	10	$\mu\text{A}$
Active Output Energy Clamp ( $I_{OUT} = 150\text{ mA}$ )	$V_{CLAMP}$	40	-	45	V
Coil Series Resistance ( $I_{OUT} = 150\text{ mA}$ )	$R_{COIL}$	120	-	-	Ohm
Coil Inductance ( $I_{OUT} = 150\text{ mA}$ )	$R_{COIL}$	-	-	400	mH
Current Limitation Flag Threshold ( $5.5\text{ V} < V_{SUP} < 27\text{ V}$ )	$V_{THSC}$	2.0	-	-	V

Table 18. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. $V_{BUS} = 18\text{ V}$	$I_{BUSLIM}$	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; $V_{BUS} = 0\text{ V}$ ; $V_{BAT} = 12\text{ V}$	$IBUS\_PAS\_DOM$	-1.0	-	-	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; $8.0\text{ V} < V_{BAT} < 18\text{ V}$ ; $8.0\text{ V} < V_{BUS} < 18\text{ V}$ ; $V_{BUS} \geq V_{BAT}$	$IBUS\_PAS\_REC$	-	-	20	$\mu\text{A}$
Input Leakage Current; GND Disconnected; $GNDDEVICE = VSUP$ ; $0 < V_{BUS} < 18\text{ V}$ ; $V_{BAT} = 12\text{ V}$	$IBUS\_NO\_GND$	-1.0	-	1.0	mA
Input Leakage Current; $V_{BAT}$ disconnected; $VSUP\_DEVICE = GND$ ; $0 < V_{BUS} < 18\text{ V}$	$IBUS\_NO\_BAT$	-	-	100	$\mu\text{A}$
Receiver Input Voltage; Receiver Dominant State	$V_{BUSDOM}$	-	-	0.4	$V_{SUP}$
Receiver Input Voltage; Receiver Recessive State	$V_{BUSREC}$	0.6	-	-	$V_{SUP}$
Receiver Threshold Center $(V_{TH\_DOM} + V_{TH\_REC})/2$	$V_{BUS\_CNT}$	0.475	0.5	0.525	$V_{SUP}$
Receiver Threshold Hysteresis $(V_{TH\_REC} - V_{TH\_DOM})$	$V_{BUS\_HYS}$	-	-	0.175	$V_{SUP}$
Voltage Drop at the serial Diode	$D_{SER\_INT}$	0.4	0.7	1.0	V

Table 18. Static Electrical Characteristics - LIN Physical Layer Interface - LIN (continued)

Ratings	Symbol	Min	Typ	Max	Unit
LIN Pull-up Resistor	$R_{SLAVE}$	20	30	60	kOhm
Bus Wake-up Threshold from Stop or Sleep <sup>(19)</sup>	$V_{WUP}$	4.5	5.0	6.0	V
Bus Dominant Voltage	$V_{DOM}$	-	-	2.5	V

Note:

19. Considering drop from VBAT to LIN, at very low VBAT level, the internal logic will detect a dominant as the threshold will not decrease with VSUP.

Table 19. Static Electrical Characteristics - High Voltage Inputs - Lx

Ratings	Symbol	Min	Typ	Max	Unit
Low Detection Threshold $7.0\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$ $5.5\text{ V} \leq V_{\text{SUP}} \leq 7\text{ V}$	$V_{\text{THL}}$	2.2 1.5	2.5 2.5	3.4 4.0	V
High Detection Threshold $7.0\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$ $5.5\text{ V} \leq V_{\text{SUP}} \leq 7\text{ V}$	$V_{\text{THH}}$	2.6 2.0	3.0 3.0	3.7 4.5	V
Hysteresis $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$	$V_{\text{HYS}}$	0.25	0.45	1.0	V
Input Current Lx ( $-0.2\text{ V} < V_{\text{IN}} < V_{\text{S1}}$ )	$I_{\text{IN}}$	-10	-	10	$\mu\text{A}$
Analog Input Impedance Lx	$R_{\text{LxIN}}$	-	-	1.2	MOhm
Lx Series Resistor	$R_{\text{Lx}}$	9.5	10	10.5	kOhm
Lx Capacitor (optional) <sup>(20)</sup>	$C_{\text{Lx}}$	-	100	-	nF
Analog Input Divider Ratio ( $\text{RATIO}_{\text{Lx}} = V_{\text{Lx}} / V_{\text{ADOUT0}}$ ) LXDS (Lx Divider Select) = 0 LXDS (Lx Divider Select) = 1	$\text{RATIO}_{\text{Lx}}$	- -	2.0 7.2	- -	
Analog Input Divider Ratio Accuracy	$\text{RATIO}_{\text{Lx}}$	-5.5	-	5.5	%
Analog Inputs Channel Ratio - Mismatch LXDS (Lx Divider Select) = 0 LXDS (Lx Divider Select) = 1	$\text{LxMATCH}$	- -	- -	5.0 5.0	%

Note:

20. The ESD behavior specified in Section 3.8, "ESD Protection and Latch-up Immunity" are guaranteed without the optional capacitor.

Table 20. Static Electrical Characteristics - General Purpose I/O - PTB[0...2]

Ratings	Symbol	Min	Typ	Max	Unit
Input high voltage	$V_{\text{IH}}$	$0.7V_{\text{DDX}}$	-	$V_{\text{DDX}}+0.3$	V
Input low voltage	$V_{\text{IL}}$	$V_{\text{SS}}-0.3$	-	$0.35V_{\text{DDX}}$	V
Input hysteresis	$V_{\text{HYS}}$	-	140	-	mV
Input high voltage ( $V_{\text{S1}} = 3.7\text{ V}$ )	$V_{\text{IH}3.7}$	2.1	-	$V_{\text{DDX}}+0.3$	V
Input low voltage ( $V_{\text{S1}} = 3.7\text{ V}$ )	$V_{\text{IL}3.7}$	$V_{\text{SS}}-0.3$	-	1.4	V
Input hysteresis ( $V_{\text{S1}} = 3.7\text{ V}$ )	$V_{\text{HYS}3.7}$	100	200	300	mV
Input leakage current (pins in high-impedance input mode) ( $V_{\text{IN}} = V_{\text{DDX}}$ or $V_{\text{SSX}}$ )	$I_{\text{IN}}$	-1.0	-	1.0	$\mu\text{A}$
Output high voltage (pins in output mode) Full drive $I_{\text{OH}} = -10\text{ mA}$	$V_{\text{OH}}$	$V_{\text{DDX}}-0.8$	-	-	V
Output low voltage (pins in output mode) Full drive $I_{\text{OL}} = +10\text{ mA}$	$V_{\text{OL}}$	-	-	0.8	V
Internal pull-up resistance ( $V_{\text{IH min}} > \text{Input voltage} > V_{\text{IL max}}$ )	$R_{\text{PUL}}$	26.25	37.5	48.75	kOhm
Input capacitance	$C_{\text{IN}}$	-	6.0	-	pF
Clamp Voltage when selected as analog input	$V_{\text{CL\_AIN}}$	VDD	-	-	V
Analog Input impedance = 10 kOhm max, Capacitance = 12 pF	$R_{\text{AIN}}$	-	-	10	kOhm
Analog Input Capacitance = 12 pF	$C_{\text{AIN}}$	-	12	-	pF
Maximum current all PTB combined (VDDX capability)	$I_{\text{BMAX}}$	-15	-	15	mA
Output Drive strength at 10 MHz	$C_{\text{OUT}}$	-	-	100	pF

Table 21. Static Electrical Characteristics - Analog Digital Converter - ADC<sup>(21)</sup>

Ratings	Symbol	Min	Typ	Max	Unit
ADC2p5 Reference Voltage 5.5 V < V <sub>SUP</sub> < 27 V	V <sub>ADC2p5RUN</sub>	2.45	2.5	2.55	V
ADC2p5 Reference Stop Mode Output Voltage	V <sub>ADC2p5STOP</sub>	-	-	100	mV
Line Regulation, Normal Mode	LR <sub>RUNA</sub>	-	10	12.5	mV
External Capacitor	C <sub>ADC2p5</sub>	0.1	-	1.0	μF
External Capacitor ESR	C <sub>VDD_R</sub>	-	-	10	Ohm
Scale Factor Error	E <sub>SCALE</sub>	-1	-	1	LSB
Differential Linearity Error	E <sub>DNL</sub>	-1.5	-	1.5	LSB
Integral Linearity Error	E <sub>INL</sub>	-1.5	-	1.5	LSB
Zero Offset Error	E <sub>OFF</sub>	-2.0	-	2.0	LSB
Quantization Error	E <sub>Q</sub>	-0.5	-	0.5	LSB
Total Error with offset compensation	TE	-5.0	-	5.0	LSB
Bandgap measurement Channel (CH14) Valid Result Range (including ±7.0% bg1p25 sleep accuracy + high-impedance measurement error of ±5.0% at f <sub>ADC</sub> ) <sup>(22)</sup>	AD <sub>CH14</sub>	1.1	1.25	1.4	V

Note:

21. No external load allowed on the ADC2p5 pin.
22. Reduced ADC frequency will lower measurement error.

Table 22. Static Electrical Characteristics - Current Sense Module - ISENSE

Ratings	Symbol	Min	Typ	Max	Unit
Gain	G	-	-	-	-
CSGS (Current Sense Gain Select) = 000		-	7.0	-	
CSGS (Current Sense Gain Select) = 001		-	9.0	-	
CSGS (Current Sense Gain Select) = 010		-	10	-	
CSGS (Current Sense Gain Select) = 011		-	12	-	
CSGS (Current Sense Gain Select) = 100		-	14	-	
CSGS (Current Sense Gain Select) = 101		-	18	-	
CSGS (Current Sense Gain Select) = 110		-	24	-	
CSGS (Current Sense Gain Select) = 111		-	36	-	
Gain Accuracy		-3.0	-	3.0	%
Offset		-1.5	-	1.5	%
Resolution <sup>(23)</sup>	RES	-	51	-	mA/LSB
ISENSEH, ISENSEL Input Common Mode Voltage Range	V <sub>IN</sub>	-0.2	-	3.0	V
Current Sense Module - Normal Mode Current Consumption Adder (CSE = 1)	I <sub>ISENSE</sub>	-	600	-	μA

Note:

23. RES = 2.44 mV/(GAIN\*R<sub>SHUNT</sub>)

Table 23. Static Electrical Characteristics - Temperature Sensor - TSENSE

Ratings	Symbol	Min	Typ	Max	Unit
Internal Chip Temperature Sense Gain <sup>(24)</sup>	$TS_G$	-	9.17	-	mV/k
Internal Chip Temperature Sense Error at the end of conversion <sup>(24)</sup>	$TS_{Err}$	-5.0	-	5.0	°C
Temperature represented by a $ADC_{IN}$ Voltage of 0.150 V <sup>(24)</sup>	$T_{0.15V}$	-55	-50	-45	°C
Temperature represented by a $ADC_{IN}$ Voltage of 1.984 V <sup>(24)</sup>	$T_{1.984V}$	145	150	155	°C

Note:

24. Guaranteed by design and characterization.

Table 24. Static Electrical Characteristics - Supply Voltage Sense - VSENSE and VS1SENSE

Ratings	Symbol	Min	Typ	Max	Unit
VSENSE Input Divider Ratio ( $RATIO_{VSENSE} = V_{VSENSE} / ADC_{IN}$ ) 5.5 V < $V_{SUP}$ < 27 V	$RATIO_{VSENSE}$		10.8		
VSENSE error - whole path (VSENSE pin to Digital value)	$ER_{VSENSE}$	-	-	5.0	%
VS1SENSE Input Divider Ratio ( $RATIO_{VS1SENSE} = V_{VS1SENSE} / ADC_{IN}$ ) 5.5 V < $V_{SUP}$ < 27 V	$RATIO_{VS1SENSE}$		10.8		
VS1SENSE error - whole path (VS1 pin to Digital value)	$ER_{VS1SENSE}$	-	-	5.0	%
VSENSE Series Resistor	$R_{VSENSE}$	9.5	10	10.5	kOhm
VSENSE Capacitor (optional) <sup>(25)</sup>	$C_{VSENSE}$	-	100	-	nF

Note:

25. The ESD behavior specified in Section 3.8, "ESD Protection and Latch-up Immunity" is guaranteed without the optional capacitor.

### 3.5.2 Static Electrical Characteristics MCU Die

#### 3.5.2.1 I/O Characteristics

This section describes the characteristics of all I/O pins except EXTAL, XTAL, TEST and supply pins.

**Table 25. 5.0 V I/O Characteristics for PTA, RESET and BKGD Pins**

Ratings	Symbol	Min	Typ	Max	Unit
Input high voltage	$V_{IH}$	$0.65 \cdot V_{DD}$	-	-	V
Input high voltage	$V_{IH}$	-	-	$V_{DD} + 0.3$	V
Input low voltage	$V_{IL}$	-	-	$0.35 \cdot V_{DD}$	V
Input low voltage	$V_{IL}$	$V_{SS} - 0.3$	-	-	V
Input hysteresis	$V_{HYS}$	-	250	-	mV
Input leakage current (pins in high-impedance input mode) $V_{in} = V_{DDX}$ or $V_{SSX}$	$I_{IN}$	-1.0	-	1.0	$\mu$ A
Output high voltage (pins in output mode) Partial Drive $I_{OH} = -2.0$ mA	$V_{OH}$	$V_{DD} - 0.8$	-	-	V
Output high voltage (pins in output mode) Full Drive $I_{OH} = -10$ mA	$V_{OH}$	$V_{DD} - 0.8$	-	-	V
Output low voltage (pins in output mode) Partial drive $I_{OL} = +2.0$ mA	$V_{OL}$	-	-	0.8	V
Output low voltage (pins in output mode) Full Drive $I_{OL} = +10$ mA	$V_{OL}$	-	-	0.8	V
Internal pull-up resistance ( $V_{IHmin} > \text{input voltage} > V_{ILmax}$ )	$R_{PUL}$	25	-	50	k $\Omega$
Internal pull-down resistance ( $V_{IHmin} > \text{input voltage} > V_{ILmax}$ )	$R_{PDH}$	25	-	50	k $\Omega$
Input capacitance	$C_{in}$	-	6.0	-	pF
Injection current <sup>(26)</sup>					mA
Single pin limit	$I_{ICS}$	-2.5	-	2.5	
Total device Limit, sum of all injected currents	$I_{ICP}$	-25	-	25	

Note:

26. Refer to Section 3.8, "ESD Protection and Latch-up Immunity" for more details.

### 3.6 Dynamic Electrical Characteristics

Dynamic electrical characteristics noted under conditions  $5.5V \leq V_{SUP} \leq 18V$ ,  $-40^\circ C \leq T_A \leq 105^\circ C$ , unless otherwise noted. Typical values noted reflect the approximate parameter mean at  $T_A = 25^\circ C$  under nominal conditions unless otherwise noted.

#### 3.6.1 Dynamic Electrical Characteristics Analog Die

**Table 26. Dynamic Electrical Characteristics - Modes of Operation**

Ratings	Symbol	Min	Typ	Max	Unit
VDD Short Timeout	$t_{VTO}$	110	150	205	ms
Analog Base Clock	$f_{BASE}$	-	100	-	kHz
Reset Delay	$t_{RST}$	140	200	280	$\mu s$

**Table 27. Dynamic Electrical Characteristics - Power Supply**

Ratings	Symbol	Min	Typ	Max	Unit
Glitch Filter Low Battery Warning (LBI) <sup>(27)</sup>	$t_{LB}$	-	2.0	-	$\mu s$
Glitch Filter Low Voltage Warning (LVI) <sup>(27)</sup>	$t_{LV}$	-	2.0	-	$\mu s$
Glitch Filter High Voltage Warning (HVI) <sup>(27)</sup>	$t_{HV}$	-	2.0	-	$\mu s$

Note:

27. Guaranteed by design.

**Table 28. Dynamic Electrical Characteristics - Die to Die Interface - D2D**

Ratings	Symbol	Min	Typ	Max	Unit
Operating Frequency (D2DCLK, D2D[0:3])	$f_{D2D}$	$f_{ADC(MIN)}$	-	$f_{BUSMAX}$ <sup>(28)</sup>	MHz

Note:

28.  $f_{BUSMAX}$  frequency ratings differ by device and is specified in [Table 1](#)

**Table 29. Dynamic Electrical Characteristics - Resets**

Ratings	Symbol	Min	Typ	Max	Unit
Reset Deglitch Filter Time	$t_{RSTDF}$	1.2	2.0	3.0	$\mu s$
Reset Low Level Duration	$t_{RSTLOW}$	140	200	280	$\mu s$

**Table 30. Dynamic Electrical Characteristics - Wake-up / Cyclic Sense**

Ratings	Symbol	Min	Typ	Max	Unit
Lx Wake-up Filter Time	$t_{WUF}$	-	20		$\mu s$
Cyclic Sense / Forced Wake-up Timing Accuracy - not trimmed	$CS_{AC}$	-35	-	35	%
Cyclic Sense / Forced Wake-up Timing Accuracy - trimmed <sup>(29)</sup>	$CS_{ACT}$	-5.0	-	5.0	%
Time between HSx on and Lx sense during cyclic sense	$t_S$	same as $t_{HSON} / t_{HSOFT}$			-
HSx ON duration during Cyclic Sense	$t_{HSON}$	140	200	280	$\mu s$
HSx ON duration during Cyclic Sense - trimmed <sup>(29)</sup>	$t_{HSOFT}$	180	200	220	$\mu s$

Note:

29. Trimming parameters are not available in Sleep mode.

Table 31. Dynamic Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Initial Non-window Watchdog Timeout	$t_{IWDTO}$	110	150	190	ms
Watchdog Timeout Accuracy - not trimmed	$WD_{AC}$	-35	-	35	%
Watchdog Timeout Accuracy - trimmed	$WD_{ACT}$	-5.0	-	5.0	%

Table 32. Dynamic Electrical Characteristics - High Side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
High Side Operating Frequency <sup>(30)</sup> Load Condition: $C_{LOAD} \leq 2.2$ nF; $R_{LOAD} \geq 500$ $\Omega$	$f_{HS}$	-	-	50	kHz

Note:

30. Guaranteed by design.

Table 33. Dynamic Electrical Characteristics - Low Side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Low Side Operating Frequency	$f_{LS}$	-	-	10	kHz

Table 34. Dynamic Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Bus Wake-up Deglitcher (Sleep and Stop Mode)	$t_{PROPWL}$	60	80	100	$\mu$ s
Fast Bit Rate (Programming Mode)	$BR_{FAST}$	-	-	100	kBit/s
Propagation Delay of Receiver, $t_{REC\_PD} = \text{MAX}(t_{REC\_PDR}, t_{REC\_PDF})^{(31)}$	$t_{REC\_PD}$	-	-	6.0	$\mu$ s
Symmetry of Receiver Propagation Delay, $t_{REC\_PDF} - t_{REC\_PDR}$	$t_{REC\_SYM}$	-2.0	-	2.0	$\mu$ s
LIN Driver - 20.0 kBit/s; Bus load conditions ( $C_{BUS}$ ; $R_{BUS}$ ): 1.0 nF; 1.0 k $\Omega$ / 6.8 nF; 660 $\Omega$ / 10 nF; 500 $\Omega$ . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 6.					
Duty Cycle 1: $TH_{REC(MAX)} = 0.744 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ $7.0 \text{ V} \leq V_{SUP} \leq 18 \text{ V}$ ; $t_{BIT} = 50$ $\mu$ s; $D1 = t_{BUS\_REC(MIN)} / (2 \times t_{BIT})$	D1	0.396	-	-	
Duty Cycle 2: $TH_{REC(MIN)} = 0.422 \times V_{SUP}$ $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$ $7.6 \text{ V} \leq V_{SUP} \leq 18 \text{ V}$ ; $t_{BIT} = 50$ $\mu$ s $D2 = t_{BUS\_REC(MAX)} / (2 \times t_{BIT})$	D2	-	-	0.581	
LIN Driver - 10.0 kBit/s; Bus load conditions ( $C_{BUS}$ ; $R_{BUS}$ ): 1.0 nF; 1.0 k $\Omega$ / 6.8 nF; 660 $\Omega$ / 10 nF; 500 $\Omega$ . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 7.					
Duty Cycle 3: $TH_{REC(MAX)} = 0.778 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$ $7.0 \text{ V} \leq V_{SUP} \leq 18 \text{ V}$ ; $t_{BIT} = 96$ $\mu$ s $D3 = t_{BUS\_REC(MIN)} / (2 \times t_{BIT})$	D3	0.417	-	-	
Duty Cycle 4: $TH_{REC(MIN)} = 0.389 \times V_{SUP}$ $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$ $7.6 \text{ V} \leq V_{SUP} \leq 18 \text{ V}$ ; $t_{BIT} = 96$ $\mu$ s $D4 = t_{BUS\_REC(MAX)} / (2 \times t_{BIT})$	D4	-	-	0.590	

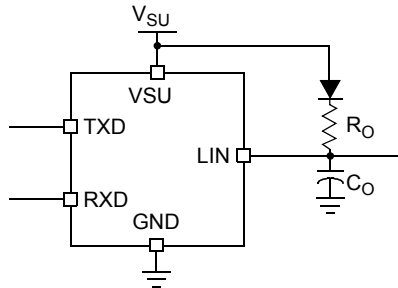


Table 34. Dynamic Electrical Characteristics - LIN Physical Layer Interface - LIN (continued)

Ratings	Symbol	Min	Typ	Max	Unit
Transmitter Symmetry $t_{TRAN\_SYM} < \text{MAX}(t_{TRAN\_SYM60\%}, t_{TRAN\_SYM40\%})$ $\text{tran\_sym60\%} = t_{\text{tran\_pdf60\%}} - t_{\text{tran\_pdr60\%}}$ $\text{tran\_sym40\%} = t_{\text{tran\_pdf40\%}} - t_{\text{tran\_pdr40\%}}$	$t_{TRAN\_SYM}$	-7.25	0	7.25	$\mu\text{s}$

Note:

- 31.  $V_{SUP}$  from 7.0 to 18 V, bus load  $R_{BUS}$  and  $C_{BUS}$  1.0 nF / 1.0 k $\Omega$ , 6.8 nF / 660  $\Omega$ , 10 nF / 500  $\Omega$ . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 8.
- 32. LIN Transmitter Timing, ( $V_{SUP}$  from 7.0 to 18 V) - See Figure 9



Note:  $R_n$  and  $C_n$ : 1.0k $\Omega$ /1.0nF, 660 $\Omega$ /6.8

Figure 5. Test Circuit for Timing Measurements

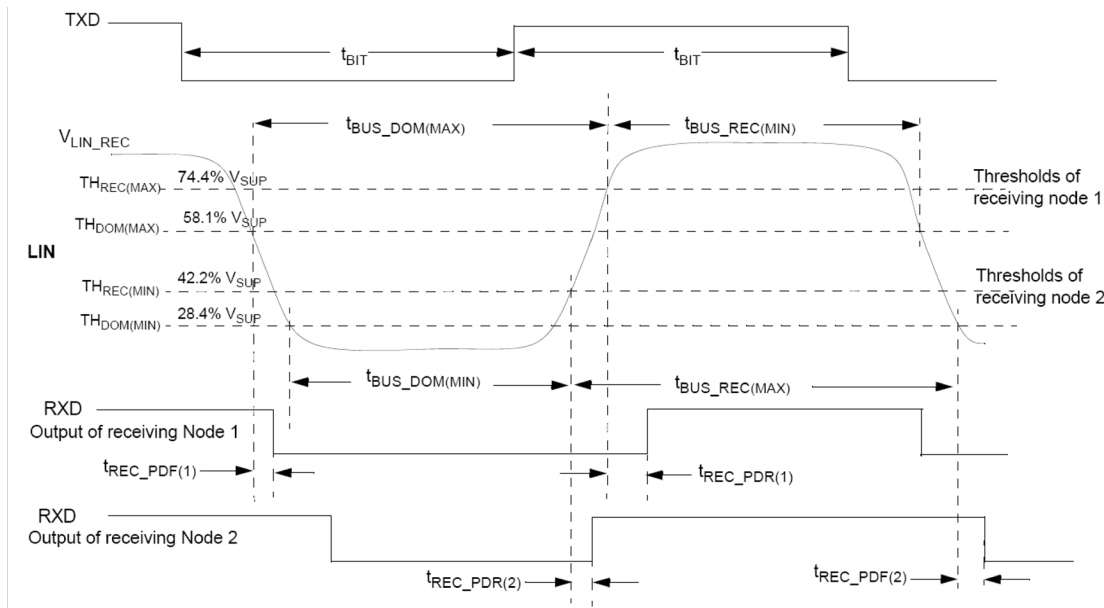


Figure 6. LIN Timing Measurements for Normal Baud Rate

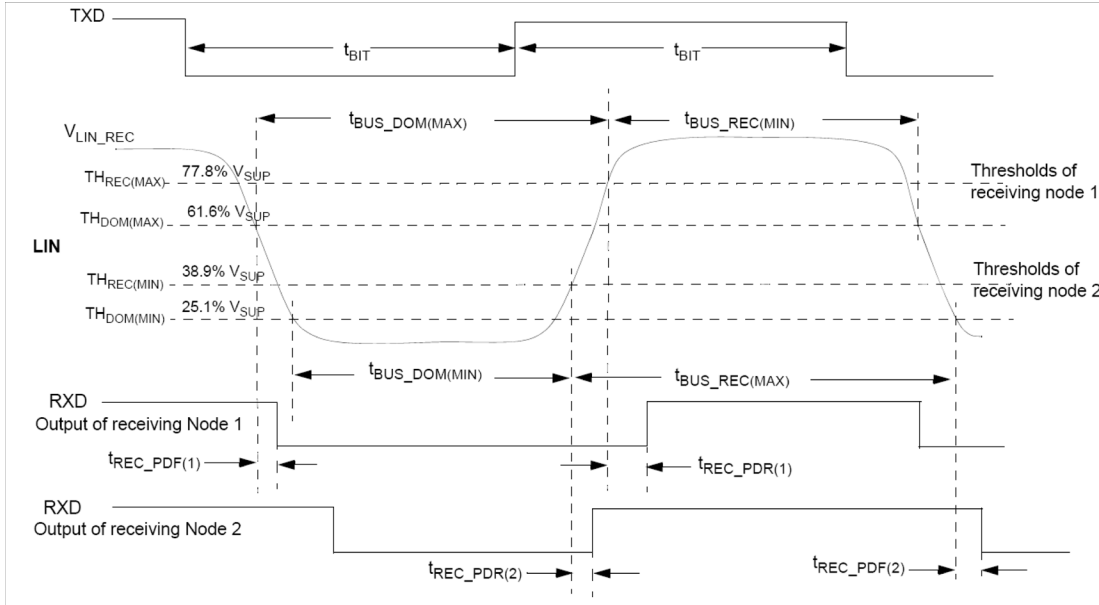


Figure 7. LIN Timing Measurements for Slow Baud Rate

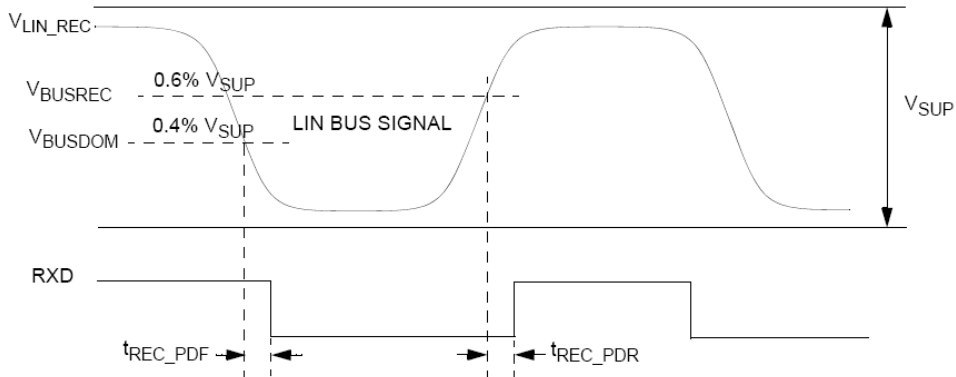


Figure 8. LIN Receiver Timing

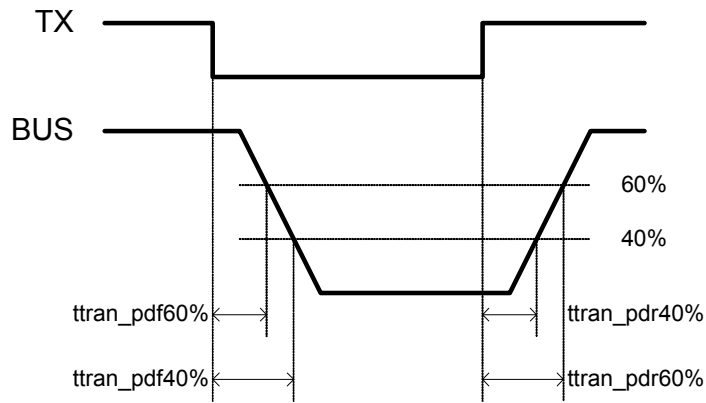


Figure 9. LIN Transmitter Timing