Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Integrated S12 Based Relay Driver with LIN

The MM912G634 (48 kB) and MM912H634 (64 kB) are integrated single package solutions that integrate an HCS12 microcontroller with a SMARTMOS analog control IC. The Die to Die Interface (D2D) controlled analog die combines system base chip and application specific functions, including a LIN transceiver.

MM912_634

48-PIN LQFP, 7.0 mm x 7.0 mm
AE SUFFIX: Exposed Pad Option
AP SUFFIX: Non Exposed Pad Option

ORDERING INFORMATION

See Page 2.

Features

- 16-Bit S12 CPU, 64/48 kByte P-FLASH,
- 6.0 kByte RAM; 4/2 kByte D-FLASH
- Background debug (BDM) & debug module (DBG)
- Die to Die bus interface for transparent memory mapping
- On-chip oscillator & two independent watchdogs
- LIN 2.1 Physical Layer Interface with integrated SCI
- 10 digital MCU GPIOs shared with SPI (PA7…0, PE1…0)
- 10-Bit, 15 Channel - Analog to Digital Converter (ADC)
- 16-Bit, 4 Channel - Timer Module (TIM16B4C)
- 8-Bit, 2 Channel - Pulse width modulation module (PWM)
- Six high voltage / Wake-up inputs (L5…0)
- Three low voltage GPIOs (PB2…0)
- Low power modes with cyclic sense & forced wake-up
- Current sense module with selectable gain
- Reverse battery protected voltage sense module
- Two protected low side outputs to drive inductive loads
- Two protected high side outputs
- Chip temperature sensor
- Hall sensor supply & integrated voltage regulator(s)

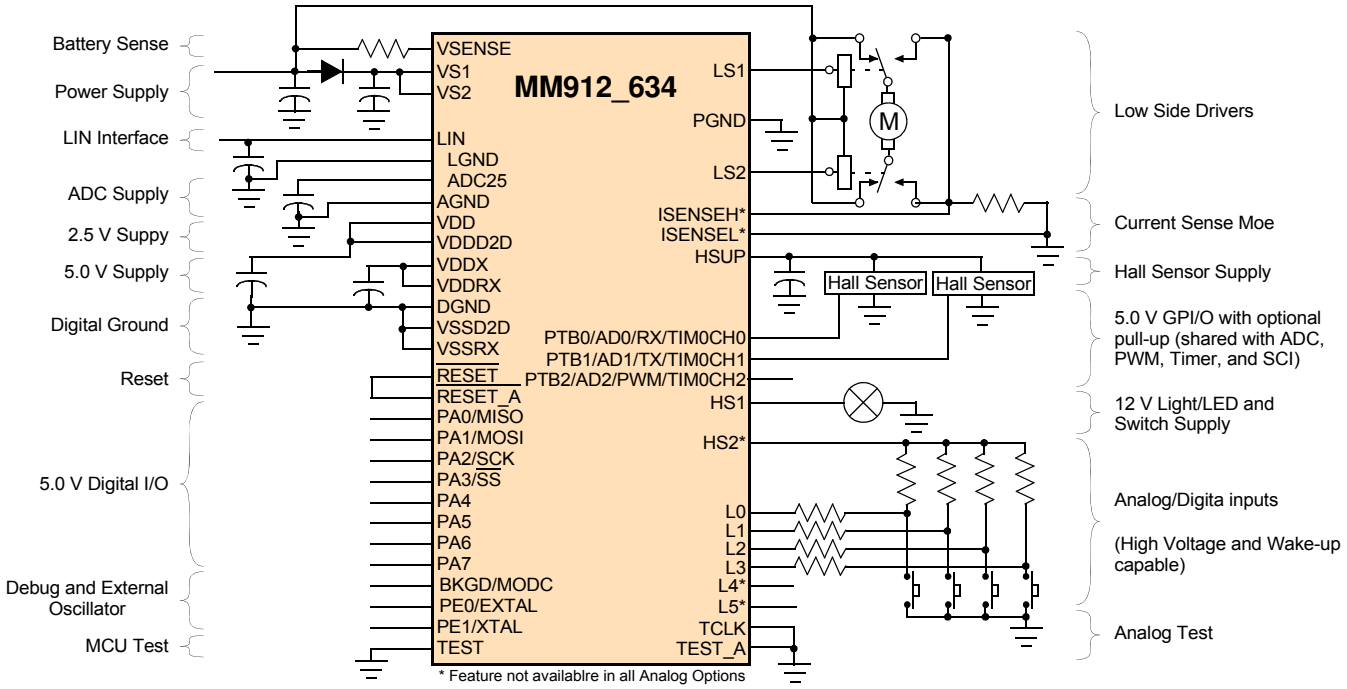

Figure 1. Simplified Application Diagram

This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

1 Ordering Information

Table 1. ORDERING INFORMATION

Device (Add an R2 suffix for Tape and Reel orders)	Temperature Range (T_A)	Package	Max. Bus Frequency in MHz (f_{BUSMAX})	Flash (kB)	Data Flash (kB)	RAM (kB)	Analog Option[1]	Stop Mode Wake-up
MM912G634CM1AE	-40°C to 125°C	LQFP48-EP	20	48[2]	2[3]	2[4]	A1	[5]
MM912G634DM1AE								Enhanced
MM912G634CV1AE	-40°C to 105°C	LQFP48-EP	20	48[2]	2[3]	2[4]	A1	[5]
MM912G634DV1AE								Enhanced
MM912G634CV2AP	-40°C to 105°C	LQFP48	16	48[2]	2[3]	2[4]	A2	[5]
MM912G634DV2AP								Enhanced
MM912H634CM1AE	-40°C to 125°C	LQFP48-EP	20	64	4	6	A1	[5]
MM912H634DM1AE								Enhanced
MM912H634CV1AE	-40°C to 105°C	LQFP48-EP	20	64	4	6	A1	[5]
MM912H634DV1AE								Enhanced

Note:
1. See Table 2.
2. The 48 kB Flash option (MM912**G**634) using the same S12I64 MCU with the tested FLASHSIZE reduced to 48 kB. This will limit the usable Flash area to the first 48 kB (0x3_4000-0x3_FFFF).
3. The 48 kB Flash option (MM912**G**634) using the same S12I64 MCU with the tested Data - FLASHSIZE reduced to 2.0 kB. This will limit the usable Data Flash area to the first 2.0 kB (0x0_4400-0x0_4BFF).
4. The 48 kB Flash option (MM912**G**634) using the same S12I64 MCU with the tested RAMSIZE reduced to 2.0 kB. This will limit the usable RAM area to the first 2.0 kB (0x0_2800-0x0_2FFF).
5. Refer to MM912_634, Silicon Analog Mask (M91W) / Digital Mask (N53A) Errata

Table 2. Analog Options[6]

Feature	A1	A2
Battery Sense Module	YES	YES
Current Sense Module	YES	NO
2nd High Side Output (HS2)	YES	YES
Wake-up Inputs (Lx)	L0…L5	L0…L3
Hall Supply Output (HSUP)	YES	YES
LIN Module	YES	YES

Note:
6. This table only highlights the analog die differences between the derivatives. Features highlighted as “NO” or the Lx Inputs not mentioned are not available in the specific option and not bonded out and/or not tested. See Section 5.3.3, “Analog Die Options" for detailed information.

2 Part Identification

This section provides an explanation of the part numbers and their alpha numeric breakdown.

2.1 Description

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

2.2 Format and Examples

Part numbers for a given device have the following format, followed by a device example:

Table 3 - Part Numbering - Analog EMBEDDED MCU + POWER:

MM 9 cc f xxx r v PPP RR - MM912G634CM1AE

2.3 Fields

These tables list the possible values for each field in the part number (not all combinations are valid).

Table 3. Part Numbering - Analog EMBEDDED MCU + POWER

FIELD	DESCRIPTION	VALUES
MM	Product Category	• MM- Qualified Standard • SM- Custom Device • PM- Prototype Device
9	Memory Type	• 9 = Flash, OTP • Blank = ROM
cc	Micro Core	• 08 = HC08 • 12 = HC12
f	Memory Size	• A 1 k • B 2 k • C 4 k • D 8 k • E 16 k • F 32 k • G 48 k • H 64 k • I 96 k • J 128 k
xxx	Analog Core/Target	• Assigned by Marketing
r	Revision	• (default A)
t	Temperature Range	• I = 0 °C to 85 °C • C = -40 °C to 85 °C • V = -40 °C to 105 °C • M = -40 °C to 125 °C
v	Variation	• (default blank)
PPP	Package Designator	• Assigned by Packaging
RR	Tape and Reel Indicator	

Table of Contents

1 Ordering Information 2
2 Part Identification 2
2.1 Description 2
2.2 Format and Examples 2
2.3 Fields 3
3 Pin Assignment 7
3.1 MM912_634 Pin Description 8
3.2 MCU Die Signal Properties 11
4 Electrical Characteristics 13
4.1 General 13
4.2 Absolute Maximum Ratings 13
4.3 Operating Conditions 15
4.4 Supply Currents 16
4.5 Static Electrical Characteristics 17
4.6 Dynamic Electrical Characteristics 24
4.7 Thermal Protection Characteristics 39
4.8 ESD Protection and Latch-up Immunity 39
4.9 Additional Test Information ISO7637-2 40
5 Functional Description and Application Information 41
5.1 Introduction 41
5.2 Device Register Maps 41
5.3 MM912_634 - Analog Die Overview 55
5.4 Modes of Operation 58
5.5 Power Supply 61
5.6 Die to Die Interface - Target 65
5.7 Interrupts 66
5.8 Resets 70
5.9 Wake-up / Cyclic Sense 72
5.10 Window Watchdog 77
5.11 Hall Sensor Supply Output - HSUP 79
5.12 High Side Drivers - HS 80
5.13 Low Side Drivers - LSx 83
5.14 PWM Control Module (PWM8B2C) 87
5.15 LIN Physical Layer Interface - LIN 102
5.16 Serial Communication Interface (S08SCIV4) 104
5.17 High Voltage Inputs - Lx 118
5.18 General Purpose I/O - PTB[0…2] 119
5.19 Basic Timer Module - TIM (TIM16B4C) 122
5.20 Analog Digital Converter - ADC 135
5.21 Current Sense Module - ISENSE 143
5.22 Temperature Sensor - TSENSE 145
5.23 Supply Voltage Sense - VSENSE 146
5.24 Internal Supply Voltage Sense - VS1SENSE 146
5.25 Internal Bandgap Reference Voltage Sense - BANDGAP 146
5.26 MM912_634 - Analog Die Trimming 147
5.27 MM912_634 - MCU Die Overview 152
5.28 Port Integration Module (S12IPIMV1) 159
5.29 Memory Map Control (S12PMMCV1) 167
5.30 Interrupt Module (S12SINTV1) 178
5.31 Background Debug Module (S12SBDMV1) 182
5.32 S12S Debug Module (S12SDBGV2) 199
5.33 Security (S12X9SECV2) 232
5.34 Impact on MCU modules 233
5.35 Secure firmware Code Overview 234
5.36 Initialization of a Virgin Device 237
5.37 Impact of Security on Test 237

5.38 S12 Clock, Reset and Power Management Unit (S12CPMU) 238
5.39 Serial Peripheral Interface (S12SPIV5) 276
5.40 64 KByte Flash Module (S12FTMRC64K1V1) 296
5.41 Die-to-Die Initiator (D2DIV1) 331
6 Packaging 343
6.1 Package Dimensions 343
7 Revision History 348

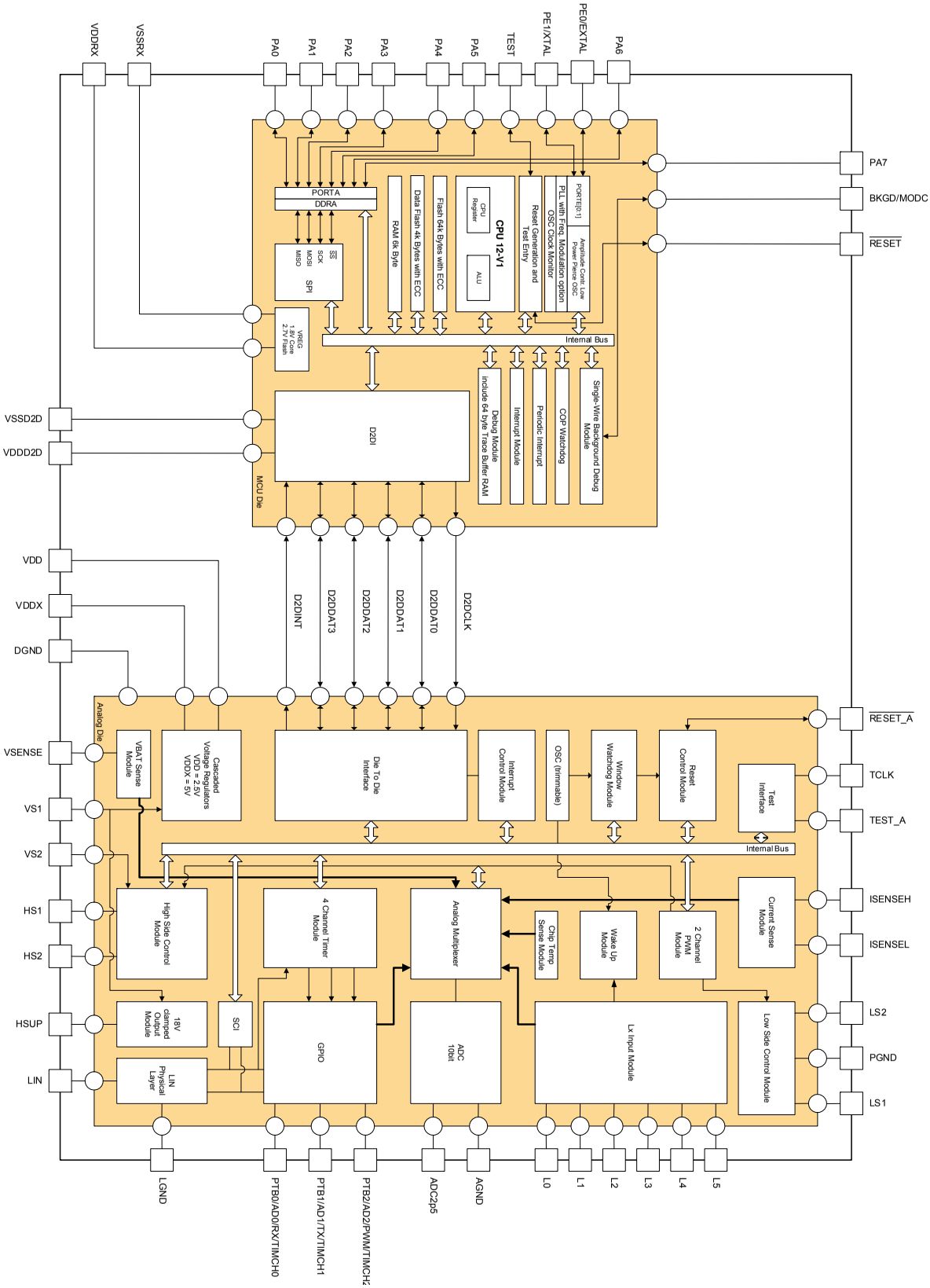

Figure 2. Device Block Diagram

3 Pin Assignment

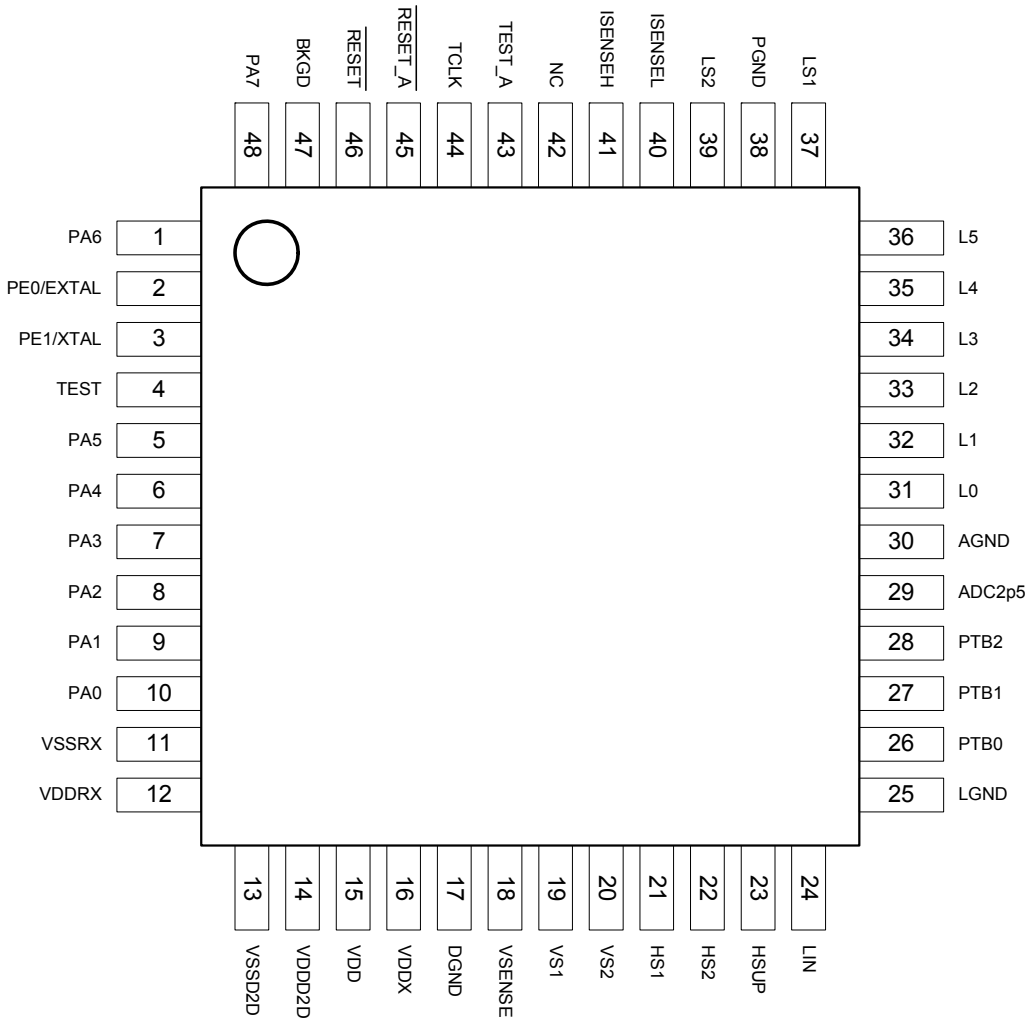

Figure 3. MM912_634 Pin Out

NOTE

The device exposed pad (package option AE only) is recommended to be connected to GND.

Not all pins are available for analog die option 2. See Section 5.3.3, “Analog Die Options" for details.

3.1 MM912_634 Pin Description

The following table gives a brief description of all available pins on the MM912_634 package. Refer to the highlighted chapter for detailed information.

Table 4. MM912_634 Pin Description

Pin #	Pin Name	Formal Name	Description
1	PA6	MCU PA6	General purpose port A input or output pin 6. See Section 5.28, “Port Integration Module (S12IPIMV1)"
2	PE0/EXTAL	MCU Oscillator	EXTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock and port PE may be used for general purpose I/O. See Section 5.38.2.2, “EXTAL and XTAL" and Section 5.28, “Port Integration Module (S12IPIMV1)".
3	PE1/XTAL	MCU Oscillator	XTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock and port PE may be used for general purpose I/O. See Section 5.38.2.2, “EXTAL and XTAL" and Section 5.28, “Port Integration Module (S12IPIMV1)".
4	TEST	MCU Test	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to EVSS in user mode.
5	PA5	MCU PA5	General purpose port A input or output pin 5. See Section 5.28, “Port Integration Module (S12IPIMV1)"
6	PA4	MCU PA4	General purpose port A input or output pin 4. See Section 5.28, “Port Integration Module (S12IPIMV1)".
7	PA3	MCU PA3 / $\overline{SS}$	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI Interface. See Section 5.28, “Port Integration Module (S12IPIMV1)".
8	PA2	MCU PA2 / SCK	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI Interface. See Section 5.28, “Port Integration Module (S12IPIMV1)".
9	PA1	MCU PA1 / MOSI	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI Interface. See Section 5.28, “Port Integration Module (S12IPIMV1)".
10	PA0	MCU PA0 / MISO	General-purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI Interface. See Section 5.28, “Port Integration Module (S12IPIMV1)".
11	VSSRX	MCU 5.0 V Ground	Ground for the MCU 5.0 V power supply.
12	VDDRX	MCU 5.0 V Supply	MCU 5.0 V - Core- and Flash Voltage Regulator supply. See Section 5.27, “MM912_634 - MCU Die Overview".
13	VSSD2D	MCU 2.5 V Ground	Ground for the MCU 2.5 V power supply.
14	VDDD2D	MCU 2.5 V Supply	MCU 2.5 V - MCU Die-to-Die Interface power supply. See Section 5.27, “MM912_634 - MCU Die Overview".
15	VDD	Voltage Regulator Output 2.5 V	+2.5 V main voltage regulator output pin. External capacitor (CVDD) needed. See Section 5.5, “Power Supply".
16	VDDX	Voltage Regulator Output 5.0 V	+5.0 V main voltage regulator output pin. External capacitor (CVDDX) needed. See Section 5.5, “Power Supply".
17	DGND	Digital Ground	This pin is the device digital ground connection for the 5.0 V and 2.5V logic. DGND, LGND, and AGND are internally connected to PGND via a back to back diode.
18	VSENSE	Voltage Sense	Battery voltage sense input. This pin can be connected directly to the battery line for voltage measurements. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC via the analog multiplexer.The pin is self-protected against reverse battery connections. An external resistor (RVSENXSE) is needed for protection[7]. See Section 5.23, “Supply Voltage Sense - VSENSE". Note: This pin function is not available on all device configurations.

Note:

7. An optional filter capacitor CVSENSE is recommended to be placed between the board connector and DVSENSE to GND for increased ESD performance.

Table 4. MM912_634 Pin Description

Pin #	Pin Name	Formal Name	Description
19	VS1	Power Supply Pin 1	This pin is the device power supply pin 1. VS1 is primarily supplying the VDDX Voltage regulator and the Hall Sensor Supply Regulator (HSUP). VS1 can be sensed via a voltage divider through the AD converter. Reverse battery protection diode is required. See Section 5.5, “Power Supply"
20	VS2	Power Supply Pin 2	This pin is the device power supply pin 2. VS2 supplies the High Side Drivers (HSx). Reverse battery protection diode required. See Section 5.5, “Power Supply"
21	HS1	High Side Output 1	This pin is the first High Side output. It is supplied through the VS2 pin. It is designed to drive small resistive loads with optional PWM. In cyclic sense mode, this output will activate periodically during low power mode. See Section 5.12, “High Side Drivers - HS".
22	HS2	High Side Output 2	This pin is the second High Side output. It is supplied through the VS2 pin. It is designed to drive small resistive loads with optional PWM. In cyclic sense mode, this output will activate periodically during low power mode. See Section 5.12, “High Side Drivers - HS". Note: This pin function is not available on all device configurations.
23	HSUP	Hall Sensor Supply Output	This pin is designed as an 18 V Regulator to drive Hall Sensor Elements. It is supplied through the VS1 pin. An external capacitor (CHSUP) is needed. See Section 5.11, “Hall Sensor Supply Output - HSUP". Note: This pin function is not available on all device configurations.
24	LIN	LIN Bus I/O	This pin represents the single-wire bus transmitter and receiver. See Section 5.15, “LIN Physical Layer Interface - LIN". Note: This pin function is not available on all device configurations.
25	LGND	LIN Ground Pin	This pin is the device LIN Ground connection. DGND, LGND, and AGND are internally connected to PGND via a back to back diode.
26	PTB0	General Purpose I/O 0	This is the General Purpose I/O pin 0 based on VDDX with the following shared functions: • PTB0 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor. • AD0 - Analog Input Channel 0, 0…2.5V (ADC2p5) analog input • TIM0CH0 - Timer Channel 0 Input/Output • Rx - Selectable connection to LIN / SCI See Section 5.18, “General Purpose I/O - PTB[0…2]".
27	PTB1	General Purpose I/O 1	This is the General Purpose I/O pin 1 based on VDDX with the following shared functions: • PTB1 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor. • AD1 - Analog Input Channel 1, 0…2.5 V (ADC2p5) analog input • TIM0CH1 - Timer Channel 1 Input/Output • Tx - Selectable connection to LIN / SCI See Section 5.18, “General Purpose I/O - PTB[0…2]".
28	PTB2	General Purpose I/O 2	This is the General Purpose I/O pin 2 based on VDDX with the following shared functions: • PTB2 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor. • AD2 - Analog Input Channel 2, 0…2.5V (ADC2p5) analog input • TIM0CH2 - Timer Channel 2 Input/Output • PWM - Selectable connection to PWM Channel 0 or 1 See Section 5.18, “General Purpose I/O - PTB[0…2]".
29	ADC2p5	ADC Reference Voltage	This pin represents the ADC reference voltage and has to be connected to a filter capacitor. See Section 5.20, “Analog Digital Converter - ADC"
30	AGND	Analog Ground Pin	This pin is the device Analog to Digital converter ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.

Table 4. MM912_634 Pin Description

Pin #	Pin Name	Formal Name	Description
31	L0	High Voltage Input 0	This pins is the High Voltage Input 0 with the following shared functions: • L0 - Digital High Voltage Input 0. When used as digital input, a series resistor (RLX) must be used to protect against automotive transients.(8) • AD3 - Analog Input 3 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU0 - Selectable Wake-up input 0 for wake up and cyclic sense during low power mode. See Section 5.17, “High Voltage Inputs - Lx"
32	L1	High Voltage Input 1	This pins is the High Voltage Input 1 with the following shared functions: • L1 - Digital High Voltage Input 1. When used as digital input, a series resistor (RLX) must be used to protect against automotive transients.(8) • AD4 - Analog Input 4 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU1 - Selectable Wake-up input 1 for wake-up and cyclic sense during low power mode. See Section 5.17, “High Voltage Inputs - Lx"
33	L2	High Voltage Input 2	This pins is the High Voltage Input 2 with the following shared functions: • L2 - Digital High Voltage Input 2. When used as digital input, a series resistor (RLX) must be used to protect against automotive transients.(8) • AD5 - Analog Input 5 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU2 - Selectable Wake-up input 2 for wake-up and cyclic sense during low power mode. See Section 5.17, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
34	L3	High Voltage Input 3	This pins is the High Voltage Input 3 with the following shared functions: • L3 - Digital High Voltage Input 3. When used as digital input, a series resistor (RLX) must be used to protect against automotive transients.(8) • AD6 - Analog Input 6 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU3 - Selectable Wake-up input 3 for wake-up and cyclic sense during low power mode. See Section 5.17, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
35	L4	High Voltage Input 4	This pins is the High Voltage Input 4 with the following shared functions: • L4 - Digital High Voltage Input 4. When used as digital input, a series resistor (RLX) must be used to protect against automotive transients.(8) • AD7 - Analog Input 7 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU4 - Selectable Wake-up input 4 for wake-up and cyclic sense during low power mode. See Section 5.17, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
36	L5	High Voltage Input 5	This pins is the High Voltage Input 5 with the following shared functions: • L5 - Digital High Voltage Input 5. When used as digital input, a series resistor (RLX) must be used to protect against automotive transients.(8) • AD8 - Analog Input 8 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU5 - Selectable Wake-up input 5 for wake-up and cyclic sense during low power mode. See Section 5.17, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.

Note:

8. An optional filter capacitor CLX is recommended to be placed between the board connector and RLX to GND for increased ESD performance.

Table 4. MM912_634 Pin Description

Pin #	Pin Name	Formal Name	Description
37	LS1	Low Side Output 1	Low Side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 5.13, “Low Side Drivers - LSx"
38	PGND	Power Ground Pin	This pin is the device Low Side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
39	LS2	Low Side Output 2	Low Side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 5.13, “Low Side Drivers - LSx"
40	ISENSEL	Current Sense Pin L	Current Sense differential input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 5.21, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pin H	Current Sense differential input “High”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. Section 5.21, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 5.10, “Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. V_{DDX} based. See Section 5.8, “Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset	The RESET pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to VDDRX.
47	BKGD	MCU Background Debug and Mode	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device.
48	PA7	MCU PA7	General purpose port A input or output pin 7. See Section 5.28, “Port Integration Module (S12IPIMV1)"

3.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 5. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
PE0	EXTAL	VD_{DRX}	PUPEE/ OSCPINS_EN	DOWN	Port E I/O, Oscillator pin
PE1	XTAL	V_{DDRX}	PUPBE/ OSCPINS_EN	DOWN	Port E I/O, Oscillator pin
$\overline{\text{RESET}}$	—	VDDRX	PULLUP		External reset
TEST	—	N.A.	$\overline{\text{RESET}}$ pin	DOWN	Test input
BKGD	MODC	VDDRX	BKPUE	UP	Background debug
PA7	—	VDDRX	NA	NA	Port A I/O

Table 5. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
PA6	—	VDDRX	NA	NA	Port A I/O
PA5	—	VDDRX	NA	NA	Port A I/O
PA4	—	VDDRX	NA	NA	Port A I/O
PA3	SS	VDDRX	NA	NA	Port A I/O, SPI
PA2	SCK	VDDRX	NA	NA	Port A I/O, SPI
PA1	MOSI	VDDRX	NA	NA	Port A I/O, SPI
PA0	MISO	VDDRX	NA	NA	Port A I/O, SPI
PC1	D2DINT	VDDD2D	PUPCE/ D2DEN	Disabled	Port C I/O, D2DI
PC0	D2DCLK	VDDD2D	NA	NA	Port C I/O, D2DI
PD7-0	D2DDAT7-0	VDDD2D	PUPDE/ D2DEN	Disabled	Port D I/O, D2DI

4 Electrical Characteristics

4.1 General

This section contains electrical information for the embedded MC9S12I64 microcontroller die, as well as the MM912_634 analog die.

4.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level. All voltages are with respect to ground, unless otherwise noted.

Table 6. Absolute Maximum Electrical Ratings - Analog Die

Ratings	Symbol	Value	Unit
Supply Voltage at VS1 and VS2 Normal operation (DC) Transient conditions (load dump) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	$V_{SUP(SS)}$ $V_{SUP(PK)}$ $V_{SUP(TR)}$	-0.3 to 27 -0.3 to 40 (9)	V
L0…L5 - Pin Voltage Normal operation with a series R_{LX} resistor (DC) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	V_{LxDC} V_{LxTR}	27 to 40 (9)	V
LIN Pin Voltage Normal operation (DC) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	V_{BUSDC} V_{BUSTR}	-33 to 40 (9)	V
Supply Voltage at VDDX	V_{DDX}	-0.3 to 5.5	V
Supply Voltage at VDD (10)	V_{DD}	-0.3 to 2.75	V
VDD Output Current	I_{VDD}	Internally Limited	A
VDDX Output Current	I_{VDDX}	Internally Limited	A
TCLK Pin Voltage	V_{TCLK}	-0.3 to 10	V
$\overline{\text{RESET\_A}}$ Pin Voltage	V_{IN}	-0.3 to V_{DDx}+0.3	V
Input / Output Pins PTB[0:2] Voltage	V_{IN}	-0.3 to V_{DDx}+0.3	V
HS1 and HS2 Pin Voltage (DC)	V_{HS}	-0.3 to VS2+0.3	V
LS1 and LS2 Pin Voltage (DC)	V_{LS}	-0.3 to 45	V
ISENSEH and ISENSEL Pin Voltage (DC)	V_{ISENSE}	-0.3 to 40	V
HSUP Pin Voltage (DC)	V_{HSUP}	-0.3 to VS1+0.3	V
VSENSE Pin Voltage (DC)	V_{VSENSE}	-27 to 40	V

Note:

9. See Section 4.9, “Additional Test Information ISO7637-2"
10. Caution: As this pin is adjacent to the VDDX pin, care should be taken to avoid a short between VDD and VDDX, for example during soldering process. A short-circuit between these pins might lead to permanent damage.

Table 7. Maximum Electrical Ratings - MCU Die[11]

Ratings	Symbol	Value	Unit
5.0 V Supply Voltage (Supplying the MCU internal regulator for core and flash)	V_{DDRX}	-0.3 to 6.0	V
2.5 V D2D - Supply Voltage	V_{DDD2D}	-0.3 to 3.6	V
Digital I/O input voltage (PA0...PA7, PE0, PE1)	V_{IN}	-0.3 to 6.0	V
EXTAL, XTAL (PE0 and PE1 in alternative configuration)	V_{ILV}	-0.3 to 2.16	V
TEST Input	V_{TEST}	-0.3 to 10.0	V
Instantaneous Maximum Current Single pin limit for all digital I/O pins	I_D	-25 to 25	mA
Instantaneous Maximum Current Single pin limit for EXTAL, XTAL	I_{DL}	-25 to 25	mA

Note:
11. All digital I/O pins are internally clamped to VSSRX and VDDRX.

Table 8. Maximum Thermal Ratings

Ratings	Symbol	Value	Unit
Storage Temperature	T_{STG}	-55 to 150	°C
Package, Thermal Resistance - LQFP48-EP			°C/W
Four layer board (JEDEC 2s2p)			
Junction to Ambient Natural Convection [12]	$R_{\theta JA}$	38	
Junction to Board [14]	$R_{\theta JB}$	16	
Two layer board (JEDEC 1s)			
Junction to Ambient Natural Convection [12], [13]	$R_{\theta JA}$	91	
Package, Thermal Resistance - LQFP48			°C/W
Four layer board (JEDEC 2s2p)			
Junction to Ambient Natural Convection [12]	$R_{\theta JA}$	59	
Junction to Board [14]	$R_{\theta JB}$	31	
Two layer board (JEDEC 1s)			
Junction to Ambient Natural Convection [12], [13]	$R_{\theta JA}$	96	
Peak Package Reflow Temperature During Reflow[15], [16]	T_{PPRT}	Note 16	°C

Notes
12. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
13. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
14. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
15. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
16. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.3 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

Table 9. Operating Conditions

Ratings	Symbol	Value	Unit
Analog Die Nominal Operating Voltage	V_{SUP}	5.5 to 18	V
Analog Die Functional Operating Voltage - Device is fully functional. All features are operating.	V_{SUPOP}	5.5 to 27	V
MCU I/O and Supply Voltage[17]	V_{DDRX}	4.75 to 5.25	V
MCU Digital Logic Supply Voltage[17]	V_{DDD2D}	2.25 to 2.75	V
MCU Oscillator MM912x634xxxAE MM912x634xxxAP	f_{OSC}	 4.0 to 16 4.0 to 16	MHz
MCU Bus frequency MM912x634xxxAE MM912x634xxxAP	f_{BUS}	f_{BUSMAX}[18]	MHz
Operating Ambient Temperature MM912x634xMxxx MM912x634xVxxx	T_A	 -40 to 125 -40 to 105	°C
Operating Junction Temperature - Analog Die	T_{J_A}	-40 to 150	°C
Operating Junction Temperature - MCU Die	T_{J_M}	-40 to 150	°C

Note:

17. During power up and power down sequence always $V_{DDD2D} < V_{DDRX}$
18. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1

4.4 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

4.4.1 Measurement Conditions

All measurements are without output loads. Currents are measured in MCU special single chip mode and the CPU code is executed from RAM, unless otherwise noted.

Table 10. Supply Currents

Ratings	Symbol	Min	Typ[19]	Max	Unit
Normal Mode analog die only, excluding external loads, LIN Recessive State (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ V_{DD} ≤ 2.75 V, 4.5 V ≤ V_{DDX} ≤ 5.5 V, -40 °C ≤ T_{J_A} ≤ 150 °C).	I_{RUN_A}	-	5.0	8.0	mA
Normal Mode MCU die only (T_{J_M}=150 °C; V_{DDD2D} = 2.75 V, V_{DDRX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS}= f_{BUSMAX}[20][21]	I_{RUN_M}	-	18	20	mA
Stop Mode internal analog die only, excluding external loads, LIN Recessive State, Lx enabled, measured at VS1+VS2 (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ V_{DD} ≤ 2.75 V, 4.5 V ≤ V_{DDX} ≤ 5.5 V) -40 °C ≤ T_{J_A} ≤ 125 °C	I_{STOP_A}	 -	 20	 40	µA
Stop Mode MCU die only (V_{DDD2D} = 2.75 V, V_{DDRX} = 5.5 V, f_{OSC}= 4.0 MHz; MCU in STOP; RTI and COP off)[22] T_{J_M}=150°C T_{J_M}=-40°C T_{J_M}=25°C	I_{STOP_M}	 - - -	 85 31 31	 150 50 50	µA
Sleep Mode (VDD = VDDX = OFF; 5.5 V ≤ V_{SUP} ≤ 18 V; -40 °C ≤ T_{J_A} ≤ 125 °C; 3.0 V > Lx > 1.0 V)	I_{SLEEP}	-	15	28	µA
Cyclic Sense Supply Current Adder (5.0 ms Cycle)	I_{CS}	-	15	20	µA

Note:

19. Typical values noted reflect the approximate parameter mean at T_A = 25 °C
20. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1
21. I_{RUN_M} denotes the sum of the currents flowing into VDD and VDDX.
22. I_{STOP_M} denotes the sum of the currents flowing into VDD and VDDX.

4.5 Static Electrical Characteristics

All characteristics noted under the following conditions:

- 5.5 V ≤ V_{SUP} ≤ 18 V
- -40 °C ≤ T_A ≤ 125 °C (MM912x634xMxxx)
- -40 °C ≤ T_A ≤ 105 °C (MM912x634xVxxx)

Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

4.5.1 Static Electrical Characteristics Analog Die

Table 11. Static Electrical Characteristics - Power Supply

Ratings	Symbol	Min	Typ	Max	Unit
Power-On Reset (POR) Threshold (measured on VS1)	V_{POR}	1.5	-	3.5	V
Low Voltage Warning (LVI)					
Threshold (measured on VS1, falling edge)	V_{LVI}	5.55	6.0	6.6	V
Hysteresis (measured on VS1)	V_{LVI_H}	-	1.0	-	
High Voltage Warning (HVI)					
Threshold (measured on VS2, rising edge)	V_{HVI}	18	19.25	20.5	V
Hysteresis (measured on VS2)	V_{HVI_H}	-	1.0	-	
Low Battery Warning (LBI)					
Threshold (measured on VSENSE, falling edge)	V_{LBI}	5.55	6.0	6.6	V
Hysteresis (measured on VSENSE)	V_{LBI_H}	-	1.0	-	
J2602 Under-voltage threshold	$V_{J2602UV}$	5.5	5.7	6.2	V
Low VDDX Voltage (LVRX) Threshold	V_{LVRX}	2.7	3.0	3.3	V
Low VDD Voltage Reset (LVR) Threshold Normal Mode	V_{LVR}	2.30	2.35	2.4	V
Low VDD Voltage Reset (LVR) Threshold Stop Mode [23]	V_{LVRS}	1.6	1.85	2.1	V
VDD Over-voltage Threshold (VROV)	V_{VDDOV}	2.575	2.7875	3.0	V
VDDX Over-voltage Threshold (VROVX)	V_{VDDXOV}	5.25	5.675	6.1	V

Note:
23. See MM912_634ER - MM912_634, Silicon Analog Mask (M91W) / Digital Mask (N53A) Errata

Table 12. Static Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Low-state Output Voltage I_{OUT} = 2.0 mA	V_{OL}	-	-	0.8	V
Pull-up Resistor	R_{RPU}	25	-	50	kOhm
Low-state Input Voltage	V_{IL}	-	-	$0.3V_{DDX}$	V
High-state Input Voltage	V_{IH}	$0.7V_{DDX}$	-	-	V
Reset Release Voltage (VDDX)	V_{RSTRV}	-	1.5	-	V
RESET_A pin Current Limitation		5.0	7.5	10	mA

Table 13. Static Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Watchdog Disable Voltage (fixed voltage)	V_{TST}	7.0	-	10	V
Watchdog Enable Voltage (fixed voltage)	V_{TSTEN}	-	-	5.5	V

Table 14. Static Electrical Characteristics - Voltage Regulator 5.0 V (VDDX)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDDX} + $I_{VDDXINTERNAL}$ < 80 mA; 5.5 V < V_{SUP} < 27 V (24)	V_{DDXRUN}	4.75	5.00	5.25	V
Normal Mode Output Current Limitation (I_{VDDX})	$I_{VDDXRUN}$	80	130	200	mA
Stop Mode Output Voltage (I_{VDDX} + $I_{VDDXINTERNAL}$ < 500 µA for T_J ≥ 25 °C; I_{VDDX} + $I_{VDDXINTERNAL}$ < 400 µA for T_J < 25 °C) (24)	$V_{DDXSTOP}$	-	5.0	5.5	V
Stop Mode Output Current Limitation (I_{VDDX})	$I_{VDDXSTOP}$	1.0	-	20	mA
Line Regulation Normal Mode, I_{VDDX} = 80 mA Stop Mode, I_{VDDX} = 500 µA	 LR_{XRUN} LR_{XSTOP}	 - -	 20 -	 25 200	mV
Load Regulation Normal Mode, 1.0 mA < I_{VDDX} < 80 mA Normal Mode, V_{SUP} = 3.6 V, 1.0 mA < I_{VDDX} < 40 mA Stop Mode, 0.1 mA < I_{VDDX} < 500 µA	 LD_{XRUN} LD_{XCRK} LD_{XSTOP}	 - - -	 15 - -	 80 200 250	mV
External Capacitor	C_{VDDX}	1.0	-	10	µF
External Capacitor ESR	C_{VDDX_R}	-	-	10	Ohm

Note:

24. $I_{VDDXINTERNAL}$ includes internal consumption from both analog and MCU die.

Table 15. Static Electrical Characteristics - Voltage Regulator 2.5 V (VDD)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDD} + $I_{VDDINTERNAL}$ ≤ 45 mA; 5.5 V < V_{SUP} < 27 V (25)	V_{DDRUN}	2,425	2.5	2,575	V
Normal Mode Output Current Limitation (I_{VDD}) T_J < 25 °C T_J ≥ 25 °C	$I_{VDDLIMRUN}$	 - -	 80 80	 120 143	mA
Stop Mode Output Voltage (I_{VDD} + $I_{VDDINTERNAL}$ < 500 µA for T_J ≥ 25 °C; I_{VDD} + $I_{VDDINTERNAL}$ < 400 µA for T_J < 25 °C) (25)	V_{DDSTOP}	2.25	2.5	2.75	V
Stop Mode Output Current Limitation (I_{VDD})	$I_{VDDLIMSTOP}$	-	-	10	mA
Line Regulation Normal Mode, I_{VDD} = 45 mA Stop Mode, I_{VDD} = 1.0 mA	 LR_{RUN} LR_{STOP}	 - -	 10 -	 12.5 200	mV
Load Regulation Normal Mode, 1.0 mA < I_{VDD} < 45 mA Normal Mode, V_{SUP} = 3.6 V, 1.0 mA < I_{VDD} < 30 mA Stop Mode, 0.1 mA < I_{VDD} < 1.0 mA	 LD_{RUN} LD_{CRK} LD_{STOP}	 - - -	 7.5 - -	 40 40 200	mV
External Capacitor	C_{VDD}	1.0	-	10	µF
External Capacitor ESR	C_{VDD_R}	-	-	10	Ohm

Note:

25. $I_{VDDINTERNAL}$ includes internal consumption from both analog and MCU die.

Table 16. Static Electrical Characteristics - Hall Sensor Supply Output - HSUP

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation	I_{HSUP}	40	70	90	mA
Output Drain-to-Source On resistance T_J = 150 °C, ILOAD = 30 mA; 5.5 V ≤ VSUP ≤ 16 V T_J = 150 °C, ILOAD = 30 mA; 3.7 V ≤ VSUP < 5.5 V	$R_{DS(ON)}$	- -	- -	10 12	Ohm
Output Voltage: (18 V ≤ V_{SUP} ≤ 27 V)	$VHSUP_{MAX}$	16	17.5	18	V
Load Regulation (1.0 mA < I_{HSUP} < 30 mA; V_{SUP} > 18 V)	LD_{HSUP}	-	-	500	mV
Hall Supply Capacitor Range	C_{HSUP}	0.22	-	10	µF
External Capacitor ESR	C_{HSUP_R}	-	-	10	Ohm

Table 17. Static Electrical Characteristics - High Side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	- - -	- - -	7.0 10 14	Ohm
Output Current Limitation (0 V < V_{OUT} < V_{SUP} - 2.0 V)	I_{LIMHSX}	60	110	250	mA
Open Load Current Detection	I_{OLHSX}	-	5.0	7.5	mA
Leakage Current (-0.2 V < V_{HSx} < V_{S2} + 0.2 V)	I_{LEAK}	-	-	10	µA
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	V_{SUP} -2	-	-	V

Table 18. Static Electrical Characteristics - Low Side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	– – –	– – –	2.5 4.5 10	Ohm
Output Current Limitation (2.0 V < V_{OUT} < V_{SUP})	I_{LIMLSX}	180	275	380	mA
Open Load Current Detection	I_{OLLSX}	-	8.0	12	mA
Leakage Current (-0.2 V < V_{OUT} < VS1)	I_{LEAK}	-	-	10	µA
Active Output Energy Clamp (I_{OUT} = 150 mA)	V_{CLAMP}	40	-	45	V
Coil Series Resistance (I_{OUT} = 150 mA)	R_{COIL}	120	-		Ohm
Coil Inductance (I_{OUT} = 150 mA)	R_{COIL}	-	-	400	mH
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	2.0	-	-	V

Table 19. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	-	-	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$	-	-	20	µA

Table 19. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Input Leakage Current; GND Disconnected; GNDDEVICE = VSUP; 0 < V_{BUS} < 18 V; V_{BAT} = 12 V	$I_{BUS\_NO\_GND}$	-1.0	-	1.0	mA
Input Leakage Current; VBAT disconnected; VSUP_DEVICE = GND; 0 < V_{BUS} < 18 V	IBUS_NO_BAT	-	-	100	µA
Receiver Input Voltage; Receiver Dominant State	V_{BUSdom}	-	-	0.4	V_{SUP}
Receiver Input Voltage; Receiver Recessive State	V_{BUSrec}	0.6	-	-	V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{BUS_HYS}	-	-	0.175	V_{SUP}
Voltage Drop at the serial Diode	D_{ser_int}	0.4	0.7	1.0	V
LIN Pull-up Resistor	R_{slave}	20	30	60	kOhm
Bus Wake-up Threshold from Stop or Sleep	V_{WUP}	4.0	5.0	6.0	V
Bus Dominant Voltage	V_{DOM}	-	-	2.5	V

Table 20. Static Electrical Characteristics - High Voltage Inputs - Lx

Ratings	Symbol	Min	Typ	Max	Unit
Low Detection Threshold	V_{THL}				V
(7.0 V ≤ V_{SUP} ≤ 27 V)		2.2	2.5	3.4	
(5.5 V ≤ V_{SUP} ≤ 7.0 V)		1.5	2.5	4.0	
High Detection Threshold	V_{THH}				V
(7.0 V ≤ V_{SUP} ≤ 27 V)		2.6	3.0	3.7	
(5.5 V ≤ V_{SUP} ≤ 7.0 V)		2.0	3.0	4.5	
Hysteresis	V_{HYS}				V
(5.5 V < V_{SUP} < 27 V)		0.25	0.45	1.0	
Input Current Lx (-0.2 V < V_{IN} < VS1)	I_{IN}	-10	-	10	µA
Analog Input Impedance Lx	R_{LxIN}	-	-	1.2	MOhm
Lx Series Resistor	R_{LX}	9.5	10	10.5	kOhm
Lx Capacitor (optional)[26]	C_{LX}	-	100	-	nF
Analog Input Divider Ratio ($RATIO_{Lx}$ = V_{Lx} / V_{ADOUT0})					
LXDS (Lx Divider Select) = 0	$RATIO_{Lx}$	-	2.0	-	
LXDS (Lx Divider Select) = 1		-	7.2	-	
Analog Input Divider Ratio Accuracy	$RATIO_{LX}$	-5.5	-	5.5	%
Analog Inputs Channel Ratio - Mismatch					
LXDS (Lx Divider Select) = 0	Lx_{MATCH}	-	-	5.0	%
LXDS (Lx Divider Select) = 1		-	-	5.0	

Note:
26. The ESD behavior specified in Section 4.8, “ESD Protection and Latch-up Immunity" are guaranteed without the optional capacitor.

Table 21. Static Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	0.7V_{DDX}	-	V_{DDX}+0.3	V
Input Low Voltage	V_{IL}	V_{SS}-0.3	-	0.35V_{DDX}	V
Input Hysteresis	V_{HYS}	-	140	-	mV
Input High Voltage (VS1 = 3.7 V)	$V_{IH3.7}$	2.1	-	V_{DDX}+0.3	V

Table 21. Static Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
Input Low Voltage (VS1 = 3.7 V)	$V_{IL3.7}$	V_{SS}-0.3	-	1.4	V
Input Hysteresis (VS1 = 3.7 V)	$V_{HYS3.7}$	100	200	300	mV
Input Leakage Current (pins in high-impedance input mode) (V_{IN} = V_{DDX} or V_{SSX})	I_{IN}	-1.0	-	1.0	µA
Output High Voltage (pins in output mode) Full drive I_{OH} = -10 mA	V_{OH}	V_{DDX}-0.8	-	-	V
Output Low Voltage (pins in output mode) Full drive I_{OL} = 10 mA	V_{OL}	-	-	0.8	V
Internal Pull-up Resistance (V_{IH} min > Input voltage > V_{IL} max)	R_{PUL}	26.25	37.5	48.75	kOhm
Input Capacitance	C_{IN}	-	6.0	-	pF
Clamp Voltage when selected as analog input	V_{CL_AIN}	VDD	-	-	V
Analog Input impedance = 10 kOhm max, Capacitance = 12 pF	R_{AIN}	-	-	10	kOhm
Analog Input Capacitance = 12 pF	C_{AIN}	-	12	-	pF
Maximum current all PTB combined (VDDX capability)	I_{BMAX}	-15	-	15	mA
Output Drive strength at 10 MHz	C_{OUT}	-	-	100	pF

Table 22. Static Electrical Characteristics - Analog Digital Converter - ADC[27]

Ratings	Symbol	Min	Typ	Max	Unit
ADC2p5 Reference Voltage 5.5 V < V_{SUP} < 27 V	$V_{ADC2p5RUN}$	2,45	2.5	2.55	V
ADC2p5 Reference Stop Mode Output Voltage	$V_{ADC2p5STOP}$	-	-	100	mV
Line Regulation, Normal Mode	LR_{RUNA}	-	10	12.5	mV
External Capacitor	C_{ADC2p5}	0.1	-	1.0	µF
External Capacitor ESR	C_{VDD_R}	-	-	10	Ohm
Scale Factor Error	E_{SCALE}	-1	-	1	LSB
Differential Linearity Error	E_{DNL}	-1.5	-	1.5	LSB
Integral Linearity Error	E_{INL}	-1.5	-	1.5	LSB
Zero Offset Error	E_{OFF}	-2.0	-	2.0	LSB
Quantization Error	E_Q	-0.5	-	0.5	LSB
Total Error with offset compensation	TE	-5.0	-	5.0	LSB
Bandgap measurement Channel (CH14) Valid Result Range (including ±7.0% bg1p25sleep accuracy + high-impedance measurement error of ±5.0% at f_{ADC})[28]	AD_{CH14}	1.1	1.25	1.4	V

Note:
27. No external load allowed on the ADC2p5 pin.
28. Reduced ADC frequency will lower measurement error.

Table 23. Static Electrical Characteristics - Current Sense Module - ISENSE

Ratings	Symbol	Min	Typ	Max	Unit
Gain					
CSGS (Current Sense Gain Select) = 000	G	-	7	-	
CSGS (Current Sense Gain Select) = 001		-	9	-	
CSGS (Current Sense Gain Select) = 010		-	10	-	
CSGS (Current Sense Gain Select) = 011		-	12	-	
CSGS (Current Sense Gain Select) = 100		-	14	-	
CSGS (Current Sense Gain Select) = 101		-	18	-	
CSGS (Current Sense Gain Select) = 110		-	24	-	
CSGS (Current Sense Gain Select) = 111		-	36	-	
Gain Accuracy		-3.0	-	3.0	%
Offset		-1.5	-	1.5	%
Resolution[29]	RES	-	51	-	mA/LSB
ISENSEH, ISENSEL Input Common Mode Voltage Range	V_{IN}	-0.2	-	3.0	V
Current Sense Module - Normal Mode Current Consumption Adder (CSE = 1)	I_{ISENSE}	-	600	-	µA

Note:
29. RES = 2.44 mV/(GAIN*R_{SHUNT})

Table 24. Static Electrical Characteristics - Temperature Sensor - TSENSE

Ratings	Symbol	Min	Typ	Max	Unit
Internal Chip Temperature Sense Gain[30]	TS_G	-	9.17	-	mV/k
Internal Chip Temperature Sense Error at the end of conversion[30]	TS_{Err}	–5.0	-	5.0	°C
Temperature represented by a ADC_{IN} Voltage of 0.150 V[30]	$T_{0.15V}$	-55	-50	-45	°C
Temperature represented by a ADC_{IN} Voltage of 1.984 V[30]	$T_{1.984V}$	145	150	155	°C

Note:
30. Guaranteed by design and characterization.

Table 25. Static Electrical Characteristics - Supply Voltage Sense - VSENSE and VS1SENSE

Ratings	Symbol	Min	Typ	Max	Unit
VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VSENSE}$	-	10.8	5.0%	
VSENSE error - whole path (VSENSE pad to Digital value)	Er_{VSENSE}	-	-	5.0	%
VS1SENSE Input Divider Ratio ($RATIO_{VS1SENSE}$ = $V_{VS1SENSE}$ / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VS1SENSE}$	-	10.8	5.0%	
VS1SENSE error - whole path (VS1 pad to Digital value)	$Er_{VS1SENSE}$	-	-	5.0	%
VSENSE Series Resistor	R_{VSENSE}	9.5	10	10.5	kOhm
VSENSE Capacitor (optional)[31]	C_{VSENSE}	-	100	-	nF

Note:
31. The ESD behavior specified in Section 4.8, “ESD Protection and Latch-up Immunity" is guaranteed without the optional capacitor.

4.5.2 Static Electrical Characteristics MCU Die

4.5.2.1 I/O Characteristics

This section describes the characteristics of all I/O pins except EXTAL, XTAL, TEST and supply pins.

Table 26. 5.0 V I/O Characteristics for PTA, PTE, $\overline{\text{RESET}}$ and BKGD Pins

Ratings	Symbol	Min	Typ	Max	Unit
Input high voltage	V_{IH}	0.65*V_{DDRX}	-	-	V
Input high voltage	V_{IH}	-	-	V_{DDRX} + 0.3	V
Input low voltage	V_{IL}	-	-	0.35*V_{DDRX}	V
Input low voltage	V_{IL}	V_{SSRX} - 0.3	-	-	V
Input hysteresis	V_{HYS}	-	250	-	mV
Input leakage current (pins in high-impedance input mode) V_{IN} = V_{DDRX} or V_{SSRX}	I_{IN}	-1.0	-	1.0	µA
Output high voltage (pins in output mode) I_{OH} = -4.0 mA	V_{OH}	V_{DDRX} – 0.8	-	-	V
Output low voltage (pins in output mode) I_{OL} = +4.0 mA	V_{OL}	-	-	0.8	V
Internal pull-up resistance (V_{IH}min > input voltage > V_{IL}max)	R_{PUL}	25	-	50	kΩ
Internal pull-down resistance (V_{IH}min > input voltage > V_{IL}max)	R_{PDH}	25	-	50	kΩ
Input capacitance	C_{in}	-	6.0	-	pF
Injection current[32] Single pin limit Total device Limit, sum of all injected currents	 I_{ICS} I_{ICP}	 -2.5 -25	 - -	 2.5 25	mA

Note:

32. Refer to Section 4.8, “ESD Protection and Latch-up Immunity" for more details.

4.5.2.2 Electrical Specification for MCU internal Voltage Regulator

Table 27. IVREG Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input Voltages	V_{VDDRA}	3.13	—	5.5	V
V_{DDRX} Low Voltage Interrupt Assert Level V_{DDRX} Low Voltage Interrupt Deassert Level	V_{LViA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V
V_{DDRX} Low Voltage Reset Deassert [33][34][35]	V_{LVRXD}	—	3.05	3.13	V
V_{DDRX} Low Voltage Reset Assert [33][34][35]	V_{LVRXA}	2.95	3.02	—	V

Note:

33. Device functionality is guaranteed on power down to the LVR assert level.
34. Monitors VDDRX, active only in Full Performance mode. MCU is monitored by the POR in RPM (see Figure 4).
35. Monitors VDDRX, active only in Full Performance mode. V_{LVRA} and V_{PORD}.

NOTE

The LVR monitors the voltages V_{DD_CORE}, $V_{DDFLASH}$ and V_{DDRX}. As soon as voltage drops on these supplies which would prohibit the correct function of the microcontroller, the LVR is triggering a reset.

4.5.2.3 Chip Power-up and Voltage Drops

LVI (low voltage interrupt), POR (power-on reset) and LVRs (low voltage reset) handle chip power-up or drops of the supply voltage.

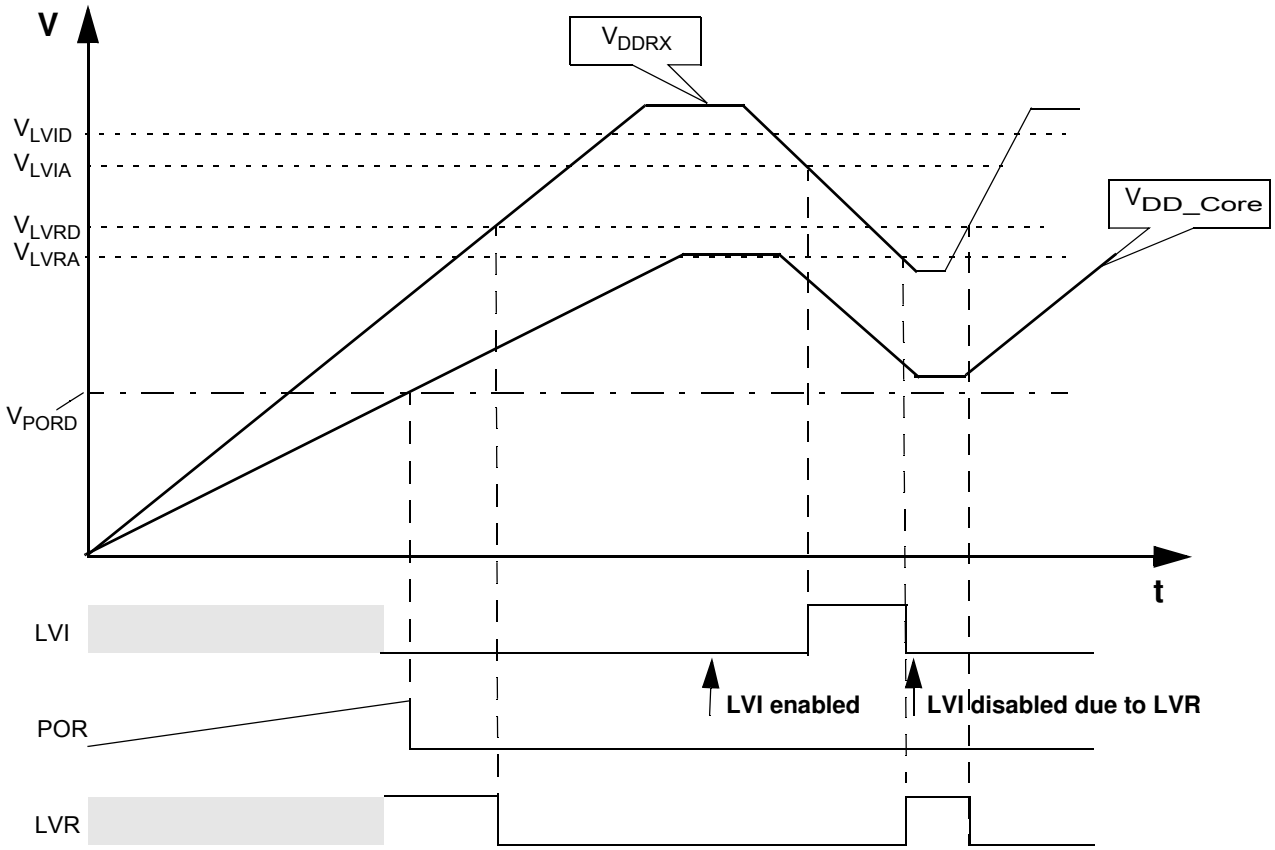

Figure 4. MC9S12I32 - Chip Power-up and Voltage Drops (not scaled)

4.6 Dynamic Electrical Characteristics

Dynamic characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

4.6.1 Dynamic Electrical Characteristics Analog Die

Table 28. Dynamic Electrical Characteristics - Modes of Operation

Ratings	Symbol	Min	Typ	Max	Unit
VDD Short Timeout	t_{VTO}	110	150	205	ms
Analog Base Clock	f_{BASE}	-	100	-	kHz
Reset Delay	t_{RST}	140	200	280	µs

Table 29. Dynamic Electrical Characteristics - Power Supply[36]

Ratings	Symbol	Min	Typ	Max	Unit
Glitch Filter Low Battery Warning (LBI)	t_{LB}	-	2.0	-	µs
Glitch Filter Low Voltage Warning (LVI)	t_{LV}	-	2.0	-	µs
Glitch Filter High Voltage Warning (HVI)	t_{HV}	-	2.0	-	µs

Note:
36. Guaranteed by design.

Table 30. Dynamic Electrical Characteristics - Die to Die Interface - D2D

Ratings	Symbol	Min	Typ	Max	Unit
Operating Frequency (D2DCLK, D2D[0:3])	f_{D2D}	-	-	f_{BUSMAX}[37]	MHz

Note:
37. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1

Table 31. Dynamic Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Reset Deglitch Filter Time	t_{RSTDF}	1.2	2.0	3.0	µs
Reset Low Level Duration	t_{RSTLOW}	140	200	280	µs

Table 32. Dynamic Electrical Characteristics - Wake-up / Cyclic Sense

Ratings	Symbol	Min	Typ	Max	Unit
Lx Wake-up Filter Time	t_{WUF}	-	20		µs
Cyclic Sense / Forced Wake-up Timing Accuracy - not trimmed	CS_{AC}	-35	-	35	%
Cyclic Sense / Forced Wake-up Timing Accuracy - trimmed[38]	CS_{ACT}	-5.0	-	5.0	%
Time between HSx on and Lx sense during cyclic sense	t_S	same as t_{HSON} / t_{HSONT}			-
HSx ON duration during Cyclic Sense	t_{HSON}	140	200	280	µs
HSx ON duration during Cyclic Sense - trimmed[38]	t_{HSONT}	180	200	220	µs

Note:
38. No trimming possible in Sleep mode.

Table 33. Dynamic Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Initial Non-window Watchdog Timeout	t_{IWDTO}	110	150	190	ms
Watchdog Timeout Accuracy - not trimmed	WD_{AC}	-35	-	35	%
Watchdog Timeout Accuracy - trimmed	WD_{ACT}	-5.0	-	5.0	%

Table 34. Dynamic Electrical Characteristics - High Side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
High Side Operating Frequency[39] Load Condition: $C_{LOAD} \leq 2.2$ nF; $R_{LOAD} \geq 500\ \Omega$	f_{HS}	-	-	50	kHz

Note:
39. Guaranteed by design.