Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Freescale Semiconductor
Advance Information

Document Number: MM912_637D1
Rev. 3.0, 1/2012

RoHS

Xtrinsic Battery Sensor with LIN for 12 V Lead-acid Batteries

MM912_637

EP SUFFIX (PB-FREE)
98ASA00343D
48-PIN QFN

Freescale's Xtrinsic MM912_637 battery sensors are fully integrated battery monitoring devices. The devices allow simultaneous measurement of battery current and voltage for precise determination of SOC (State of Charge), SOH (State of Health), and other parameters.

The integrated temperature sensor combined with the close proximity to the battery allows battery temperature measurement. Multiple application-specific hardware blocks reduce MCU overhead and related power consumption. Configurable low-power modes with automated battery state observation and sophisticated wake-up capability further reduce current consumption. The integrated LIN 2.1 interface allows communication and control of battery monitoring functions.

Features

- Battery voltage measurement
- Battery current measurement in up to eight ranges
- On chip temperature measurement
- Normal and two low-power modes
- Current threshold detection and current averaging in standby => wake-up from low-power mode
- Triggered wake-up from LIN and periodic wake-up
- Signal low pass filtering (current, voltage)
- PGA (programmable low-noise gain amplifier) with automatic gain control feature
- Accurate internal oscillator (an external quartz oscillator may be used for extended accuracy)
- Communication via a LIN 2.1, LIN2.0 bus interface
- S12 microcontroller with 128 kByte flash, 6.0 kByte RAM, 4.0 kByte data flash
- Background debug module
- External temperature sensor option (TSUP, VTEMP)
- Optional 2nd external voltage sense input (VOPT)
- Four x 5.0 V GPIO including one Wake-up capable high voltage input (PTB3/L0)
- Eight x MCU general purpose I/O including SPI functionality
- Industry standard EMC compliance

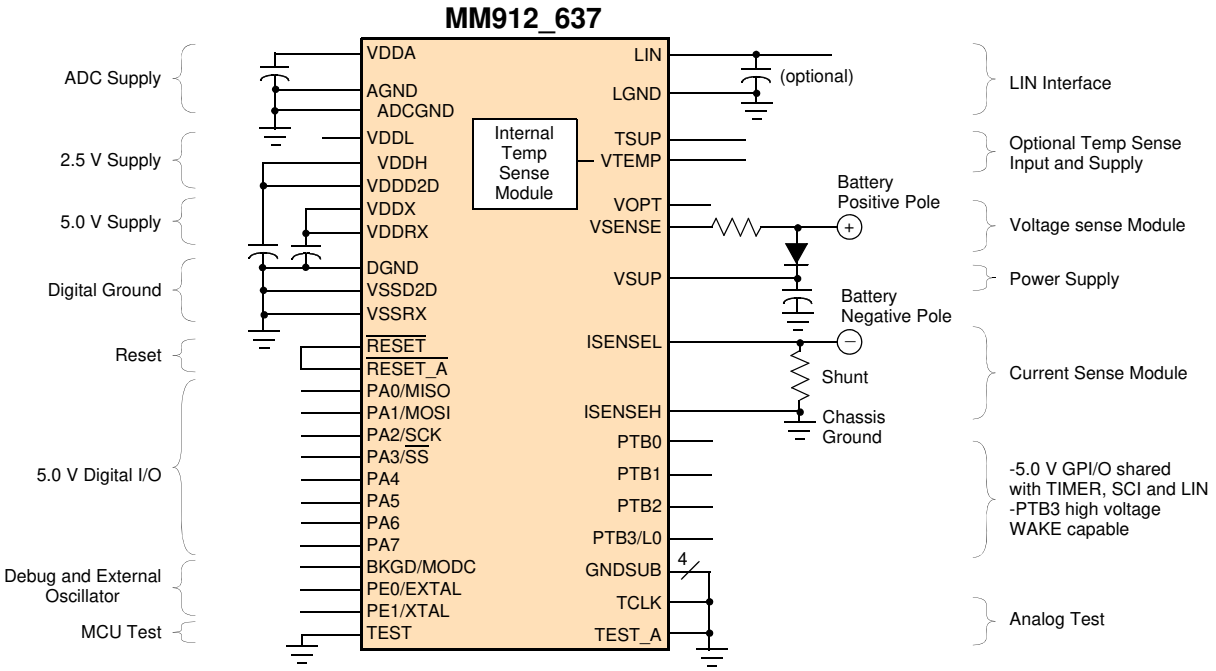


Figure 1. Simplified Application Diagram

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

freescale Xtrinsic

1 Ordering Information

Table 1. Ordering Information

Device (Add an R2 suffix for Tape and Reel orders)	Temperature Range (T_A)	Package	Maximum Input Voltage	Analog Option	Flash (kB)
MM912I637AM2EP	-40 °C to 125 °C	48 QFN-EP	42 V	2	96
MM912J637AM2EP					128
MM912I637AV1EP	-40 °C to 105 °C			1	96
MM912J637AV1EP					128

Table 2. Analog Options

Feature	Analog Option 1	Analog Option 2
Cranking Mode	Not Characterized or Tested	Fully Characterized and Tested
External Wake-up (PTB3/L0)	No	Yes
External Temperature Sensor Option (VTEMP)	No	Yes
Optional 2nd External Voltage Sense Input (VOPT)	No	Yes

2 Part Identification

This section provides an explanation of the part numbers and their alpha numeric breakdown.

2.1 Description

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

2.2 Format and Examples

Part numbers for a given device have the following format, followed by a device example:
Table 3 _ Part Numbering - Analog EMBEDDED MCU + POWER.

MM 9 cc f xxx r v PPP RR - MM912I637AM2EP

2.3 Fields

These tables list the possible values for each field in the part number (not all combinations are valid).

Table 3. Part Numbering - Analog EMBEDDED MCU + POWER

FIELD	DESCRIPTION	VALUES
MM	Product Category	• MM- Qualified Standard • SM- Custom Device • PM- Prototype Device
9	Memory Type	• 9 = Flash, OTP • Blank = ROM
cc	Micro Core	• 08 = HC08 • 12 = HC12
f	Memory Size	• A 1 k • B 2 k • C 4 k • D 8 k • E 16 k • F 32 k • G 48 k • H 64 k • I 96 k • J 128 k
xxx	Analog Core/Target	• Assigned by Marketing
r	Revision	• (default A)
t	Temperature Range	• I = 0 °C to 85 °C • C = -40 °C to 85 °C • V = -40 °C to 105 °C • M = -40 °C to 125 °C
v	Variation	• (default blank)
PPP	Package Designator	• Assigned by Packaging
RR	Tape and Reel Indicator	

Table of Contents

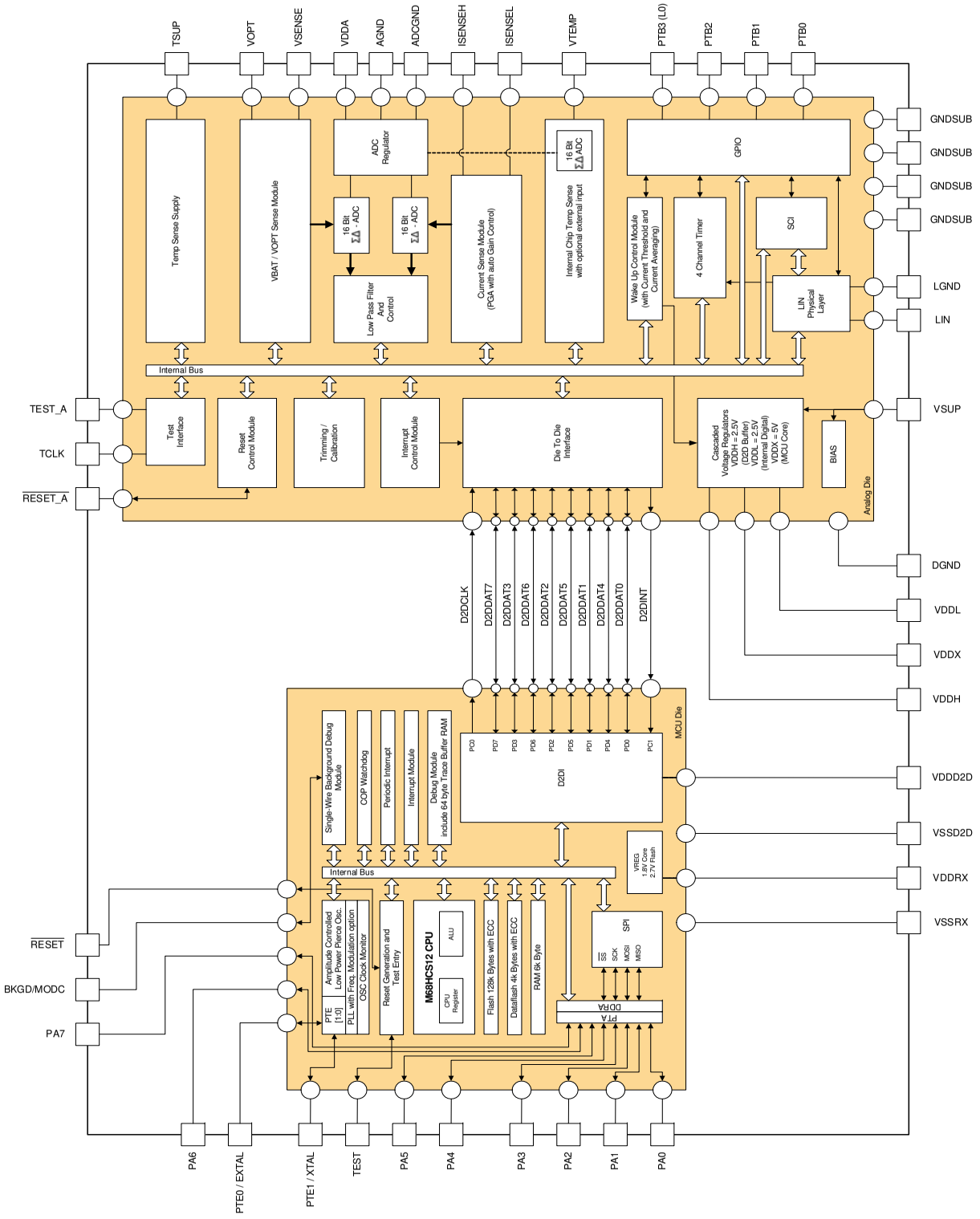


Figure 2. Sample Block Diagram

3 Pin Assignment

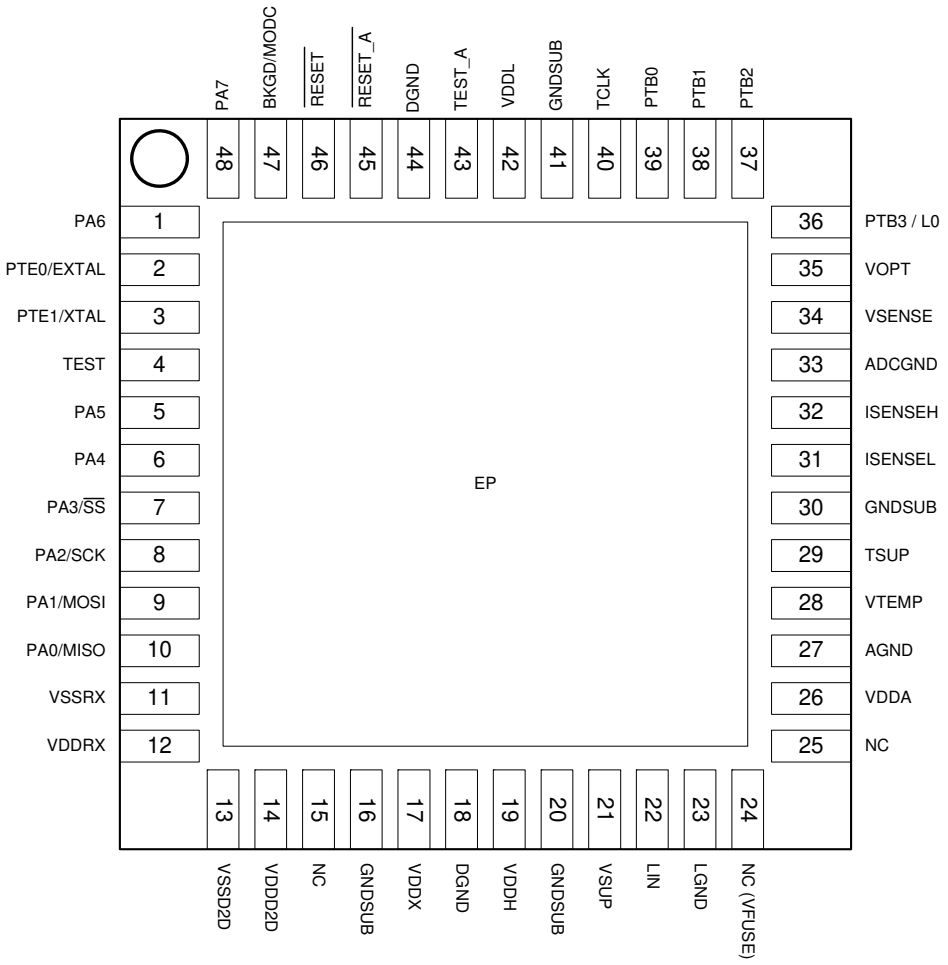


Figure 3. MM912_637 Pin Connections

3.1 MM912_637 Pin Description

The following table gives a brief description of all available pins on the MM912_637 device. Refer to the highlighted chapter for detailed information

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
1	PA6	MCU PA6	General purpose port A input or output pin 6. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
2	PE0/EXTAL	MCU Oscillator	EXTAL in one of the optional crystal/resonator drivers and external clock pins, and the PE0 port may be used as a general purpose I/O. On reset, all the device clocks are derived from the internal reference clock. See Section 5.22, “S12 Clock, Reset, and Power Management Unit (S12CPMU)".

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
3	PE1/XTAL	MCU Oscillator	XTAL is one of the optional crystal/resonator drivers and external clock pins, and the PE1 port may be used as a general purpose I/O. On reset all the device clocks are derived from the internal reference clock. See Section 5.22, “S12 Clock, Reset, and Power Management Unit (S12CPMU)”.
4	TEST	MCU Test	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to VSSRX in user mode.
5	PA5	MCU PA5	General purpose port A input or output pin 5. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)”.
6	PA4	MCU PA4	General purpose port A input or output pin 4. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)”.
7	PA3	MCU PA3 / $\overline{SS}$	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)”.
8	PA2	MCU PA2 / SCK	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)”.
9	PA1	MCU PA1 / MOSI	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)”.
10	PA0	MCU PA0 / MISO	General purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)”.
11	VSSRX	MCU 5.0 V Ground	External ground for the MCU - VDDRX return path.
12	VDDRX	MCU 5.0 V Supply	5.0 V MCU power supply. MCU core- (internal 1.8 V regulator) and flash (internal 2.7 V regulator) supply.
13	VSSD2D	MCU 2.5 V Ground	External ground for the MCU - VDDD2D return path.
14	VDDD2D	MCU 2.5 V Supply	2.5 V MCU power supply. Die to die buffer supply.
15	NC	Not connected	This pin must be grounded in the application.
16	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
17	VDDX	Voltage Regulator Output 5.0 V	5.0 V main voltage regulator output pin. An external capacitor (C_{VDDX}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.
18	DGND	Digital Ground	This pin is the device digital ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.
19	VDDH	Voltage Regulator Output 2.5 V	2.5 V high power main voltage regulator output pin to be connected with the VDDD2D MCU pin. An external capacitor (C_{VDDH}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.
20	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
21	VSUP	Power Supply	This pin is the device power supply pin. A reverse battery protection diode is required. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.
22	LIN	LIN Bus I/O	This pin represents the single-wire bus transmitter and receiver. See Section 5.11, “LIN”.
23	LGND	LIN Ground Pin	This pin is the device LIN ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.
24	NC	Not connected (reserved)	This pin must be grounded in the application.
25	NC	Not connected	This pin must be grounded in the application.
26	VDDA	Analog Voltage Regulator Output	Low power analog voltage regulator output pin, permanently supplies the analog front end. An external capacitor (C_{VDDA}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.
27	AGND	Analog Ground	This pin is the device analog voltage regulator and LP oscillator ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR”.

Table 4. MM912_637 Pin Description

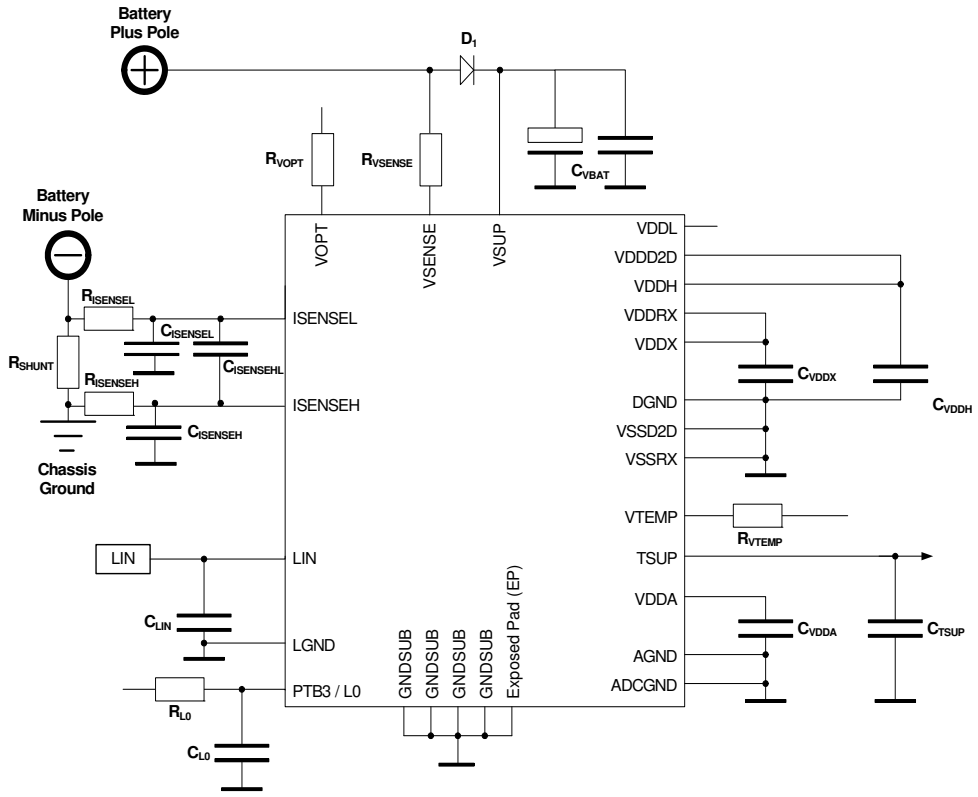
Pin #	Pin Name	Formal Name	Description
28	VTEMP	Temperature Sensor Input	External temperature sensor input. See Section 5.6, “Temperature Measurement - TSENSE".
29	TSUP	Temperature Sensor Supply Output	Supply for the external temperature sensor. TSUP frequency compensation option to allow capacitor CTSUP. See Section 5.6, “Temperature Measurement - TSENSE".
30	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
31	ISENSEL	Current Sense L	Current sense input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 5.4, “Current Measurement - ISENSE".
32	ISENSEH	Current Sense H	Current sense input “high”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. See Section 5.4, “Current Measurement - ISENSE".
33	ADCGND	Analog Digital Converter Ground	Analog digital converter ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
34	VSENSE	Voltage Sense	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection. See Section 5.5, “Voltage Measurement - VSENSE".
35	VOPT	Optional Voltage Sense	Optional voltage measurement input. See Section 5.5, “Voltage Measurement - VSENSE".
36	PTB3 / L0	General Purpose Input 3 - High Voltage Input 0	This is the high voltage general purpose input pin 3, based on VDDX with the following shared functions: • Internal clamping structure to operate as a high voltage input (L0). When used as high voltage input, a series resistor (RL0) and capacitor to GND (C_{L0}) must be used to protect against automotive transients, when used to connect outside the PCB. • 5.0 V (VDDX) digital port input • Selectable internal pull-down resistor • Selectable wake-up input during low power mode. • Selectable timer channel input • Selectable connection to the LIN / SCI (Input only) See Section 5.10, “General Purpose I/O - GPIO".
37	PTB2	General Purpose I/O 2	This is the general purpose I/O pin 2 based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".
38	PTB1	General Purpose I/O 1	This is the general purpose I/O pin 1, based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".
39	PTB0	General Purpose I/O 0	This is the general purpose I/O pin 0 based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
40	TCLK	Test Clock Input	Test mode clock input pin for Test mode only. This pin must be grounded in user mode.
41	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
42	VDDL	Low Power Voltage Regulator Output	2.5 V low power voltage regulator output pin. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
43	TEST_A	Test Mode	Analog die Test mode pin for Test mode only. This pin must be grounded in user mode.
44	DGND	Digital Ground	This pin is the device digital ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
45	$\overline{\text{RESET\_A}}$	Reset I/O	Reset output pin of the analog die. Active low signal with internal pull-up. V_{DDX} based. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
46	$\overline{\text{RESET}}$	MCU Reset	Bidirectional reset I/O pin of the MCU die. Active low signal with internal pull-up. V_{DDRX} based. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
47	BKGD	MCU Background Debug and Mode	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as an MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device. See Section 5.19, “MCU - Debug Module (S12SDBG)".
48	PA7	MCU PA7	General purpose port A input or output pin 7. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".

3.2 Recommended External Components

Figure 4 and Table 5 list the required / recommended / optional external components for the application.



Note: Module GND connected to Battery Minus or Chassis Ground – based on configuration.

Figure 4. Required / Recommended External Components

Table 5. Required / Recommended External Components

Name	Description	Value	Connection	Comment
D_1	Reverse Battery Diode	n.a.	VSUP-VBAT	
C_{VBAT}	Battery Blocking Capacitor	4.7 µF/100 nF	VSUP-GND	Ceramic
R_{VSENSE}	VSENSE Current Limitation	2.2 kΩ	VSENSE-VBAT	
R_{VOPT}	VOPT Current Limitation	2.2 kΩ	VOPT-signal	optional[(1)]
R_{SHUNT}	Current Shunt Resistor	100 µΩ	ISENSEH-ISENSEL	
$R_{ISENSEL}$	EMC Resistor	500 Ω max		select for best EMC performance
$R_{ISENSEH}$	EMC Resistor	500 Ω max		select for best EMC performance
$C_{ISENSEL}$	EMC Capacitor	TBD		select for best EMC performance
$C_{ISENSEHL}$	EMC Capacitor	TBD		select for best EMC performance
$C_{ISENSEH}$	EMC Capacitor	TBD		select for best EMC performance

Table 5. Required / Recommended External Components

Name	Description	Value	Connection	Comment
C_{VDDH}	Blocking Capacitor	1.0 µF	VDDH-GND	
C_{VDDX}	Blocking Capacitor	220 nF	VDDX-GND	
C_{VDDA}	Blocking Capacitor	47 nF	VDDA-GND	
C_{VDDL}	Blocking Capacitor	n.a.	VDDL-GND	not required
C_{LIN}	LIN Bus Filter	n.a.	LIN-LGND	not required
R_{L0}	PTB3 / L0 Current Limitation	47 kΩ	L0	
C_{L0}	PTB3 / L0 ESD Protection	47 nF	L0-GND	
C_{TSUP}	Blocking Capacitor	220 pF	TSUP-GND	not required(2)
R_{VTEMP}	VTEMP Current Limitation	20 kΩ	VTEMP-signal	optional(1)

Notes

1.Required if extended EMC protection is needed

2.If an external temperature sensor is used, EMC compliance may require the addition of CTSUP. In this case the ECAP bit must be set to ensure the stability of the TSUP power supply circuit. See Section 5.6.1.2, “Block Diagram".

3.3 Pin Structure

Table 6 documents the individual pin characteristic.

Table 6. Pin Type / Structure

Pin #	Pin Name	Alternative Pin Function	Power Supply	Structure
1	PA6	n.a.	VDDRX	n.a.
2	PE0	EXTAL	VDDRX	PUPEE / OSCPINS_EN
3	PE1	XTAL	VDDRX	PUPEE / OSCPINS_EN
4	TEST	n.a.	n.a.	n.a.
5	PA5	n.a.	VDDRX	n.a.
6	PA4	n.a.	VDDRX	n.a.
7	PA3	SS	VDDRX	n.a.
8	PA2	SCK	VDDRX	n.a.
9	PA1	MOSI	VDDRX	n.a.
10	PA0	MISO	VDDRX	n.a.
11	VSSRX	n.a.		GND
12	VDDRX	n.a.		
13	VSSD2D	n.a.		GND
14	VDDD2D	n.a.		
15	NC	n.a.		
16	GNDSUB	n.a.		GND
17	VDDX	n.a.	VDDX	
18	DGND	n.a.	GND	B2B-Diode to GNDSUB
19	VDDH	n.a.	VDDH	Negative Clamp Diode, Dynamic ESD (transient protection)
20	GNDSUB	n.a.	GND	GNDSUB
21	VSUP	n.a.	VSUP	Negative Clamp Diode, >42 V ESD
22	LIN	n.a.	VSUP	No Negative Clamping Diode (-40 V), >42 V ESD
23	LGND	n.a.	GND	B2B-Diode to GNDSUB

Table 6. Pin Type / Structure

Pin #	Pin Name	Alternative Pin Function	Power Supply	Structure
24	NC	n.a.	n.a.	Negative Clamp Diode, >15 V ESD
25	NC	n.a.	n.a.	n.a.
26	VDDA	n.a.	VDDA	Negative Clamp Diode, Dynamic ESD (transient protection)
27	AGND	n.a.	GND	B2B-Diode to GNDSUB
28	VTEMP		VDDA	Negative Clamp Diode, >6.0 V ESD
29	TSUP		TSUP	Negative Clamp Diode, Dynamic ESD (transient protection)
30	GNDSUB		GND	GND
31	ISENSEL		n.a.	Negative Clamp Diode, 2nd Clamp Diode to VDDA
32	ISENSEH		n.a.	Negative Clamp Diode, 2nd Clamp Diode to VDDA
33	ADCGND		GND	B2B-Diode to GNDSUB
34	VSENSE		n.a.	No Negative Clamping Diode (-40 V), >42 V ESD
35	VOPT		n.a.	No Negative Clamping Diode (-40 V), >42 V ESD
36	PTB3 / L0		VDDRX	Negative Clamp Diode, >6.0 V ESD
37	PTB2		VDDRX	Negative Clamp, Dynamic 5.5 V ESD
38	PTB1		VDDRX	Negative Clamp, Dynamic 5.5 V ESD
39	PTB0		VDDRX	Negative Clamp, Dynamic 5.5 V ESD
40	TCLK		VDDRX	Negative Clamp, Dynamic 5.5 V ESD
41	GNDSUB		GND	GND
42	VDDL		VDDL	Negative Clamp Diode, Dynamic ESD (transient protection)
43	TEST_A		VDDRX	Negative Clamp, positive 10 V Clamp
44	DGND		GND	B2B-Diode to GNDSUB
45	$\overline{\text{RESET\_A}}$		VDDRX	Negative Clamp, positive 10 V Clamp
46	$\overline{\text{RESET}}$		VDDRX	Pull-up
47	BKGD	MODC	VDDRX	BKPUE
48	PA7		VDDRX	n.a.

4 Electrical Characteristics

4.1 General

This section contains electrical information for the microcontroller, as well as the MM912_637 analog die.

4.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside these maximums is not guaranteed. Stress beyond these limits may affect the reliability, or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level. All voltages are with respect to ground, unless otherwise noted.

Table 7. Absolute Maximum Electrical Ratings - Analog Die

Ratings	Symbol	Value	Unit
VSUP pin voltage	V_{VSUP}	-0.3 to 42	V
VSENSE pin voltage[3]	V_{VSENSE}	-16 to 42	V
VOPT pin voltage	V_{VOPT}	-16 to 42	V
VTEMP pin voltage	V_{VTEMP}	-0.3 to V_{DDA}+0.25	V
ISENSEH and ISENSEL pin voltage	V_{ISENSE}	-0.5 to V_{DDA}+0.25	V
ISENSEH and ISENSEL pin current	I_{ISENSE}	-1 to 1	mA
LIN pin voltage	V_{BUS}	-33 to 42	V
LIN pin current (internally limited)	I_{BUSLIM}	on page 18	mA
L0 pin voltage with R_{PTB3}	V_{PTB3}	-0.3 to 42 max.	V
Input / Output pins PTB[0:2] voltage	V_{PTB0-2}	-0.3 to V_{DDX}+0.5	V
Pin voltage at VDDX	V_{DDX}	-0.3 to 5.75	V
Pin voltage at VDDH	V_{DDH}	-0.3 to 2.75	V
VDDH output current	I_{VDDH}	internally limited	A
VDDX output current	I_{VDDX}	internally limited	A
TCLK pin voltage	V_{TCLK}	-0.3 to V_{DDX}+0.5	V
$\overline{\text{RESET\_A}}$ pin voltage	V_{IN}	-0.3 to V_{DDX}+0.5	V

Notes

3.It has to be assured by the application circuit that these limits will not be exceeded, e.g. by ISO pulse 1.

Table 8. Maximum Electrical Ratings - MCU Die

Ratings	Symbol	Value	Unit
5.0 V supply voltage	V_{DDRX}	-0.3 to 6.0	V
2.5 V supply voltage	V_{DDD2D}	-0.3 to 3.6	V
Digital I/O input voltage (PTA0...7)	V_{IN}	-0.3 to 6.0	V
EXTAL, XTAL	V_{IN}	-0.3 to 2.16	V
Instantaneous maximum current single pin limit for all digital I/O pins[4]	I_D	-25 to 25	mA
Instantaneous maximum current single pin limit for EXTAL, XTAL	I_{DL}	-25 to 25	mA

Notes

4.All digital I/O pins are internally clamped to V_{SSRX} and V_{DDRX}.

Table 9. Maximum Thermal Ratings

Ratings	Symbol	Value	Unit
Storage temperature	T_{STG}	-55 to 150	°C
Package thermal resistance [5]	$R_{\theta JA}$	25 typ.	°C/W

Notes
5.$R_{\theta JA}$ value is derived using a JEDEC 2s2p test board

4.3 Operating Conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

Table 10. Operating Conditions

Ratings	Symbol	Value	Unit
Functional operating supply voltage - Device is fully functional. All features are operating.	V_{SUP}	3.5 to 28	V
Extended range for RAM Content is guaranteed. Other device functionary is limited. With cranking mode enabled (see Section 5.2.3.4, "Low Voltage Operation - Cranking Mode Device Option").	V_{SUPL}	2.5 to 3.5	V
Functional operating VSENSE voltage [6]	V_{SENSE}	0 to 28	V
Functional operating VOPT voltage	V_{OPT}	0 to 28	V
External temperature sense input - VTEMP	V_{TEMP}	0 to 1.25	V
LIN output voltage range	V_{VSUP_LIN}	7 to 18	V
ISENSEH / ISENSEL terminal voltage	V_{ISENSE}	-0.5 to 0.5	V
MCU 5.0 V supply voltage	V_{DDRX}	3.13 to 5.5	V
MCU 2.5 V supply voltage	V_{DDD2D}	2.25 to 3.6	V
MCU oscillator	f_{OSC}	4 to 16	MHz
MCU bus frequency	f_{BUS}	max. 32.768	MHz
Operating ambient temperature	T_A	-40 to 125	°C
Operating junction temperature - analog die	T_{J_A}	-40 to 150	°C
Operating junction temperature - MCU die	T_{J_M}	-40 to 150	°C

Notes
6.Values V_{SENSE} > 28 V are flagged in the VSENSE

4.4 Supply Currents

This section describes the current consumption characteristics of the device, as well as the conditions for the measurements.

4.4.1 Measurement Conditions

All measurements are without output loads. The currents are measured in MCU special single chip mode, and the CPU code is executed from RAM, unless otherwise noted.

For Run and Wait current measurements, PLL is on and the reference clock is the IRC1M, trimmed to 1.024 MHz. The bus frequency is 32.768 MHz and the CPU frequency is 65.536 MHz. Table 11 and Table 12 show the configuration of the CPMU module for Run, Wait, and Stop current measurements. Table 13 shows the configuration of the peripherals for run current measurements

Table 11. CPUM Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]=01,SYNDIV[5:0] = 32.768 MHz
CPMUPOSTDIV	POSTDIV[4:0]=0,
CPMUCLKS	PLLSEL=1
CPMUOSC	OSCE=0, Reference clock for PLL is $f_{REF}=f_{IRC1M}$ trimmed to 1.024 MHz

Table 12. CPMU Configuration for Pseudo Stop Current Measurements

CPMU REGISTER	Bit settings/Conditions
CPMUCLKS	PLLSEL=0, PSTP=1, PRE=PCE=RTIOSCSEL=COPOSCSEL=1
CPMUOSC	OSCE=1, External square wave on EXTAL f_{EXTAL}=16 MHz, V_{IH}= 1.8 V, V_{IL}=0 V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table 13. MCU Peripheral Configurations for Run Supply Current Measurements

Peripheral	Configuration
SPI	configured to master mode, continuously transmit data (0x55 or 0xAA) at 1.0 Mbit/s
D2DI	continuously transmit data (0x55 or 0xAA)
COP	COP Watchdog Rate 2^{24}
RTI	enabled, RTI Control Register (RTICTL) set to $FF
DBG	The module is enabled and the comparators are configured to trigger in outside range. The range covers all the code executed by the core.

Table 14. Analog Die Configurations for Normal Mode Supply Current Measurements

Peripheral	Configuration
D2D	maximum frequency
LIN	enabled, recessive state
TIMER	enabled
LTC	enabled
Channels	Current, voltage, and temperature measurement enabled, LPF and Auto Gain enabled

Table 15. Supply Currents[7]

Ratings	Symbol	Min	Typ.[8]	Max	Unit
MM912_637 COMBINED CONSUMPTION					
Normal mode current both dice.	I_{RUN}		25	35	mA
ANALOG DIE CONTRIBUTION - EXCLUDING MCU AND EXTERNAL LOAD CURRENT, (3.5 V ≤ V_{SUP} ≤ 28 V; -40 °C ≤ T_A ≤ 125 °C)					
Normal mode current measured at V_{SUP}	I_{NORMAL}		1.5	4.0	mA
Stop mode current measured at V_{SUP} Continuous base current[9] Stop current during cranking mode Current adder during current trigger event - (typ. 10 ms duration[10], temperature measurement = OFF)	I_{STOP}		 75 107 1500	 100 130 1750	µA
Sleep mode measured at V_{SUP} Continuous base current[9] Current adder during current trigger event - (typ. 10 ms duration[10], temperature measurement = OFF)	I_{SLEEP}		 52 1500	 85 1750	µA
MCU DIE CONTRIBUTION, V_{DDRX} = 5.5 V					
Run Current, T_A = 125 °C	I_{RUN}		13.5	18.8	mA
Wait current, T_A = 125 °C	I_{WAIT}		7.0	8.8	mA
Stop current T_A = 125 °C T_A = 25 °C T_A = -40 °C	I_{STP}		 90 25 15	 200 40 25	µA
Pseudo stop current, RTI and COP enabled T_A = 150 °C T_A = 25 °C T_A = -40 °C	I_{STP}		 450 350 330	 520 500 410	µA

Notes

7. See Table 11, Table 12, Table 13, and Table 14 for conditions. Currents measured in Test mode with external loads (100 pF) and the external clock at 64 MHz.
8. Typical values noted reflect the approximate parameter mean at T_A = 25 °C.
9. From V_{SUP} 6.0 to 28 V
10. Duration based on channel configuration. 10ms typical for Decimation Factor = 512, Chopper = ON.

4.5 Static Electrical Characteristics

All characteristics noted under conditions 3.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

4.5.1 Static Electrical Characteristics Analog Die

Table 16. Static Electrical Characteristics - Power Supply

Ratings	Symbol	Min	Typ	Max	Unit
Low Voltage Reset L (POR) Assert (measured on VDDL) Cranking Mode Disabled	V_{PORL}	 1.75	 1.9	 2.1	V
Low Voltage Reset L (POR) Deassert (measured on VDDL) Cranking Mode Disabled	V_{PORH}	 1.85	 2.1	 2.35	V

Table 16. Static Electrical Characteristics - Power Supply

Ratings	Symbol	Min	Typ	Max	Unit
Low Voltage Reset L (POR) Assert (measured on VDDL) Cranking Mode Enabled[11]	V_{PORCL}	1.0	1.3	1.7	V
Low Voltage Reset A (LVRA) Assert (measured on VDDA)	V_{LVRAL}	1.9	2.05	2.2	V
Low Voltage Reset A (LVRA) Deassert (measured on VDDA)	V_{LVRAH}	2.0	2.15	2.3	V
Low Voltage Reset X (LVRX) Assert (measured on VDDX)	V_{LVRXL}	2.5	2.75	3.0	V
Low Voltage Reset X (LVRX) Deassert (measured on VDDX)	V_{LVRXH}	2.7	2.95	3.25	V
Low Voltage Reset H (LVRH) Assert (measured on VDDH)	V_{LVRHL}	1.95	2.075	2.2	V
Low Voltage Reset H (LVRH) Deassert (measured on VDDH)	V_{LVRHH}	2.05	2.175	2.3	V
Under-voltage Interrupt (UVI) Assert (measured on VSUP), Cranking Mode Disabled	V_{UVIL}	4.65	5.2	6.1	V
Under-voltage Interrupt (UVI) Deassert (measured on VSUP), Cranking Mode Disabled	V_{UVIH}	4.9	5.4	6.2	V
Under-voltage Cranking Interrupt (UVI) Assert (measured on VSUP) Cranking Mode Enabled	V_{UVCIL}	3.4	3.6	4.0	V
Under-voltage Cranking Interrupt (UVI) Deassert (measured on VSUP) Cranking Mode Enabled	V_{UVCIH}	3.5	3.8	4.1	V
VSENSE/VOPT High Voltage Warning Threshold Assert[12]	V_{TH}		28		V

Notes

11.Deassert with Cranking off = V_{PORH}

12.5.0 V < V_{SUP} < 28 V, Digital Threshold at the end of channel chain (incl. compensation)

Table 17. Static Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Low-state Output Voltage I_{OUT} = 2.0 mA	V_{OL}			0.8	V
Pull-up Resistor	R_{RPU}	25		50	kOhm
Low-state Input Voltage	V_{IL}			$0.3V_{DDX}$	V
High-state Input Voltage	V_{IH}	$0.7V_{DDX}$			V
Reset Release Voltage (VDDX)	V_{RSTRV}	0	0.02	1.0	V
RESET_A pin Current Limitation	I_{LIMRST}			10	mA

Table 18. Static Electrical Characteristics - Voltage Regulator Outputs

Ratings	Symbol	Min	Typ	Max	Unit
Analog Voltage Regulator - VDDA[13]					
Output Voltage 1.0 mA ≤ I_{VDDA} ≤ 1.5 mA	V_{DDA}	2.25	2.5	2.75	V
Output Current Limitation	I_{VDDA}			10	mA
Low Power Digital Voltage Regulator - VDDL[13]					
Output Voltage	V_{DDL}	2.25	2.5	2.75	V
High Power Digital Voltage Regulator - VDDH[14]					
Output Voltage 1.0 mA ≤ I_{VDDH} ≤ 30 mA	V_{DDH}	2.4	2.5	2.75	V
Output Current Limitation	I_{VDDH}			65	mA
5.0 V Voltage Regulator - VDDX[14]					
Output Voltage 1.0 mA ≤ I_{VDDX} ≤ 30 mA	V_{DDX}	3.15	5.0	5.9	V
Output Current Limitation	I_{VDDX}	45	60	80	mA

Notes

13.No additional current must be taken from those outputs.

14.The specified current ranges does include the current for the MCU die. No external loads recommended.

Table 19. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor R_{SLAVE}; Driver OFF; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0			mA
Input Leakage Current at the Receiver incl. Pull-up Resistor R_{SLAVE}; Driver OFF; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$			20	µA
Input Leakage Current; GND Disconnected; GND_{DEVICE} = V_{SUP}; 0 < V_{BUS} < 18 V; V_{BAT} = 12 V	$I_{BUS\_NO\_GND}$	-1.0		1.0	mA
Input Leakage Current; V_{BAT} disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V	$I_{BUS\_NO\_BAT}$			100	µA
Receiver Input Voltage; Receiver Dominant State	V_{BUSDOM}			0.4	V_{SUP}
Receiver Input Voltage; Receiver Recessive State	V_{BUSREC}	0.6			V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{BUS_HYS}			0.175	V_{SUP}
Voltage Drop at the serial Diode	D_{SER_INT}	0.3	0.7	1.0	V
LIN Pull-up Resistor	R_{SLAVE}	20	30	60	kOhm
Low Level Output Voltage, I_{BUS}=40 mA	V_{DOM}			0.3	V_{SUP}
High Level Output Voltage, I_{BUS}=-10 µA, R_L=33 kOhm	V_{REC}	VSUP-1			V
J2602 Detection Deassert Threshold for VSUP level	V_{J2602H}	5.9	6.3	6.7	V
J2602 Detection Assert Threshold for VSUP level	V_{J2602L}	5.8	6.2	6.6	V
J2602 Detection Hysteresis	$V_{J2602HYS}$	70	190	250	mV
BUS Wake-up Threshold	V_{LINWUP}	4.0	5.25	6.0	V

Table 20. Static Electrical Characteristics - High Voltage Input - PTB3 / L0

Ratings	Symbol	Min	Typ	Max	Unit
Wake-up Threshold - Rising Edge	V_{WTHR}	1.3	2.6	3.4	V
Input High Voltage (digital Input)	V_{IH}	$0.7V_{DDX}$		V_{DDX}+0.3	V
Input Low Voltage (digital Input)	V_{IL}	V_{SS}-0.3		$0.35V_{DDX}$	V
Input Hysteresis	V_{HYS}	50	140	200	mV
Internal Clamp Voltage	V_{L0CLMP}	4.9	6.0	7.0	V
Input Current PTB3 / L0 (V_{IN} = 42 V; R_{L0}=47 kOhm)	I_{IN}			1.1	mA
Internal pull-down resistance[15]	R_{PD}	50	100	200	kOhm
PTB3 / L0 Series Resistor	R_{PTB3}	42.3	47	51.7	kOhm
PTB3 / L0 Capacitor	C_{L0}	42.3	47	51.7	nF

Notes
15.Disabled by default.

Table 21. Static Electrical Characteristics - General Purpose I/O - PTB[0...2]

Ratings	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	$0.7V_{DDX}$		V_{DDX}+0.3	V
Input Low Voltage	V_{IL}	V_{SS}-0.3		$0.35V_{DDX}$	V
Input Hysteresis	V_{HYS}	50	140	200	mV
Input Leakage Current (pins in high-impedance input mode) (V_{IN} = V_{DDX} or V_{SSX})	I_{IN}	-1.0		1.0	µA
Output High Voltage (pins in output mode) Full drive I_{OH} = –5.0 mA	V_{OH}	V_{DDX}-0.8			V
Output Low Voltage (pins in output mode) Full drive I_{OL} = 5.0 mA	V_{OL}			0.8	V
Internal Pull-up Resistance (V_{IH} min. > Input voltage > V_{IL} max)[16]	R_{PUL}	25	37.5	50	kOhm
Input Capacitance	C_{IN}		6.0		pF
Maximum Current All PTB Combined[17]	I_{BMAX}	-17		17	mA
Output Drive strength at 10 MHz	C_{OUT}			100	pF

Notes
16.Disabled by default.
17.Overall VDDR Regulator capability to be considered.

Table 22. Static Electrical Characteristics - Current Sense Module[18]

Ratings	Symbol	Min	Typ	Max	Unit
Gain Error with temperature based gain compensation adjustment[19], [20] with default gain compensation	$I_{GAINERR}$	 -0.5 -1.0	 +/-0.1	 0.5 1.0	%
Offset Error[21], [22]	$I_{OFFSETERR}$			0.5	µV
Resolution	I_{RES}		0.1		µV
ISENSEH, ISENSEL terminal voltage differential signal voltage range	 V_{INC} V_{IND}	 -300 -200		 300 200	mV
Differential Leakage Current: differential voltage between ISENSEH/ ISENSEL, ≤200 mV	I_{SENSE_DLC}	-2.0		2.0	nA
Wake-up Current Threshold Resolution	$I_{RESWAKE}$		0.2		µV
Resistor Threshold for OPEN Detection	R_{OPEN}	0.8	1.25	1.8	MOhm

Notes
18.3.5 V ≤ V_{SUP} ≤ 28 V, after applying default trimming values - see Section 6, “MM912_637 - Trimming".
19.Gain Compensation adjustment on calibration request interrupt with TCALSTEP
20.±0.65%, including lifetime drift for gain 256 and 512
21.Chopper Mode = ON, Gain with automatic gain control enabled
22.Parameter not tested. Guaranteed by design and characterization

Table 23. Static Electrical Characteristics - Voltage Sense Module[23]

Ratings	Symbol	Min	Typ	Max	Unit
Gain Error[24] 18 V < V_{IN} ≤ 28 V 3.5 V ≤ V_{IN} ≤ 18 V 3.5 V ≤ V_{IN} < 5.0 V[25] 5.0 V ≤ V_{IN} ≤ 18 V[25],[27]	$V_{GAINERR}$	 -0.5 -0.4 -0.25 -0.15	 0.1 0.1 0.1 0.1	 0.5 0.4 0.25 0.15	%
Offset Error[26],[28]	$V_{OFFSETERR}$	-1.5		1.5	mV
Resolution with R_{VSENSE} = 2.2 kOhm	V_{RES}			0.5	mV

Notes
23.3.5 V ≤ V_{SUP} ≤ 28 V, after applying default trimming values - see Section 6, “MM912_637 - Trimming".
24.Including resistor mismatch drift
25.Gain Compensation adjustment on calibration request interrupt with TCALSTEP
26.Chopper Mode = ON.
27.±0.2%, including lifetime drift
28.Parameter not tested. Guaranteed by design and characterization.

Table 24. Static Electrical Characteristics - Temperature Sense Module[29]

Ratings	Symbol	Min	Typ	Max	Unit
Measurement Range	T_{RANGE}	-40		150	°C
Accuracy -40 °C ≤ T_A ≤ 60 °C[30] -40 °C ≤ T_A ≤ 150 °C	T_{ACC}	 -2.0 -3.0		 2.0 3.0	K
Resolution	T_{RES}		8.0		mK
TSUP Voltage Output, 10 µA ≤ I_{TSUP} ≤ 100 µA	V_{TSUP}	1.1875	1.25	1.3125	V
TSUP Capacitor with ECAP = 1	C_{TSUP}	209	220	231	pF

Table 24. Static Electrical Characteristics - Temperature Sense Module[29]

Ratings	Symbol	Min	Typ	Max	Unit
Max Calibration Request Interrupt Temperature Step	$T_{CALSTEP}$	-25		25	K

Notes

29.3.5 V ≤ V_{SUP} ≤ 28 V, after applying default trimming values - see Section 6, “MM912_637 - Trimming".

30.Temperature not tested in production. Guaranteed by design and characterization.

4.5.2 Static Electrical Characteristics MCU Die

Table 25. Static Electrical Characteristics - MCU

Ratings	Symbol	Min	Typ	Max	Unit
Power On Reset Assert (measured on VDDRX)	V_{PORA}	0.6	0.9	-	V
Power On Reset Deassert (measured on VDDRX)	V_{PORD}	-	0.95	1.6	V
Low Voltage Reset Assert (measured on VDDD2D)	V_{LVRA}	2.97	3.06	-	V
Low Voltage Reset Deassert (measured on VDDD2D)	V_{LVRD}	-	3.09	3.3	V
Low Voltage Interrupt Assert (measured on VDDD2D)	V_{LVIA}	4.06	4.21	4.36	V
Low Voltage Interrupt Deassert (measured on VDDD2D)	V_{LVID}	4.19	4.34	4.49	V

Table 26. Static Electrical Characteristics - Oscillator (OSCLCP)

Ratings	Symbol	Min	Typ	Max	Unit
Startup Current	i_{OSC}	100			µA
Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7.0		pF
EXTAL Pin Input Hysteresis	$V_{HYS,EXTAL}$	—	180	—	mV
EXTAL Pin oscillation amplitude (loop controlled Pierce)	$V_{PP,EXTAL}$	—	0.9	—	V

Table 27. 5.0 V I/O Characteristics for all I/O pins except EXTAL, XTAL, TEST, D2DI, and supply pins (4.5 V < V_{DDRX} < 5.5 V; T_J: –40 °C to +150 °C, unless otherwise noted)

Ratings	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	0.65*V_{DDRX}	—	—	V
Input High Voltage	V_{IH}	—	—	V_{DDRX}+0.3	V
Input Low Voltage	V_{IL}	—	—	0.35*V_{DDRX}	V
Input Low Voltage	V_{IL}	V_{SSRX}–0.3	—	—	V
Input Hysteresis	V_{HYS}		250	—	mV
Input Leakage Current (pins in high-impedance input mode)[31] V_{IN} = V_{DDRX} or V_{SSRX}	I_{IN}	–1.00	—	1.00	µA

Table 27. 5.0 V I/O Characteristics for all I/O pins except EXTAL, XTAL, TEST, D2DI, and supply pins (4.5 V < V_{DDRX} < 5.5 V; T_J: –40 °C to +150 °C, unless otherwise noted)

Ratings	Symbol	Min	Typ	Max	Unit
Input Leakage Current (pins in high-impedance input mode)[32] V_{IN} = V_{DDX} or V_{SSX} T_A = –40 °C T_A = 25 °C T_A = 70 °C T_A = 85 °C T_A = 105 °C T_A = 110 °C T_A = 120 °C T_A = 125 °C T_A = 130 °C T_A = 150 °C	I_{IN}		 ±1.0 ±1.0 ±8.0 ±14 ±26 ±32 ±40 ±60 ±74 ±92 ±240		nA
Output High Voltage (pins in output mode), I_{OH} = –4.0 mA	V_{OH}	V_{DDRX} – 0.8	—	—	V
Output Low Voltage (pins in output mode), I_{OL} = 4.0 mA	V_{OL}	—	—	0.8	V
Internal Pull-up Current, V_{IH} min > input voltage > V_{IL} max	I_{PUL}	-10	—	-130	µA
Internal Pull-down Current, V_{IH} min > input voltage > V_{IL} max	I_{PDH}	10	—	130	µA
Input Capacitance	C_{in}	—	7	—	pF
Injection Current[33] Single pin limit Total device Limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	 — 	 2.5 25	 mA

Notes

31. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8.0 °C to 12 °C in the temperature range from 50 °C to 125 °C.
32. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8.0 °C to 12 °C in the temperature range from 50 °C to 125 °C.
33. Refer to Section 4.5.2.1, “Current Injection" for more details

4.5.2.1 Current Injection

The power supply must maintain regulation within the V_{DDX} operating range during instantaneous and operating maximum current conditions. If positive injection current (V_{IN} > V_{DDX}) is greater than I_{DDX}, the injection current may flow out of VDDX and could result in the external power supply going out of regulation. Ensure that the external V_{DDX} load will shunt current greater than the maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if the clock rate is very low, which would reduce overall power consumption.

4.6 Dynamic Electrical Characteristics

Dynamic characteristics noted under conditions 3.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

4.6.1 Dynamic Electrical Characteristics Analog Die

Table 28. Dynamic Electrical Characteristics - Modes of Operation

Ratings	Symbol	Min	Typ	Max	Unit
Low Power Oscillator Frequency	f_{OSCL}	—	512	—	kHz
Low Power Oscillator Tolerance over full temperature range	f_{TOL_A}				
Analog Option 2		-4.0	—	4.0	%
Analog Option 1		-5.0	—	5.0	
Low Power Oscillator Tolerance - synchronized ALFCLK[34]	f_{TOLC_A}				
ALF clock cycle = 1.0 ms		f_{TOL}-0.2	f_{TOL}	f_{TOL}+0.2	%
ALF clock cycle = 2.0 ms		f_{TOL}-0.1		f_{TOL}+0.1	
ALF clock cycle = 4.0 ms		f_{TOL}-0.05		f_{TOL}+0.05	
ALF clock cycle = 8.0 ms		f_{TOL}-0.025		f_{TOL}+0.025	

Notes
34.Parameter not tested. Guaranteed by design and characterization.

Table 29. Dynamic Electrical Characteristics - Die to Die Interface - D2D

Ratings	Symbol	Min	Typ	Max	Unit
Operating Frequency (D2DCLK, D2D[0:3])	f_{D2D}	—	—	32.768	MHz

Table 30. Dynamic Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Reset Deglitch Filter Time	t_{RSTDF}	1.0	2.0	3.2	µs
Reset Release Time for WDR and HWR	t_{RSTRT}	—	32	—	µs

Table 31. Dynamic Electrical Characteristics - Wake-up / Cyclic Sense

Ratings	Symbol	Min	Typ	Max	Unit
Cyclic Wake-up Time[35]	t_{WAKEUP}	ALFCLK	—	TIM4CH	ms
Cyclic Current Measurement Step Width[36]	t_{STEP}	ALFCLK	—	16Bit	ms

Notes
35.Cyclic wake-up on ALFCLK clock based 16 Bit TIMER with maximum 128x prescaler (min 1x)
36.Cyclic wake-up on ALFCLK clock with 16 Bit programmable counter

Table 32. Dynamic Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Initial Non-window Watchdog Timeout	t_{IWDTO}	see Figure 2			ms

Table 33. Dynamic Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Bus Wake-up Deglitcher (Sleep and Stop Mode)	t_{PROPWL}	60	80	100	µs
Fast Bit Rate (Programming Mode)	BR_{FAST}	—	—	100	kBit/s
Propagation delay of receiver	t_{RX_PD}	—	—	6.0	µs
Symmetry of receiver propagation delay rising edge w.r.t. falling edge	t_{RX_SYM}	-2.0	—	2.0	µs
LIN DRIVER - 20.0 KBIT/S; BUS LOAD CONDITIONS (C_{BUS}; R_{BUS}): 1.0 NF; 1.0 KΩ / 6,8 NF;660 Ω / 10 NF;500 Ω					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7.0 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 50 µs; D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT})	D1	0.396	—	—	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 x V_{SUP} $TH_{DOM(MIN)}$ = 0.284 x V_{SUP} 7.6 V ≤ V_{SUP} ≤ 18 V; t_{Bit} = 50 µs D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D2	—	—	0.581	
LIN DRIVER - 10.0 KBIT/S; BUS LOAD CONDITIONS (C_{BUS}; R_{BUS}): 1.0 NF; 1.0 KΩ / 6,8 NF;660 Ω / 10 NF;500 Ω					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7.0 V ≤ V_{SUP} ≤ 18 V; t_{Bit} = 96 µs D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT})	D3	0.417	—	—	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D4	—	—	0.590	
LIN Transmitter Timing, (V_{SUP} from 7.0 to 18 V) - See Figure 5					
Transmitter Symmetry t_{TRAN_SYM} < MAX(ttran_sym60%, t_{TRAN_SYM}40%) t_{TRAN_SYM}60% = t_{TRAN_PDF}60% - t_{TRAN_PDR}60% t_{TRAN_SYM}40% = t_{TRAN_PDF}40% - t_{TRAN_PDR}40%	t_{TRAN_SYM}	-7.25	0	7.25	µs

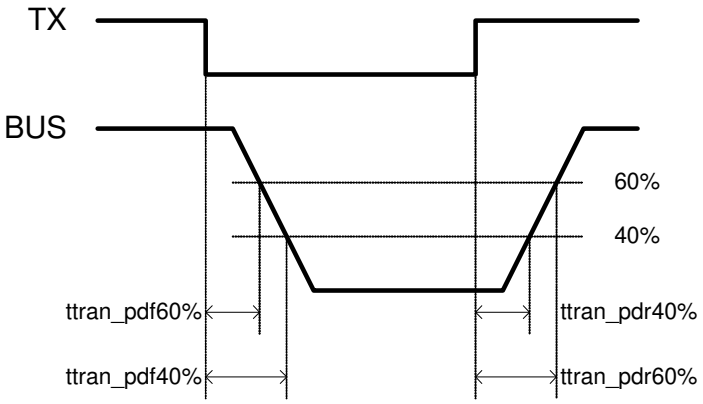


Figure 5. LIN Transmitter Timing

Table 34. Dynamic Electrical Characteristics - General Purpose I/O - PTB3 / L0]

Ratings	Symbol	Min	Typ	Max	Unit
Wake-up Glitch Filter Time	t_{WUPF}		20		µs

Table 35. Dynamic Electrical Characteristics - General Purpose I/O - PTB[0...2]

Ratings	Symbol	Min	Typ	Max	Unit
GPIO Digital Frequency	f_{PTB}			10	MHz
Propagation Delay - Rising Edge[37]	t_{PDr}			20	ns
Rise Time - Rising Edge[37]	t_{RISE}			17.5	ns
Propagation Delay - Falling Edge[37]	t_{PDf}			20	ns
Rise Time - Falling Edge[37]	t_{FALL}			17.5	ns

Notes
37.Load PTBx = 100 pF

Table 36. Dynamic Electrical Characteristics - Current Sense Module

Ratings	Symbol	Min	Typ	Max	Unit
Frequency Attenuation[38],[39] <100 Hz (f_{PASS}) >500 Hz (f_{STOP})		 40		 3.0	dB
Signal Update Rate[40]	$f_{IUPDATE}$	0.5		8.0	kHz
Signal Path Match with Voltage Channel	$f_{IVMATCH}$		2.0		µs
Gain Change Duration (Automatic GCB active)[41]	t_{GC}			14	µs

Notes
38.Characteristics identical to Voltage Sense Module
39.With default LPF coefficients
40.After passing decimation filter
41.Parameter not tested. Guaranteed by design and characterization.

Table 37. Dynamic Electrical Characteristics - Voltage Sense Module

Ratings	Symbol	Min	Typ	Max	Unit
Frequency attenuation[42],[43] 95...105 Hz (f_{PASS}) >500 Hz (f_{STOP})		 40		 3.0	dB
Signal update rate[44]	$f_{VUPDATE}$	0.5		8.0	kHz
Signal path match with Current Channel[45]	$f_{IVMATCH}$		2.0		µs

Notes
42.Characteristics identical to Voltage Sense Module
43.With default LPF coefficients
44.After passing decimation filter
45.Parameter not tested. Guaranteed by design and characterization.