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Document Number: MM9Z1_638D1
Rev. 4.0, 10/2016

Intelligent battery sensor with CAN and LIN

The MM9Z1_638 is a fully integrated intelligent battery monitoring system. The device supports precise current measurement via an external shunt resistor. It features four voltage measurements via internal calibrated resistor dividers or external dividers. It includes an internal temperature sensor, allowing close proximity battery temperature measurements, plus four external temperature sensor inputs.

The MM9Z1_638 features the LIN 2.2 protocol and physical interface, as well as an msCAN protocol controller, for interfacing to automotive buses. The MM9Z1_638 is able to supply and control external CAN interfaces.

This device is powered by SMARTMOS technology.

MM9Z1_638

BATTERY MONITORING SYSTEM

EP SUFFIX (WF-TYPE)
98ASA00343D
48-PIN QFN

Features

- Wide range battery current measurement; On-chip temperature measurement
- Four battery voltage measurements with internal resistor dividers, and up to five direct voltage measurements for use with an external resistor divider
- Measurement synchronization between voltage channels and current channels
- Five external temperature sensor inputs with internal supply for external sensors
- Low-power modes with low-current operation
- Multiple wake-up sources: LIN, timer, high-voltage input, external CAN interface, and current threshold and integration
- Precision internal oscillator and connections for external crystal
- LIN 2.2/ 2.1/ 2.0 protocol and physical interface
- msCAN protocol controller, and supply capability for 8 and 14 pin CAN interfaces
- MM9Z1_638: S12Z microcontroller with 96/128 kByte Flash, 8.0 kByte RAM, 4.0 kByte EEPROM

Applications

- 12 V lead-acid battery monitoring
- Multi-cell battery (Li-ion) monitoring
- HV battery pack sensor
- Truck battery monitoring

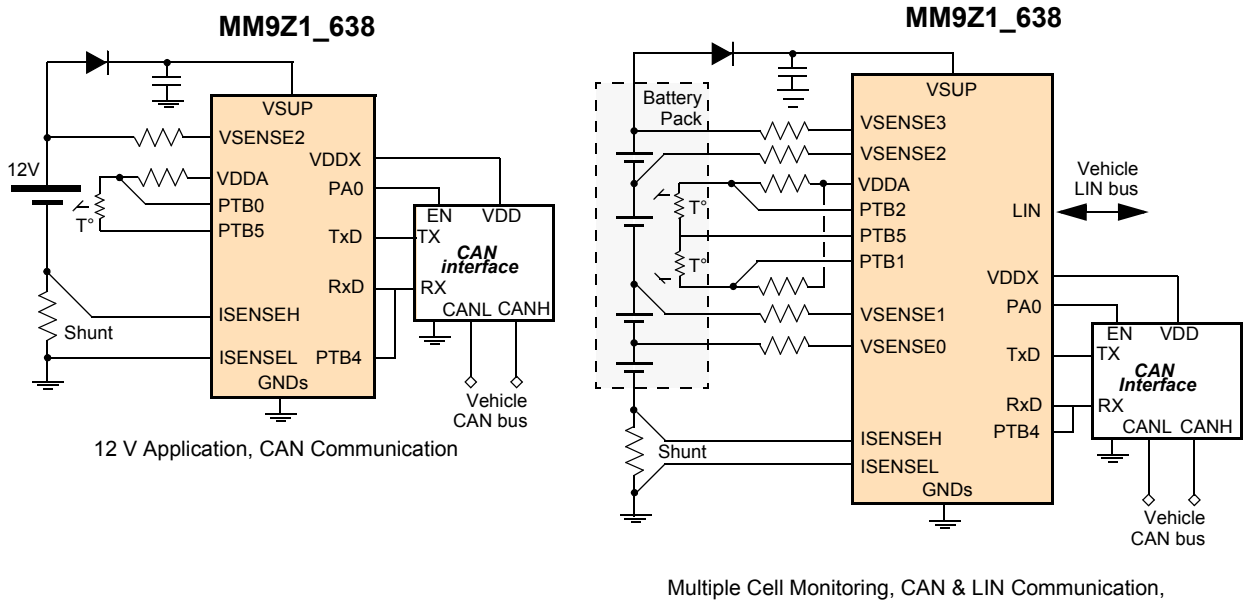

Figure 1. 12 V simplified application diagrams

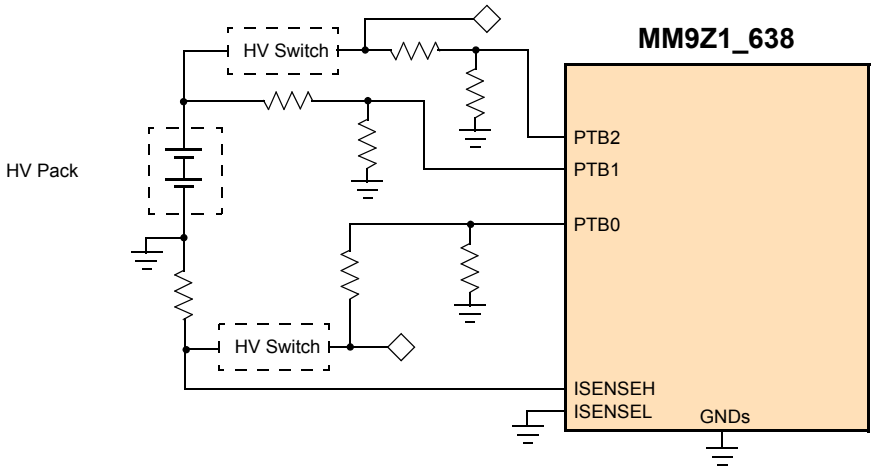

Figure 2. Simplified application diagram for HV pack monitoring - Use of an external divider principle schematic

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1 Ordering information

Table 1. Ordering information

Device (Add an R2 suffix for tape and reel orders)	Temperature range (T_A)	Package	Flash (kB)	RAM (kB)	EEPROM (kB)
MM9Z1J638BM2EP	-40 °C to 125 °C	48 QFN-EP	128	8.0	4.0
MM9Z1I638BM2EP			96		

2 Internal block diagram

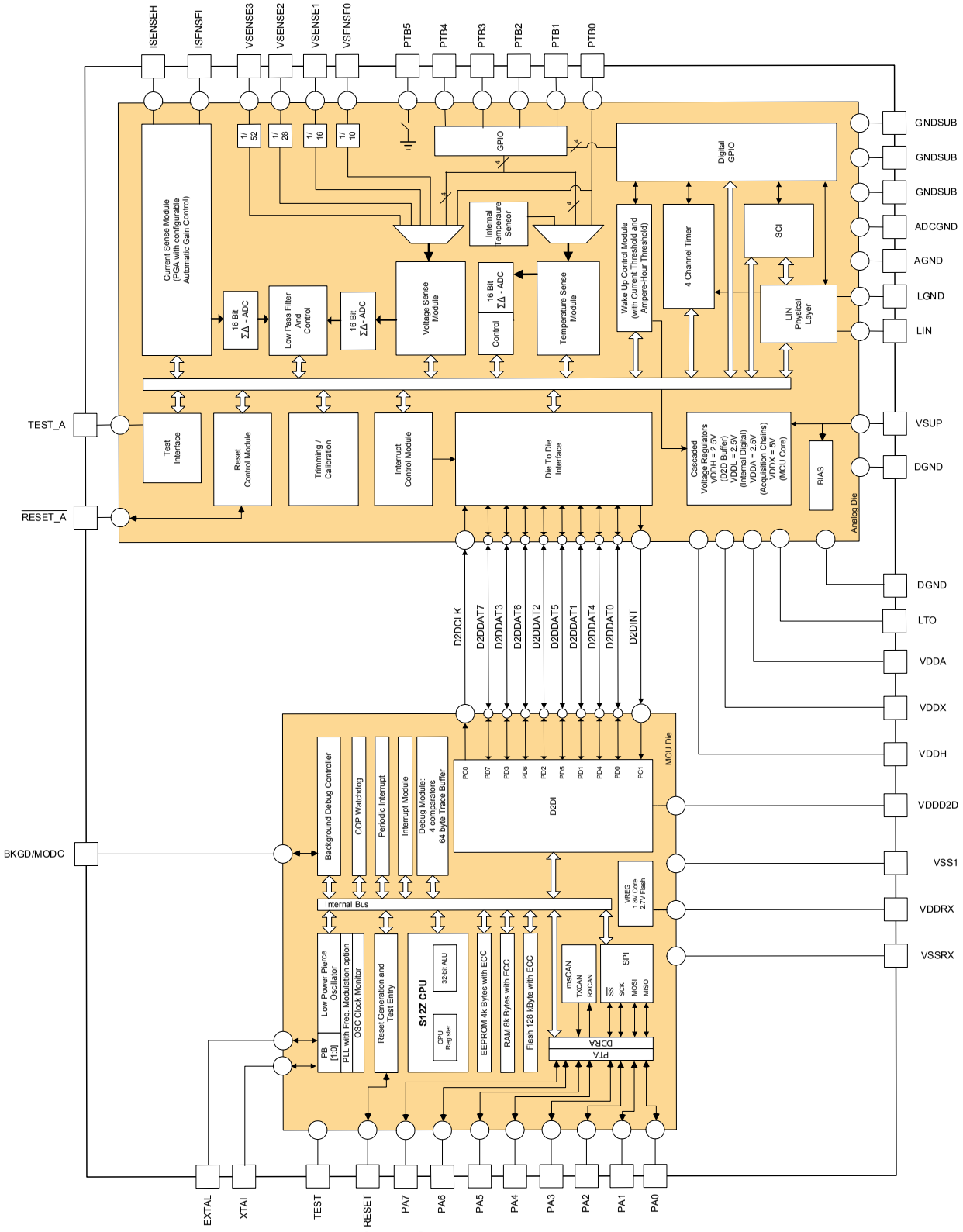


Figure 3. Simplified internal block diagram

3 Pin assignment

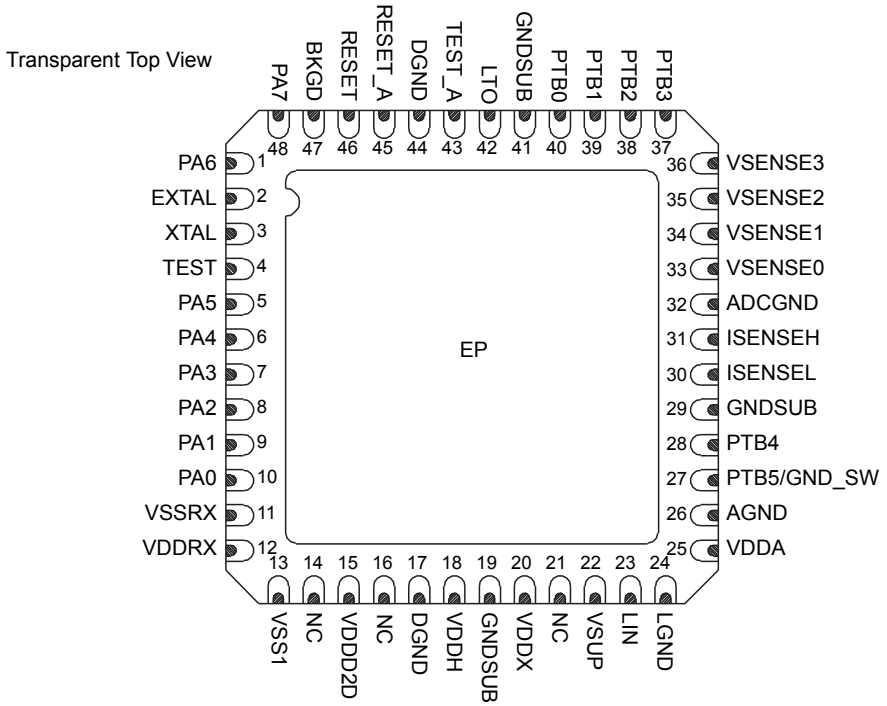


Figure 4. MM9Z1_638 pin connections

3.1 MM9Z1_638 pin description

The following table gives a brief description of all available pins on the MM9Z1_638 device. Refer to the highlighted chapter for detailed information

Table 2. MM9Z1_638 pin description

Pin #	Pin name	Formal name	Description
1	PA6	MCU PA6	General purpose port A input or output pin 6. See Port integration module (S12ZIPIMV1).
2	EXTAL	MCU Oscillator	EXTAL is one of the optional crystal/resonator drivers and external clock pins, and the PB0 port may be used as a general purpose I/O. On reset, all the device clocks are derived from the internal reference clock. See S12Z clock, reset and power management unit (S12ZCPMU).
3	XTAL	MCU Oscillator	XTAL is one of the optional crystal/resonator drivers and external clock pins, and the PB1 port may be used as a general purpose I/O. On reset all the device clocks are derived from the internal reference clock. See S12Z clock, reset and power management unit (S12ZCPMU).
4	TEST	MCU Test	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to VSSRX in user mode.
5	PA5	MCU PA5/CAN TXD	General purpose port A input or output pin 5. This pin is shared with the TXDCAN of the integrated msCAN module. See Port integration module (S12ZIPIMV1).
6	PA4	MCU PA4/CAN RXD	General purpose port A input or output pin 4. This pin is shared with the RXDCAN of the integrated msCAN module. See Port integration module (S12ZIPIMV1).
7	PA3	MCU PA3 / $\overline{SS}$	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI interface. See Port integration module (S12ZIPIMV1).
8	PA2	MCU PA2 / SCK	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI interface. See Port integration module (S12ZIPIMV1).

Table 2. MM9Z1_638 pin description (continued)

Pin #	Pin name	Formal name	Description
9	PA1	MCU PA1 / MOSI	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI interface. See Port integration module (S12ZIPIMV1).
10	PA0	MCU PA0 / MISO	General purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI interface. See Port integration module (S12ZIPIMV1).
11	VSSRX	MCU 5.0 V Ground	External ground for the MCU - VDDRX return path.
12	VDDRX	MCU 5.0 V Supply	5.0 V MCU input power supply. This pin must be connected to VDDX.
13	VSS1	MCU 2.5 V Ground	External ground for the MCU - VDDD2D return path.
14	NC	Not connected	This pin must be grounded in the application.
15	VDDD2D	MCU 2.5 V Supply	2.5 V MCU input power supply for the die to die interface. This pin must be connected to VDDH.
16	NC	Not connected	This pin must be grounded in the application.
17	DGND	Digital Ground	This pin is the device digital ground connection.
18	VDDH	Voltage Regulator Output 2.5 V	2.5 V output voltage. This pin must be connected to the VDDD2D. An external capacitor (C_{VDDH}) is needed.
19	GNDSUB	Substrate Ground	Substrate ground connection.
20	VDDX	MCU 5.0 V and External CAN Supply	5.0 V output power supply for the internal MCU die and an external 8 or 14 pin CAN interface. This pin must be connected to VDDRX. An external capacitor (C_{VDDX}) is needed.
21	NC	Not connected	This pin is not connected to the die. Within the application, it could be connected or left open.
22	VSUP	Power Supply	This pin is the device power supply pin. A reverse battery protection diode is required. External capacitor(s) needed.
23	LIN	LIN Bus	This pin is the single-wire LIN bus.
24	LGND	LIN Ground	This pin is the device LIN ground connection.
25	VDDA	Analog Voltage Regulator Output	Voltage regulator output pin, to supply the analog front end, and the external temperature sensor circuitry. An external capacitor (C_{VDDA}) is needed.
26	AGND	Analog Ground	This pin is the device analog voltage regulator and LP oscillator ground connection.
27	PTB5/ GND_SW	GND Switch Temp	This pin is a switch to GND for connection of the external temperature sensors circuitry.
28	PTB4	Analog Input & General Purpose Input 4	General purpose 5.0 V Input (connection to timer and selectable pull-down). This pin shares several functions: Temperature sensor input. Direct voltage sense, used with an external resistor divider Wake-up input. General purpose 5.0 V input
29	GNDSUB	Substrate Ground	Substrate ground connection.
30	ISENSEL	Current Sense L	Current sense input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor.
31	ISENSEH	Current Sense H	Current sense input “high”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor.
32	ADCGND	Analog Digital Converter Ground	Analog digital converter ground connection.
33	VSENSE0	Voltage Sense 0	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection.
34	VSENSE1	Voltage Sense 1	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self-protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection.

Table 2. MM9Z1_638 pin description (continued)

Pin #	Pin name	Formal name	Description
35	VSENSE2	Voltage Sense 2	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self-protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection.
36	VSENSE3	Voltage Sense 3	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self-protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection.
37	PTB3	Analog Input & General Purpose I/O 3	This pin shares several functions: Temperature sensor input. Direct voltage sense, used with an external resistor divider General purpose 5.0 V I/O (connection to timer, LIN SCI, and selectable pull-up to VDDX).
38	PTB2	Analog Input & General Purpose I/O 2	This pin shares several functions: Temperature sensor input. Direct voltage sense, used with an external resistor divider General purpose 5.0 V I/O (connection to timer, LIN SCI, and selectable pull-up to VDDX).
39	PTB1	Analog Input & General Purpose I/O 1	This pin shares several functions: Temperature sensor input. Direct voltage sense, used with an external resistor divider General purpose 5.0 V I/O (connection to timer, LIN SCI, and selectable pull-up to VDDX).
40	PTB0	Analog Input 0	This pin shares several functions: Temperature sensor input. Direct voltage sense, used with an external resistor divider
41	GNDSUB	Substrate Ground	Substrate ground connection.
42	LTO	Logic Test Output	Reserved pin for logic test output signal. Typical voltage is 2.5 V. Should be left open during device operation.
43	TEST_A	Test Mode	Test mode pin. This pin must be grounded in applications.
44	DGND	Digital Ground	This pin is the device digital ground connection.
45	RESET_A	Reset I/O	Reset output pin of the analog die in Normal mode. Bidirectional reset I/O of the analog die in Stop mode. Active low signal with internal pull-up to VDDX. This pin must be connected to RESET.
46	RESET	MCU Reset	Bidirectional reset I/O pin of the MCU die. Active low signal with internal pull-up to VDDRX. This pin must be connected to RESETA.
47	BKGD	MCU Background Debug and Mode	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as an MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device. See Background debug controller (BDC).
48	PA7	MCU PA7	General purpose port A input or output pin 7. See Port integration module (S12ZIPIMV1).

3.2 Typical applications

Figure 5 and Table 3 show a typical application to illustrate some of the device capabilities.

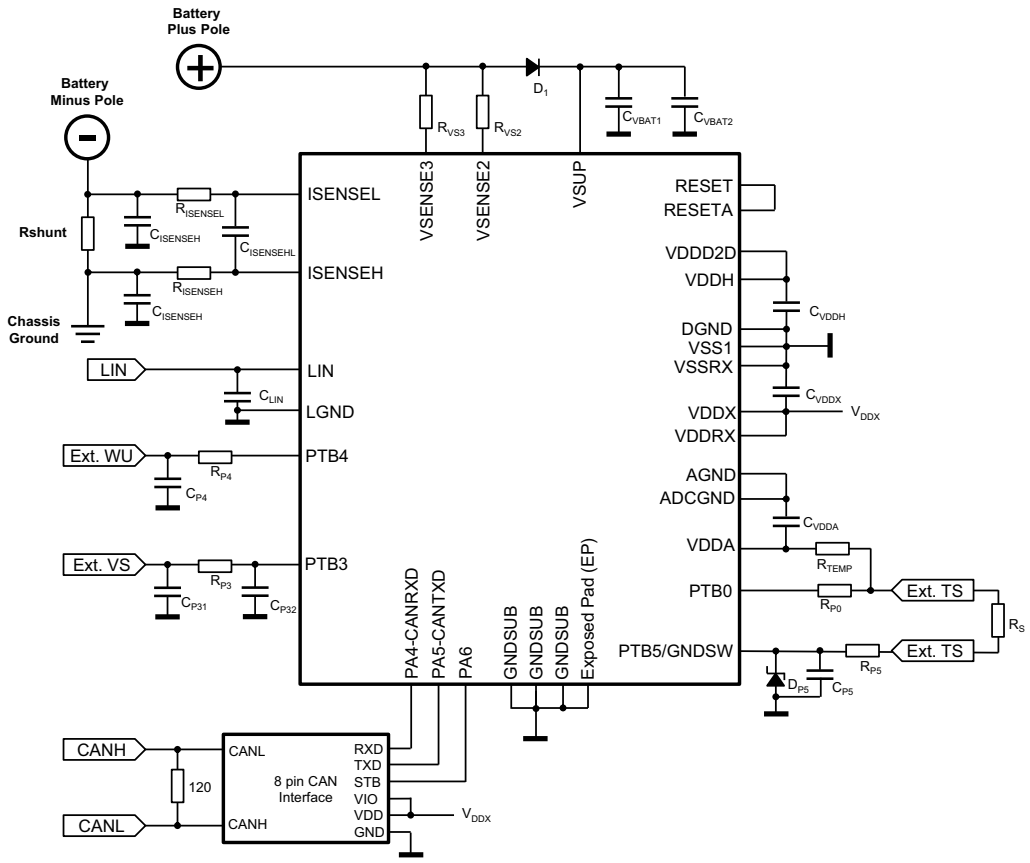
Both CAN and LIN communications are described.

VSENSE_2 and VSENSE_3 inputs are used to show possible redundancy.

External wake-up via PTB4 is used.

Single external voltage sense is used utilizing PTB3.

Single external temperature sense is used utilizing PTB0.



Note: Module GND connected to Battery Minus or Chassis Ground – based on configuration

Figure 5. Typical application example

Table 3. External components

Name	Description	value	Comment
D1	Reverse Battery Diode	N/A	
C_{VBAT1}	Battery Decoupling Capacitor	4.7 µF	
C_{VBAT2}	Battery Decoupling Capacitor	100 nF	
R_{VS2}	Vsense Current Limitation	2.2 kΩ	
R_{VS3}	Vsense Current Limitation	2.2 kΩ	
R_{SHUNT}	Current Measurement	50 to 200 µΩ	
$R_{ISENSEL}$	EMC resistor	max 500 Ω	Selection for best EMC perfomance
$R_{ISENSEH}$	EMC resistor	max 500 Ω	
$C_{ISENSEL}$	EMC capacitor	2.2 nF (typ)	
$C_{ISENSEH}$	EMC capacitor	2.2 nF (typ)	
$C_{ISENSEHL}$	EMC capacitor	2.2 nF (typ)	
C_{LIN}	LIN bus filter	Optional 220 pF	Selection per OEM requirement, for EMC and ESD performance.
R_{P4}	PTB4 Protection Resistor	10 kΩ	Minimum value to meet max rating
C_{P4}	PTB4 Protection Capacitor	10 nF	Minimum value to meet max rating
C_{VDDX}	VDDX Decoupling Capacitor	470 nF	
C_{VDDH}	VDDH Decoupling Capacitor	470 nF	An additionnal 4.7 nF capacitor might be required for specific EMC test conditions.

Table 3. External components (continued)

Name	Description	value	Comment
C_{VDDA}	VDDA Decoupling Capacitor	47 nF	
R_{TEMP}	Temp Sense Serial Resistor	100 kΩ	
R_S	Temperature Sensor	N/A	ex: NTC temperature Sensor
R_{P0}	PTB0 Protection Resistor	2.2 kΩ	To meet maximum rating. Higher or different value might be required. These components are optional and required to sustain EMC and ESD requirements when the pins go outside of the module.
R_{P5}	PTB5 Protection Resistor	1.0 kΩ	
C_{P5}	PTB5 Protection Capacitor	2.2 nF	
D_{P5}	PTB5 Protection Zener Diode	5.1 V	
C_{P31}	VSENSE_EXT Protection Capacitor	2.2 nF	To meet maximum rating. Higher or different value might be required. These components are optional and required to sustain EMC and ESD requirements when the pins go outside of the module.
C_{P32}	VSENSE_EXT Protection Capacitor	22 nF	
R_{P3}	VSENSE_EXT Protection Resistor	10 kΩ	

4 Electrical characteristics

4.1 General

This section contains electrical information for the microcontroller and the analog die.

4.2 Absolute maximum ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside these maximums is not guaranteed. Stress beyond these limits may affect the reliability, or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level. All voltages are with respect to ground, unless otherwise noted.

Table 4. Absolute maximum electrical ratings - analog die

Ratings	Symbol	Value	Unit
VSUP pin voltage	V_{VSUP}	-0.3 to 42	V
VSENSE0, VSENSE1, VSENSE2 pin voltage with 2.2 k resistor in serial (1)	$V_{VSENSE012}$	-40 to 42	V
VSENSE3 pin voltage with 2.2k resistor in serial (1)	$V_{VSENSE3}$	-40 to 62	V
PTB0, PTB1, PTB2, and PTB3 Voltage	VPTB0-3	-0.3 to VDDX+0.3	V
PTB4 direct voltage PTB4 with external 47 k serial resistor	VPTB4	-0.3 to 7.0 -27 to 42	V
PTB5 GND Switch current	IPTB5	1.0	mA
ISENSEH and ISENSEL pin voltage	V_{ISENSE}	-0.5 to V_{DDA}+0.25	V
ISENSEH and ISENSEL pin current	I_{ISENSE}	-1.0 to 1.0	mA
LIN pin voltage	V_{BUS}	-27 to 42	V
LIN pin current (internally limited)	I_{BUSLIM}	on page 18	mA
Voltage at VDDX	V_{DDX}	-0.3 to 5.55	V
Voltage at VDDH	V_{DDH}	-0.3 to 3.0	V
VDDH output current	I_{VDDH}	internally limited	mA
VDDX output current	I_{VDDX}	internally limited	mA
$\overline{\text{RESET\_A}}$ pin voltage	V_{IN}	-0.3 to V_{DDX}+0.3	V

Notes:
1.It has to be assured by the application circuit that these limits will not be exceeded, e.g. by ISO pulse 1.

Table 5. Maximum thermal ratings

Ratings	Symbol	Value	Unit
Storage temperature	T_{STG}	-55 to 150	°C
Package thermal resistance (2)	$R_{\theta JA}$	32 typ.	°C/W

Notes:
2.$R_{\theta JA}$ value is derived using a JEDEC 2s2p test board

4.3 Operating conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

Table 6. Operating Conditions [3]

Ratings	Symbol	Value	Unit
Functional operating supply voltage - Device is fully functional. All features are operating.	V_{SUP}	3.5 to 28	V
Extended range for RAM Content is guaranteed. Other device functionality is limited. With Cranking mode enabled (see Cranking mode).	V_{SUPL}	2.5 to 3.5	V
Functional operating VSENSE0 voltage[4]	V_{SENSE0}	0.0 to 10	V
Functional operating VSENSE1 voltage[4]	V_{SENSE1}	0.0 to 16	V
Functional operating VSENSE2 voltage[4]	V_{SENSE2}	0.0 to 28	V
Functional operating VSENSE3 voltage[4]	V_{SENSE3}	0.0 to 52	V
External voltage and temperature sense input - PTB0-4	V_{PTB0-4}	0.0 to 1.0	V
ISENSEH, ISENSEL voltage	VISH/L	-0.3 to 0.3	V
LIN output voltage range	V_{VSUP_LIN}	7.0 to 18	V
MCU oscillator	f_{OSC}	4.0 to 16.384	MHz
MCU bus frequency	f_{BUS}	51.2	MHz
Operating ambient temperature	T_A	-40 to 125	°C
Operating junction temperature - analog die	T_{J_A}	-40 to 150	°C
Operating junction temperature - MCU die	T_{J_M}	-40 to 150	°C

Notes:
3. The parametric data are guaranteed while the pins are within Operating Conditions. Other conditions are presented at top of parametric tables or noted into parameters.
4. Values for $V_{SENSE-x}$ > Max. Specified Value are flagged in the VTH bit.

4.4 Supply currents

This section describes the current consumption characteristics of the device, as well as the conditions for the measurements.

4.4.1 Measurement conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in special single chip mode and the CPU code is executed from RAM. For Run and Wait current measurements PLL is on and the reference clock is the IRC1M trimmed to 1.024 MHz. The bus frequency is 51.2 MHz and the CPU frequency is 102.4 MHz. Table 7 and Table 8 show the configuration of the CPMU module for Run, Wait and Stop current measurement. Table 9 shows the configuration of the peripherals for run current measurement

Table 7. CPMU configuration for pseudo stop current measurement

CPMU REGISTER	Bit settings/conditions
CPMUCLKS	PLLSEL = 0, PSTP = 1, CSAD = 0, PRE = PCE = RTIOSCSEL = COPOSCSEL = 1
CPMUOSC	OSCE = 1, External Square wave on EXTAL f_{EXTAL} = 4.0 MHz, V_{IH} = 1.8 V, V_{IL} = 0 V
CPMURTI	RTDEC = 0, RTR[6:4] = 111, RTR[3:0] = 1111;
CPMUCOP	WCOP = 1, CR[2:0] = 111

Table 8. CPUM Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/conditions
CPMUSYNR	VCOFRQ[1:0] = 3,SYNDIV[5:0] = 49
CPMUPOSTDIV	POSTDIV[4:0] = 0,
CPMUCLKS	PLLSEL = 1, CSAD = 0
CPMUOSC	OSCE = 0, Reference clock for PLL is f_{REF} = f_{IRC1M} trimmed to 1.024 MHz
API settings for stop current measurement	
CPMUAPICTL	APIEA = 0, APIFE = 1, APIE = 0
CPMUACLKTR	trimmed to ≥ 10 kHz
CPMUAPIRH/RL	set to 0xFFFF

Table 9. Peripheral configurations for run supply current measurements

Peripheral	Configuration
SPI	configured to master mode, continuously transmit data (0x55 or 0xAA) at 1.0 Mbit/s
msCAN	continuously transmit data (0x55 and 0xAA) at 1.0 MBaud/s
D2DI	continuously read data
COP	COP Warchdog Rate 2^{24}
RTI	enabled, RTI Control Register (RTICTL) set to $FF
DBG	the module is disabled

Table 10. Analog die configurations for normal mode supply current measurements

Peripheral	Configuration
D2D	maximum frequency (25.600 MHz)
LIN	enabled, 50% dominant, 50% recessive
TIMER	enabled, all channels active in output compare mode with minimum timeout
LTC	enabled, maximum timeout
SCI	continuously transmitting data (0x55 or 0xAA) with 19.2 kBit/s
Channels	Current/voltage: highest sampling rate (8.0 kHz), LPF enabled, chopper ON for Current and Temperature channels, OFF for Voltage channels and compensation enabled, automatic gain adjustment enabled temperature: internal temperature measurement enabled, 1.0 kHz sampling rate

Table 11. Supply currents

Parameter	Symbol	Min.	Typ.[5]	Max.	Unit
MM9Z1_638 combined consumption					
Normal mode current measured at V_{SUP} excluding external load current, (3.5 V ≤ V_{SUP} ≤ 28 V; -40 °C ≤ T_A ≤ 125 °C) parameter tested up to T_A = 85 °C	I_{RUN}	–	35	40	mA
Normal mode current measured at V_{SUP} - analog die contribution - excluding mcu and external load current, (3.5 V ≤ V_{SUP} ≤ 28 V; -40 °C ≤ T_A ≤ 125 °C) parameter tested up to T_A = 85 °C	I_{NORMAL}	–	1.5	4.0	mA
Stop mode current measured at V_{SUP}					
• Continuous base current [6]					
T = -40 °C	I_{STOP}	–	105	125	µA
T = 85 °C		–	110	195	
T = 125 °C [7]		–	210	450	
• Stop current during Cranking mode [6]					
T = -40 °C		–	110	135	
T = 85 °C		–	130	235	
T = 125 °C [7]		–	235	500	

Table 11. Supply currents

Parameter	Symbol	Min.	Typ.[5]	Max.	Unit
Sleep mode measured at V_{SUP} • Continuous base current [6] T = -40 °C T = 85 °C T = 125 °C [7]	I_{SLEEP}	 – – –	 65 65 85	 85 135 145	µA
Pseudo stop current [6] T = -40 °C T = 85 °C T = 125 °C [7]		 – – –	 205 210 310	 225 305 550	µA
Current adder during current trigger event in stop or sleep modes- (typ. 10 ms duration [8], temperature measurement = OFF)		–	1500	1750	µA

Notes:

5.Typical values noted reflect the approximate parameter mean at T_A = 25 °C.

6.From V_{SUP} 6.0 to 28 V

7.Guaranteed by design and characterization

8.Duration based on channel configuration. 10 ms typical for Decimation Factor = 512, Chopper = ON.

4.5 Analog die electrical characteristics

4.5.1 Static electrical characteristics

All characteristics noted under conditions 3.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Parameters tested up to T_A = 85 °C unless otherwise noted.Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Table 12. Static electrical characteristics - power supply

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low Voltage Reset L (POR) Assert (measured on LTO) • Cranking Mode Disabled	V_{PORL}	1.75	1.9	2.12	V
Low Voltage Reset L (POR) Deassert (measured on LTO) • Cranking Mode Disabled	V_{PORH}	1.85	2.1	2.35	V
Low Voltage Reset L (POR) Assert (measured on LTO) • Cranking Mode Enabled(9)	V_{PORCL}	1.0	1.3	1.7	V
Low Voltage Reset A (LVRA) Assert (measured on VDDA)	V_{LVRAL}	1.9	2.05	2.2	V
Low Voltage Reset A (LVRA) Deassert (measured on VDDA)	V_{LVRAH}	2.0	2.15	2.3	V
Low Voltage Reset X (LVRX) Assert (measured on VDDX)	V_{LVRXL}	2.5	2.75	3.0	V
Low Voltage Reset X (LVRX) Deassert (measured on VDDX)	V_{LVRXH}	2.7	2.95	3.25	V
Low Voltage Reset H (LVRH) Assert (measured on VDDH)	V_{LVRHL}	1.9	2.075	2.2	V
Low Voltage Reset H (LVRH) Deassert (measured on VDDH)	V_{LVRHH}	2.05	2.175	2.3	V
Undervoltage Interrupt (UVI) Assert (measured on VSUP), Cranking Mode Disabled	V_{UVIL}	4.65	5.2	6.15	V
Undervoltage Interrupt (UVI) Deassert (measured on VSUP), Cranking Mode Disabled	V_{UVIH}	4.9	5.4	6.3	V
Undervoltage Cranking Interrupt (UVI) Assert (measured on VSUP) Cranking Mode Enabled	V_{UVCIL}	3.4	3.6	4.0	V
Undervoltage Cranking Interrupt (UVI) Deassert (measured on VSUP) Cranking Mode Enabled	V_{UVCIH}	3.5	3.8	4.15	V
VSENSE2 High Voltage Warning Threshold Assert(10)	V_{TH}		28		V

Notes:
9.Deassert with Cranking off = V_{PORH}

10.5.0 V < V_{SUP} < 28 V, Digital Threshold at the end of channel chain (incl. compensation)

Table 13. Static electrical characteristics - resets

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low-state Output Voltage I_{OUT} = 2.0 mA	V_{OL}	–	–	0.8	V
Pull-up Resistor	R_{RPU}	25	–	50	kΩ
Low-state Input Voltage	V_{IL}	–	–	$0.3V_{DDX}$	V
High-state Input Voltage	V_{IH}	$0.7V_{DDX}$	–	–	V
Reset Release Voltage (VDDX)	V_{RSTRV}	0.0	0.02	1.0	V
RESET_A pin Current Limitation	I_{LIMRST}	–	–	10	mA

Table 14. Static electrical characteristics - voltage regulator outputs

Parameter	Symbol	Min.	Typ.	Max.	Unit
Analog Voltage Regulator - VDDA(11)					
Output Voltage I_{VDDA} ≤ 1.0 mA	V_{DDA}	2.25	2.5	2.75	V
Output Current Limitation (Max. value occurs under VDDA short to GND condition)	I_{VDDA}	–	–	30	mA
Load current available for external sensor supply(i.e Temp sensor)	$I_{VDDA\ EXT}$	–	–	1.0	mA
Line regulation, V_{SUP} 3.5 to 28 V, I_Load 1.0 mA	LINE REGA	-30	–	30	mV

Table 14. Static electrical characteristics - voltage regulator outputs (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Load regulation, I_Load 2.0 µA - 3.0 mA[12]	LOAD REGA	-50	–	50	mV
Voltage in Low-power modes (sleep and stop)	$V_{DDA\ LP}$	–	0.0	100	mV
Logic Test Output - LTO[11]					
Output Voltage	V_{LTO}	2.25	2.5	2.75	V
Output current limitation (for pin FMEA purpose only)	I_{LTO}	1.0	–	30	mA
High Power Digital Voltage Regulator - VDDH[13]					
Output Voltage 1.0 mA ≤ I_{VDDH} ≤ 18 mA	V_{DDH}	2.4	2.5	2.75	V
Output Current Limitation	I_{VDDH}	–	–	65	mA
5.0 V Voltage Regulator - VDDX[13]					
Output Voltage in Normal Mode, 1.0 mA ≤ I_{VDDX} ≤ 150 mA, V_{SUP} > 5.5 V	V_{DDX}	4.75	5.0	5.25	V
Output Current Limitation	I_{VDDX}	150	–	300	mA
Load current available for external supply - V_{SUP}> 5.5 V, for all external loads like: CAN transceiver, MCU I/Os, and PTBx for external temperature sensors.	$I_{VDDX\ EXT}$	–	–	100	mA
Output Voltage in Low-power Stop mode I_{VDDX} ≤ 2.0 mA • V_{SUP}> 5.5 V • V_{SUP} > 3.5 V	V_{DDXSTP}	4.75 3.2	5.0 –	5.25 –	V
Line regulation in normal mode, V_{SUP} 6.0 to 18 V, no load and I_{LOAD} = 150 mA	Line Reg Vx	-50	–	50	mV
Load regulation in normal mode, V_{SUP} 6.0 V, I_{LOAD} < 150 mA	Load Reg Vx	–	–	300	mV
Line regulation in Low-power Stop mode V_{SUP} 5.5 to 18 V	Line Reg VxLP	-50	–	50	mV
Load regulation in Low-power Stop mode	Load Reg VxLP	–	–	100	mV
Output current limitation in Low-power Stop mode	$I_{VDDXSTP}$	3.0	–	10	mA
Drop voltage, I_{LOAD} < I_{LIM} (I_{VDDX})	$VDDX_{DRP}$	–	–	300	mV
External decoupling capacitor	C at V_{DDX}	–	470	–	nF

Notes:
11.No additional current must be taken from those outputs.
12.Total VDDA regulator current, including internal device consumption
13.The specified current ranges does include the current for the MCU die. No external loads recommended.

Table 15. Static electrical characteristics - LIN physical layer interface - LIN

Parameter	Symbol	Min.	Typ.	Max.	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor R_{SLAVE}; Driver OFF; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	–	–	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor R_{SLAVE}; Driver OFF; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$	–	–	20	µA
Input Leakage Current; GND Disconnected; GND_{DEVICE} = V_{SUP}; 0 < V_{BUS} < 18 V; V_{BAT} = 12 V	$I_{BUS\_NO\_GND}$	-1.0	–	1.0	mA
Input Leakage Current; V_{BAT} disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V	$I_{BUS\_NO\_BAT}$	–	–	10	µA
Receiver Input Voltage; Receiver Dominant State	V_{BUSDOM}	–	–	0.4	V_{SUP}
Receiver Input Voltage; Receiver Recessive State	V_{BUSREC}	0.6	–	–	V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{BUS_HYS}	–	–	0.175	V_{SUP}
Voltage Drop at the serial Diode	D_{SER_INT}	0.3	0.7	1.0	V
LIN Pull-up Resistor	R_{SLAVE}	20	30	60	kΩ
LIN Internal Capacitor [14]	C_{LIN}	–	5.0	30	pF

Table 15. Static electrical characteristics - LIN physical layer interface - LIN (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low Level Output Voltage, I_{BUS}=40 mA	V_{DOM}	–	–	0.3	V_{SUP}
High Level Output Voltage, I_{BUS}=-10 µA, R_L=33 kΩ	V_{REC}	VSUP-1	–	–	V
J2602 Detection Deassert Threshold for VSUP level	V_{J2602H}	5.9	6.3	6.7	V
J2602 Detection Assert Threshold for VSUP level	V_{J2602L}	5.8	6.2	6.6	V
J2602 Detection Hysteresis	$V_{J2602HYS}$	70	190	250	mV
BUS Wake-up Threshold	V_{LINWUP}	4.0	5.25	6.0	V

Notes:
14.This parameter is guaranteed by process monitoring but not production tested.

Table 16. Static electrical characteristics - high voltage input - PTB4

Parameter	Symbol	Min.	Typ.	Max.	Unit
Wake-up Threshold - Rising Edge	V_{WTHR}	1.3	2.6	3.4	V
Input High-voltage (digital Input)	V_{IH}	$0.7V_{DDX}$	–	V_{DDX}+0.3	V
Input Low-voltage (digital Input)	V_{IL}	V_{SS}-0.3	–	$0.35V_{DDX}$	V
Input Hysteresis	V_{HYS}	–	140	–	mV
Internal Positive Clamp Voltage	$V_{PTB4CLMP}$	–	9.8	–	V
Input Current PTB4, V_{IN} = 8V	I_{IN}	-10	0	10	uA
Internal Pull-down Resistance[15]	R_{PD}	50	100	200	kΩ
External Series Resistor	R_{PTB4}	42.3	47	51.7	kΩ
External Capacitor	C_{PTB4}	–	2.2	–	nF

Notes:
15.Disabled by default.

Table 17. Static electrical characteristics - general purpose I/O - PTB[1…3]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	$0.7V_{DDX}$	–	V_{DDX}+0.3	V
Input Low Voltage	V_{IL}	V_{SS}-0.3	–	$0.35V_{DDX}$	V
Input Hysteresis	V_{HYS}	–	140	–	mV
Input Leakage Current (pins in high-impedance input mode) (V_{IN} = V_{DDX} or V_{SSX})	I_{IN}	-1.0	–	1.0	µA
PTB1, 2, 3. Output High Voltage (pins in output mode), I_{OH} = –5.0 mA	V_{OH}	V_{DDX}-0.8	–	–	V
PTB1, 2, 3. Output Low Voltage (pins in output mode), I_{OL} = 5.0 mA	V_{OL}	–	–	0.8	V
Internal Pull-up Resistance for PTB1, 2, 3 only (V_{IH} min. > Input voltage > V_{IL} max)[16]	R_{PUL}	25	37.5	50	kΩ
Input Capacitance	C_{IN}	–	6.0	–	pF
Output Drive strength at 10 MHz	C_{OUT}	–	–	100	pF

Notes:
16.Disabled by default.

Table 18. Static electrical characteristics - general purpose I/O - PTB5

Parameter	Symbol	Min.	Typ.	Max.	Unit
PTB5 switch to GND: On resistance	$PTB5_{RON}$	20	50	100	Ω

Table 19. Static electrical characteristics - current sense module

Parameter	Symbol	Min.	Typ.	Max.	Unit
Gain Error (17), (18) • without common mode from -40 °C to 85 °C (20) without life time drift including life time drift • without common mode from 85 °C to 125 °C (20) without life time drift including life time drift • additional common mode error for gain 64 and 256 (20)	$I_{GAINERR}$	 -0.3 -0.5 -0.5 -0.7 -0.2	 – – – – –	 0.3 0.5 0.5 0.7 0.2	%
Offset Error (17),(18),(19)	$I_{OFFSETERR}$	–	–	0.5	µV
Resolution (LSB) • COMP_TF.IRSEL = 000 (50 µΩ) • COMP_TF.IRSEL = 001 (75 µΩ) • COMP_TF.IRSEL = 010 (100 µΩ) • COMP_TF.IRSEL = 011 (150 µΩ) • COMP_TF.IRSEL = 100 (200 µΩ)	I_{RES}	 – – – – –	 0.05 0.75 0.1 0.15 0.2	 – – – – –	µV
ISENSEH, ISENSEL (20) • terminal voltage range for gain 4 and 16 for specified gain error without additional common mode error • terminal voltage range for gain 64 for specified gain error without additional common mode error • terminal voltage range for gain 256 for specified gain error without additional common mode error • differential signal voltage range	V_{INC} V_{IND}	 -300 -100 -50 -150	 – – – –	 300 100 50 150	mV
PGA Gains • gain 4 • gain 16 • gain 64 • gain 256	PGA_{GAIN}	 – – – –	 4 16 64 256	 – – – –	
Differential Leakage Current: differential voltage between ISENSEH/ ISENSEL, with IsenseH or IsenseL connected to GND	I_{SENSE_DLC}	-2.0	–	2.0	nA
Wake-up Current Threshold Resolution	$I_{RESWAKE}$	–	0.2	–	µV
Resistor Threshold for OPEN Detection	R_{OPEN}	0.8	1.25	1.8	MΩ

Notes:
17.Device trimmed and after system calibration. Automatic gain compensation over temperature.
18.Chopper Mode = ON, Gain with automatic gain control enabled
19.Parameter not tested. Guaranteed by design and characterization
20.Voltage level referred to AGND.

Table 20. Static electrical characteristics - voltage sense module (22)

Parameter	Symbol	Min.	Typ.	Max.	Unit
VSENSE0 internal resistor divider ratio	VS0_div	–	10	–	
VSENSE1 internal resistor divider ratio	VS1_div	–	16	–	
VSENSE2 internal resistor divider ratio	VS2_div	–	28	–	
VSENSE3 internal resistor divider ratio	VS3_div	–	52	–	
VSENSE0, accuracy (accuracy includes both gain and offset errors) (21), (23) • from -40 to 85 °C, input range 1.8 V to 10 V • from -40 to 85 °C, input range 1.25 V to 1.8 V • from 85 to 125 °C, input range 1.8 V to 10 V • from 85 to 125 °C, input range 1.25 V to 1.8 V	$VS0_{ACC}$	 -0.25 -0.5 -0.5 -0.6	 – – – –	 0.25 0.5 0.5 0.6	%
VSENSE1, accuracy (accuracy includes both gain and offset errors) (21), (23) • from -40 to 85 °C, input range 2.8 V to 16 V • from -40 to 85 °C, input range 2.0 V to 2.8 V • from 85 °C to 125 °C, input range 2.8 V to 16 V • from 85 °C to 125 °C, input range 2.0 V to 2.8 V	$VS1_{ACC}$	 -0.15 -0.5 -0.25 -0.5	 – – – –	 0.15 0.5 0.25 0.5	%

Table 20. Static electrical characteristics - voltage sense module [22] (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
VSENSE2, accuracy (accuracy includes both gain and offset errors) [21], [23] • from -40 to 85 °C, input range 5.0 V to 28 V • from -40 to 85 °C, input range 3.5 V to 5.0 V • from 85 °C to 125 °C, input range 5.0 V to 28 V • from 85 °C to 125 °C, input range 3.5 V to 5.0 V	$VS2_{ACC}$	 -0.15 -0.5 -0.25 -0.5	 – – – –	 0.15 0.5 0.25 0.5	%
VSENSE3, accuracy (accuracy includes both gain and offset errors) [21], [23] • from -40 to 85 °C, input range 9.4 V to 50 V • from -40 to 85 °C, input range 6.5 V to 9.4 V or > 50 V • from 85 °C to 125 °C, input range 9.4 V to 50 V • from 85 °C to 125 °C, input range 6.5 V to 9.4 V and > 50 V	$VS3_{ACC}$	 -0.15 -0.5 -0.25 -0.5	 – – – –	 0.15 0.5 0.25 0.5	%
VSENSE[0..3] Drift • drift due to MSL3 (according JEDEC J-STD-020) reflow • drift due to Life Time Drift	VS_{DRIFT}	 – –	 0.03 -6.0	 – –	 % ppb/h
VSENSE0,resolution and offset [21] • voltage measurement resolution • extrapolated offset error	$VS0_{RO}$	 – –	 0.25 ±3.7	 – –	mV
VSENSE1,resolution and offset [21] • voltage measurement resolution • extrapolated offset error	$VS1_{RO}$	 – –	 0.25 ±3.7	 – –	mV
VSENSE2,resolution and offset [21] • voltage measurement resolution • extrapolated offset error	$VS2_{RO}$	 – –	 0.5 ±6.2	 – –	mV
VSENSE3,resolution and offset [21] • voltage measurement resolution • extrapolated offset error	$VS3_{RO}$	 – –	 1.0 ±19.4	 – –	mV

Notes:
21.Device trimmed and after system calibration. Automatic gain compensation over temperature.
22.The data are valid for both chop modes (off and on). The dies are delivered with chop off compensation values.
23.Including 2.2 kΩ perfect resistor into measurement path.

Table 21. Static electrical characteristics - internal temperature sense module

Parameter	Symbol	Min.	Typ.	Max.	Unit
Measurement Range	T_{RANGE}	-40	–	150	°C
Accuracy • -40 °C ≤ T_J ≤ 85 °C • 85 °C < T_J ≤ 150 °C [24]	T_{ACC}	 -2.0 -3.0	 – –	 2.0 3.0	K
Resolution	T_{RES}	–	8.0	–	mK
Max. Calibration Request Interrupt Temperature Step	$T_{CALSTEP}$	-25	–	25	K

Notes:
24.Temperature not tested in production. Guaranteed by design and characterization.

Table 22. Static electrical characteristics - PTB0 to 4 voltage and temperature measurements

Parameter	Symbol	Min.	Typ.	Max.	Unit
PTB0, 1, 2, 3, and 4: measurement resolution for voltage measurement (PTBx routed to Voltage Analog to Digital Converter)	$PTB0\text{-}4_{VRES}$	–	25	–	µV
PTB0, 1, 2, 3 and 4: voltage sense gain error from -40 °C to 85 °C • input range 0.13 V to 1.0 V [25] PTB0, 1, 2, 3 and 4: voltage sense gain error from 85 °C to 125 °C • input range from 0.13V to 1.0V [25]	$PTB0\text{-}4_{ACC}$	 -0.15 -0.25	 – –	 0.15 0.25	%
PTB0, 1, 2, 3 and 4: extrapolated voltage sense offset error, obtained by linear regression at 25 °C.	$PTB0\text{-}4_{OFF}$	-0.5	–	0.5	mV

Table 22. Static electrical characteristics - PTB0 to 4 voltage and temperature measurements (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PTB0, 1, 2, 3, and 4: measurement resolution for temperature measurement (PTBx routed to Temperature Analog to Digital Converter)	$PTB0\text{-}4_{TRES}$	–	19	–	µV
PTB0, 1, 2, 3 and 4: temperature sense gain error (25)	$PTB0\text{-}4_{TSG}$	-0.15	–	0.15	%
Offset temperature coefficient		-12	-7.0	0.0	µV/°C

Notes:
25.Device trimmed and after system calibration. Automatic gain compensation over temperature.

4.5.2 Dynamic electrical characteristics

Dynamic characteristics noted under conditions 3.5 V ≤ V_{SUP} ≤ 28 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Parameters tested up to T_A = +85° C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Table 23. Dynamic electrical characteristics - modes of operation

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low Power Oscillator Frequency	f_{OSCL}	–	512	–	kHz
Low Power Oscillator Tolerance overtemperature range (26) • -40 to 85 °C • after life time -40 to 85 °C • 85 to 125 °C	f_{TOL_A}	-3.0 -3.5 -8.0	– – –	3.0 3.5 3.5	%
Low Power Oscillator Tolerance - synchronized ALFCLK(27) • ALF clock cycle = 1.0 ms • ALF clock cycle = 2.0 ms • ALF clock cycle = 4.0 ms • ALF clock cycle = 8.0 ms	f_{TOLC_A}	f_{TOL}-0.2 f_{TOL}-0.1 f_{TOL}-0.05 f_{TOL}-0.025	f_{TOL}	f_{TOL}+0.2 f_{TOL}+0.1 f_{TOL}+0.05 f_{TOL}+0.025	%

Notes:
26.At T = 125 °C: min = -8.0%, max = -1.0%.
27.Parameter not tested. Guaranteed by design and characterization.

Table 24. Dynamic electrical characteristics - die to die interface - D2D

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Frequency (D2DCLK, D2D[0:3])	f_{D2D}	–	–	25.600	MHz

Table 25. Dynamic electrical characteristics - resets

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset Deglitch Filter Time	t_{RSTDF}	1.0	2.0	3.2	µs
Reset Release Time for WDR and HWR	t_{RSTRT}	–	32	–	µs

Table 26. Dynamic electrical characteristics - wake-up / cyclic sense

Parameter	Symbol	Min.	Typ.	Max.	Unit
Cyclic Wake-up Time(28)	t_{WAKEUP}	ALFCLK	–	TIM4CH	ms
Cyclic Current Measurement Step Width(29)	t_{STEP}	ALFCLK	–	16Bit	ms

Notes:
28.Cyclic wake-up on ALFCLK clock based 16 Bit TIMER with maximum 128x prescaler (min 1x)
29.Cyclic wake-up on ALFCLK clock with 16 Bit programmable counter

Table 27. Dynamic electrical characteristics - window watchdog

Parameter	Symbol	Min.	Typ.	Max.	Unit
Initial Non-window Watchdog Timeout	t_{IWDTO}	256 ms. see Section 6.2.3			ms

Table 28. Dynamic electrical characteristics - LIN physical layer interface - LIN

Parameter	Symbol	Min.	Typ.	Max.	Unit
Bus Wake-up Deglitcher (Sleep and Stop Mode)	t_{PROPWL}	60	80	100	µs
Fast Bit Rate (Programming Mode)	BR_{FAST}	–	–	100	kBit/s
Propagation delay of receiver	t_{RX_PD}	–	–	6.0	µs
Symmetry of receiver propagation delay rising edge w.r.t. falling edge	t_{RX_SYM}	-2.0	–	2.0	µs
TxD Dominant Timeout	t_{TxDDOM}	4	–	8	ms
LIN Driver - 20.0 kBit/s; bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω					
Duty Cycle 1: $TH_{REC(MAX)} = 0.744 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$ $7.0\ V \le V_{SUP} \le 18\ V$; $t_{BIT} = 50\ µs$; $D1 = t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$	D1	0.396	–	–	
Duty Cycle 2: $TH_{REC(MIN)} = 0.422 \times V_{SUP}$ $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$ $7.6\ V \le V_{SUP} \le 18\ V$; $t_{Bit} = 50\ µs$ $D2 = t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$	D2	–	–	0.581	
LIN Driver - 10.0 kBit/s; bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω					
Duty Cycle 3: $TH_{REC(MAX)} = 0.778 \times V_{SUP}$ $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$ $7.0\ V \le V_{SUP} \le 18\ V$; $t_{Bit} = 96\ µs$ $D3 = t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$	D3	0.417	–	–	
Duty Cycle 4: $TH_{REC(MIN)} = 0.389 \times V_{SUP}$ $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$ $7.6\ V \le V_{SUP} \le 18\ V$; $t_{BIT} = 96\ µs$ $D4 = t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$	D4	–	–	0.590	
LIN Transmitter Timing, (V_{SUP} from 7.0 to 18 V) - See Figure 6					
Transmitter Symmetry $t_{TRAN\_SYM} < MAX(ttran\_sym60\%, t_{TRAN\_SYM}40\%)$ $t_{TRAN\_SYM}60\% = t_{TRAN\_PDF}60\% - t_{TRAN\_PDR}60\%$ $t_{TRAN\_SYM}40\% = t_{TRAN\_PDF}40\% - t_{TRAN\_PDR}40\%$	t_{TRAN_SYM}	-7.25	0.0	7.25	µs

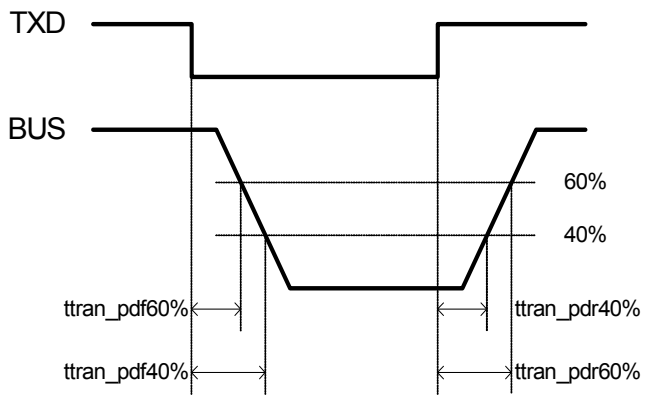


Figure 6. LIN Transmitter Timing

Table 29. Dynamic electrical characteristics - general purpose I/O - PTB4

Ratings	Symbol	Min.	Typ.	Max.	Unit
Wake-up filter time, positive edge	$t_{PTB4-PF}$	–	20	–	µs
Wake up filter time 1, negative edge	$t_{PTB4-NF1}$	350	700	1000	ns
Wake up filter time 2, negative edge	$t_{PTB4-NF2}$	0.8	1.6	2.2	us

Table 30. Dynamic electrical characteristics - general purpose I/O - PTB[1…3]

Parameter	Symbol	Min.	Typ.	Max.	Unit
GPIO Digital Frequency	f_{PTB}	–	–	5.0	MHz
Propagation Delay - Rising Edge[30]	t_{PDr}	–	–	20	ns
Rise Time - Rising Edge[30]	t_{RISE}	–	–	17.5	ns
Propagation Delay - Falling Edge[30]	t_{PDf}	–	–	20	ns
Rise Time - Falling Edge[30]	t_{FALL}	–	–	17.5	ns

Notes:
30.Load PTBx = 100 pF

Table 31. Dynamic electrical characteristics - current sense module

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency Attenuation[31],[32] • <100 Hz (f_{PASS}) • >500 Hz (f_{STOP})		 – 40	 – –	 3.0 –	dB
Signal Update Rate[33]	$f_{IUPDATE}$	0.5	–	8.0	kHz
Signal Path Match with Voltage Channel [34]	$f_{IVMATCH}$	–	2.0	–	µs
Gain Change Duration (Automatic GCB active)[34]	t_{GC}	–	–	14	µs

Notes:
31.Characteristics identical to Voltage Sense Module
32.With default LPF coefficients
33.After passing decimation filter
34.Parameter not tested. Guaranteed by design and characterization.

Table 32. Dynamic electrical characteristics - voltage sense module

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency attenuation[35],[36] • 95 to 105 Hz (f_{PASS}) • >500 Hz (f_{STOP})		 – 40	 – –	 3.0 –	dB
Signal update rate[37]	$f_{VUPDATE}$	0.5	–	8.0	kHz
Signal path match with Current Channel[38]	$f_{IVMATCH}$	–	2.0	–	µs

Notes:
35.Characteristics identical to Voltage Sense Module
36.With default LPF coefficients
37.After passing decimation filter
38.Parameter not tested. Guaranteed by design and characterization.

Table 33. Dynamic electrical characteristics - temperature sense module

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal Update Rate[39]	$f_{TUPDATE}$	1.0	–	4.0	kHz

Notes:
39.1.0 kHz with Chopper Enabled, 4.0 kHz with Chopper Disabled (fixed decimeter = 128)

4.6 S12ZI128 electrical characteristics

4.6.1 Electrical Characteristics

4.6.1.1 General

This supplement contains the most accurate electrical information for the MC9S12ZI-Family microcontroller available at the time of publication.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

4.6.1.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

Note

This classification is shown in the column labeled “C” in the parameter tables where appropriate.

- P: Those parameters are guaranteed during production testing on each individual device.
- C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
- T: Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
- D: Those parameters are derived mainly from simulations.

4.6.1.3 Power supply

The VDDD2D, VSSD2D/VSSD2D1 pin pair supplies the D2DI interface.

The VDDRX, VSSRX pin pair supplies the I/O pins.

VSSD2D & VSSD2D1 pins are internally connected by metal.

4.6.1.4 Pins

There are four groups of functional pins.

4.6.1.4.1 I/O Pins

The I/O pins have a level in the range of 3.13 V to 5.5 V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the $\overline{\text{RESET}}$ pins. Some functionality may be disabled.

4.6.1.4.2 D2DI interface

The pins D2DI interface pins have a level in the range of 2.5 V +/-5%.

4.6.1.4.3 Oscillator

The pins EXTAL, XTAL have a nominal 1.8 V level. Whenever the MCU is running on the internal clock, the oscillator pins may be used as I/O pins at a voltage level of 3.13 V to 5.5 V.

4.6.1.4.4 TEST

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.