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MMA26xx, DSI Inertial Sensor

The MMA26xx family, a SafeAssure solution, includes DSI2.5 compatible overdamped X-axis satellite accelerometers.

Features

- ± 25 g to ± 312.5 g nominal full-scale range
- Selectable 180 Hz, 2-pole, 400 Hz, 4-pole, or 800 Hz, 4-pole LPF
- DSI2.5 compatible with full support of mandatory commands
- Internal high side bus switch for DSI2.5 daisy chain applications
- 16 μ s internal sample rate, with interpolation to 1 ms
- -40 °C to 125 °C operating temperature range
- Pb-free 16-pin QFN, 6 mm x 6 mm package

Typical Applications

- Airbag front and side crash detection

Referenced Documents

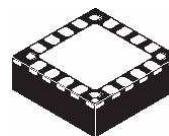
- Qualified AEC-Q100, Revision G, Grade 1 (-40°C to +125°C)
(<http://www.aecouncil.com/>)

Ordering information

Device	Axis	Range	Package	Shipping
MMA2602KGCW	X	25 g	98ASA00690D	Tubes
MMA2605KGCW	X	50 g	98ASA00690D	Tubes
MMA2606KGCW	X	62.5 g	98ASA00690D	Tubes
MMA2612KGCW	X	125 g	98ASA00690D	Tubes
MMA2618KGCW	X	187 g	98ASA00690D	Tubes
MMA2631KGCW	X	312 g	98ASA00690D	Tubes
MMA2602KGCWR2	X	25 g	98ASA00690D	Tape & Reel
MMA2605KGCWR2	X	50 g	98ASA00690D	Tape & Reel
MMA2606KGCWR2	X	62.5 g	98ASA00690D	Tape & Reel
MMA2612KGCWR2	X	125 g	98ASA00690D	Tape & Reel
MMA2618KGCWR2	X	187 g	98ASA00690D	Tape & Reel
MMA2631KGCWR2	X	312 g	98ASA00690D	Tape & Reel

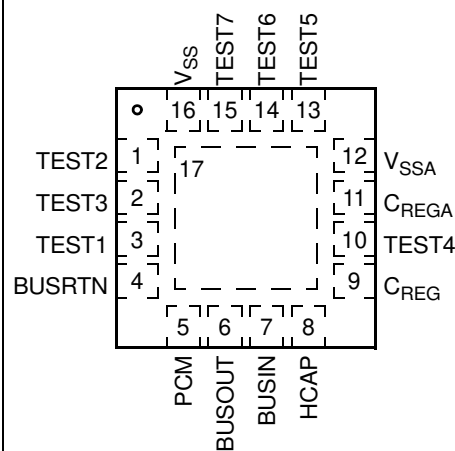
MMA26xx

Bottom View



Pb-free, 16-pin QFN
6 mm x 6 mm x 1.98 mm package

Top View



Pin connections

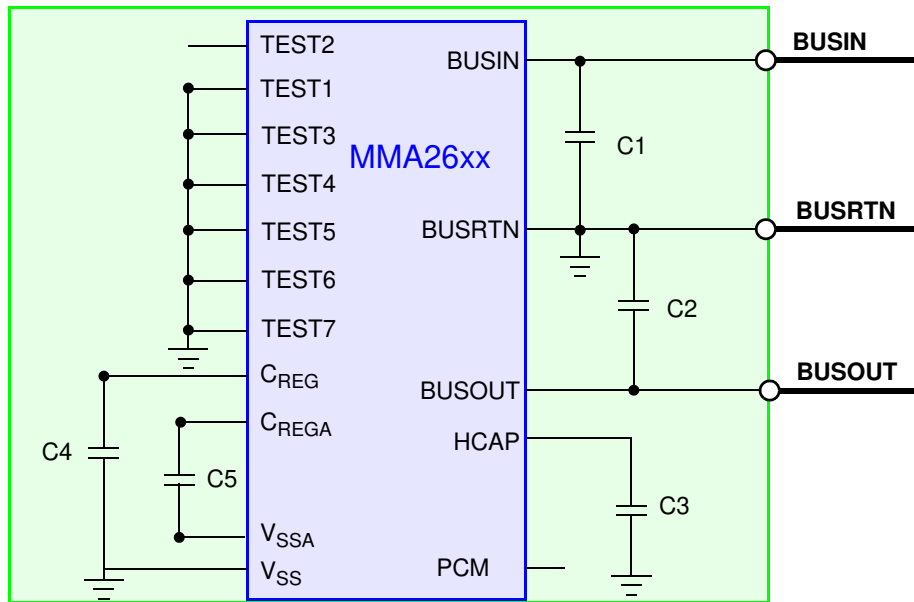


Figure 1. Application Diagram

Table 1. External Component Recommendations

Ref Des	Type	Description	Purpose
C1	Ceramic	100 pF ≤ C1 ≤ 1500 pF 10%, 50 V, X7R	BUSIN Power Supply Decoupling, ESD
C2	Ceramic	100 pF ≤ C2 ≤ 1500 pF, 10%, 50 V, X7R	BUSOUT Power Supply Decoupling, ESD
C3	Ceramic, Tantalum	1 μF ≤ C3 ≤ 100 μF, 10 %, 50 V, X7R	Reservoir Capacitor for Keep Alive during Signaling
C4	Ceramic	1 μF, 10%, 10 V, X7R	Voltage Regulator Output Capacitor (C _{REG})
C5	Ceramic	1 μF, 10%, 10 V, X7R	Voltage Regulator Output Capacitor (C _{REGA})

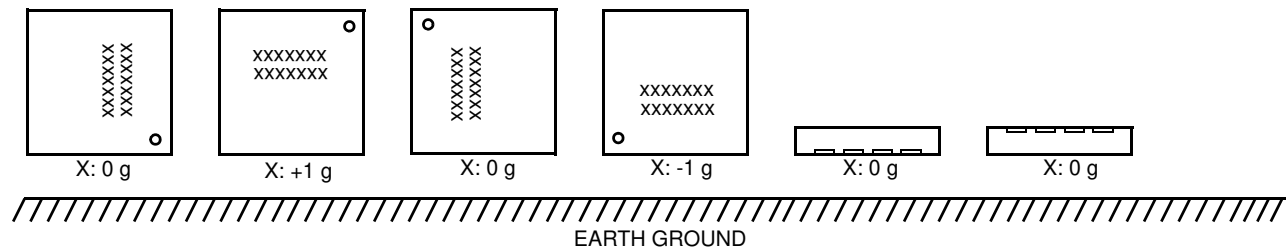


Figure 2. Device Orientation Diagram

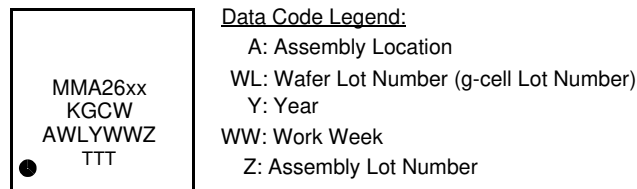


Figure 3. Part Marking

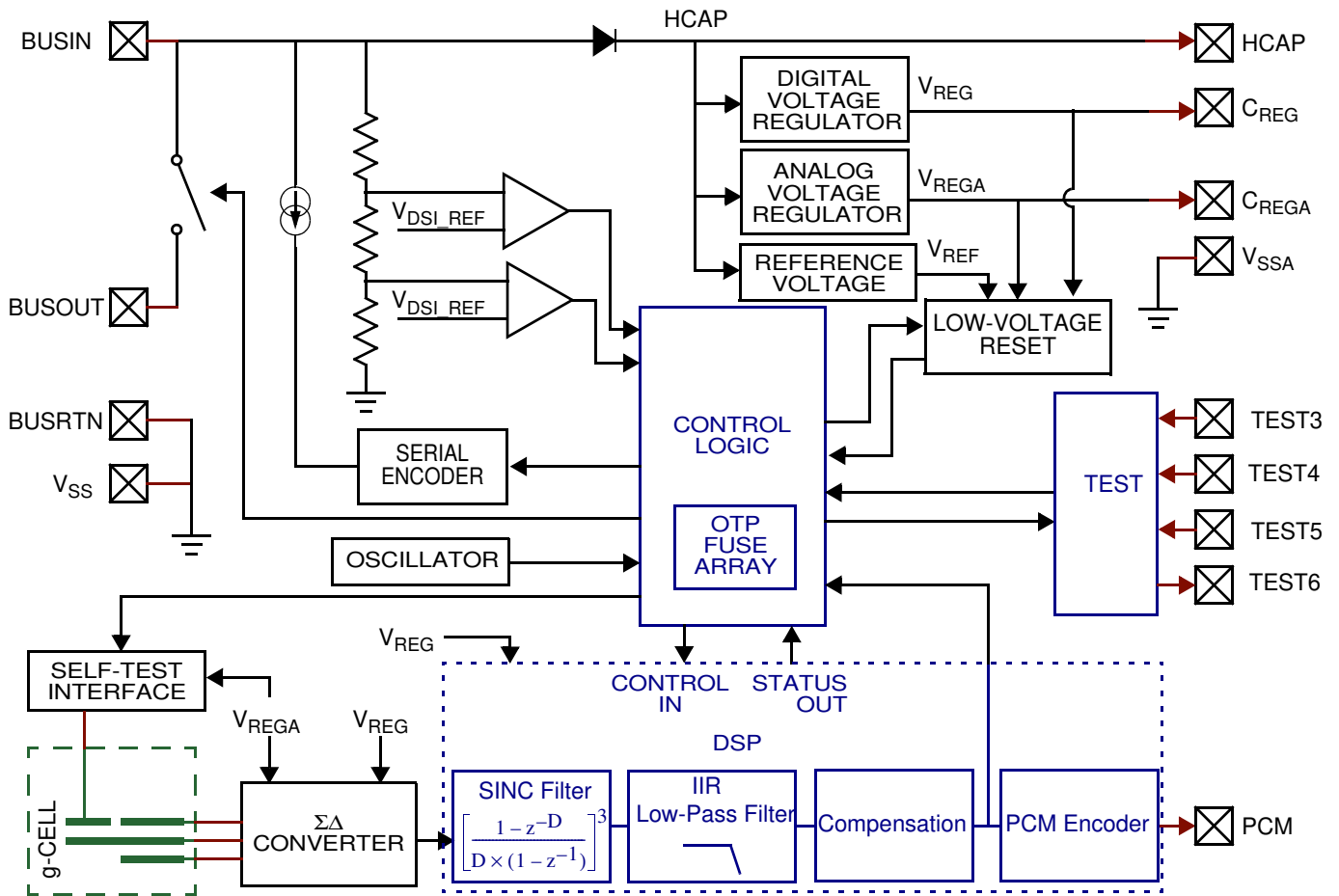


Figure 4. Internal Block Diagram

1 Pin Connections

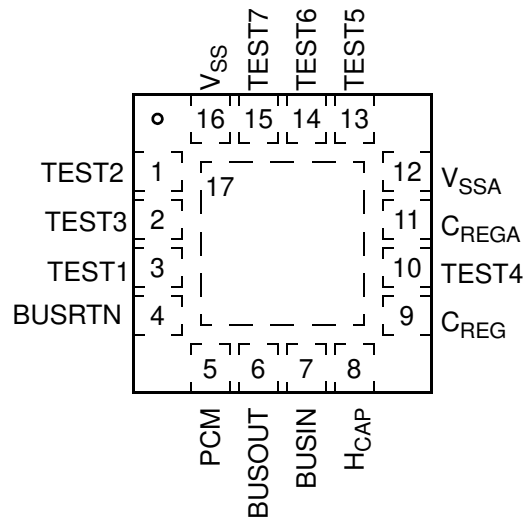


Figure 5. Pinout

Table 2. Pin Description

Pin	Pin Name	Formal Name	Definition
1	TEST2	Test Pin	This pin must be left unconnected in the application.
2	TEST3	Test Pin	This pin must be grounded in the application.
3	TEST1	Test Pin	This pin must be grounded in the application.
4	BUSRTN	Ground	This pin is the common return for power and signalling.
5	PCM	PCM Output	This pin provides a 4 MHz PCM signal proportional to the acceleration data for test purposes. The output can be enabled or disabled via OTP. If unused, this pin must be left unconnected in the application. Reference Section 3.5.3.6 .
6	BUSOUT	BUS output	This pin is internally connected to BUSIN through a switch. For daisy chain configurations, this pin is connected to the BUSIN pin of the next slave on the DSI bus. The internal bus switch is open following reset, and is closed when an Initialization command is received.
7	BUSIN	Supply / Comm	This pin is connected to the DSI positive bus node and provides the power supply and communication to the system master. An external capacitor must be connected between this pin and the BUSRTN pin. Reference Figure 1 .
8	HCAP	Hold Capacitor	This pin rectifies the supply voltage on the BUSIN pin to create the supply voltage for the device. An external capacitor must be connected between this pin and the BUSRTN pin to store energy for operation during master communication signalling. Reference Figure 1 .
9	C _{REG}	Digital Supply	This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V _{SS} . Reference Figure 1 .
10	TEST4	Test Pin	This pin must be grounded in the application.
11	C _{REGA}	Analog Supply	This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V _{SSA} . Reference Figure 1 .
12	VSSA	Analog GND	This pin is the power supply return node for analog circuitry.
13	TEST5	Test Pin	This pin enables test mode, and provides the SPI programming voltage in test mode. This pin is must be grounded in the application.
14	TEST6	Test Pin	This pin must be grounded in the application.
15	TEST7	Test Pin	This pin must be grounded in the application.
16	V _{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
17	PAD	Die Attach Pad	This pin is the die attach flag, and should be connected to VSS in the application. Reference Section 5 .

Table 2. Pin Description

Pin	Pin Name	Formal Name	Definition
	Corner Pads	Corner Pads	The corner pads are internally connected to V_{SS} .

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. Do not apply voltages higher than those shown in the table below.

#	Rating	Symbol	Value	Unit	
1	Supply Voltage (continuous) (BUSIN,BUSOUT, HCAP)	V_{CC}	-0.3 to +30.0	V	(3)
2	Supply Voltage (pulsed < 400 ms, repetition rate 60s) (BUSIN,BUSOUT, HCAP)	V_{CC}	-0.3 to +34.0	V	(3)
3	C_{REG} , C_{REGA} , PCM, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7		-0.3 to +3.0	V	(3)
4	BUSIN,BUSOUT, BUSRTN and HCAP Current	I_{IN}	400	mA	(3)
5	Maximum duration 1 s Continuous	I_{IN}	75	mA	(3)
6	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	± 2000	g	(5)
7	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	± 2000	g	(5)
8	Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation)	h_{DROP}	1.2	m	(5)
9	Electrostatic Discharge (per AECQ100)	V_{ESD}	± 2000	V	(5)
10	HBM (100 pF, 1.5 k Ω)	V_{ESD}	± 500	V	(5)
11	CDM (R = 0 Ω) MM (200 pF, 0 Ω)	V_{ESD}	± 200	V	(5)
12	Temperature Range	T_{stg}	-40 to +125	$^{\circ}C$	(3)
13	Storage Junction	T_J	-40 to +150	$^{\circ}C$	(3)
14	Thermal Resistance	θ_{JC}	2.5	$^{\circ}C/W$	(11)

2.2 Operating Range

The operating ratings are the limits normally expected in the application.

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
15	Supply Voltage	V_L	6.3	—	V_H	V	(1,12)
16	V_{HCAP} BUSIN	V_{HCAP} V_{BUS}	-0.3	—	30	V	(1,12)
17	Programming Voltage Applied to BUSIN (DSI)	V_{PP}	14.0	—	30.0	V	(3)
18	Programming Current BUSIN	I_{PP}	85	—	—	mA	(3)
19	Operating Temperature Range	T_L	-40	—	T_H	$^{\circ}C$	(1)
20		T_A	-40	—	+105 +125	$^{\circ}C$	(3)

2.3 Electrical Characteristics - Supply and I/O

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units		
21	Quiescent Supply Current *	I_{DD}	—	—	8.0	mA	(1)	
22	Inrush Current (excluding HCAP Capacitor charge current) Power On until V_{REG} Stable	I_{INRUSH}	—	—	20	mA	(3)	
23	Internally Regulated Voltages	V_{REG}	2.425	2.50	2.575	V	(1)	
24		V_{REGA}	2.425	2.50	2.575	V	(1)	
25	V_{HCAP} Under-Voltage Detection (See Figure 6) Under-Voltage Detection Threshold	$V_{PORHCAP_f}$	5.8	6.0	6.2	V	(3,6)	
26		$V_{PORHCAP_r}$	—	—	6.3	V	(3,6)	
27		Hysteresis ($V_{PORHCAP_r} - V_{PORHCAP_f}$)	V_{HYST_HCAP}	70	100	140	mV	(3)
28	Internal Regulator Low Voltage Detection Threshold	$V_{PORVREG_f}$	2.15	2.25	2.40	V	(3,6)	
29		$V_{PORVREGA_f}$	2.15	2.25	2.40	V	(3,6)	
30		Hysteresis	V_{HYST_VREG}	0.05	0.10	0.15	V	(3)
31		V_{HYST_VREGA}	0.05	0.10	0.15	V	(3)	
32	External Capacitor (C_{REG} , C_{REGA}) Capacitance	C_{REG} , C_{REGA}	500	1000	1500	nF	(9)	
33		ESR (including interconnect resistance)	R_{CREG} , $R_{CREGESR}$, R_{CREGAE} , $R_{CREGASER}$	—	—	200	m Ω	(9)
34	Output High Voltage (PCM) $I_{Load} = 100 \mu A$	V_{OH}	$V_{REG} - 0.1$	—	—	V	(9)	
35	Output Low Voltage (PCM) $I_{Load} = 100 \mu A$	V_{OL}	—	—	0.1	V	(9)	

2.4 Electrical Characteristics - DSI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
36	BUSOUT Bus Switch Resistance $0V \leq V_{BUSIN} \leq 30V$, $I_{SW} = 160mA$	R_{SW}	—	4.0	8.0	Ω	(1)
37	HCAP Rectifier Leakage Current $V_{BUSIN} = 0V$, $V_{HCAP} = 9.0V$	I_{RLKG}	—	—	100	μA	(1)
38	BUSIN to HCAP Rectifier Voltage Drop ($V_{BUSIN} = 7V$) $I_{HCAP} = -15mA$ $I_{HCAP} = -100mA$	V_{RECT}	—	0.75	1.0	V	(1)
39		V_{RECT}	—	0.9	1.2	V	(1)
40	BUSIN Bias Current $V_{BUSIN} = 8.0V$, $V_{HCAP} = 9.0V$ $V_{BUSIN} = 4.5V$, $V_{HCAP} = 24V$, No Response Current	I_{BUSIN_BIAS}	0	—	100	μA	(1)
41		I_{BUSIN_BIAS}	0	—	100	μA	(1)
42	BUSOUT Bias Current $V_{BUSOUT} = 8.0V$, $V_{HCAP} = 9.0V$ $V_{BUSOUT} = 4.5V$, $V_{HCAP} = 24V$, No Response Current	I_{BUSOUT_BIAS}	0	—	100	μA	(1)
43		I_{BUSOUT_BIAS}	0	—	100	μA	(1)
44	BUSOUT Discharge Resistance	$R_{BUSOUT_Discharge}$	3500	—	8000	Ω	(3)
45	BUSIN Response Current $V_{BUSIN} = 4.0V$	I_{RESP}	9.9	11	12.1	mA	(1)
46	BUSIN to BUSOUT Leakage Current (BUS SWITCH open) $V_{BUSIN} = 24.0V$, $V_{BUSOUT} = 0V$ $V_{BUSIN} = 0V$, $V_{BUSOUT} = 16V$	I_{SW_Leak}	-20	—	20	μA	(1)
47		I_{RSW_Leak}	-20	—	20	μA	(1)
48	BUSIN Logic Thresholds Signal Threshold Frame Threshold	V_{THS}	2.8	3.0	3.2	V	(1)
49		V_{THF}	5.5	6.0	6.5	V	(1)
50	BUSIN Logic Hysteresis Signal Frame	V_{HYSS}	30	—	90	mV	(3)
51		V_{HYSF}	100	—	300	mV	(3)

2.5 Electrical Characteristics - Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
52	Sensitivity (10-bit @ 100Hz referenced to 0Hz) 25g Range	* SENS	—	20.48	—	LSB/g	(1,14)
53	50g Range	* SENS	—	10.24	—	LSB/g	(1,14)
54	62.5g Range	* SENS	—	8.192	—	LSB/g	(1,14)
55	125g Range	* SENS	—	4.096	—	LSB/g	(1,14)
56	187g Range	* SENS	—	2.731	—	LSB/g	(1,14)
57	312g Range	* SENS	—	1.638	—	LSB/g	(1,14)
58	Total Sensitivity Error (including non-linearity) $T_A = 25^\circ\text{C}$	* ΔSENS_{25}	-5	—	+5	%	(1)
59	$T_L \leq T_A \leq T_H$	* ΔSENS	-7	—	+7	%	(1)
60	Digital Offset 10-bit output	* $\text{OFF}_{10\text{Bit}}$	460	512	564	LSB	(1)
61	Range of Output (10-Bit Mode) Acceleration	$\text{RANGE}_{\text{ACC}}$	1	—	1023	LSB	(3)
62	Internal Error	$\text{RANGE}_{\text{ERR}}$	—	0	—	LSB	(3)
63	Cross-Axis Sensitivity Z-axis to X-axis	V_{ZX}	-5	—	+5	%	(3)
64	Y-axis to X-axis	V_{YX}	-5	—	+5	%	(3)
65	ADC Output Noise Peak (1 Hz - 1 kHz, 10-Bit)	η_{SD}	-4	—	+4	LSB	(3)
66	System Output Noise (10-Bit, RMS, All Ranges)	η_{RMS}	—	—	+1.2	LSB	(3)
67	Non-linearity (all ranges) 10-bit output, Range < 50g	$\text{NL}_{\text{OUT_sub50g}}$	-2	—	+2	%	(3)
68	10-bit output, $50\text{g} \leq \text{Range} \leq 312.5\text{g}$	$\text{NL}_{\text{OUT_sub250g}}$	-2	—	+2	%	(3)

2.6 Electrical Characteristics - Self-Test and Overload

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
69	Acceleration (without hitting internal g-cell stops) ±25g, ±50g, ±62.5g, ±125g	$g_{g-cell_Clip60X}$	400	456	500	g	(9)
70	Acceleration (without hitting internal g-cell stops) ±187g, ±312g	$g_{g-cell_Clip240X}$	1750	2065	2300	g	(9)
71	ΣΔ and Sinc Filter Clipping Limit ±25g	$g_{ADC_Clip60X}$	98	108	121	g	(9)
72	ΣΔ and Sinc Filter Clipping Limit ±50g	$g_{ADC_Clip60X}$	191	210	232	g	(9)
73	ΣΔ and Sinc Filter Clipping Limit ±62.5g	$g_{ADC_Clip60X}$	191	210	232	g	(9)
74	ΣΔ and Sinc Filter Clipping Limit ±125g	$g_{ADC_Clip120X}$	353	379	409	g	(9)
75	ΣΔ and Sinc Filter Clipping Limit ±187g	$g_{ADC_Clip240X}$	1690	1876	2106	g	(9)
76	ΣΔ and Sinc Filter Clipping Limit ±312g	$g_{ADC_Clip480X}$	1690	1876	2106	g	(9)
77	Deflection, 10-Bit, Self-Test - Offset, 30 sample ave, $T_A = 25^\circ\text{C}$) ±25g Range *	$\Delta\text{DFLCT_X25}$	—	246	—	LSB	(1)
78	±50g Range *	$\Delta\text{DFLCT_X50}$	—	123	—	LSB	(1)
79	±62.5g Range *	$\Delta\text{DFLCT_X62}$	—	98	—	LSB	(1)
80	±125g Range *	$\Delta\text{DFLCT_X125}$	—	49	—	LSB	(1)
81	±187g Range *	$\Delta\text{DFLCT_X187}$	—	82	—	LSB	(1)
82	±312g Range *	$\Delta\text{DFLCT_X312}$	—	49	—	LSB	(1)
83	Self-test deflection range, $T_A = 25^\circ\text{C}$	ΔDFLCT	-10	—	+10	%	(1)
84	Self-test deflection range, $T_L \leq T_A \leq T_H$	ΔDFLCT	-20	—	+20	%	(1)

2.7 Dynamic Electrical Characteristics - DSI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
85	Reset Recovery (See Figure 21) POR negated to 1st DSI Command (Initialization Command)	t_{DSI_INIT}	—	$400 / f_{OSC}$	—	s	(7)
86	POR negated to Acceleration Data Valid (Including LPF Init)	t_{DSP_INIT}	—	—	$10000 / f_{OSC}$	s	(7)
87	DSI Clear Command to 1st DSI Command (Initialization Command)	t_{DSI_INIT}	—	$400 / f_{OSC}$	—	s	(7)
88	DSI Clear Command to Acceleration Data Valid (Including LPF Init)	t_{DSP_INIT}	—	—	$10000 / f_{OSC}$	s	(7)
89	HCAP Under-Voltage Reset Delay (See Figure 6) $V_{HCAP} < V_{PORHCAP_f}$ to POR assertion	t_{HCAP_POR}	—	$880 / f_{OSC}$	—	s	(7)
90	V_{REG} Under-Voltage Reset Delay (See Figure 7) $V_{REG} < V_{PORVREG_f}$ to POR assertion	t_{VREG_POR}	—	—	5	μ s	(3)
91	V_{REGA} Under-Voltage Reset Delay (See Figure 8) $V_{REGA} < V_{PORVREGA_f}$ to POR assertion	t_{VREGA_POR}	—	—	5	μ s	(3)
92	V_{REG} : V_{REGA} Capacitor Monitor POR to first Capacitor Test Disconnect	$t_{POR_CAPTEST}$	—	$12000 / f_{OSC}$	—	s	(7)
93	Disconnect Time ()	$t_{CAPTEST_TIME}$	—	$6 / f_{OSC}$	—	s	(7)
94	Disconnect Rate ()	$t_{CAPTEST_RATE}$	—	$256 / f_{OSC}$	—	s	(7)
95	Initialization to Bus Switch Closing	t_{BS}	89	—	138	μ s	(7)
96	BUSOUT Discharge Resistance Activation Time	$t_{BUSOUT_Discharge}$	9.5	10	10.5	μ s	(3)
97	Communication Data Rate	D_{RATE}	100	—	200	kbps	(7)
98	Loss of Signal Reset Time Maximum time below frame threshold	t_{TO}	2.00	—	4.00	ms	(7)
99	BUSIN Response Current Slew Rate 1.0 mA to 9.0 mA, 9.0 to 1.0 mA	t_{ITR}	0.33	—	10.0	mA/ μ s	(3)
100	BUSIN Timing to Response Current BUSIN Negative Voltage Transition =3.0V to $I_{RSP} = 7.0$ mA rise	t_{RSP_R}	—	—	2.50	μ s	(7)
101	BUSIN Negative Voltage Transition =3.0V to $I_{RSP} = 5.0$ mA fall	t_{RSP_F}	—	—	2.50	μ s	(7)
102	DSI BUSIN Signal Duty Cycle Logic '0'	D_{CL}	10	33	40	%	(7)
103	Logic '1'	D_{CH}	60	67	90	%	(7)
104	Inter-frame Separation Time (See Figure 9) Following Read Write NVM Command	t_{IFS}	12	—	—	ms	(7)
105	Following Initialization, BS = 1	t_{IFS}	200	—	—	μ s	(7)
106	Following Initialization, BS = 0	t_{IFS}	20	—	—	μ s	(7)
107	Following other DSI bus commands	t_{IFS}	20	—	—	μ s	(7)
108	DSI Data Latency	t_{LAT_DSI}	$4 / f_{OSC}$	—	$5 / f_{OSC}$	s	(7)
109	Bus Switch Open Time Reset Asserted to $I_{SW_LEAK} \leq 20$ μ A	t_{BSOPEN}	—	—	500	μ s	(3)
110	Self-Test Response Time Self-Test Activation time (EOF _{Slave} to 90% Δ DFLCT _{xxx} , 180 Hz LPF)	$t_{ST_ACT_180}$	2.00	—	5.00	ms	(7)
111	Self-Test Deactivation time (EOF _{Slave} to 10% Δ DFLCT _{xxx} , 180 Hz LPF)	$t_{ST_DEACT_180}$	2.00	—	5.00	ms	(7)
112	Self-Test Activation time (EOF _{Slave} to 90% Δ DFLCT _{xxx} , 400 Hz LPF)	$t_{ST_ACT_400}$	1.00	—	2.50	ms	(7)
113	Self-Test Deactivation time (EOF _{Slave} to 10% Δ DFLCT _{xxx} , 400 Hz LPF)	$t_{ST_DEACT_400}$	1.00	—	2.50	ms	(7)
114	Self-Test Activation time (EOF _{Slave} to 90% Δ DFLCT _{xxx} , 800 Hz LPF)	$t_{ST_ACT_800}$	0.50	—	1.75	ms	(7)
115	Self-Test Deactivation time (EOF _{Slave} to 10% Δ DFLCT _{xxx} , 800 Hz LPF)	$t_{ST_DEACT_800}$	0.50	—	1.75	ms	(7)
116	Error Detection Response Time Mirror Register CRC Error to Status Flag (S) set (Factory or User Array)	t_{CRC_Err}	—	$75 / f_{OSC}$	—	s	(7)

2.8 Dynamic Electrical Characteristics - Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
117	Internal Oscillator Frequency *	f_{OSC}	3.80	4	4.20	MHz	(1)
118	Data Interpolation Latency	t_{LAT_INTERP}	$64 / f_{OSC}$	—	$65 / f_{OSC}$	s	(7)
119	DSP Low-Pass Filter						
120	Cutoff frequency LPF0 (referenced to 0 Hz)	f_{C_LPF0}	171	180	189	Hz	(7)
121	Filter Order LPF0	O_{LPF0}	—	2	—	1	(7)
122	Cutoff frequency LPF1 (referenced to 0 Hz)	f_{C_LPF1}	380	400	420	Hz	(7)
123	Filter Order LPF1	O_{LPF1}	—	4	—	1	(7)
124	Cutoff frequency LPF2 (referenced to 0 Hz)	f_{C_LPF2}	760	800	840	Hz	(7)
125	Filter Order LPF2	O_{LPF2}	—	4	—	1	(7)
125	Sensing Element Rolloff Frequency (-3db) $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$	$f_{gcell_3dB_xlo}$	938	—	2592	Hz	(9)
126	$\pm 187g, \pm 312g$	$f_{gcell_3dB_xhi}$	3952	—	14370	Hz	(9)
127	Sensing Element Natural Frequency $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$	f_{gcell_xlo}	12651	—	13871	Hz	(9)
128	$\pm 187g, \pm 312g$	f_{gcell_xhii}	26000	—	28700	Hz	(9)
129	Sensing Element Damping Ratio $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$	ζ_{gcell_xlo}	2.760	—	6.770	—	(9)
130	$\pm 187g, \pm 312g$	ζ_{gcell_xhi}	1.260	—	3.602	—	(9)
131	Sensing Element Delay (@100Hz) $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$	$f_{gcell_delay100_xlo}$	63	—	170	μs	(9)
132	$\pm 187g, \pm 312g$	$f_{gcell_delay100_xhi}$	13	—	40	μs	(9)
133	Package Resonance Frequency	$f_{Package}$	100	—	—	kHz	(9)

Notes:

- Parameters tested 100% at final test at -40°C, 25°C, and 105°C.
- Parameters tested 100% at probe.
- Verified by characterization.
- * Indicates critical characteristic.
- Verified by qualification testing, not tested in production.
- Parameters verified by pass/fail testing in production.
- Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
- Verified by user system level characterization, not tested in production, or at component level.
- Verified by Simulation.
- Measured at final test. Self-test activation occurs under control of the test program.
- Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
- Maximum voltage characterized. Minimum voltage tested 100% at final test. Maximum voltage tested 100% to 24 V at final test.
- N/A.
- Sensitivity, and overload capability specifications will be reduced when 800Hz filter is selected.
- Filter cut-off frequencies are directly dependent upon the internal oscillator frequency.
- Target values. Actual values to be determined during device characterization.

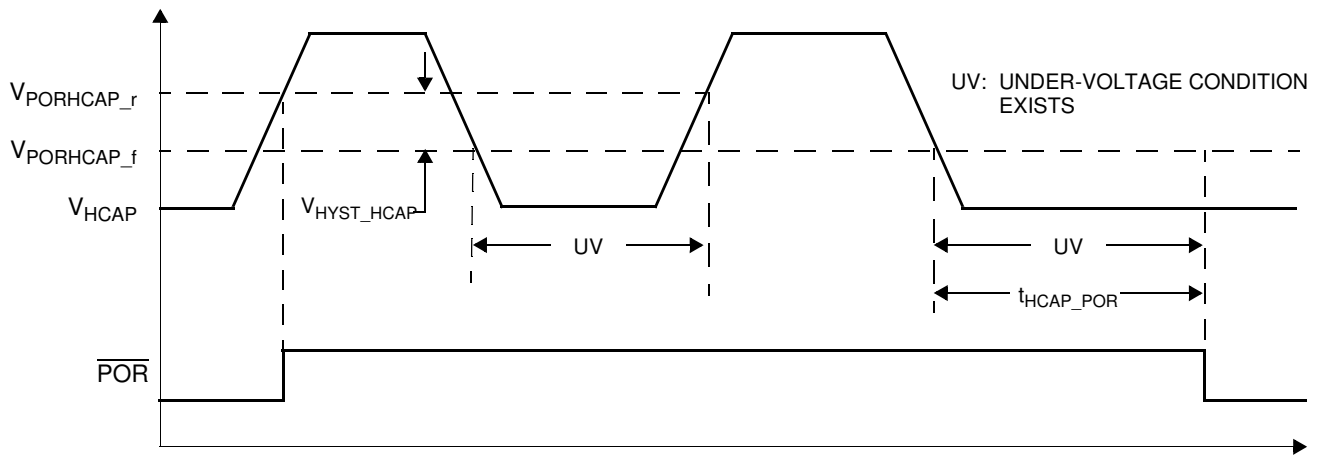


Figure 6. V_{HCAP} Under-Voltage Detection

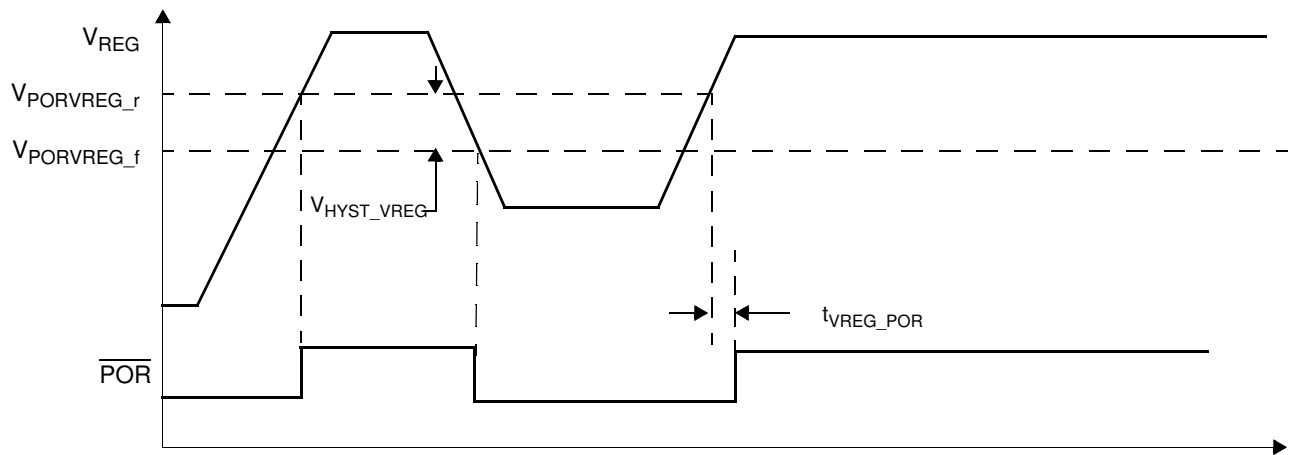


Figure 7. V_{REG} Under-Voltage Detection

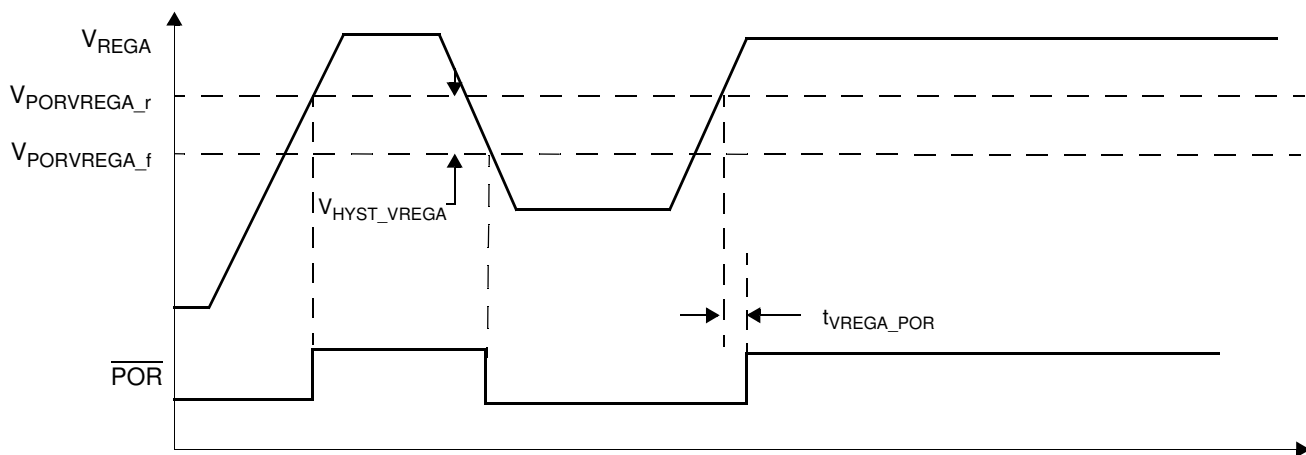


Figure 8. V_{REGA} Under-Voltage Detection

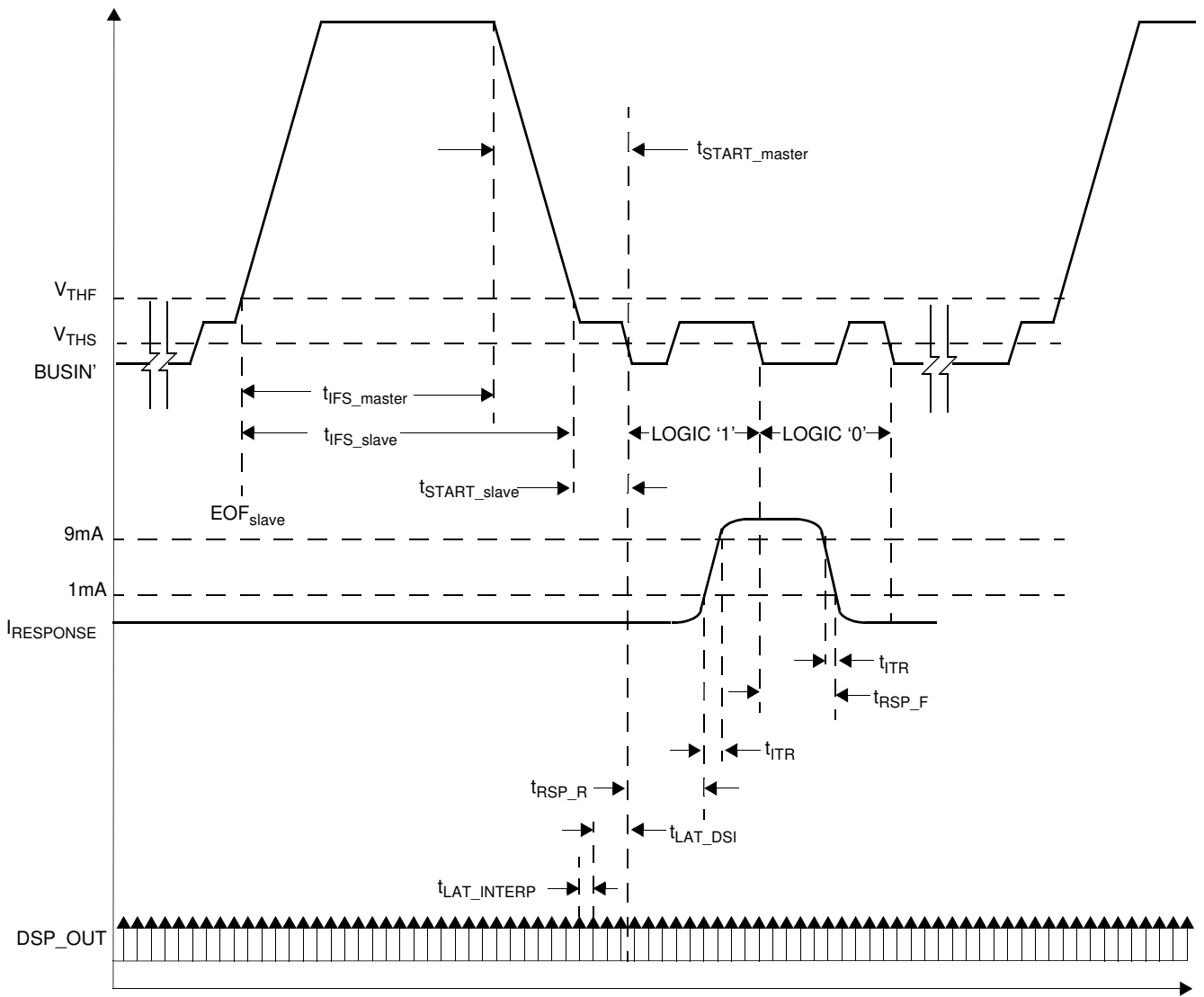


Figure 9. DSI Bus Inter-frame Timing

3 Functional Description

3.1 User Accessible Data Array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable array, an OTP user programmable array, and read only registers for device status. The OTP arrays incorporate independent error detection for fault detection (reference [Section 3.2](#)). Portions of the factory programmable array are reserved for factory-programmed trim values. The user accessible data is shown in the table below.

Table 3. User Accessible Data

Byte Addr RA[3:0]	Register	Nibble Addr WA[3:0]	Bit Function				Nibble Addr (WA[3:0])	Bit Function				Type	
			7	6	5	4		3	2	1	0		
\$00	SN0		SN[7]	SN[6]	SN[5]	SN[4]		SN[3]	SN[2]	SN[1]	SN[0]	F	
\$01	SN1		SN[15]	SN[14]	SN[13]	SN[12]		SN[11]	SN[10]	SN[9]	SN[8]		
\$02	SN2		SN[23]	SN[22]	SN[21]	SN[20]		SN[19]	SN[18]	SN[17]	SN[16]		
\$03	SN3		SN[31]	SN[30]	SN[29]	SN[28]		SN[27]	SN[26]	SN[25]	SN[24]		
\$04	TYPE	Reference Table 40	LPF[1]	LPF[0]	1	0	Reference Table 40	RNG[3]	RNG[2]	RNG[1]	RNG[0]	U/F	
\$05	DEVCFG		DEVID	0	0	0		0	0	0	0		0
\$06	DEVCFG1		0	0	0	0		0	0	AT_OTP[1]	AT_OTP[0]		
\$07	DEVCFG2		LOCK_U	0	PCM	0		ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]		
\$08	UD01		UD01[7]	UD01[6]	UD01[5]	UD01[4]		UD01[3]	UD01[2]	UD01[1]	UD01[0]		
\$09	UD02		UD02[7]	UD02[6]	UD02[5]	UD02[4]		UD02[3]	UD02[2]	UD02[1]	UD02[0]		
\$0A	UD03		UD03[7]	UD03[6]	UD03[5]	UD03[4]		UD03[3]	UD03[2]	UD03[1]	UD03[0]		
\$0B	UD04		UD04[7]	UD04[6]	UD04[5]	UD04[4]		UD04[3]	UD04[2]	UD04[1]	UD04[0]		
\$0C	UD05		UD05[7]	UD05[6]	UD05[5]	UD05[4]		UD05[3]	UD05[2]	UD05[1]	UD05[0]		
\$0D	UD06		UD06[7]	UD06[6]	UD06[5]	UD06[4]		UD06[3]	UD06[2]	UD06[1]	UD06[0]		
\$0E	UD07		UD07[7]	UD07[6]	UD07[5]	UD07[4]		UD07[3]	UD07[2]	UD07[1]	UD07[0]		
\$0F	UD08		UD08[7]	UD08[6]	UD08[5]	UD08[4]		0	0	0	0		

Type codes

F: NXP programmed OTP location

U/F: User and/or NXP programmed OTP location

Note: Unused and Unprogrammed Spare bits always read '0'.

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each device during manufacturing. The serial number is composed of the following information:

Bit Range	Content
SN[12:0]	Serial Number
SN[31:13]	Lot Number

Serial numbers begin at 1 for all produced devices in each lot, and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the factory programmed OTP CRC verification. Reference [Section 3.2.1](#) for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Device Type Register (TYPE)

The Device Type Register is an OTP configuration register which contains device configuration information. Bit 5 - Bit 0 are factory programmed and are included in the factory programmed OTP CRC verification. These bits are read only to the user. Bit 7 - Bit 6 are user programmable OTP bits and are included in the user programmable OTP error detection.

Table 4. Factory Configuration Register

Location		Bit									
RA[3:0]	Register	WA[3:0]	7	6	5	4	WA[3:0]	3	2	1	0
\$04	TYPE	Bank0 \$08	LPF[1]	LPF[0]	1	0		RNG[3]	RNG[2]	RNG[1]	RNG[0]
Factory Default			0	0	1	0		0	0	0	0

3.1.2.1 Low-Pass Filter Selection Bits (LPF[1:0]) (TYPE[7:6])

The Low Pass Filter selection bit selects between one of three low pass filter options. These bits can be factory or user programmed.

LPF[1]	LPF[0]	Low Pass Filter Selected
0	0	400 Hz, 4-Pole
0	1	Not Enabled ¹
1	0	180 Hz, 2-Pole
1	1	800 Hz, 4-Pole

¹This filter option is not implemented. LPF[1:0] must not be set to this value to guarantee proper operation and performance.

3.1.2.2 Range Selection Bits (RNG[3:0]) (TYPE[3:0])

The Range Selection Bits indicate the full-scale range of the device, as shown below. These bits are factory programmed.

RNG[3]	RNG[2]	RNG[1]	RNG[0]	Full-Scale Range	g-Cell Design
0	0	0	0	N/A	N/A
0	0	0	1	25g	Medium-g
0	0	1	0	50g	Medium-g
0	0	1	1	62g	Medium-g
0	1	0	0	125g	Medium-g
0	1	0	1	187g	High-g
0	1	1	0	312g	High-g
0	1	1	1	N/A	N/A
1	0	0	0	Reserved	N/A
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

3.1.3 Device Configuration Register (DEVCFG)

The Device configuration register is a user programmable OTP register which contains device configuration information. This register is included in the user register error detection. Refer to [Section 3.2.2](#) for details regarding the user programmable OTP array.

Table 5. Device Configuration Register

Location		Bit									
RA[3:0]	Register	WA[3:0]	7	6	5	4	WA[3:0]	3	2	1	0
\$05	DEVCFG	Bank0 \$0A	DEVID	0	0	0	Bank0 \$09	0	0	0	0
Factory Default			1	0	0	0		0	0	0	0

3.1.3.1 Device ID Bit (DEVCFG[7])

The Device ID Bit is a user programmable bit which allows the user to select between 2 device IDs. The Device ID is transmitted in response to the Request ID DSI command. Reference [Section 4.2.1.5](#) for more information regarding the Request ID DSI command. This bit can be factory or user programmed.

DEVID	Device ID
0	'00110'
1	'00100'

3.1.4 Device Configuration Register 1 (DEVCFG1)

The Device configuration register is a user programmable OTP register which contains device configuration information. This register is included in the user register error detection. Refer to [Section 3.2.2](#) for details.

Table 6. Device Configuration Register 1

Location		Bit									
RA[3:0]	Register	WA[3:0]	7	6	5	4	WA[3:0]	3	2	1	0
\$06	DEVCFG1	Bank2 \$06	0	0	0	0	Bank1 \$06	0	0	AT_OTP[1]	AT_OTP[0]
Factory Default			0	0	0	0		0	0	0	0

3.1.4.1 Attribute Bits (AT_OTP[1:0], DEVCFG1[1:0])

The Attribute Bits are user defined bits which are transmitted in response to the Request Status, Disable Self-Test Stimulus or Enable Self-Test Stimulus DSI commands. The transmitted values are qualified by the LOCK_U bit as shown in the table below. These bits can be factory or user programmed.

LOCK_U	DEVCFG1 Values		DSI Transmitted Values	
	AT_OTP[1]	AT_OTP[0]	AT[1]	AT[0]
0	X	X	1	0
1	0	0	0	0
	0	1	0	1
	1	0	1	0
	1	1	1	1

3.1.5 Device Configuration Register 2 (DEVCFG2)

Device configuration register 2 is a user programmable OTP register which contains device configuration information. This register is included in the user register error detection. Refer to [Section 3.2.2](#) for details.

Table 7. Device Configuration Register 2

Location		Bit									
RA[3:0]	Register	WA[3:0]	7	6	5	4	WA[3:0]	3	2	1	0
\$07	DEVCFG2	Bnk0 \$07 Bnk2 \$07 Bnk3 \$07 Bnk3 \$0F	LOCK_U	0	PCM	0	Bnk1 \$07	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]
Factory Default			0	0	0	0		0	0	0	0

3.1.5.1 User Configuration Lock Bit (LOCK_U, DEVCFG2[7])

The LOCK_U bit is a factory or user programmed OTP bit which inhibits writes to the user configuration array when active. Reference [Section 3.2.2](#) for details regarding the LOCK_U bit and error detection.

3.1.5.2 PCM Bit (DEVCFG2[5])

The PCM Bit enables the PCM output pin. When the PCM bit is set, the PCM output pin is active and outputs a Pulse Code Modulated signal proportional to the acceleration response. Reference [Section 3.5.3.6](#) for more information regarding the PCM output. When the PCM output is cleared, the PCM output pin is actively pulled low. This bit can be factory or user programmed.

3.1.5.3 Device Address (ADDR[3:0], DEVCFG2[3:0])

The Device Address bits define the preprogrammed DSI Bus device address. If the Device Address bits are programmed to '0000', there is not preprogrammed address, and the address must be assigned via the Initialization DSI command. Reference [Section 4.2.1.1](#) for more details regarding the Initialization DSI command. These bits can be factory or user programmed.

3.1.6 User Data Registers (UDx)

The User Data Registers are user programmable OTP register which can be programmed with user or assembly specific information. These registers have no impact on the device performance, but are included in the user register error detection. Refer to [Section 3.2.2](#) for details.

Location		Bit									
RA[3:0]	Register	WA[3:0]	7	6	5	4	WA[3:0]	3	2	1	0
\$08	UD01	Bnk2 \$08	UD01[7]	UD01[6]	UD01[5]	UD01[4]	Bnk1 \$08	UD01[3]	UD01[2]	UD01[1]	UD01[0]
\$09	UD02	Bnk2 \$09	UD02[7]	UD02[6]	UD02[5]	UD02[4]	Bnk1 \$09	UD02[3]	UD02[2]	UD02[1]	UD02[0]
\$0A	UD03	Bnk2 \$0A	UD03[7]	UD03[6]	UD03[5]	UD03[4]	Bnk1 \$0A	UD03[3]	UD03[2]	UD03[1]	UD03[0]
\$0B	UD04	Bnk2 \$0B	UD04[7]	UD04[6]	UD04[5]	UD04[4]	Bnk1 \$0B	UD04[3]	UD04[2]	UD04[1]	UD04[0]
\$0C	UD05	Bnk2 \$0C	UD05[7]	UD05[6]	UD05[5]	UD05[4]	Bnk1 \$0C	UD05[3]	UD05[2]	UD05[1]	UD05[0]
\$0D	UD06	Bnk2 \$0D	UD06[7]	UD06[6]	UD06[5]	UD06[4]	Bnk1 \$0D	UD06[3]	UD06[2]	UD06[1]	UD06[0]
\$0E	UD07	Bnk2 \$0E	UD07[7]	UD07[6]	UD07[5]	UD07[4]	Bnk1 \$0E	UD07[3]	UD07[2]	UD07[1]	UD07[0]
\$0F	UD08	Bnk2 \$0F	UD08[7]	UD08[6]	UD08[5]	UD08[4]		0	0	0	0
Factory Default			0	0	0	0		0	0	0	0

3.2 OTP Array Lock and Error Detection

3.2.1 Factory Programmed OTP Array Lock and Error Detection

The Factory programmed OTP array is verified for errors with a 3-bit CRC. The CRC verification is enabled only when the Factory programmed OTP array is locked and the lock is active. The lock is active only after an automatic OTP readout in which the internal lock bit is read as '1'. Automatic OTP readouts occur only after POR or a DSI Clear Command is received.

Factory Lock Bit Value in Fuse Array	Lock Bit Value in Mirror Register After Automatic Readout	Lock Bit Active?	CRC Verification Enabled?
0	N/A	NO	NO
1	0	NO	NO
1	1	YES	YES

The Factory programmed OTP array is locked by NXP and will always be active after POR. The CRC is continuously calculated on the factory programmed OTP array, which includes the registers listed below:

Register Name	Register Addresses	Included in Factory CRC?
Serial Number Registers	SN0, SN1, SN2, SN3	Yes
Type Register	TYPE[5:0]	Yes
Factory Programmable Device Configuration Bits	Internal Register Map	Yes
Factory OTP Array CRC	CRC_F[2:0]	No
Factory OTP Array Lock Bit	LOCK_F	No

Bits are fed in from right to left (LSB first), and top to bottom (lower addresses first) in the register map. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'. The calculated CRC is compared against the CRC_F[2:0] bits. If a CRC mismatch is detected, an internal data error is set and the device responds to DSI messages as specified in [Section 4.3](#). The CRC verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.2.2 User Programmable OTP Array Lock and Error Detection

The User Programmable OTP array is independently verified for errors. The error detection is enabled only when the User Programmable OTP array is locked as shown below.

Factory Lock Bit Value in Fuse Array	Lock Bit Value in Mirror Register After Automatic Readout	Lock Bit Active?	CRC Verification Enabled?
0	N/A	NO	NO
1	0	NO	NO
1	1	YES	YES

When the LOCK_U bit is set, the error detection code is calculated on the user programmable OTP Array registers listed below and stored NVM.

Register Name	Register Addresses
Type Register	TYPE[7:6]
Device ID Bit	DEVCFG[7]: DEVID
Attribute Bits	DEVCFG1[1:0]: AT_OTP[1:0]
PCM Bit	DEVCFG2[5]: PCM
RESERVED Bit	DEVCFG2[4]
Device Address	DEVCFG2[3:0]: ADDR[3:0]
User Data Registers 1 - 8	UD01 - UD08

During normal operation, the error detection code is continuously compared against the stored error detection code. If a mismatch is detected, an internal data error is set, and the device responds to DSI messages as specified in [Section 4.3](#). The error detection code is calculated on the memory registers which hold a copy of the fuse array values, not the fuse array values.

Writes to the User Programmable OTP array using the Write NVM Command will update the mirror registers and result in a change to the error detection code regardless of the state of the LOCK_U bit. An error detection mismatch will only be detected if the LOCK_U bit is active.

3.3 Voltage Regulators

The device derives its internal supply voltage from the HCAP supply voltage. The device includes separate internal voltage regulators for the analog (V_{REGA}) and digital circuitry (V_{REG}). External filter capacitors are required, as shown in Figure 1.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the HCAP and internal voltages have stabilized sufficiently for proper operation. The voltage monitor asserts internal reset when the HCAP supply or internally regulated voltages fall below predetermined levels. A reference generator provides a stable voltage which is used by the $\Sigma\Delta$ converter.

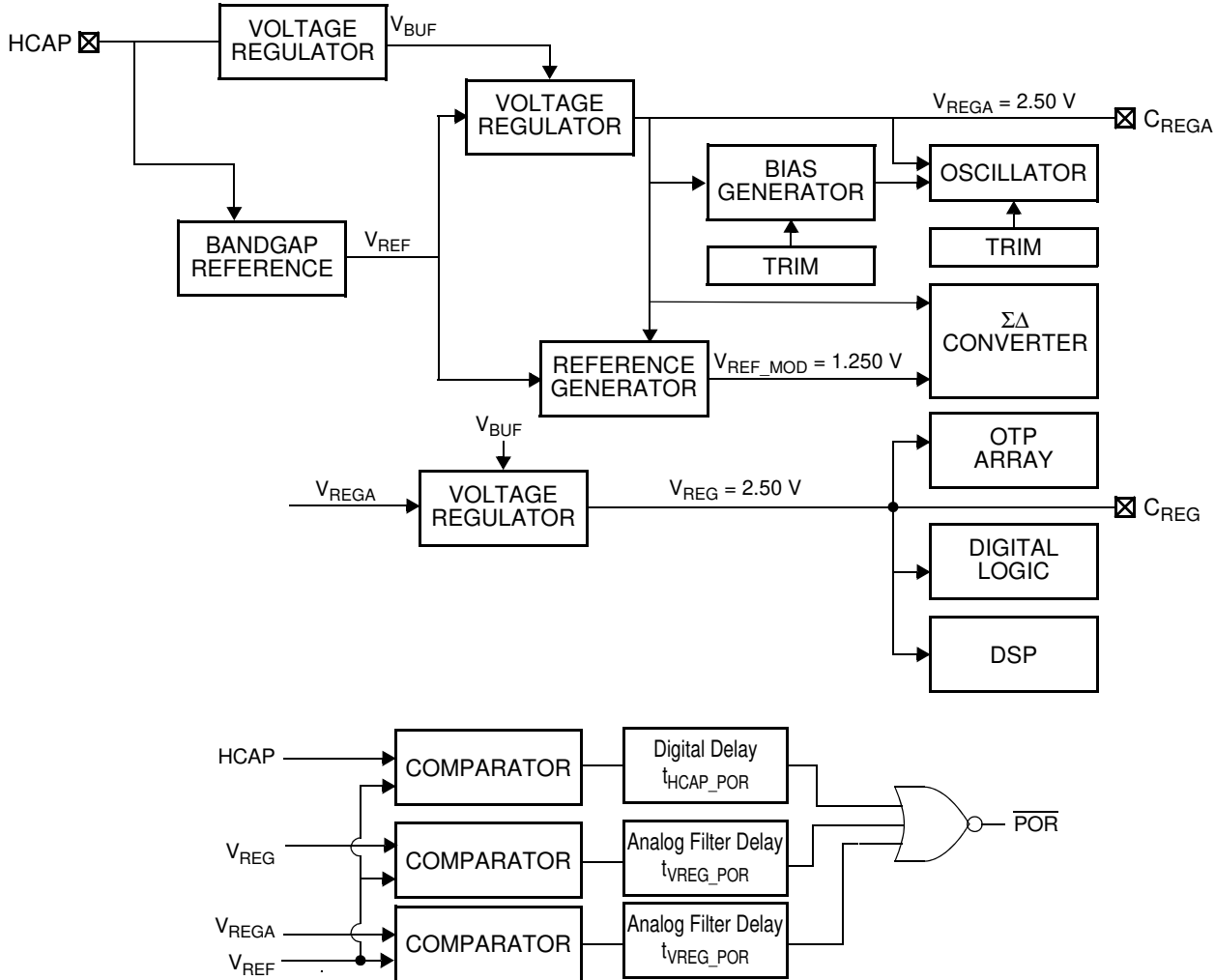


Figure 10. Voltage Regulation and Monitoring

3.3.1 C_{REG} and C_{REGA} Regulator Capacitor

The internal regulator requires an external capacitor between the C_{REG} pin and V_{SS} pin, and the C_{REGA} pin and V_{SSA} pin for stability. Figure 1 shows the recommended types and values for each of these capacitors.

3.3.2 V_{HCAP} Voltage Monitor

The device includes a circuit to monitor the voltage on the HCAP pin. If the voltage falls below the specified threshold in Section 2, the device will be reset within the reset delay time (t_{HCAP_POR}) specified in Section 2.7.

3.3.3 V_{REG} and V_{REGA} Under-Voltage Monitor

The device includes a circuit to monitor the internally regulated voltages (V_{REG} and V_{REGA}). If either of the internal regulator voltages fall below the specified thresholds in Section 2, the device will be reset within the reset delay time (t_{VREG_POR} , t_{VREGA_POR}) specified in Section 2.7.

3.3.4 V_{REG} and V_{REGA} Capacitance Monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external C_{REG} or C_{REGA} capacitor becomes open. At a continuous rate specified in Section 2.7 ($t_{CAPTEST_RATE}$), both regulators are simultaneously disabled for a short duration ($t_{CAPTEST_TIME}$). If either of the external capacitors are not present, the associated regulator voltage will fall below the internal reset threshold, forcing a device reset.

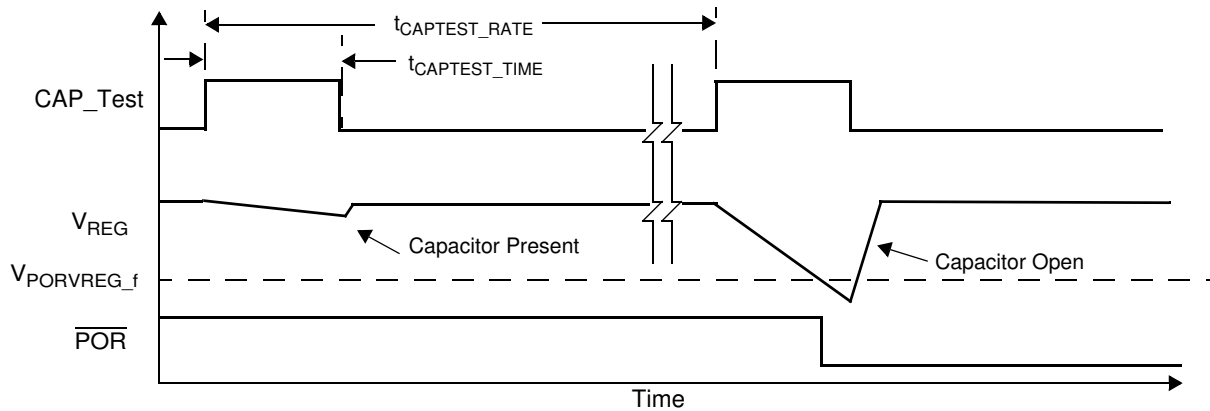


Figure 11. V_{REG} Capacitor Monitor

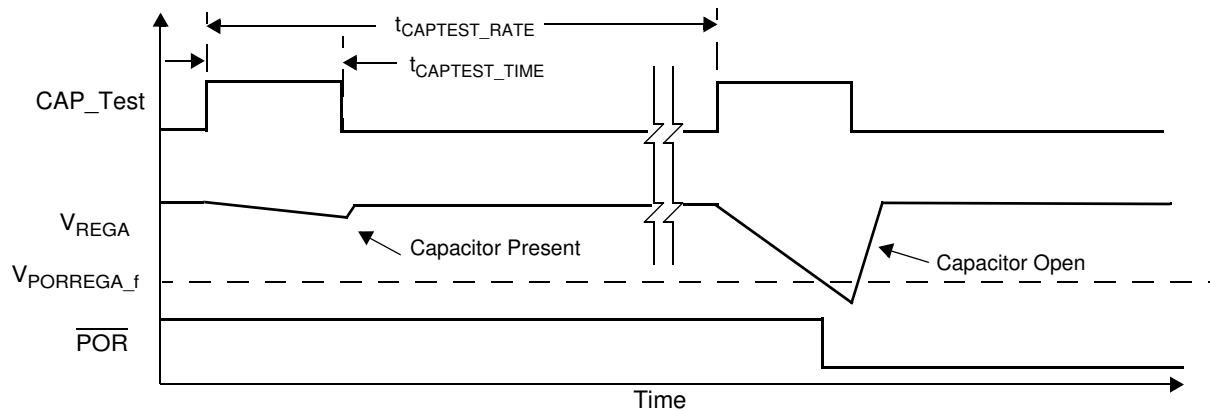


Figure 12. V_{REGA} Capacitor Monitor

3.4 Internal Oscillator

The device includes a factory trimmed oscillator as specified in Section 2.8.

3.5 Acceleration Signal Path

3.5.1 Transducer

The device transducer is an overdamped mass-spring-damper system described by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

where:

ξ = Damping Ratio

ω_n = Natural Frequency = $2 \cdot \pi \cdot f_n$

Reference [Section 2.8](#) for transducer parameters.

3.5.2 $\Sigma\Delta$ Converter

The sigma delta converter provides the interface between the g-cell and the DSP block. The output of the $\Sigma\Delta$ converter is a data stream at a nominal frequency of 1 MHz.

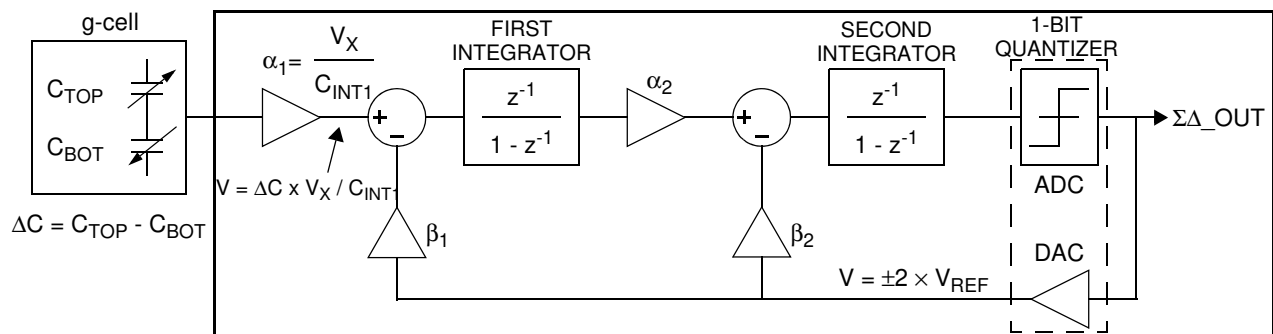


Figure 13. $\Sigma\Delta$ Converter Block Diagram

3.5.3 Digital Signal Processing Block

A digital signal processing (DSP) block is used to perform signal filtering and compensation operations. A diagram illustrating the signal processing flow within the DSP block is shown in [Figure 14](#).

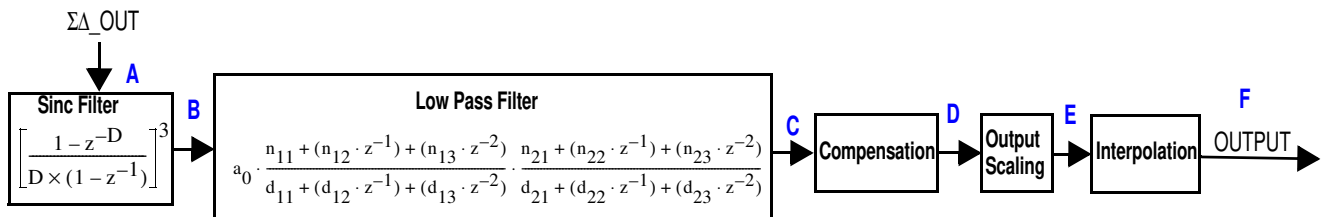


Figure 14. Signal Chain Diagram

Table 8. Signal Chain Characteristics

	Description	Sample Time (μs)	Data Width (Bits)	Over Range (Bits)	Signal Width (Bits)	Signal Noise (Bits)	Signal Margin (Bits)	Typical Block Latency	Reference
A	$\Sigma\Delta$	1	1		1			112/f _{osc}	Section 3.5.2
B	SINC Filter	16	20		12	4			Section 3.5.3.1
C	Low Pass Filter	16	26	1	12	4	9	Reference Section 3.5.3.2	Section 3.5.3.2
D	Compensation	16	26	4	10	3	9		24/f _{osc}
E	DSP Sampling	16			10			4/f _{osc}	Section 3.5.3.5
	10-Bit Output Scaling								
F	Interpolation	1			10			64/f _{osc}	Section 3.5.3.5

3.5.3.1 Decimation Sinc Filter

The serial data stream produced by the $\Sigma\Delta$ converters is decimated and converted to parallel values by a 3rd order 16:1 sinc filter with a decimation factor of 16.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})} \right]^3$$

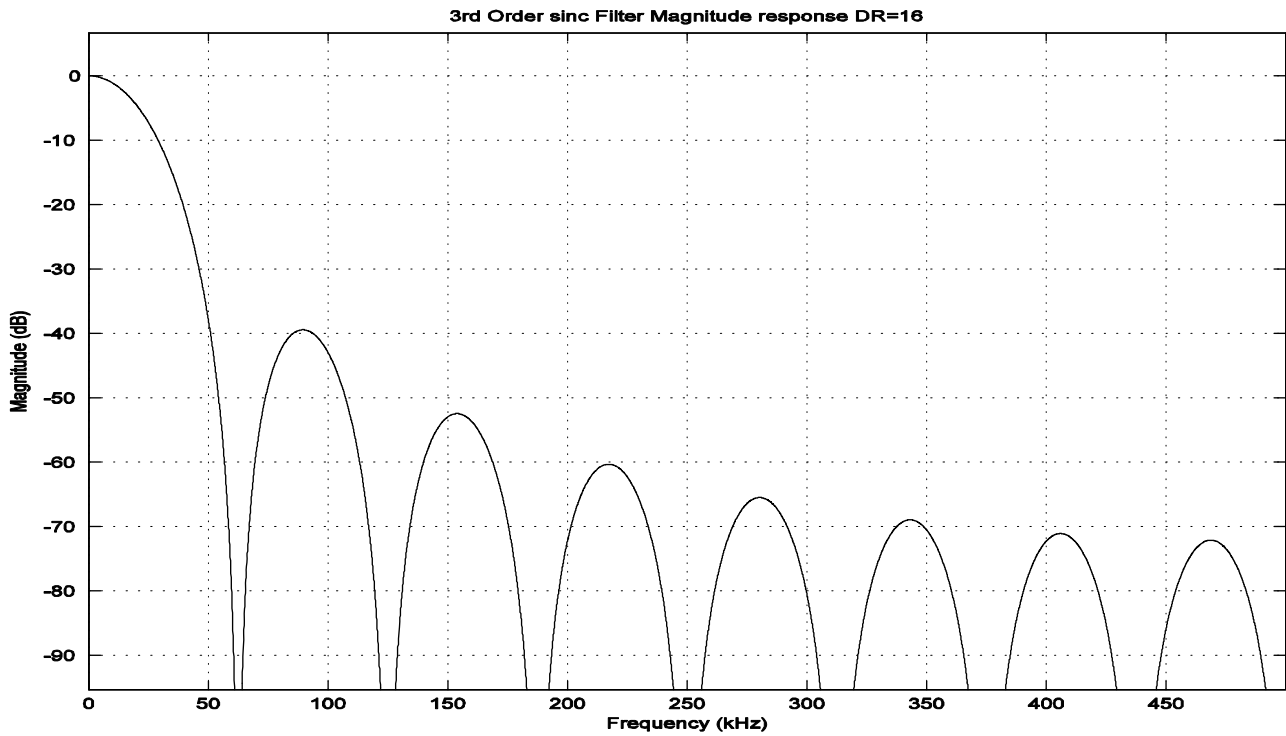


Figure 15. Sinc Filter Response, $t_S = 16 \mu s$

3.5.3.2 Low Pass Filter

Data from the Sinc filter is processed by an infinite impulse response (IIR) low pass filter.

$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})}$$

The device provides the option for one of three low-pass filters. The filter is selected with the LPF[1:0] bits in the TYPE register. The filter selection options are listed in [Section 3.1.2.1](#), [Table 9](#). Response parameters for the low-pass filter are specified in [Section 2.8](#). Filter characteristics are illustrated in the figures below.

Table 9. Low Pass Filter Coefficients

Description	Filter Coefficients				Group Delay
180 Hz LPF	a ₀	0.000534069200512			4608/f _{osc}
	n ₁₁	0.25	d ₁₁	1	
	n ₁₂	0.499999985098839	d ₁₂	-1.959839582443237	
	n ₁₃	0.25	d ₁₃	0.960373640060425	
	n ₂₁	1	d ₂₁	1	
	n ₂₂	0	d ₂₂	0	
	n ₂₃	0	d ₂₃	0	
400 Hz LPF	a ₀	0.003135988372378			3392/f _{osc}
	n ₁₁	0.000999420881271	d ₁₁	1.0	
	n ₁₂	0.001998946070671	d ₁₂	-1.892452478408814	
	n ₁₃	0.000999405980110	d ₁₃	0.89558845758438	
	n ₂₁	0.250004753470421	d ₂₁	1.0	
	n ₂₂	0.499986037611961	d ₂₂	-1.919075012207031	
	n ₂₃	0.250009194016457	d ₂₃	0.923072755336761	
800 Hz LPF	a ₀	0.011904109735042			1728/f _{osc}
	n ₁₁	0.003841564059258	d ₁₁	1.0	
	n ₁₂	0.007683292031288	d ₁₂	-1.790004611015320	
	n ₁₃	0.003841534256935	d ₁₃	0.801908731460571	
	n ₂₁	0.250001862645149	d ₂₁	1.0	
	n ₂₂	0.499994158744812	d ₂₂	-1.836849451065064	
	n ₂₃	0.250003993511200	d ₂₃	0.852215826511383	

Note: Low Pass Filter Figures do not include g-cell frequency response.

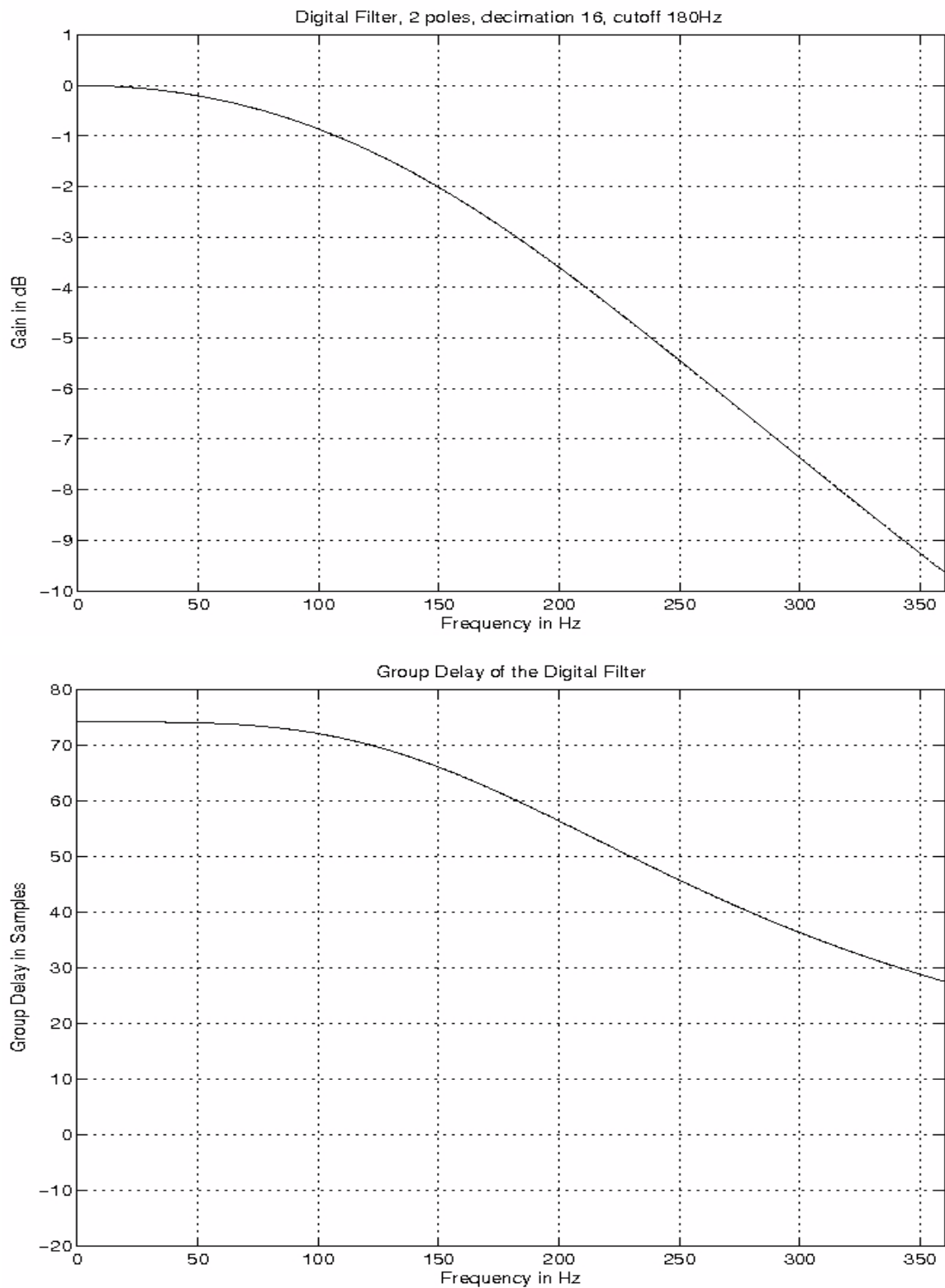


Figure 16. Low-Pass Filter Characteristics: $f_C = 180$ Hz, 2-Pole, $t_S = 16 \mu s$

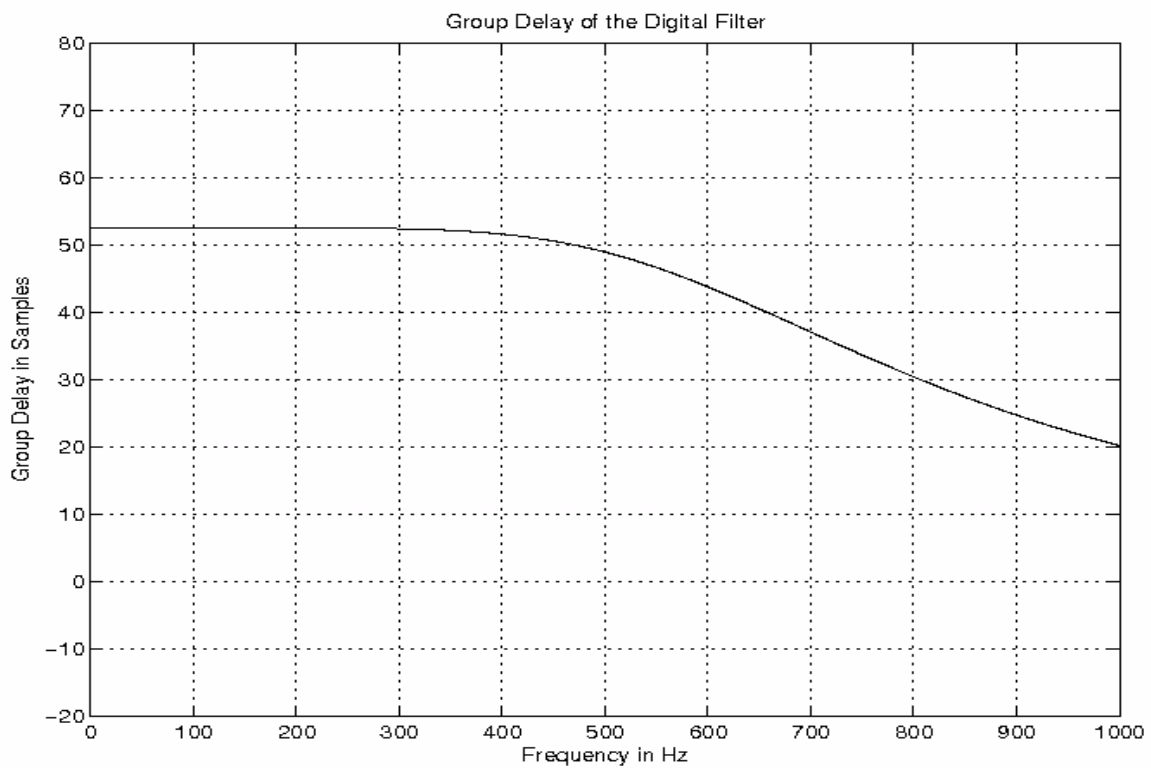
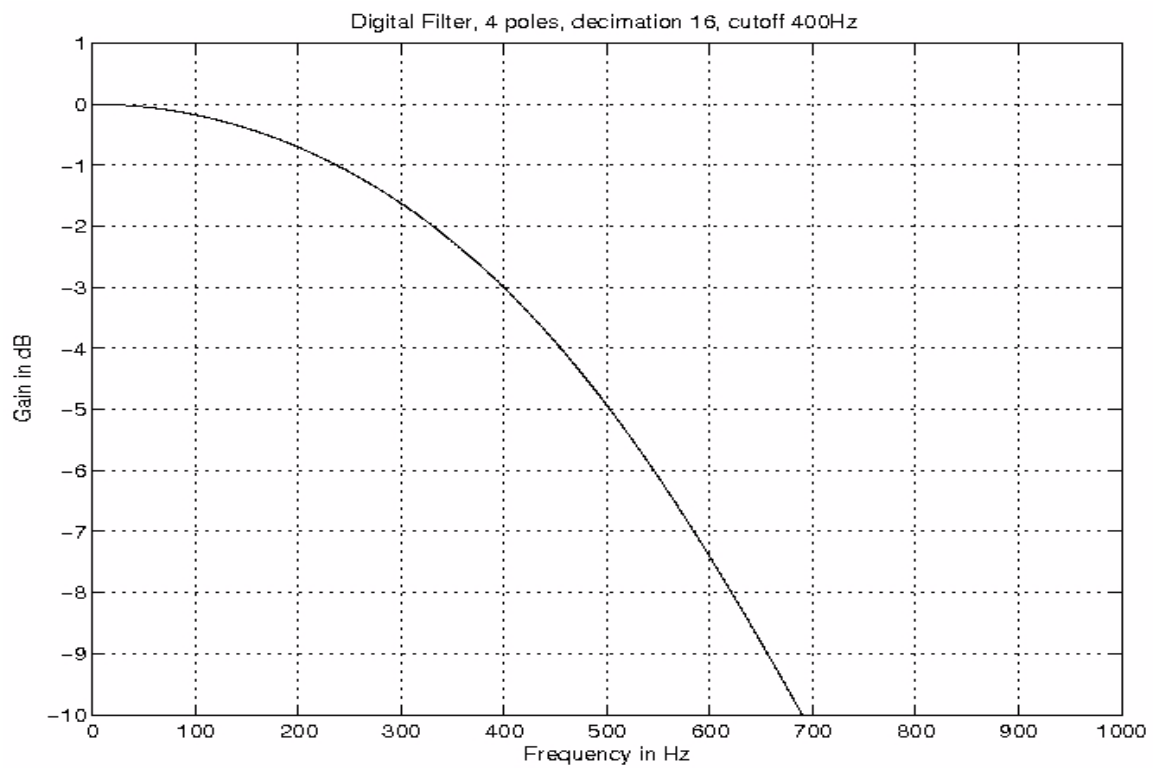


Figure 17. Low-Pass Filter Characteristics: $f_c = 400$ Hz, 4-Pole, $t_s = 16 \mu s$