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Document Number: MMA27XXW
Rev. 0.5, 4/2013

RoHS

SAFE ASSURE by Freescale

Xtrinsic MMA27XXW/17XXW DSI3 Inertial Sensor

MMA27XXW
MMA17XXW

MMA27XXW/17XXW family, a SafeAssure solution, includes the DSI3 compatible overdamped X-axis or Z-axis satellite accelerometers.

Features

- ±25 g, ±125 g, ±187 g, ±250 g, ±375 g, X-axis nominal full-scale range
- ±250 g, Z-axis nominal full-scale range
- DSI3 compatible
  - Discovery Mode for physical location identification
  - High-side bus switch output driver
  - Command and Response Mode support for device configuration
  - Periodic Data Collection Mode support for acceleration data transfers
  - Background Diagnostic Mode support during Periodic Data Collection Mode
- -40°C to 125°C operating temperature range
- 16 µs internal sample rate, with interpolation to 1 µs
- Six selectable low-pass filter options from 180 Hz to 1200 Hz
- Single-pole, IIR high-pass filter with fast startup and optional output rate limiting
- Pb-Free, 16-pin QFN, 6 x 6 package

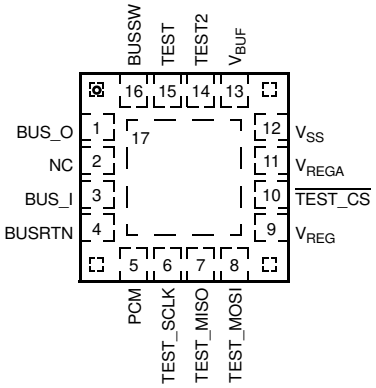
Referenced Documents

- DSI3 Standard Revision 1.0, Dated February 16, 2011
- AEC-Q100, Revision G, dated May 14, 2007

Bottom View

16-PIN QFN
6 MM X 6 MM X 2 MM
CASE 2086-01

Top View



Pin Connections

ORDERING INFORMATION				
Part Number	**Axis**	**Range**	**Package**	**Shipping**
MMA2702W	X	±25 g	2086-01	Rail
MMA2712W	X	±125 g	2086-01	Rail
MMA2718W	X	±187 g	2086-01	Rail
MMA2725W	X	±250 g	2086-01	Rail
MMA2737W	X	±375 g	2086-01	Rail
MMA1725W	Z	±250 g	2086-01	Rail
MMA2702WR2	X	±25 g	2086-01	Tape & Reel
MMA2712WR2	X	±125 g	2086-01	Tape & Reel
MMA2718WR2	X	±187 g	2086-01	Tape & Reel
MMA2725WR2	X	±250 g	2086-01	Tape & Reel
MMA2737WR2	X	±375 g	2086-01	Tape & Reel
MMA1725WR2	Z	±250 g	2086-01	Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice. Freescale reserves the right to change the detail

freescale Xtrinsic

Contents

Related Documentation

The MMA27XXW and MMA17XXW devices features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA27XXW or MMA17XXW.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Block Diagram, Pin Descriptions, Application Diagram, and Device Orientation

1.1 Block diagram

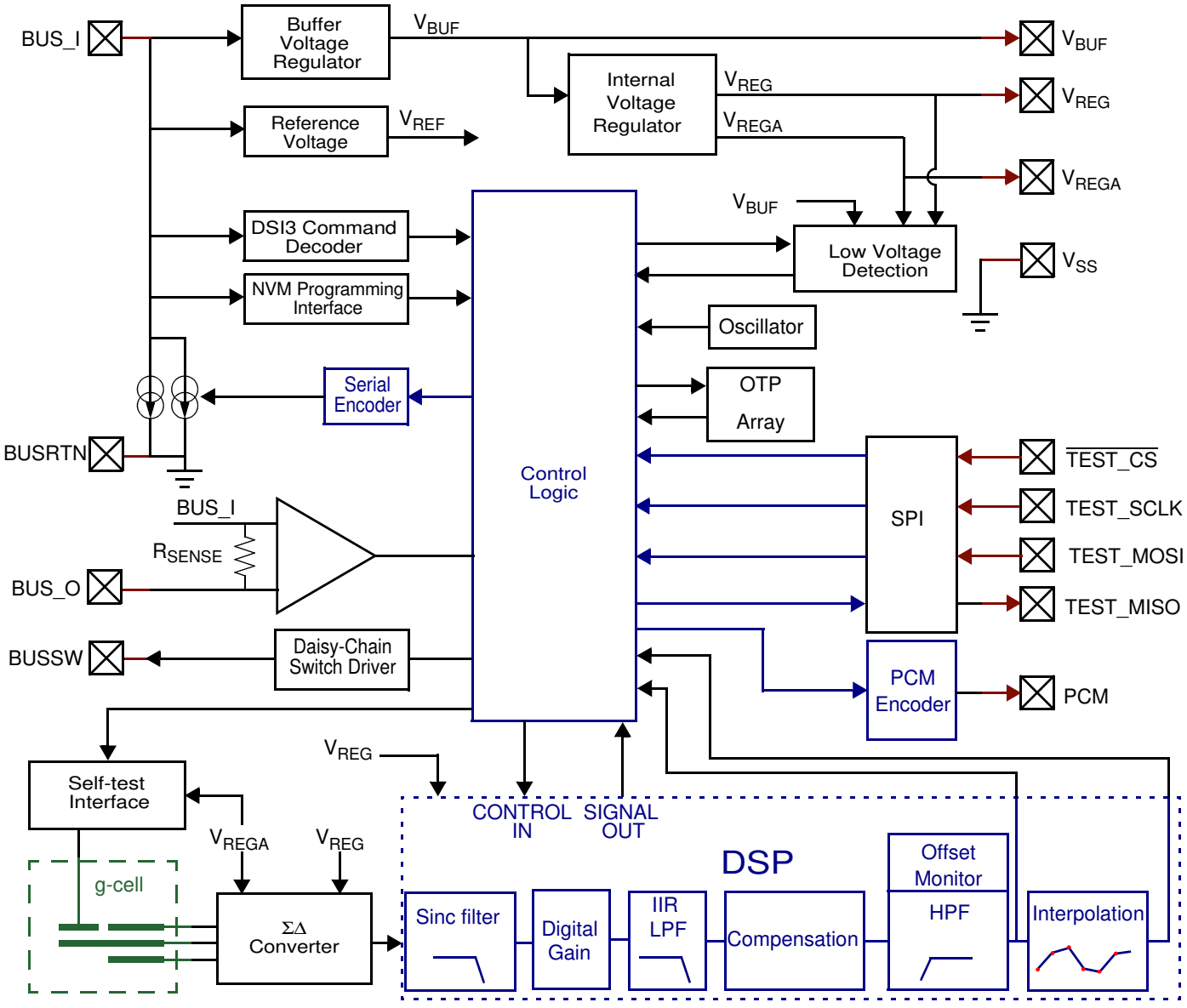


Figure 1. Internal block diagram

1.2 Pin descriptions

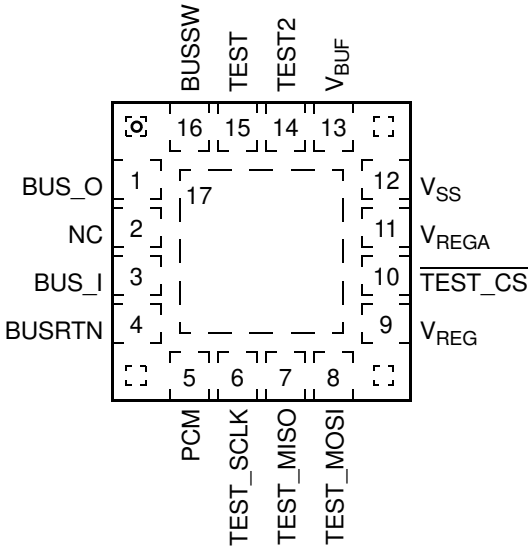


Figure 2. Pin connections

Table 1. Pin descriptions

Pin	Pin name	Formal name	Definition
1	BUS_O	Supply out	This pin is connected to the BUS_I pin through an internal sense resistor and provides the supply connection to the next slave in a daisy-chain configuration. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 3.
2	NC	Not connected	This pin is not internally connected and must be left unconnected or tied to V_{SS} in the application.
3	BUS_I	Supply and communication	This pin is connected to the DSI supply line and supplies power to the device. An external capacitor must be connected between this pin and BUSRTN. Reference Figure 3.
4	BUSRTN	Supply return	This pin is the DSI supply return node.
5	PCM	Pulse code modulated output	If the PCM output is enabled, this pin provides a 4 MHz PCM signal proportional to the acceleration data for test purposes. If PCM is unused, this pin must be left unconnected.
6	TEST_SCLK	SPI clock	This input pin provides the serial clock to the SPI port for test purposes. An internal pull-down device is connected to this pin. This pin must be grounded or left unconnected in the application.
7	TEST_MISO	SPI data out	This pin functions as the serial data output from the SPI port for test purposes. This pin must be left unconnected in the application.
8	TEST_MOSI	SPI data in	This pin functions as the serial data input to the SPI port for test purposes. An internal pull-down device is connected to this pin. This pin must be grounded or left unconnected in the application.
9	V_{REG}	Internal supply	This pin is connected to the power supply for the internal circuitry. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 3.
10	$\overline{TEST\_CS}$	Chip select	This input pin provides the chip select to the SPI port for test purposes. An internal pullup device is connected to this pin. This pin must be left unconnected in the application.
11	V_{REGA}	Internal supply	This pin is connected to the power supply for the internal circuitry. An external capacitor must be connected between this pin and V_{SSA}. Reference Figure 3.
12	V_{SS}	Internal supply return	This pin is the power supply return node for the internal power supplies and must be connected to BUSRTN in this application.
13	V_{BUF}	Power supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies the internal regulators to provide immunity from EMC and supply dropouts. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 3.
14	TEST2	Test pin	This pin is must be connected to V_{SS} in the application.
15	TEST	Test pin	This pin is must be connected to V_{SS} in the application.
16	BUSSW	Bus switch gate drive	This pin is the drive for a high-side, daisy-chain switch. When switch is connected, daisy-chain mode is used, this pin is connected to the gate of a p-channel FET which connects BUS_I to the next slave in the daisy chain. An external pullup resistor is required on the gate of the p-channel FET. Reference Section 3.6.4. If unused, this pin must be left unconnected.
17	PAD	Die attach pad	This pin is the die attach flag, and is internally connected to V_{SS}. Reference Section 6 for die attach pad connection details.
	Corner pads	Corner pads	The corner pads are internally connected to V_{SS}.

1.3 Application diagram

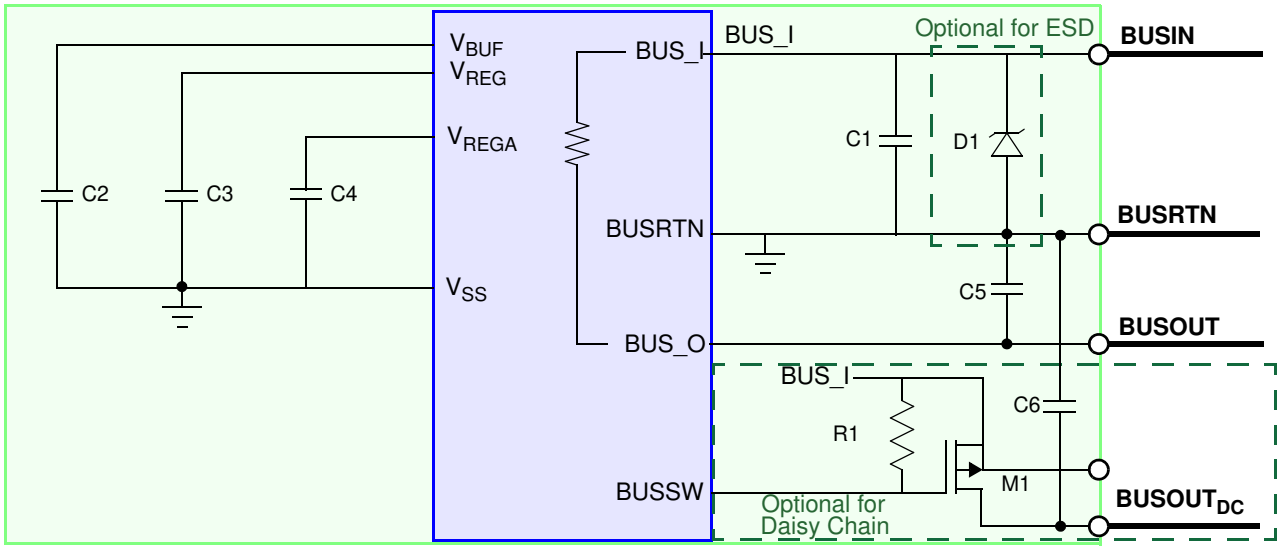


Figure 3. MMA27XXW/17XXW application diagram

Table 2. External component recommendations

Ref Des	Type	Description	Purpose
C1	Ceramic	220 pF, 10%, 50 V minimum, X7R	BUSIN EMC and ESD protection. Capacitor value is dependent on the DSI3 master device and must be chosen by the system implementer.
C2	Ceramic	1 µF, 10%, 10 V minimum, X7R	Voltage regulator output capacitor
C3	Ceramic	1 µF, 10%, 10 V minimum, X7R	Voltage regulator output capacitor
C4	Ceramic	1 µF, 10%, 10 V minimum, X7R	Voltage regulator output capacitor
C5	Ceramic	100 pF, 10%, 50 V minimum, X7R	BUSOUT EMC and ESD protection
C6	Ceramic	100 pF, 10%, 50 V minimum, X7R	BUSOUT EMC and ESD protection
R1	General purpose	100 kΩ, 5%, 200 PPM	Pullup resistor for external high-side, daisy-chain FET
M1	P-channel MOSFET		High-side, daisy-chain transistor
D1	Zener diode	MMBZ27Vxxxx or equivalent	ESD protection diode

1.4 Device orientation and device marking

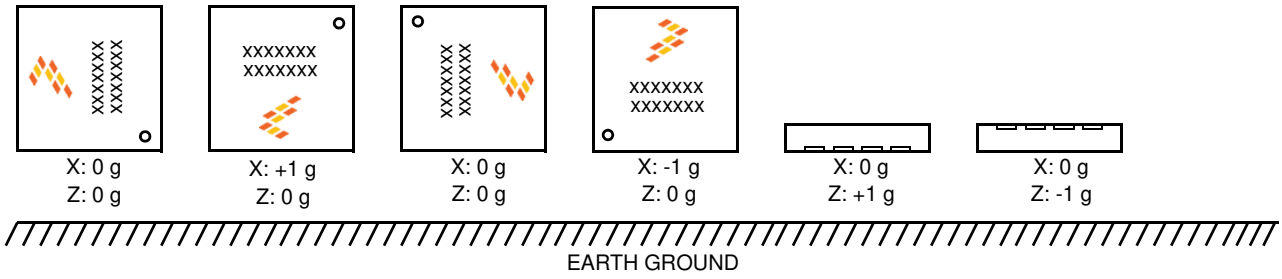


Figure 4. Device orientation diagram

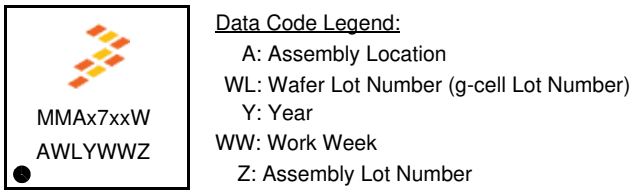


Figure 5. Device marking

2 Electrical Characteristics

2.1 Maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	
1	Supply voltage (BUS_I, BUS_O, BUSSW)				
2	Reverse current ≤ 160 mA, t ≤ 80 ms	$BUS\_I_{\_REV}$	-0.7	V	(6)
3	Continuous	$BUS\_I_{\_MAX}$	+20.0	V	(6)
4	Transient (< 10 us)	$BUS\_I_{\_TRANS}$	+25.0	V	(9)
5	V_{BUF}		-0.3 to +4.0	V	(6)
6	V_{REG}, V_{REGA}, TEST_SCLK, $\overline{TEST\_CS}$, TEST_MOSI, TEST_MISO, PCM		-0.3 to +3.0	V	(6)
7	BUS_I, BUS_O and BUSRTN current				
8	Maximum duration 560 µs, with 10 ms repetition rate	I_{IN}	200	mA	(6)
9	Continuous	I_{IN}	150	mA	(6)
10	Powered shock (six sides, 0.5 ms duration)	g_{pms}	±2000	g	(5)
11	Unpowered shock (six sides, 0.5 ms duration)	g_{shock}	±2000	g	(5)
12	Drop shock (to concrete, tile or steel surface, 10 drops, any orientation)	h_{DROP}	1.2	m	(5)
13	Electrostatic discharge (per AEC-Q100), external pins				
14	BUS_I, BUS_O, BUSRTN, HBM (100 pF, 1.5 kΩ)	V_{ESD}	±4000	V	(5)
15	Electrostatic discharge (per AEC-Q100)				
16	HBM (100 pF, 1.5 kΩ)	V_{ESD}	±2000	V	(5)
17	CDM (R = 0 Ω)	V_{ESD}	±500	V	(5)
18	MM (200 pF, 0 Ω)	V_{ESD}	±200	V	(5)
19	Temperature range				
20	Storage	T_{stg}	-40 to +125	°C	(5)
21	Junction	T_J	-40 to +150	°C	(9)
22	Thermal resistance	θ_{JC}	2.5	°C/W	(9,11)

2.2 Operating range

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12°C$/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
23	Supply voltage (measured at BUS_I pin)						
24	V_{HIGH} *	$V_{BUS\_I\_HIGH\_max}$	—	—	20.0	V	(1,6)
25	V_{LOW} rising	$V_{BUS\_I\_LOW\_Rise}$	4.5	—	—	V	(9)
26	V_{LOW} falling *	$V_{BUS\_I\_LOW\_Fall}$	4.0	—	—	V	(1)
27	Supply voltage (undervoltage)	$V_{BUS\_I\_UV}$	$V_{BUS\_I\_UV\_F}$	—	$V_{BUS\_I\_LOW\_Fall}$	V	(3,6)
28	Programming voltage (I_{RD} ≤ 85 mA) Applied to BUS_I	VPP	14.0	—	$V_{BUS\_I\_HIGH\_max}$	V	(6)
29	ESD operating voltage						
30	(No device reset, C_{BUS_IN} = 220 pF, D1 = MMBZ27Vxxxx)						
31	Maximum ±15 kV air discharge, 330 pF, 2.0 kΩ	VBUS_I_ESD	—	—	12.0	V	(9)
32	Operating temperature range		T_L		T_H		
33		T_A	-40	—	+105	°C	(1)
34		T_A	-40	—	+125	°C	(5,6)

2.3 Electrical characteristics - supply and I/O

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12$ °C/min, unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
35	Quiescent supply current V_{BUS_I} = 4 V, V_{BUS_I} = 20 V	*	I_q	4.0	—	8.0	mA	(1)
	Response current							
36	Low	*	I_{RESP}	I_q+ 10.50	I_q+ 12.0	I_q+ 13.5	mA	(1)
37	High	*	2*I_{RESP}	I_q+ 21.0	I_q+ 24.0	I_q+ 27.0	mA	(1)
38	V_{BUF} current limit		I_{INRUSH_MAX}	—	—	30	mA	(6)
	Internally regulated voltages							
39	V_{BUF}, V_{BUS_I} = 4 V, V_{BUS_I} = 20 V		V_{BUF}	3.250	3.400	3.550	V	(1)
40	V_{REG}, V_{BUS_I} = 4 V		V_{REG}	2.400	2.500	2.600	V	(1)
41	V_{REGA}, V_{BUS_I} = 4 V, V_{BUS_I} = 20 V	*	V_{REGA}	2.425	2.500	2.575	V	(1)
	Low-voltage detection threshold							
42	BUS_I falling		$V_{BUS\_I\_UV\_F}$	3.60	3.75	3.90	V	(3,6)
43	V_{BUF} falling		$V_{BUF\_UV\_F}$	2.80	3.05	3.20	V	(3,6)
44	V_{REG} falling		$V_{REG\_UV\_F}$	2.15	2.25	2.35	V	(3,6)
45	V_{REGA} falling		$V_{REGA\_UV\_F}$	2.15	2.25	2.35	V	(3,6)
46	Low-voltage detection hysteresis		V_{HYST}	0.04	—	—	V	(6)
	External capacitor (V_{BUF}, V_{REG}, V_{REGA})							
47	Capacitance		C_{VBUF}, C_{VREG}, C_{VREGA}	500	1000	1500	nF	(9)
48	ESR (including interconnect resistance)		ESR	0	—	200	mΩ	(9)
	V_{LOW} detection threshold (Section 3.6.1)							
49	V_{LOW} detection threshold	*	V_{DELTA_THRESH}	V_{HIGH}-1.25	V_{HIGH}-1.0	V_{HIGH}-0.75	V	(3,6)
50	V_{LOW} detection hysteresis	*	$V_{DELTA\_THRESH\_Hyst}$	40	60	80	mV	(6)
	Discovery Mode current sense (Section 3.6.3)							
51	Sense resistor		R_{SENSE}	1.3	2.15	3	Ω	(6)
52	I_{RESP} detection threshold ($I_{BUS\_O\_q} \le 24$ mA)		I_{RESP_Det}, V_{IRESP_Offset}	6	12	18	mA	(3,6)
	Bus switch output low voltage (Section 3.6.4)							
53	I_{Load} = 100 µA		$V_{BUS\_SW\_OL}$	0.0	—	0.45	V	(3,6)
	Bus switch open drain output leakage current (BUSSW)							
54	V_{BUSSW} = 20 V		$I_{BUS\_SW\_ODL}$	—	—	10	µA	(3,6)
	Output high voltage (PCM)							
55	I_{Load} = -100 µA		V_{OH}	V_{REG} - 0.1	—	—	V	(3)
	Output low voltage (PCM)							
56	I_{Load} = 100 µA		V_{OL}	—	—	0.1	V	(3)

2.4 Electrical Characteristics - sensor and signal chain

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12$ °C/min, unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	Sensitivity (T_A = 25°C, 10-bit output @ 100 Hz, referenced to 0Hz: ±5%)							
57	±25 g range	*	$SENS_{025}$	19.456	20.480	21.504	LSB/g	(1)
58	±125 g range	*	$SENS_{125}$	3.8912	4.0960	4.3008	LSB/g	(1)
59	±187 g range	*	$SENS_{187}$	2.5944	2.7310	2.8676	LSB/g	(1)
60	±250 g range	*	$SENS_{250}$	1.9456	2.0480	2.1504	LSB/g	(1)
61	±375 g range	*	$SENS_{375}$	1.2967	1.3650	1.4333	LSB/g	(1)
	Sensitivity ($T_L \le T_A \le T_H$, $V_{BUS\_I\_UV\_F} \le V_{BUS\_I} \le V_{LOW}$ 10-bit output @ 100 Hz, referenced to 0 Hz: ±7%)							
62	±25 g range	*	$SENS_{025}$	19.046	20.480	21.914	LSB/g	(1)
63	±125 g range	*	$SENS_{125}$	3.8092	4.0960	4.3828	LSB/g	(1)
64	±187 g range	*	$SENS_{187}$	2.5398	2.7310	2.9222	LSB/g	(1)
65	±250 g range	*	$SENS_{250}$	1.9046	2.0480	2.1914	LSB/g	(1)
66	±375 g range	*	$SENS_{375}$	1.2694	1.3650	1.4606	LSB/g	(1)
	Digital offset before offset cancellation (10-bit)							
67	±25 g, ±125 g, ±250 g Z-axis	*	OFF_{10Bit}	-100	0	+100	LSB	(1)
68	$V_{BUS\_I\_UV\_F} \le V_{BUS\_I} \le V_{LOW}$, ±25 g, ±125 g, ±250 g Z-axis		OFF_{10Bit}	-100	0	+100	LSB	(6)
69	±187 g, ±250 g X-axis, ±375 g	*	OFF_{10Bit}	-52	0	+52	LSB	(1)
70	$V_{BUS\_I\_UV\_F} \le V_{BUS\_I} \le V_{LOW}$, ±187 g, ±250 g X-axis, ±375 g		OFF_{10Bit}	-52	0	+52	LSB	(6)
71	Digital offset after offset cancellation (10-bit, all filter options)		OFF_{10Bit}	-1	0	+1	LSB	(6,8,9)
	Continuous offset monitor limit							
72	10-bit output, before compensation, ±25 g		OFF_{MON}	-150	—	+150	LSB	(7,8)
73	10-bit output, before compensation, ±125 g, ±250 g Z-axis		OFF_{MON}	-120	—	+120	LSB	(7,8)
74	10-bit output, before compensation, ±187 g, ±250 g X-axis, ±375 g		OFF_{MON}	-70	—	+70	LSB	(7,8)
	Range of output (10-bit mode)							
75	Acceleration (signed)		$RANGE_{Signed}$	-511	—	+511	LSB	(7,8)
76	Acceleration (unsigned)		$RANGE_{Unsigned}$	1	—	1023	LSB	(7,9)
77	Error code (signed)		ERR_{Signed}	—	-512	—	LSB	(7,8)
78	Error code (unsigned)		$ERR_{Unsigned}$	—	0	—	LSB	(7,9)
	Cross-axis sensitivity							
79	Z-axis to X-axis		V_{ZX}	-5	—	+5	%	(6)
80	Y-axis to X-axis		V_{YX}	-5	—	+5	%	(6)
81	X-axis to Z-axis		V_{XZ}	-5	—	+5	%	(6)
82	Y-axis to Z-axis		V_{YZ}	-5	—	+5	%	(6)
	System output noise peak (peak value of 100 samples @ 2 kHz)							
83	10-bit mode, LPF = 180 Hz, 2-Pole, All Ranges		n_{Peak_180}	-3	—	+3	LSB	(1)
84	10-bit mode, LPF = 400 Hz, 4-Pole, All Ranges		n_{Peak_400}	-4	—	+4	LSB	(6)
	System output noise average (average value of 100 samples @ 2 kHz)							
85	10-bit mode, LPF = 180 Hz, 2-pole, all ranges	*	n_{RMS_180}	—	—	+1.0	LSB	(1)
86	10-bit mode, LPF = 400 Hz, 4-pole, all ranges	*	n_{RMS_400}	—	—	+1.0	LSB	(6)
87	Nonlinearity (10-bit output, all ranges)		NL_{OUT}	-2	—	+2	%	(6)

2.5 Electrical characteristics - self-test and overload

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12°C$/min, unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	10-bit output during active self-test			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
88	±25 g range, X-axis	*	g_{ST10_25X}	124	—	208	LSB	(1)
89	±125 g range, X-axis	*	g_{ST10_125X}	236	—	395	LSB	(1)
90	±187 g range, X-axis	*	g_{ST10_187X}	156	—	263	LSB	(1)
91	±250 g range, X-axis	*	g_{ST10_250X}	117	—	198	LSB	(1)
92	±375 g range, X-axis	*	g_{ST10_375X}	77	—	131	LSB	(1)
93	±250 g range, Z-axis	*	g_{ST10_250Z}	80	—	160	LSB	(1)
	Self-test accuracy: Δ from stored value, including sensitivity error							
94	-40°C ≤ T_A ≤ 125°C (Section 3.5.2)	*	ΔSTACC	-10	—	+10	%	(1,5)
	Transducer clipping limit							
95	±25 g, X-axis, positive/negative		$g_{g\text{-}cell\_ClipLowX}$	400	470	500	g	(9)
96	±125 g, ±187 g, ±250 g, ±375 g, X-axis, positive/negative		$g_{g\text{-}cell\_ClipHiX}$	1700	2100	2300	g	(9)
97	±250 g, Z-axis positive		$g_{g\text{-}cell\_ClipHiZP}$	2200	2700	3300	g	(9)
98	±250 g, Z-axis negative		$g_{g\text{-}cell\_ClipHiZN}$	-3700	-3200	-2700	g	(9)
	Sinc filter clipping limit							
99	±25 g, X-axis, positive/negative (MMA2702WR2)		$g_{ADC\_Clip\_25X\_H}$	190	210	240	g	(9)
100	±125 g, X-axis, positive/negative (MMA2712WR2)		$g_{ADC\_Clip\_125X\_H}$	920	1100	1300	g	(9)
101	±187 g, X-axis positive/negative (MMA2718WR2)		$g_{ADC\_Clip\_187X\_H}$	1600	1900	2200	g	(9)
102	±250 g, X-axis positive/negative (MMA2725WR2)		$g_{ADC\_Clip\_250X\_H}$	1600	1900	2200	g	(9)
103	±375 g, X-axis positive/negative (MMA2737WR2)		$g_{ADC\_Clip\_375X\_H}$	1600	1900	2200	g	(9)
104	±250 g, Z-axis, positive (MMA1725WR2)		$g_{ADC\_Clip\_250ZPH}$	1500	2000	2500	g	(9)
105	±250 g, Z-axis, negative (MMA1725WR2)		$g_{ADC\_Clip\_250ZNH}$	-3200	-2900	-2500	g	(9)

2.6 Dynamic electrical characteristics - DSI3

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12°C/min$, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Reset recovery (all modes, excluding V_{BUS_I} voltage ramp time)						
106	POR to 1st command (Section 3.6)	t_{DSI_POR}	—	5	—	ms	(7,8)
107	POR to acceleration data ready (Section 3.6)	t_{DSP_POR}	—	t_{DSI_POR}	—	s	(7,8)
	Command reception (general)						
108	V_{HIGH} low-pass filter time constant (Section 3.6.1)	t_{VHIGH_RC}	60	120	180	µs	(8,9)
109	V_{HIGH} detection analog delay (Section 3.6.1)	t_{VHIGH_Delay}	—	—	600	ns	(8,9)
110	i_q low-pass filter time constant (Section 3.6.3)	t_{IQ_RC}	200	400	600	µs	(8,9)
111	Command valid time (Section 3.6.1)	t_{Cmd_Valid}	—	2	—	µs	(7,9)
	Response transmission (general, Section 4.2.3)						
112	Response slew time: 2.0 mA to 10.0 mA, 10.0 mA to 2.0 mA	t_{SLEW1_RESP}	200	400	600	ns	(6,8)
113	Response slew time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA	t_{SLEW2_RESP}	200	400	600	ns	(6,8)
114	t_{SLEW1_RESP}- t_{SLEW2_RESP}	Δt_{SLEW}	-100	—	100	ns	(8,9)
115	$t_{SLEW1\_RESP\_Rise}$- $t_{SLEW2\_RESP\_Fall}$	Δt_{SLEW_rf}	-250	—	250	ns	(8,9)
116	Response current activation time: current activated to 50%	t_{ACT_RESP}	200	—	400	ns	(8,9)
	Command reception (Discovery Mode)						
117	Command start time (Section 4.1)	t_{START_DISC}	t_{DSI_POR}	—	12	ms	(7,8)
118	Command bit time (Section 4.1)	$t_{DISC\_BitTime}$	—	16	—	µs	(7,8)
119	Command transmission period (Section 4.1)	t_{PER_DISC}	$1000/f_{OSC}$	—	—	s	(7,8)
120	Command blocking time, Discovery Mode (Section 3.6.1)	$t_{CmdBlock\_DISC}$	—	96	—	µs	(7,8)
121	I_{CCQ} sample delay time (Section 3.6.3)	t_{Disc_Dly}	—	48	—	µs	(7,9)
122	I_{CCQ} sample time (Section 3.6.3)	$t_{Disc\_Iccqsamp}$	—	15	—	µs	(7,9)
123	I_{DISC} sample delay time (Section 3.6.3)	$t_{IDiscsamp\_Dly}$	—	65	—	µs	(7,9)
124	I_{DISC} sample time (Section 3.6.3)	$t_{IDiscsamp}$	—	31	—	µs	(7,9)
	Response transmission (Discovery Mode)						
125	Response start delay (Section 4.1)	$t_{START\_DISC\_RSP}$	—	64	—	µs	(7,8)
126	Response ramp time (Section 4.1)	$t_{DISC\_Ramp\_RSP}$	—	16	—	µs	(7,8)
127	Response ramp rate (Section 4.1)	I_{DISC_Ramp}	—	1.5	—	mA/µs	(6,8)
128	Response idle time (Section 4.1)	$t_{DISC\_Idle\_RSP}$	—	16	—	µs	(7,8)
129	Response peak current (Section 4.1)	I_{DISC_Peak}	—	$2*I_{RESP}$	—	mA	(6,8)
	Command reception (Command and Response Mode)						
130	Command bit time (Section 4.2)	$t_{Cmd\_BitTime}$	—	8	—	µs	(7,8)
131	Command transmission period (Section 4.2)	t_{PER_CRM}	t_{PER_PDCM}	—	8 x t_{PER_PDCM}	s	(7,8)
132	Command blocking time, CRM (Section 3.6.1)	$t_{CmdBlock\_CRM}$	—	456	—	µs	(7,8)
133	Command blocking start time, CRM (Section 3.6.1)	$t_{CmdBlock\_ST\_CRM}$	—	268	—	µs	(7,8)
	Response transmission (Command and Response Mode)						
134	Response chip time	t_{CHIP_CRM}	—	5	—	µs	(7,8)
135	Response start time (Section 4.2)	t_{START_CRM}	—	295	—	µs	(7,8)
	Command reception (Periodic Data Collection Mode)						
136	Command bit time (Section 4.3)	$t_{Cmd\_BitTime}$	—	8	—	µs	(7,8)
137	Command transmission period (Section 4.3)	t_{PER_PDCM}	100	—	5000	µs	(7,8)
138	Command transmission period resolution	$t_{PER\_PDCM\_Res}$	—	5	—	µs	(7,8)
139	Command blocking time, PDCM (Section 4.3.2)	$t_{CmdBlock\_PDCM}$	1	—	4095	µs	(7,8)
140	Command blocking time resolution, PDCM (Section 4.3.2)	$t_{CmdBlockRes\_PDCM}$	—	1	—	µs	(7,8)
141	Command blocking start time, PDCM (Section 4.3.2)	$t_{CmdBlock\_ST\_PDCM}$	—	20	—	µs	(7,8)
142	Command blocking start time, BDM command	$t_{CmdBlock\_ST\_BDM}$	—	44	—	µs	(7,8)
	Response transmission (Periodic Data Collection Mode)						
143	Response chip time typical (Section 3.1.15.3)	t_{CHIP_PDCM}	3	—	6.5	µs	(7,8)
144	Response chip resolution (Section 3.1.15.3)	$t_{CHIPRes\_PDCM}$	—	0.5	—	µs	(7,8)
145	Response start time typical (Section 4.3)	t_{START_PDCM}	20	—	4095	µs	(7,8)
146	Response start time typical, BDM enabled (Section 4.3)	$t_{START\_PDCM\_BDM}$	44	—	4095	µs	(7,8)
147	Response start time resolution	$t_{ST\_RES\_PDCM}$	—	1	—	µs	(7,8)
	Response transmission (Background Diagnostic Mode)						
148	Response start time (Section 4.3)	t_{START_BDM}	—	20	—	µs	(7,8)
149	Register write to BUSSW active	t_{BS}	—	456	—	µs	(7,8)
150	DSI data latency	t_{LAT_DSI}	—	0.5	6.25	µs	(7,9)
	OTP program timing						
151	Time to program the user OTP array	$t_{NVM\_WRITE\_MAX}$	—	—	60	ms	(7,8)

2.7 Dynamic electrical characteristics - signal chain

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12$ °C/min, unless otherwise specified.

Table 3.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	DSP low-pass filter							
152	Cutoff frequency LPF0, 2-pole (referenced to 0 Hz)	*	f_{C_LPF0}	—	180	—	Hz	(6,7)
153	Cutoff frequency LPF6, 3-pole (referenced to 0 Hz)	*	f_{C_LPF6}	—	325	—	Hz	(6,7)
154	Cutoff frequency LPF8, 3-pole (referenced to 0 Hz)	*	f_{C_LPF8}	—	400	—	Hz	(7,8)
155	Cutoff frequency LPF9, 4-pole (referenced to 0 Hz)	*	f_{C_LPF9}	—	400	—	Hz	(7,8)
156	Cutoff frequency LPF11, 4-pole (referenced to 0 Hz)	*	f_{C_LPF11}	—	800	—	Hz	(7,8)
157	Cutoff frequency LPF14, 4-pole (referenced to 0 Hz)	*	f_{C_LPF14}	—	1200	—	Hz	(7,8)
	DSP offset cancellation low-pass filter							
159	Offset Cancellation low-pass filter Input sample Rate		$t_{OC\_SampleRate}$	—	256	—	µs	(7,9)
160	Cutoff frequency, startup Phase 1, 1-pole		f_{C_OCPH1}	—	10.0	—	Hz	(7,9)
161	Startup Phase 1 time		t_{OCPH1}	—	80	—	ms	(7,9)
162	Cutoff frequency, startup Phase 2, 1-pole		f_{C_OCPH2}	—	1.0	—	Hz	(7,9)
163	Startup Phase 2 time		t_{OCPH2}	—	70	—	ms	(7,9)
164	Offset cancellation output update rate (10-bit)		$t_{OffRate}$	—	2	—	s	(7,9)
165	Offset cancellation output step size (10-bit)		OFF_{Step}	—	0.5	—	LSB	(7,9)
166	Offset monitor update rate		$OFFMON_{OSC}$	—	500	—	µs	(7,8)
167	Offset monitor count limit		$OFFMON_{CNTLIMIT}$	—	4096	—	1	(7,8)
168	Offset monitor counter size		$OFFMON_{CNTSIZE}$	—	8192	—	1	(7,8)
169	Signal delay excluding LPF group delay and interpolation		t_{SIG_DELAY}	—	—	100	µs	(7,9)
170	Interpolation latency		t_{LAT_INTERP}	—	16	—	µs	(7,9)
	Self-test response time (CS Rising to 90% g_{ST10_xxx})							
171	Self-test activation time (180 Hz LPF)		$t_{ST\_ACT\_180}$	2.00	—	4.00	ms	(3,6)
172	Self-test deactivation time (180 Hz LPF)		$t_{ST\_DEACT\_180}$	2.00	—	4.00	ms	(3,6)
173	Self-test activation time (325 Hz LPF, 3 Pole)		$t_{ST\_ACT\_325}$	1.30	—	2.70	ms	(6)
174	Self-test deactivation time (325 Hz LPF, 3 Pole)		$t_{ST\_DEACT\_325}$	1.30	—	2.70	ms	(6)
175	Self-test activation time (400 Hz LPF, 3 or 4 Pole)		$t_{ST\_ACT\_400}$	1.00	—	2.50	ms	(6)
176	Self-test deactivation time (400 Hz LPF, 3 or 4 Pole)		$t_{ST\_DEACT\_400}$	1.00	—	2.50	ms	(6)
177	Self-test activation time (800 Hz LPF)		$t_{ST\_ACT\_800}$	0.50	—	1.75	ms	(6)
178	Self-test deactivation time (800 Hz LPF)		$t_{ST\_DEACT\_800}$	0.50	—	1.75	ms	(6)
179	Self-test activation time (1200 Hz LPF)		$t_{ST\_ACT\_800}$	0.40	—	1.50	ms	(6)
180	Self-test deactivation time (1200 Hz LPF)		$t_{ST\_DEACT\_800}$	0.40	—	1.50	ms	(6)
	Sensing element rolloff frequency (-3 db)							
181	±25 g, X-axis		$f_{gcell\_3dB\_xlo}$	938	1600	2592	Hz	(6)
182	±125 g, ±187 g, ±250 g, ±375 g, X-axis		$f_{gcell\_3dB\_xhi}$	3952	7200	14370	Hz	(6)
183	±250 g, Z-axis		$f_{gcell\_3dB\_zhi}$	3100	4500	6500	Hz	(6)
	Sensing element natural frequency							
184	±25 g, X-axis		f_{gcell_xlo}	12651	13200	13871	Hz	(9)
185	±125 g, ±187 g, ±250 g, ±375 g, X-axis		f_{gcell_xhi}	26000	27500	28700	Hz	(9)
186	±250 g, Z-axis		f_{gcell_zhi}	15000	17000	17500	Hz	(9)
	Sensing element damping ratio							
187	±25 g, X-axis		ζ_{gcell_xlo}	2.76	4.20	6.77		(9)
188	±125 g, ±187 g, ±250 g, ±375 g, X-axis		ζ_{gcell_xhi}	1.26	2.00	3.60		(9)
189	±250 g, Z-axis		ζ_{gcell_zhi}	1.40	2.00	2.90		(9)
	Sensing element delay (@100 Hz)							
190	±25 g, X-axis		$f_{gcell\_delay100\_xlo}$	63	100	170	µs	(9)
191	±125 g, ±187 g, ±250 g, ±375 g, X-axis		$f_{gcell\_delay100\_xhi}$	13	24	40	ms	(9)
192	±250 g, Z-axis		$f_{gcell\_delay100\_zhi}$	35	40	55	µs	(9)
193	Package resonance frequency		$f_{Package}$	100	—	—	kHz	(9)

2.8 Dynamic electrical characteristics - supply and support circuitry

$V_{BUS\_I\_L} \le (V_{BUS\_I} - V_{SS}) \le V_{BUS\_I\_H}$, $T_L \le T_A \le T_H$, $\Delta T \le 12$ °C/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Internal oscillator period						
194	Untrained *	f_{OSC}	7.600	8.000	8.400	MHz	(1)
195	With oscillator training	f_{OSC}	7.879	8.000	8.121	MHz	(7,8,9)
	Oscillator training (Section 3.4.1)						
196	Oscillator training time (CRM and PDCM)	$t_{OscTrain}$	—	4	—	ms	(7)
197	Oscillator training window (CRM and PDCM)	$OscTrain_{WIN}$	3.4	—	4.6	ms	(7)
198	Oscillator training adjustment threshold (CRM and PDCM)	$OscTrain_{ADJ}$	-60	—	60	µs	(7)
199	Oscillator training step size (CRM and PDCM)	$OscTrain_{RES}$	—	28	—	µs	(7)
200	Quiescent current settling time (power applied to Iq = I_{IDLE} ±2 mA)	t_{SET}	—	—	4	ms	(6)
	BUS_I microcut						
201	Survival time (BUS_I disconnect without reset, C_{BUF}=C_{REG}=C_{REGA}=700nF)	$t_{BUS\_I\_MICROCUT}$	30	—	—	µs	(8)
202	Reset time (BUS_I disconnect time to reset, C_{BUF}=C_{REG}=C_{REGA}=1µF)	$t_{BUS\_I\_RESET}$	—	—	1000	µs	(8)
	BUS_I undervoltage detection delay						
203	BUS_I < $V_{BUS\_I\_UV\_F}$ to I_{RESP} deactivation	$t_{BUS\_I\_POR}$	—	—	5	µs	(6)
	V_{BUF} undervoltage detection delay						
204	V_{BUF} < $V_{BUF\_UV\_F}$ to I_{RESP} deactivation	t_{VBUF_POR}	—	—	5	µs	(6)
	V_{REG}, V_{REGA} undervoltage reset delay						
205	V_{REG} < $V_{REG\_UV\_F}$ to $\overline{POR}$ assertion, V_{REGA} < $V_{REGA\_UV\_F}$ to $\overline{POR}$ assertion	t_{VREG_POR}	—	—	50	µs	(6)
	V_{BUF}, V_{REG}, V_{REGA} capacitor monitor						
206	POR to capacitor disconnect	$t_{POR\_CAPTEST}$	—	950	—	µs	(7,8)
207	Disconnect time	t_{CAPTST_TIME}	—	1.5	—	µs	(7,8)

NOTES

1. Parameter tested 100% at final test. Temperature = -40°C, 25°C and 105°C, V_{BUS_I} = 8 V, Unless otherwise stated.
2. Not Applicable.
3. Parameter verified by pass/fail testing at final test
4. Parameter verified by pass/fail testing at final test during safe launch.
5. Parameter verified by qualification testing.
6. Parameter verified by characterization.
7. Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
8. Parameter verified by functional evaluation.
9. Parameter verified by simulation.
10. Not Applicable.
11. Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.

* Indicates critical characteristic.

3 Functional Description

3.1 User-accessible data array

A user-accessible data array allows for each device to be customized. The array consists of an OTP factory-programmable block, an OTP user-programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification (reference Section 3.2). Portions of the factory-programmable array are reserved for factory-programmed trim values.

Table 4. User-accessible data

Byte Addr	Register	Bit Function				Bit Function				Type
		7	6	5	4	3	2	1	0	
$00	ICTYPEID	0	0	0	0	0	0	0	1	R
$01	ICMFGID	0	0	0	0	0	0	1	0	R
$02	ICREVID	0	0	1	ICREVID[4]	0	0	0	0	R
$03	MODTYPE	0	0	0	0	0	MODTYPE[2]	MODTYPE[1]	MODTYPE[0]	U,R
$04	MODMFGID	0	0	0	0	0	MODMFGID[2]	MODMFGID[1]	MODMFGID[0]	U,R
$05	MODREV	0	0	0	0	0	MODREV[2]	MODREV[1]	MODREV[0]	U,R
$06	USERID1	USERID1[7]	USERID1[6]	USERID1[5]	USERID1[4]	USERID1[3]	USERID1[2]	USERID1[1]	USERID1[0]	U,R
$07 - $08	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	R
$09	PN	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]	F,R
$0A	SN0	SN[7]	SN[6]	SN[5]	SN[4]	SN[3]	SN[2]	SN[1]	SN[0]	F,R
$0B	SN1	SN[15]	SN[14]	SN[13]	SN[12]	SN[11]	SN[10]	SN[9]	SN[8]	F,R
$0C	SN2	SN[23]	SN[22]	SN[21]	SN[20]	SN[19]	SN[18]	SN[17]	SN[16]	F,R
$0D	SN3	SN[31]	SN[30]	SN[29]	SN[28]	SN[27]	SN[26]	SN[25]	SN[24]	F,R
$0E - $0F	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	R
$10	DSIREV	0	0	0	0	0	0	0	1	R
$11	PHYSADDR	0	0	0	0	PADDR[3]	PADDR[2]	PADDR[1]	PADDR[0]	U,R/W
$12	BDM_CFG	0	0	0	0	0	0	0	BDM_EN	R/W
$13	CRM_CFG	0	0	0	CK_CAL_RST	CRM_PER[1]	CRM_PER[0]	CK_CAL_EN	SS_EN	R/W
$14	PDCM_CFG	0	0	0	0	0	0	DATALENGTH	STATLENGTH	R/W
$15	PDCM_EN	PDCM_EN	0	0	0	0	0	0	0	R/W
$16	CHIPTIME	0	0	0	0	0	CHIPTIME[2]	CHIPTIME[1]	CHIPTIME[0]	R/W
$17	PDCM_PER	0	0	0	0	0	PDCM_PER[2]	PDCM_PER[1]	PDCM_PER[0]	R/W
$18	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	R/W
$19	PDCM_RSPST_L	PDCM_RSPST[7]	PDCM_RSPST[6]	PDCM_RSPST[5]	PDCM_RSPST[4]	PDCM_RSPST[3]	PDCM_RSPST[2]	PDCM_RSPST[1]	PDCM_RSPST[0]	R/W
$1A	PDCM_RSPST_H	0	0	0	0	PDCM_RSPST[11]	PDCM_RSPST[10]	PDCM_RSPST[9]	PDCM_RSPST[8]	R/W
$1B	PDCM_CMD_B_L	PDCM_CMD_B[7]	PDCM_CMD_B[6]	PDCM_CMD_B[5]	PDCM_CMD_B[4]	PDCM_CMD_B[3]	PDCM_CMD_B[2]	PDCM_CMD_B[1]	PDCM_CMD_B[0]	R/W
$1C	PDCM_CMD_B_H	0	0	0	0	PDCM_CMD_B[11]	PDCM_CMD_B[10]	PDCM_CMD_B[9]	PDCM_CMD_B[8]	R/W
$1D	SOURCEID	0	0	0	0	SOURCEID[3]	SOURCEID[2]	SOURCEID[1]	SOURCEID[0]	R/W
$1E	BUSSW_CTRL	0	0	0	0	0	0	0	BUSSW_CTRL	R/W
$1F	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	R
$20	DEVLOCK	LOCK_U	0	0	0	0	0	0	0	U,R
$21	DEVSTAT	RESERVED	DEVRES	OSCTRAIN_ERR	BUSSW	TESTMODE	ST_ACTIVE	OFFSET_ERR	OC_INIT	R
$22	DEVSTAT2	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_UNLOCKED	RESERVED	ST_INCMPLT	VBUF_UV_ERR	BUSI_UV_ERR	R
$23	ST_CONTROL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ST_5_PTRN	ST_A_PTRN	SELFTEST	R/W
$24	WRITE_NVM_EN	0	0	0	0	0	0	WR_NVM_EN[1]	WR_NVM_EN[0]	R/W
$25	C_CRMCRCPLY	C_CRMCRCPLY[7]	C_CRMCRCPLY[6]	C_CRMCRCPLY[5]	C_CRMCRCPLY[4]	C_CRMCRCPLY[3]	C_CRMCRCPLY[2]	C_CRMCRCPLY[1]	C_CRMCRCPLY[0]	R/W
$26	R_CRMCRCPLY	R_CRMCRCPLY[7]	R_CRMCRCPLY[6]	R_CRMCRCPLY[5]	R_CRMCRCPLY[4]	R_CRMCRCPLY[3]	R_CRMCRCPLY[2]	R_CRMCRCPLY[1]	R_CRMCRCPLY[0]	R/W
$27	PDCMCRCPLY	PDCMCRCPLY[7]	PDCMCRCPLY[6]	PDCMCRCPLY[5]	PDCMCRCPLY[4]	PDCMCRCPLY[3]	PDCMCRCPLY[2]	PDCMCRCPLY[1]	PDCMCRCPLY[0]	R/W
$28 - $2F	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	R
$30	ACC_FCTCFG	0	PCM	AXIS	RNG[4]	RNG[3]	RNG[2]	RNG[1]	RNG[0]	F,R
$31	ACC_STDATA	ACC_ST[7]	ACC_ST[6]	ACC_ST[5]	ACC_ST[4]	ACC_ST[3]	ACC_ST[2]	ACC_ST[1]	ACC_ST[0]	F,R
$32	ACC_CFG	LPF[3]	LPF[2]	LPF[1]	LPF[0]	SD	OC_FILT[2]	OC_FILT[1]	OC_FILT[0]	R/W
$33	ACC_DATAL	ACC_D[7]	ACC_D[6]	ACC_D[5]	ACC_D[4]	ACC_D[3]	ACC_D[2]	ACC_D[1]	ACC_D[0]	R
$34	ACC_DATAH	ACC_D[15]	ACC_D[14]	ACC_D[13]	ACC_D[12]	ACC_D[11]	ACC_D[10]	ACC_D[9]	ACC_D[8]	R
$35	ACC_STAT	0	0	0	0	0	ST_ACTIVE	OFFSET_ERR	OC_INIT	R

Type codes:
F: Freescale programmed OTP location.
U: User programmable OTP location.
R: Readable register.
R/W: User writable register.

3.1.1 IC Type register

The IC Type register is a read-only register which contains the IC type as defined in the DSI3 standard.

Table 5. IC Type register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$00	ICTYPEID	0	0	0	0	0	0	0	1

3.1.2 IC Manufacturer Identification register

The IC Manufacturer Identification register is a read-only register which contains the IC manufacturer ID as defined in the DSI3 standard.

Table 6. IC Manufacturer Identification register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$01	ICMFGID	0	0	0	0	0	0	1	0

3.1.3 IC Manufacturer Revision register

The IC revision register is a read-only register which contains the IC revision as defined in the DSI3 standard. ICREVID[4] is set to ‘0’ for the MMAx7xxJWR2 part numbers and set to ‘1’ for the MMAx7xxWR2 part numbers.

Table 7. IC Manufacturer Revision register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$02	ICREVID	0	0	1	ICREVID[4]	0	0	0	0

3.1.4 Module Type register (MODTYPE)

The module type register is a user programmed OTP register which contains user specific module identification information as defined in the DSI3 Standard. The register is included in the user programmed OTP verification described in Section 3.2.

Table 8. Module Type register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$03	MODTYPE	0	0	0	0	0	MODTYPE[2]	MODTYPE[1]	MODTYPE[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.5 Module Manufacturer ID register (MODMFGID)

The module manufacturer identification register is a user-programmed OTP register which contains user specific module identification information as defined in the DSI3 Standard. The register is included in the user programmed OTP verification described in Section 3.2.

Table 9. Module Manufacturer ID register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$04	MODMFGID	0	0	0	0	0	MODMFGID[2]	MODMFGID[1]	MODMFGID[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.6 Module Revision register (MODREV)

The Module Revision register is a user programmed OTP register which contains user specific module identification information as defined in the DSI3 Standard. The register is included in the user programmed OTP verification described in Section 3.2.

Table 10. Module Revision register (MODREV)

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$05	MODREV	0	0	0	0	0	MODREV[2]	MODREV[1]	MODREV[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.7 User ID 1 registers (USERID1)

User ID registers 1 is a user programmable OTP register which contains user specific information. The bits have no impact on the device performance. The register is included in the user programmed OTP verification described in Section 3.2.

Table 11. User ID 1 registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$06	USERID1	USERID1[7]	USERID1[6]	USERID1[5]	USERID1[4]	USERID1[3]	USERID1[2]	USERID1[1]	USERID1[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.8 Part Number register

The Part Number register is a factory-programmed OTP register which includes the numeric portion of the device part number. The register is included in the factory-programmed OTP verification described in Section 3.2. Beyond this, the contents of the part number register have no impact on device operation or performance.

Table 12. Part Number register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$09	PN	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]
Factory Default		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

PN Register Value		Range (g)	Transducer
Decimal	**HEX**		
2	0x02	25	Medium-g Lateral
12	0x0C	125	High-g Lateral
18	0x12	187	High g Lateral
25	0x19	250	High-g Lateral / High-g Vertical
37	0x25	375	High-g Lateral

3.1.9 Device Serial Number registers

The serial number registers are factory-programmed OTP registers which include a unique serial number and lot number combination for each device, regardless of range or axis of sensitivity. Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned. The serial number registers are included in the factory-programmed OTP verification described in Section 3.2. Beyond this, the contents of the serial number registers have no impact on device operation or performance.

Table 13. Device Serial Number registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0A	SN0	SN[7]	SN[6]	SN[5]	SN[4]	SN[3]	SN[2]	SN[1]	SN[0]
$0B	SN1	SN[15]	SN[14]	SN[13]	SN[12]	SN[11]	SN[10]	SN[9]	SN[8]
$0C	SN2	SN[23]	SN[22]	SN[21]	SN[20]	SN[19]	SN[18]	SN[17]	SN[16]
$0D	SN3	SN[31]	SN[30]	SN[29]	SN[28]	SN[27]	SN[26]	SN[25]	SN[24]
Factory Default		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

The serial number is composed of the following information:

Bit range	Content
SN[12:0]	Serial Number
SN[31:13]	Lot Number

3.1.10 DSI Protocol Revision register (DSI_REV)

The factory-configuration register is a read-only register which contains the DSI revision supported, as specified in the DSI3 standard. The protocol revision value for DSI3 is $01.

Table 14. DSI Protocol Revision register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$10	DSIREV	0	0	0	0	0	0	0	1

3.1.11 Physical Address register (PHYSADDR)

The physical address register is a user programmed OTP register which contains the physical address of the slave.

If the physical address is zero, the address is assigned either during Discovery Mode as described in Section 4.1.3 or during Command and Response Mode as described in Section 4.1.2.

If the physical address is non-zero, the device ignores Discovery Mode and uses the programmed physical address for Command and Response Mode, as described in Section 4.2. The physical address register value can be changed by a Command and Response Mode register write command. However, if the LOCK_U bit is set, the value will always be reset to the OTP array value after a reset.

The OTP register value is included in the user programmed OTP verification described in Section 3.2. The value is also stored in a secondary register that can be written as described above. This secondary register is included in the read/write array verification described in Section 3.2.

Table 15. Physical Address register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$11	PHYSADDR	0	0	0	0	PADDR[3]	PADDR[2]	PADDR[1]	PADDR[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.12 DSI3 Background Diagnostic Mode Configuration register (BDM_CFG)

The DSI3 Background Diagnostic Mode configuration register is a user programmed read/write register which contains user specific configuration information for DSI3 Background Diagnostic Mode. The register is included in the read/write array verification described in Section 3.2. Reference Section 4.3 for details regarding Background Diagnostic Mode.

Table 16. DSI3 Background Diagnostic Mode Configuration register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$12	BDM_CFG	0	0	0	0	0	0	0	BDM_EN
Factory Default		0	0	0	0	0	0	0	0

3.1.12.1 Background Diagnostic Mode Enable (BDM_EN)

The Background Diagnostic Mode enable bit enables Background Diagnostic Mode as described below and in Section 3.1.14. Reference Section 4.3 for details regarding Background Diagnostic Mode.

BDM_EN	BDM command fragment length
0	Disabled
1	4

3.1.13 DSI3 Command and Response Mode Configuration register (CRM_CFG)

The DSI3 Command and Response Mode configuration register is a user programmed read/write register which contains user specific configuration information for DSI3 Command and Response Mode. The register is included in the read/write array verification described in Section 3.2.

Table 17. DSI3 Command and Response Mode Configuration register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$13	CRM_CFG	0	0	0	CK_CAL_RST	CRM_PER[1]	CRM_PER[0]	CK_CAL_EN	SS_EN
Factory Default		0	0	0	0	0	0	0	0

3.1.13.1 Clock Calibration Value Reset (CK_CAL_RST)

The clock calibration reset bit controls the state of the oscillator training when the CK_CAL_EN bit is cleared as described in the table in Section 3.1.13.3. Reference Section 3.4.1 for details regarding oscillator training.

3.1.13.2 Command and Response Mode Period (CRM_PER[1:0])

The Command and Response Mode Period bits set the period for Command and Response Mode commands in increments of the Periodic Data Collection Mode Period (PDCM_PER). This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the CRM_CFG register. Command and Response Mode commands will be decoded and responded to regardless of the value of this register as long as the general Command and Response Mode timing parameters specified in Section 2.6 are met. Reference Section 3.4.1 for details regarding oscillator training.

CRM_PER[1]	CRM_PER[0]	Command and Response Mode period (Multiples of the Periodic Data Collection Mode period)
0	0	1
0	1	2
1	0	4
1	1	8

3.1.13.3 Clock Calibration Enable (CK_CAL_EN)

The clock calibration enable bit enables oscillator training over the DSI communication interface. Reference Section 3.4.1 for details regarding oscillator training.

CK_CAL_EN	CK_CAL_RST	Oscillator training
0	0	The oscillator value is maintained at the last trained value prior to clearing the CK_CAL_RST bit.
0	1	The oscillator value is reset to the untrained value with a tolerance specified in Section 2.8.
1	x	Oscillator is trained as specified in Section 3.4.1

3.1.13.4 Simultaneous Sampling Enable (SS_EN)

The simultaneous sampling enable bit selects between one of two data latency methods. Reference Section 3.7 for details regarding sample timing.

SS_EN	Data latency
0	Synchronous Sampling Mode: Latency relative to transmission start time (PDCM_RSPST)
1	Simultaneous Sampling Mode: Latency relative to the start of the Periodic Data Collection Mode command (falling edge)

3.1.14 Periodic Data Collection Mode Enable register (PDCM_EN)

The Periodic Data Collection Mode register is a read/write register which contains the Periodic Data Collection Mode Enable bit. The register is included in the read/write array verification described in Section 3.2.

Table 18. Periodic Data Collection Mode Enable register

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$15	PDCM_EN	PDCM_EN	0	0	0	0	0	0	0
Factory Default		0	0	0	0	0	0	0	0

The Periodic Data Collection Mode Enable bit enables Periodic Data Collection Mode as described in Section 4.3. The PDCM_EN bit can be set by receiving the Enter PDCM command in Command and Response Mode, or by a Command and Response Mode register write command. Once Periodic Data Collection Mode is enabled, the registers listed in Section 3.2.3 are locked and the user array read/write register array verification is enabled.

Once set, the PDCM_EN bit can only be cleared by a device reset.

PDCM_EN	BDM_EN	Command and Response Mode	Periodic Data Collection Mode	Background Diagnostic Mode
0	0	Enabled	Disabled	Disabled
0	1	Enabled	Disabled	Disabled
1	0	Disabled	Enabled	Disabled
1	1	Disabled	Enabled	Enabled

3.1.15 DSI3 Periodic Data Collection Mode Configuration registers (PDCM_CFG1, PDCM_CFG2)

The DSI3 Periodic Data Collection Mode configuration registers are user programmed read/write registers which contain user specific configuration information for DSI3 Periodic Data Collection Mode. The registers are included in the read/write array verification described in Section 3.2.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$14	PDCM_CFG	0	0	0	0	0	0	DATALENGTH	STATLENGTH
$16	CHIPTIME	0	0	0	0	0	CHIPTIME[2]	CHIPTIME[1]	CHIPTIME[0]
$17	PDCM_PER	0	0	0	0	0	PDCM_PER[2]	PDCM_PER[1]	PDCM_PER[0]
$18	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
$19	PDCM_RSPST_L	PDCM_RSPST[7]	PDCM_RSPST[6]	PDCM_RSPST[5]	PDCM_RSPST[4]	PDCM_RSPST[3]	PDCM_RSPST[2]	PDCM_RSPST[1]	PDCM_RSPST[0]
$1A	PDCM_RSPST_H	0	0	0	0	PDCM_RSPST[11]	PDCM_RSPST[10]	PDCM_RSPST[9]	PDCM_RSPST[8]
$1B	PDCM_CMD_B_L	PDCM_CMD_B[7]	PDCM_CMD_B[6]	PDCM_CMD_B[5]	PDCM_CMD_B[4]	PDCM_CMD_B[3]	PDCM_CMD_B[2]	PDCM_CMD_B[1]	PDCM_CMD_B[0]
$1C	PDCM_CMD_B_H	0	0	0	0	PDCM_CMD_B[11]	PDCM_CMD_B[10]	PDCM_CMD_B[9]	PDCM_CMD_B[8]
Factory Default		0	0	0	0	0	0	0	0

3.1.15.1 Data Field Length (DATALENGTH)

The data field length bits set the data field length in the Periodic Data Collection Mode response as described below. The sensitivity of the data is the same for both the 10-bit and 14-bit data lengths. If the 14-bit data length is selected, four additional bits of range are transmitted. These additional four bits of range are intended for test use only and are not covered by the specifications listed in Section 2.

DATALENGTH	Data Length
0	10 Bits
1	14 Bits

3.1.15.2 Status Field Length (STATLENGTH)

The status field length bits set the status field length in the Periodic Data Collection Mode response as described below. Reference Section 4.3.2.2 for details regarding the Periodic Data Collection Mode status field.

STATLEN	Status Field Length (Bits)	Data Transmitted
0	4	Reference Section 4.3.2.2
1	0	N/A

3.1.15.3 Chip time (CHIPTIME)

The DSI3 Periodic Data Collection Mode configuration chip time bits set the chip time for Periodic Data Collection Mode as described below.

CHIPTIME[2]	CHIPTIME[1]	CHIPTIME[0]	Chip time
0	0	0	3.0 µs
0	0	1	3.5 µs
0	1	0	4.0 µs
0	1	1	4.5 µs
1	0	0	5.0 µs
1	0	1	5.5 µs
1	1	0	6.0 µs
1	1	1	6.5 µs

3.1.15.4 Periodic Data Collection Mode Period (PDCM_PER[3:0])

The Periodic Data Collection Mode period selection bits set the period data collection mode period to be used by the DSI master as shown in the table below. This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the CRM_CFG register. Periodic Data Collection Mode and Background Diagnostic Mode commands will be decoded and responded to regardless of the value of this register as long as the general Periodic Data Collection Mode timing parameters specified in Section 2.6 are met. Reference Section 3.4.1 for details regarding oscillator training.

PDCM_PER[2]	PDCM_PER[1]	PDCM_PER[0]	Periodic Data Collection Mode Period
0	0	0	500 µs
0	0	1	125 µs
0	1	0	250 µs
0	1	1	333 µs
1	0	0	500 µs
1	0	1	1000 µs
1	1	0	2000 µs
1	1	1	4000 µs

3.1.15.5 Periodic Data Collection Mode Response Start Time (PDCM_RSPST[11:0])

The DSI3 Periodic Data Collection Mode Response Start Time bits set the Periodic Data Collection Mode response start time. The value is stored in 1 µs increments, with zero as the default value of 20 µs.

Care must be taken to prevent from programming response start times which cause data contention in the system.

PDCM_RSPST[11:0]	Periodic Data Collection Mode Response Start Time
0 - 20	20 µs
21 - 4095	PDCM response start = PDCM_RSPST x 1µs

3.1.15.6 Periodic Data Collection Mode Command Blocking time (PDCM_CMD_B[11:0])

The DSI3 Periodic Data Collection Mode command blocking time bits set the Periodic Data Collection Mode command blocking time. in 1µs increments, with zero as the default value of 450 µs. Reference Section 3.6.1 for details regarding the command receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper command decoding in the system and to ensure proper sampling of the V_{HIGH} voltage. As shown in Section 3.6.1, Figure 29, The V_{HIGH} voltage is initially captured at the end of the command blocking time and then filtered. The user must ensure that the command blocking end time is set for a time when no command or response transmissions are occurring to provide the most stable BUS_I voltage.

PDCM_CMD_B[11:0]	Periodic Data Collection Mode Command blocking time
0	450 µs
Non-Zero	PDCM Command blocking time = PDCM_CMD_B x 1 µs

3.1.16 Source Identification register (SOURCEID)

The source identification register is a user programmed read/write register which contains the source identification which will be used for Periodic Data Collection Mode as described in Section 4.3.2.2. The register is included in the read/write array verification described in Section 3.2. SOURCEID[3:0] is initialized to the values stored in PADDR[3:0] after reset.

Table 19. Source Identification register

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$1D	SOURCEID	0	0	0	0	SOURCEID[3]	SOURCEID[2]	SOURCEID[1]	SOURCEID[0]
Factory Default		0	0	0	0	PADDR[3]	PADDR[2]	PADDR[1]	PADDR[0]

3.1.17 Bus Switch Control register (BUSSW_CTRL)

The bus switch control register is a user programmed read/write register which controls the state of the bus switch output driver. The register is included in the read/write array verification describe in Section 3.2.

Table 20. Bus Switch Control register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$1E	BUSSW_CTRL	0	0	0	0	0	0	0	BUSSW_CTRL
Factory Default		0	0	0	0	0	0	0	0

The BUSSW_CTRL bit controls the state of the BUSSW pin.

BUSSW_CTRL	BUSSW Pin Sate
0	High impedance An External Pullup is required if an external switch is connected
1	Output Actively Driven Low

3.1.18 Device Lock register (DEVLOCK)

The device lock register is a user programmed OTP register which contains the LOCK_U bit. The register is included in the user programmed OTP verification describe in Section 3.2. The LOCK_U bit allows the user to prevent writes to the user configuration array once OTP programming is complete. If the LOCK_U bit is written to '1' when an "Execute Programming of NVM" command is executed, the LOCK_U OTP bit will be programmed. Upon completion of the OTP programming, future OTP writes to both the OTP array and the mirror registers for the array are prevented and the User Programmable OTP Array Verification is activated. The exception to this is the PADDR[3:0] bits. Once the LOCK_U bit is set, the PADDR[3:0] OTP bits cannot be written. However, the mirror register bits for PADDR[3:0] can be written to allow changes to the physical address through Command and Response Mode.

Table 21. Device Lock register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$20	DEVLOCK	LOCK_U	0	0	0	0	0	0	0
Factory Default		0	0	0	0	0	0	0	0

3.1.19 Device Status registers (DEVSTAT, DEVSTAT2)

The device status registers are read-only registers which contain device status information.

Table 22. Device Status registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$21	DEVSTAT	RESERVED	DEVRES	OSCTRAIN_ERR	BUSSW	TESTMODE	ST_ACTIVE	OFFSET_ERR	OC_INIT
$22	DEVSTAT2	F_OTP_ERR	U_OTP_ERR	U_RW_ERR	U_UNLOCKED	RESERVED	ST_INCMPLT	VBUF_UV_ERR	BUSIN_UV_ERR

3.1.19.1 Device Reset (DEVRES)

The device reset bit is set following a device reset. The device reset bit is cleared only by a read of the DEVSTAT register.

DEVRES	Error Condition
0	Normal operation
1	Device reset occurred

3.1.19.2 Oscillator Training Error (OSCTRAIN_ERR)

The oscillator training error bit is set if an error detected in either the oscillator training settings, or the master communication timing. Reference Section 3.4.2.

OSCTRAIN_ERR	Error Condition
0	No error detected
1	Oscillator Training Error. Reference Section 3.4.2

3.1.19.3 Bus Switch Status (BUSSW)

The Bus Switch status bit is set if the bus switch output pin is activated.

BUSSW	BUSSW Pin State
0	BUSSW pin is inactive
1	BUSSW pin is active

3.1.19.4 Test Mode (TESTMODE)

The test mode bit is set if the device is in test mode.

TESTMODE	Operating Mode
0	Test Mode is not active
1	Test Mode is active

3.1.19.5 Self-Test Active (ST_ACTIVE)

The self-test active bit is set if any of the self-test bits in the ST_CONTROL register are set.

ST_ACTIVE	Condition
0	ST_5_PTRN & ST_A_PTRN & SELFTEST = 0
1	ST_5_PTRN | ST_A_PTRN |SELFTEST = 1

3.1.19.6 Offset Error Flag (OFFSET_ERR)

The offset error flag is set if the acceleration signal reaches the offset limit.

OFFSET_ERR	Error Condition
0	No error detected
1	Offset error detected

3.1.19.7 Offset Cancellation Init Status Flag (OC_INIT)

The offset cancellation initialization status bit is set once the offset cancellation initialization process is complete, and the filter has switched to normal mode.

OC_INIT	Error Condition
0	Offset Cancellation in initialization
1	Offset Cancellation initialization complete

3.1.19.8 Freescale OTP Array Error (F_OTP_ERR)

The factory OTP array error bit is set if a register data fault is detected in the factory OTP array. A device reset is required to clear the error.

F_OTP_ERR	Error Condition
0	No error detected
1	Error Detected in the Factory OTP Array

3.1.19.9 User OTP Array Error (U_OTP_ERR)

The user OTP array error bit is set if a register data fault is detected in the user OTP array. A device reset is required to clear the error.

U_OTP_ERR	Error Condition
0	No error detected
1	Error Detected in the User OTP Array

3.1.19.10 User Read/Write Array Error (U_RW_ERR)

The user read/write array error bit is set if a register data fault is detected in the user read/write array. A device reset is required to clear the error.

U_RW_ERR	Error Condition
0	No error detected
1	Error Detected in the User Read/Write Array

3.1.19.11 User OTP Array Unlocked (U_UNLOCKED)

The user OTP array unlocked bit is set if LOCK_U bit in the DEVLOCK register is not set, indicating that the user array is not locked.

U_UNLOCKED	Condition
0	User Array is Locked
1	User Array is not Locked

3.1.19.12 Self-Test Incomplete (ST_INCMPLT)

The self-test incomplete bit is set after a device reset and is only cleared when the SELFTEST bit is written to a ‘1’ through Command and Response Mode.

ST_INCMPLT	Condition
0	Self-test has been activated since the last Reset
1	Self-test has not been activated since the last Reset

3.1.19.13 V_{BUF} Undervoltage Error (VBUF_UV_ERR)

The V_{BUF} undervoltage error bit is set if the VBUF voltage falls below the voltage specified in Section 2.3. Reference Section 3.3 for details on the V_{BUF} undervoltage monitor. The VBUF_UV_ERR bit is cleared on a read of the DEVSTAT2 register.

VBUF_UV_ERR	Error Condition
0	No error detected
1	VBUF Voltage Low

3.1.19.14 BUS IN Undervoltage Error (BUSI_UV_ERR)

The BUS IN undervoltage error bit is set if the BUS_I voltage falls below the voltage specified in Section 2.3. Reference Section 3.3 for details on the BUS IN undervoltage monitor. The BUSI_UV_ERR bit is cleared on a read of the DEVSTAT2 register.

BUSI_UV_ERR	Error Condition
0	No error detected
1	BUS_I Voltage Low

3.1.20 Self-Test Control register (ST)

The self-test control register is a user programmed read/write register which contains user specific device configuration information. The register is included in the read/write array verification described in Section 3.2.

Table 23. Self-Test Control register

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$23	ST_CONTROL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ST_PTRN_5	ST_PTRN_A	SELFTEST
Factory Default		0	0	0	0	0	0	0	0

3.1.20.1 Self-Test Pattern Write Bits (ST_PTRN_5, ST_PTRN_A)

The self-test pattern write bits inhibit DSP writes to the ACC_DATAH and ACC_DATAL registers and forces a write of specific values to the registers when set. When cleared, DSP writes to the ACC_DATAH and ACC_DATAL registers resume as specified. These bits are automatically cleared when the PDCM bit is set.

ST_PTRN_A	ST_PTRN_5	Function
0	0	DSP writes to the ACC_DATAH and ACC_DATAL registers as specified
0	1	0x5555 written to ACC_DATAH and ACC_DATAL. DSP write to registers inhibited.
1	0	0xAAAA written to ACC_DATAH and ACC_DATAL. DSP write to registers inhibited.
1	1	0xFFFF written to ACC_DATAH and ACC_DATAL. DSP write to registers inhibited.

3.1.20.2 Self-Test Control (SELFTEST)

The self-test control bit activates and deactivates self-test as described below. Reference Section 3.5.2 for details regarding self-test. This bit is automatically cleared when the PDCM bit is set.

Self-test	Function
0	Self-test deactivated
1	Self-test activated

After a device reset, the ST_INCMPLT bit is set in the DEVSTAT2 register and the device status defaults to Self-test Activation Incomplete as defined in Section 4.3.2.2. The ST_INCMPLT bit will only be cleared by writing the SELFTEST bits to ‘1’ through Command and Response Mode. If PDCM is entered without activating self-test, the status bits will include the Self-test Activation Incomplete” status until a device reset.

If both the SELFTEST bit and one of the Self-test Pattern Write bits are set, the self-test pattern data will be written to the ACC_DATAH and ACC_DATAL registers. However, the transducer self-test will still be activated as described in Section 3.5.2.