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Xtrinsic MMA51xxKW PSI5 Inertial Sensor

The MMA51xxKW family, a SafeAssure solution, includes the AKLV27 and PSI5 Version 1.3 compatible overdamped Z-axis satellite accelerometers.

Features

- $\pm 60g$ to $\pm 480g$ Full-Scale Range
- Selectable 400 Hz, 3-Pole, or 4-pole Low-Pass Filter
- Single Pole High Pass Filter with Fast Startup and Output Rate Limiting
- PSI5 Version 1.3 Compatible
 - PSI5-P10P-500/3L Compatible
 - Programmable Time Slots with 0.5 μs Resolution
 - Selectable Baud Rate: 125 kBaud or 190.5 kBaud
 - Selectable Data Length: 8 or 10 bits
 - Selectable Error Detection: Even Parity, or 3-bit CRC
 - Optional Daisy Chain with External Low-Side Switch
 - Two-Wire Programming Mode
- 16 μs Internal Sample Rate, with Interpolation to 1 μs
- Pb-Free 16-Pin QFN, 6 by 6 Package
- Qualified AECQ100, Revision G, Grade 1 (-40°C to +125°C)
(<http://www.aecouncil.com/>)

Typical Applications

- Airbag Front and Side Crash Detection

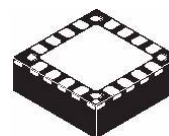
ORDERING INFORMATION

Device	Axis	Range	Package	Shipping
MMA5106KW	Z	$\pm 60g$	2086-01	Tubes
MMA5112KW	Z	$\pm 120g$	2086-01	Tubes
MMA5124KW	Z	$\pm 240g$	2086-01	Tubes
MMA5148KW	Z	$\pm 480g$	2086-01	Tubes
MMA5106KWR2	Z	$\pm 60g$	2086-01	Tape & Reel
MMA5112KWR2	Z	$\pm 120g$	2086-01	Tape & Reel
MMA5124KWR2	Z	$\pm 240g$	2086-01	Tape & Reel
MMA5148KWR2	Z	$\pm 480g$	2086-01	Tape & Reel

For user register array programming, please consult your Freescale representative.

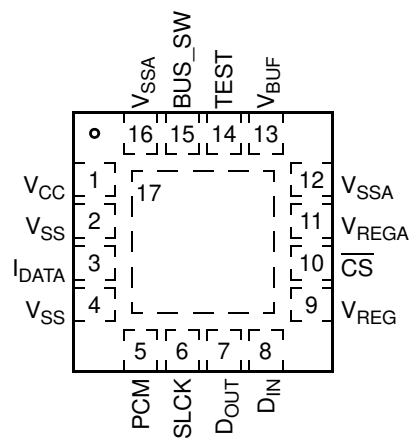
MMA51xxKW

Bottom View



16-PIN QFN
CASE 2086-01

Top View



PIN CONNECTIONS

Application Diagram

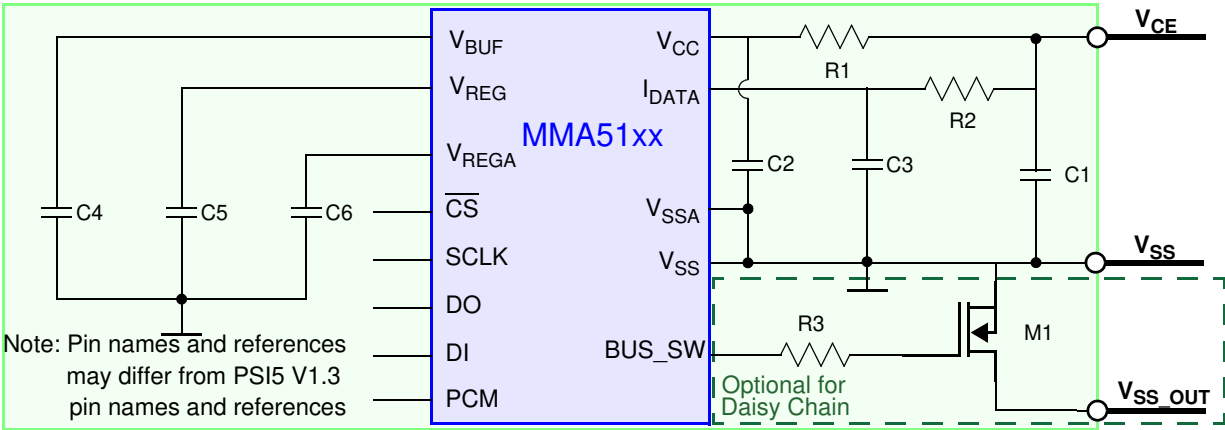


Figure 1. Application Diagram

External Component Recommendations			
Ref Des	Type	Description	Purpose
C1	Ceramic	2.2 nF, 10%, 50V minimum, X7R	V_{CC} Power Supply Decoupling and Signal Damping
C3	Ceramic	470 pF, 10%, 50V minimum, X7R	I_{DATA} Filtering and Signal Damping
C2	Ceramic	15 nF, 10%, 50V minimum, X7R	V_{CC} Power Supply Decoupling
C4, C5, C6	Ceramic	1 μ F, 10%, 10V minimum, X7R	Voltage Regulator Output Capacitor(s)
R1	General Purpose	82 Ω , 5%, 200 PPM	V_{CC} Filtering and Signal Damping
R2	General Purpose	27 Ω , 5%, 200 PPM	I_{DATA} Filtering and Signal Damping
R3	General Purpose	20 k Ω , 5%, 200 PPM	Gate Resistor for External Low-Side Daisy Chain FET
M1	N-Channel MOSFET	—	Low-Side Daisy Chain Transistor

Device Orientation

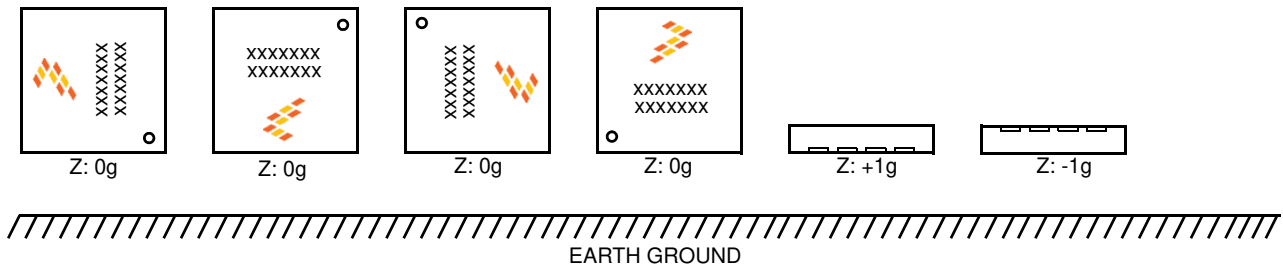


Figure 2. Device Orientation Diagram

Internal Block Diagram

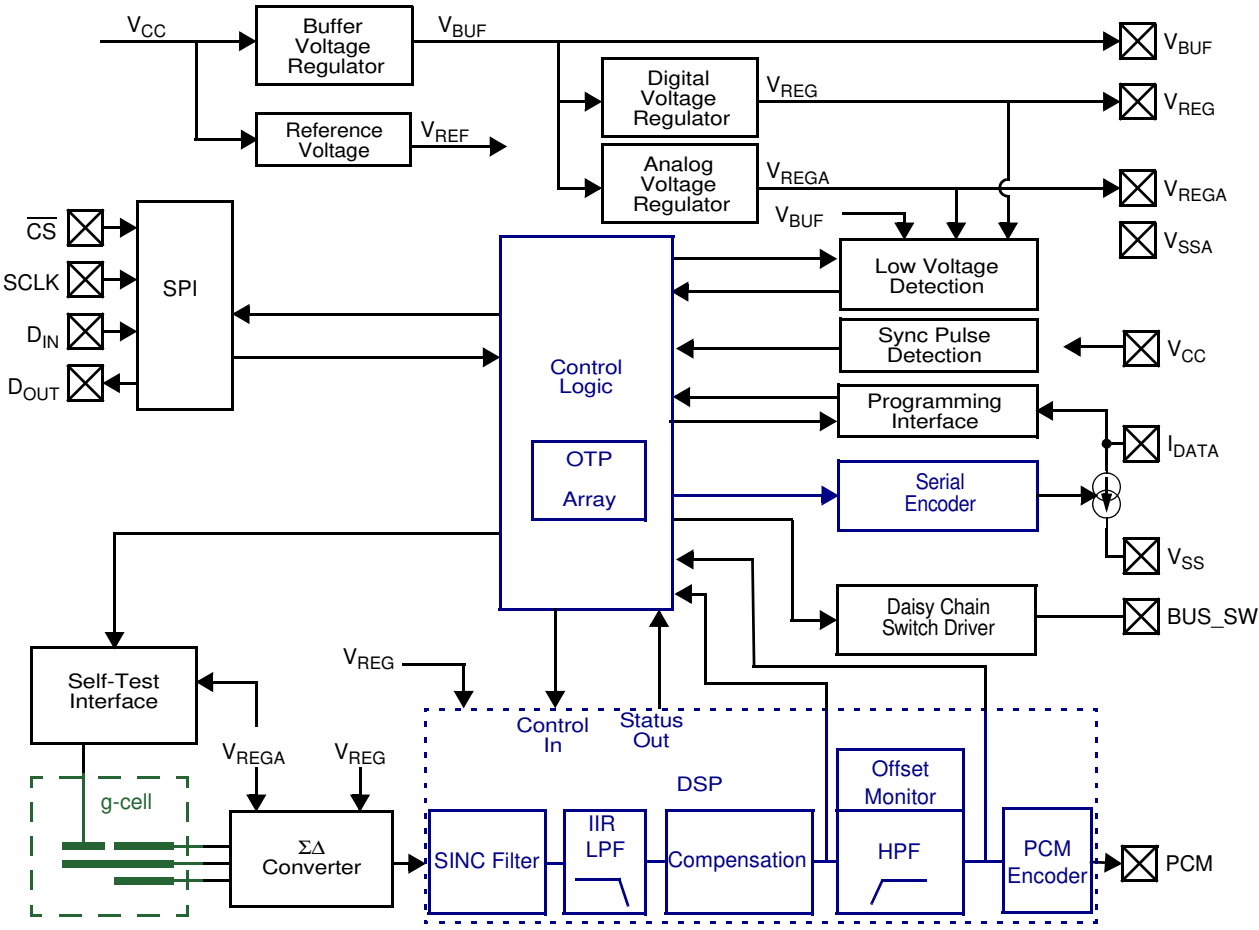


Figure 3. Block Diagram

1 Pin Connections

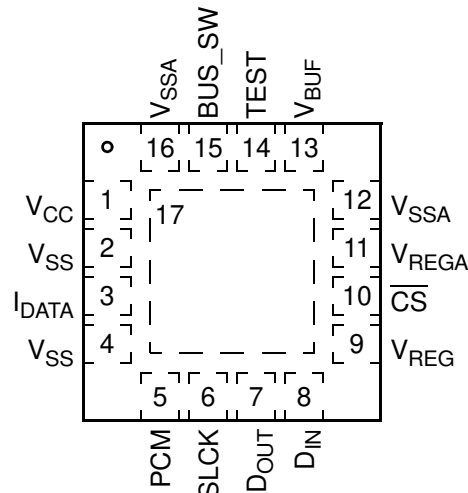


Figure 4. Top View, 16-Pin QFN Package

Table 1. Pin Description

Pin	Pin Name	Formal Name	Definition
1	V _{CC}	Supply	This pin is connected to the PSI5 power and data line through a resistor and supplies power to the device. An external capacitor must be connected between this pin and V _{SS} . Reference Figure 1 .
2	V _{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
3	I _{DATA}	Response Current	This pin is connected to the PSI5 power and data line through a resistor and modulates the response current for PSI5 communication. Reference Figure 1 .
4	V _{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
5	PCM	PCM Output	This pin provides a 4 MHz PCM signal proportional to the acceleration data for test purposes. The output can be enabled via OTP. Reference Section 3.5.3.7 . If unused, this pin must be left unconnected.
6	SCLK	SPI Clock	This input pin provides the serial clock to the SPI port for test purposes. An internal pulldown device is connected to this pin. This pin must be grounded or left unconnected in the application.
7	D _{OUT}	SPI Data Out	This pin functions as the serial data output from the SPI port for test purposes. This pin must be left unconnected in the application.
8	D _{IN}	SPI Data In	This pin functions as the serial data input to the SPI port for test purposes. An internal pulldown device is connected to this pin. This pin must be grounded or left unconnected in the application.
9	V _{REG}	Digital Supply	This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V _{SS} . Reference Figure 1 .
10	CS	Chip Select	This input pin provides the chip select to the SPI port for test purposes. An internal pullup device is connected to this pin. This pin must be left unconnected in the application.
11	V _{REGA}	Analog Supply	This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V _{SSA} . Reference Figure 1 .
12	V _{SSA}	Analog GND	This pin is the power supply return node for the analog circuitry.
13	V _{BUF}	Power Supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies both the analog (V _{REGA}) and digital (V _{REG}) supplies to provide immunity from EMC and supply dropouts on V _{CC} . An external capacitor must be connected between this pin and V _{SS} . Reference Figure 1 .
14	TEST	Test Pin	This pin is must be grounded or left unconnected in the application.
15	BUS_SW	Bus Switch Gate Drive	This pin is the drive for a low-side daisy chain switch. When daisy chain mode is enabled, this pin is connected to the gate of an n-channel FET which connects V _{SS} to V _{SS_OUT} . Reference Figure 1 . If unused, this pin must be left unconnected.
16	V _{SSA}	Analog GND	This pin is the power supply return node for the analog circuitry.
17	PAD	Die Attach Pad	This pin is the die attach flag, and is internally connected to V _{SS} . Reference Section 7 for die attach pad connection details.
	Corner Pads	Corner Pads	The corner pads are internally connected to V _{SS} .

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	
1	Supply Voltage (V_{CC} , I_{DATA})				(3)
2	Reverse Current ≤ 160 mA, $t \leq 80$ ms	V_{CC_REV}	-0.7	V	(3)
3	Continuous	V_{CC_MAX}	+20.0	V	(9)
	Transient (< 10 μ s)	V_{CC_TRANS}	+25.0	V	
4	V_{BUF} , Test, BUS_SW		-0.3 to +4.2	V	(3)
5	V_{REG} , V_{REGA} , SCLK, \overline{CS} , D_{IN} , D_{OUT} , PCM		-0.3 to +3.0	V	(3)
6	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	± 2000	g	(3)
7	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	± 2500	g	(3)
8	Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation)	h_{DROP}	1.2	m	(5)
9	Electrostatic Discharge (per AEC-Q100)				
10	External Pins (V_{CC} , I_{DATA} , V_{SS} , V_{SSA}), HBM (100 pF, 1.5 k Ω)	V_{ESD}	± 4000	V	(5)
11	HBM (100 pF, 1.5 k Ω)	V_{ESD}	± 2000	V	(5)
12	CDM (R = 0 Ω)	V_{ESD}	± 1500	V	(5)
	MM (200 pF, 0 Ω)	V_{ESD}	± 200	V	(5)
13	Temperature Range				
14	Storage	T_{stg}	-40 to +125	$^{\circ}$ C	(3)
	Junction	T_J	-40 to +150	$^{\circ}$ C	(9)
15	Thermal Resistance	θ_{JC}	2.5	$^{\circ}$ C/W	(9,14)

2.2 Operating Range

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
16	Supply Voltage	V_{CC}	V_L 4.2	—	V_H 17.0	V	(1)
17		V_{CC_UV}	$V_{VCC_UV_F}$	—	V_L	V	(9)
18	Programming Voltage ($I_{DATA} \leq 85$ mA) Applied to I_{DATA} , V_{CC}	V_{PP}	14.0	—	—	V	(3)
19	Operating Temperature Range						
20		T_A	T_L -40	—	T_H +105	$^{\circ}$ C	(1)
		T_A	-40	—	+125	$^{\circ}$ C	(3)

2.3 Electrical Characteristics - Supply and I/O

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
21	Quiescent Supply Current *	I_{IDLE}	4.0	—	8.0	mA	(1)
22	Modulation Supply Current *	I_{MOD}	$I_{IDLE} + 22.0$	$I_{IDLE} + 26.0$	$I_{IDLE} + 30.0$	mA	(1)
23	Inrush Current (Power On until V_{BUF} , V_{REG} , V_{REGA} Stable)	I_{INRUSH}	—	—	30	mA	(3)
24	Internally Regulated Voltages *	V_{BUF}	3.60	3.80	4.00	V	(1)
25	V_{REG} *	V_{REG}	2.425	2.50	2.575	V	(1)
26	V_{REGA} *	V_{REGA}	2.425	2.50	2.575	V	(1)
27	Low Voltage Detection Threshold						
28	V_{CC} Falling	$V_{VCC_UV_F}$	3.40	3.70	4.0	V	(3, 6)
29	V_{BUF} Falling	$V_{V_{BUF}_UV_F}$	2.95	3.15	3.35	V	(3, 6)
30	V_{REG} Falling	$V_{V_{REG}_UV_F}$	2.15	2.25	2.35	V	(3, 6)
	V_{REGA} Falling	$V_{V_{REGA}_UV_F}$	2.15	2.25	2.35	V	(3, 6)
	Hysteresis						
31	V_{CC}	$V_{V_{CC}_HYST}$	0.10	0.25	0.40	V	(3)
32	V_{BUF}	$V_{V_{BUF}_HYST}$	0.05	0.10	0.15	V	(3)
33	V_{REG}	$V_{V_{REG}_HYST}$	0.05	0.10	0.15	V	(3)
34	V_{REGA}	$V_{V_{REGA}_HYST}$	0.05	0.10	0.15	V	(3)
35	External Capacitor (V_{BUF} , V_{REG} , V_{REGA}) Capacitance		500	1000	1500	nF	(9)
36	ESR (including interconnect resistance)	ESR	0	—	200	m Ω	(9)
37	Synchronization Pulse (See Figure 5) V_{IDLE} Voltage Range *	V_{IDLE}	—	—	15.4	V	(3, 11)
38	DC Sync Pulse Detection Threshold *	ΔV_{SYNC}	$V_{IDLE} + 1.4$	$V_{IDLE} + 2.0$	$V_{IDLE} + 2.6$	V	(3, 6)
39	Sync Pulse Pulldown Current	I_{SYNC_PD}	—	$I_{MOD} - I_{IDLE}$	—	mA	(3)
40	Output High Voltage (DO) $I_{Load} = 100 \mu A$	V_{OH}	$V_{REG} - 0.1$	—	—	V	(9)
41	Output Low Voltage (DO) $I_{Load} = 100 \mu A$	V_{OL}	—	—	0.1	V	(9)
42	Input High Voltage CS, SCLK, DI	V_{IH}	$0.7 * V_{REG}$	—	—	V	(9)
43	Input Low Voltage CS, SCLK, DI	V_{IL}	—	—	$0.3 * V_{REG}$	V	(9)
44	Input Current High (at V_{IH}) (DI)	I_{IH}	-100	—	-10	μA	(9)
45	Low (at V_{IL}) (CS)	I_{IL}	10	—	100	μA	(9)
46	Pulldown Resistance (SCLK)	R_{PD}	20	—	100	k Ω	(9)
47	BUS_SW Output High Voltage (BUS_SW) $I_{Load} = 100 \mu A$	$V_{BUS_SW_OH}$	3.15	—	V_{BUF}	V	(9)
48	Output Low Voltage (BUS_SW) $I_{Load} = 100 \mu A$	$V_{BUS_SW_OL}$	0.0	—	0.45	V	(9)
49	Daisy Chain Addressing Mode Sync Pulse Period		—	$t_{S_S_PM_L}$	—	s	(7)
50	Bus Switch Output Activation Time (C = 50 pF) From last bit of "SetAdr" Response to 80% of $V_{BUS_SW_OH}$	t_{BUS_SW}	—	—	300	μs	(7)
51	Sync Pulse Blanking Time after "SetAdr" Command Received From last bit of "SetAdr" Response	$t_{DC_BLANKING}$		$200000 / f_{OSC}$		s	(7)

2.4 Electrical Characteristics - Sensor and Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
52	Sensitivity (10-bit output @ 100 Hz, referenced to 0 Hz)						
	±60g Range	* SENS	—	8	—	LSB/g	(1)
53	±120g Range	* SENS	—	4	—	LSB/g	(1)
54	±240g Range	* SENS	—	2	—	LSB/g	(1)
55	±480g Range	* SENS	—	1	—	LSB/g	(1)
	Total Sensitivity Error (including non-linearity)						
56	$T_A = 25^\circ\text{C}, \leq \pm 240\text{g}$	* ΔSENS_{240}	-5	—	+5	%	(1)
57	$T_L \leq T_A \leq T_H, \leq \pm 240\text{g}$	* ΔSENS_{240}	-7	—	+7	%	(1)
58	$T_L \leq T_A \leq T_H, \leq \pm 240\text{g}, V_{VCC_UV_F} \leq V_{CC} \leq V_L$	* ΔSENS_{240}	-7	—	+7	%	(9)
59	$T_A = 25^\circ\text{C}, > \pm 240\text{g}$	* ΔSENS_{480}	-5	—	+5	%	(1)
60	$T_L \leq T_A \leq T_H, > \pm 240\text{g}$	* ΔSENS_{480}	-7	—	+7	%	(1)
61	$T_L \leq T_A \leq T_H, > \pm 240\text{g}, V_{VCC_UV_F} \leq V_{CC} \leq V_L$	* ΔSENS_{480}	-7	—	+7	%	(9)
62	Digital Offset Before Offset Cancellation						
	10-bit	* $\text{OFF}_{10\text{Bit}}$	-52	0	+52	LSB	(1)
63	10-bit, $T_L \leq T_A \leq T_H, V_{VCC_UV_F} \leq V_{CC} \leq V_L$	* $\text{OFF}_{10\text{Bit}}$	-52	0	+52	LSB	(9)
64	Digital Offset After Offset Cancellation						
	10-bit, 0.3 Hz HPF or 0.1 Hz HPF	* $\text{OFF}_{10\text{Bit}}$	-1	0	+1	LSB	(1)
65	10-bit, 0.04 Hz HPF	* $\text{OFF}_{10\text{Bit}}$	-2	0	+2	LSB	(9)
66	Continuous Offset Monitor Limit						
	10-bit output, before compensation	OFF_{MON}	-66	—	+66	LSB	(3)
67	Range of Output (10-Bit Mode)						
	Acceleration	RANGE	-480	—	+480	LSB	(3)
68	Cross-Axis Sensitivity						
	X-axis to Z-Axis	* V_{XZ}	-5	—	+5	%	(3)
69	Y-axis to Z-Axis	* V_{YZ}	-5	—	+5	%	(3)
70	System Output Noise Peak (10-bit Mode, 1 Hz - 1 kHz, All Ranges)	* η_{Peak}	-4	—	+4	LSB	(3)
71	System Output Noise RMS (10-bit mode, 1 Hz - 1 kHz, All Ranges)	* η_{RMS}	—	—	+1.0	LSB	(3)
72	Non-linearity						
	10-bit output, $\leq \pm 240\text{g}$	$\text{NL}_{\text{OUT}_{240\text{g}}}$	-2	—	+2	%	(3)
73	10-bit output, $> \pm 240\text{g}$	$\text{NL}_{\text{OUT}_{480\text{g}}}$	-2	—	+2	%	(3)

2.5 Electrical Characteristics - Self-Test and Overload

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
74	10-Bit Output During Active Self-Test ($T_L \leq T_A \leq T_H$)						(3)
75	±60g Range	* g_{ST10_60Z}	120	—	280	LSB	(3)
76	±120g Range	* g_{ST10_120Z}	40	—	160	LSB	(3)
77	±240g Range	* g_{ST10_240Z}	35	—	153	LSB	(3)
77	±480g Range	* g_{ST10_480Z}	12	—	94	LSB	(3)
78	Acceleration (without hitting internal g-cell stops)						(9)
79	±60g Range Positive	$g_{g-cell_Clip60ZP}$	425	642	980	g	(9)
79	±60g Range Negative	$g_{g-cell_Clip60ZN}$	-1205	-720	-512	g	(9)
80	Acceleration (without hitting internal g-cell stops)						(9)
81	±120g Range Positive	$g_{g-cell_Clip120ZP}$	425	642	980	g	(9)
81	±120g Range Negative	$g_{g-cell_Clip120ZN}$	-1205	-720	-512	g	(9)
82	Acceleration (without hitting internal g-cell stops)						(9)
83	±240g Range Positive	$g_{g-cell_Clip240ZP}$	1450	2180	2800	g	(9)
83	±240g Range Negative	$g_{g-cell_Clip240ZN}$	-3100	-2210	-1800	g	(9)
84	Acceleration (without hitting internal g-cell stops)						(9)
85	±480g Range Positive	$g_{g-cell_Clip480ZP}$	2200	2800	3300	g	(9)
85	±480g Range Negative	$g_{g-cell_Clip480ZN}$	-3700	-3220	-2780	g	(9)
86	ΣΔ and Sinc Filter Clipping Limit						(9)
87	±60g Range Positive	$g_{ADC_Clip60ZP}$	159	238	336	g	(9)
87	±60g Range Negative	$g_{ADC_Clip60ZN}$	-334	-274	-216	g	(9)
88	ΣΔ and Sinc Filter Clipping Limit						(9)
89	±120g Range Positive	$g_{ADC_Clip120ZP}$	305	433	577	g	(9)
89	±120g Range Negative	$g_{ADC_Clip120ZN}$	-693	-544	-414	g	(9)
90	ΣΔ and Sinc Filter Clipping Limit						(9)
91	±240g Range Positive	$g_{ADC_Clip240ZP}$	836	1178	1599	g	(9)
91	±240g Range Negative	$g_{ADC_Clip240ZN}$	-1909	-1566	-1245	g	(9)
92	ΣΔ and Sinc Filter Clipping Limit						(9)
93	±480g Range Positive	$g_{ADC_Clip480ZP}$	1591	2014	2478	g	(9)
93	±480gZ Range Negative	$g_{ADC_Clip480ZN}$	-3217	-2856	-2524	g	(9)

2.6 Dynamic Electrical Characteristics - PSI5

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
Initialization Timing							
94	Phase 1	t_{PSI5_INIT1}	—	$532000 / f_{OSC}$	—	s	(7)
95	Phase 2 (10-Bit, Synchronous Mode, k = 4)	$t_{PSI5_INIT2_10s}$	—	$256 * t_{S-S}$	—	s	(7)
96	Phase 2 (8-Bit, Synchronous Mode, k = 8)	$t_{PSI5_INIT2_8s}$	—	$288 * t_{S-S}$	—	s	(7)
97	Phase 2 (10-Bit, Asynchronous Mode 0, k = 8)	$t_{PSI5_INIT2_10a0}$	—	$512 * t_{ASYN}$	—	s	(7)
98	Phase 2 (8-Bit, Asynchronous Mode 0, k = 16)	$t_{PSI5_INIT2_8a0}$	—	$576 * t_{ASYN}$	—	s	(7)
99	Phase 3 (10-Bit, Synchronous Mode, ST_RPT = 0)	$t_{PSI5_INIT3_10s}$	—	$2 * t_{S-S}$	—	s	(7, 12)
100	Phase 3 (8-Bit, Synchronous Mode, ST_RPT = 0)	$t_{PSI5_INIT3_8s}$	—	$2 * t_{S-S}$	—	s	(7, 12)
101	Phase 3 (10-Bit, Asynchronous Mode 0, ST_RPT = 0)	$t_{PSI5_INIT3_10a0}$	—	$19 * t_{ASYN}$	—	s	(7, 12)
102	Phase 3 (8-Bit, Asynchronous Mode 0, ST_RPT = 0)	$t_{PSI5_INIT3_8a0}$	—	$2 * t_{ASYN}$	—	s	(7, 12)
103	Offset Cancellation Stage 1 Operating Time	t_{OC1}	—	$320000 / f_{OSC}$	—	s	(7)
104	Offset Cancellation Stage 2 Operating Time	t_{OC2}	—	$280000 / f_{OSC}$	—	s	(7)
105	Self-Test Stage 1 Operating Time	t_{ST1}	—	$128000 / f_{OSC}$	—	s	(7)
106	Self-Test Stage 2 Operating Time	t_{ST2}	—	$128000 / f_{OSC}$	—	s	(7)
107	Self-Test Stage 3 Operating Time	t_{ST3}	—	$128000 / f_{OSC}$	—	s	(7)
108	Self-Test Repetitions	ST_RPT	0	—	5		(7, 12)
109	Programming Mode Entry Window	t_{PME}	—	$300000 / f_{OSC}$	—	s	(7)
Synchronization Pulse (Figure 5, Figure 28 and Figure 32)							
110	Reset to first sync pulse (Program Mode Entry)	t_{RS_PM}	58	—	—	ms	(7)
111	Reset to first sync pulse (Normal Mode)	t_{RS}	t_{PSI5_INIT1}	—	—	s	(7)
112	Sync Pulse Period	t_{S-S}	t_{SYNC_OFF}	—	—	μ s	(7)
113	Sync Pulse Width	t_{SYNC}	9	—	—	μ s	(7)
114	Sync Pulse Reference LPF time constant	t_{SYNC_LPF}	120	280	—	μ s	(9)
115	Sync Pulse Reference Discharge Start Time	$t_{SYNC_LPF_RST_ST}$	—	$66 / f_{OSC}$	—	s	(7)
116	Sync Pulse Reference Discharge Activation Time	$t_{SYNC_LPF_RST}$	—	$616 / f_{OSC}$	—	s	(7)
117	Sync Pulse Detection Disable Time (BLANKTIME = 0)	$t_{SYNC_OFF_500}$	—	$1810 / f_{OSC}$	—	s	(7)
118	Analog Delay of Sync Pulse Detection	$t_{A_SYNC_DLY}$	50	—	600	ns	(9)
119	Sync Pulse Pulldown Function Delay Time	t_{PD_DLY}	—	$74 / f_{OSC}$	—	s	(7)
120	Sync Pulse Pulldown Function Activate Time	t_{PD_ON}	—	$64 / f_{OSC}$	—	s	(7)
121	Sync Pulse Detection Jitter	t_{SYNC_JIT}	0	—	$2 / f_{OSC}$	s	(7)
122	Data Transmission Single Bit Time (PSI5 Low Bit Rate)	t_{BIT_LOW}	7.6000	8.0000	8.4000	μ s	(7)
123	Data Transmission Single Bit Time (PSI5 High Bit Rate)	t_{BIT_HI}	4.9875	5.2500	5.5125	μ s	(7)
Modulation Current (20% to 80% of $I_{MOD} - I_{IDLE}$)							
124	Rise Time	t_{RISE}	324	463	602	ns	(3)
125	Fall Time	t_{FALL}	324	463	602	ns	(3)
126	Position of bit transition (PSI5 Low Baud Rate)	$t_{Bittrans_LowBaud}$	49	50	51	%	(7)
127	Position of bit transition (PSI5 High Baud Rate)	$t_{Bittrans_HighBaud}$	47	—	53	%	(7)
128	Asynchronous Response Time	t_{ASYN}	—	$912 / f_{OSC}$	—	s	(7)
Time Slots							
129	Minimum Programmed Time Slot (TIMESLOTx = 0x001)	$t_{TIMESLOTx_MIN}$	—	$2 / f_{OSC}$	—	s	(7, 9)
130	Maximum Programmed Time Slot (TIMESLOTx = 0x3FF)	$t_{TIMESLOTx_MAX}$	—	$2046 / f_{OSC}$	—	s	(3, 7)
131	Default Time Slot (TIMESLOTx = 0x000)	$t_{TIMESLOT_DFLT}$	—	$186 / f_{OSC}$	—	s	(3, 7)
132	Time Plot Resolution	$t_{TIMESLOTx_RES}$	—	$2 / f_{OSC}$	—	s/LSB	(7)
133	Sync Pulse to Daisy Chain Default Time Slot 1	$t_{TIMESLOT_DC1}$	—	$186 / f_{OSC}$	—	s	(7)
134	Sync Pulse to Daisy Chain Default Time Slot 2	$t_{TIMESLOT_DC2}$	—	$768 / f_{OSC}$	—	s	(7)
135	Sync Pulse to Daisy Chain Default Time Slot 3	$t_{TIMESLOT_DC3}$	—	$1400 / f_{OSC}$	—	s	(7)
136	Sync Pulse to Daisy Chain Programming Time Slot	$t_{TIMESLOT_DCP}$	—	$186 / f_{OSC}$	—	s	(7)
137	Data Interpolation Latency (Figure 35, Figure 36)	t_{LAT_INTERP}	$64 / f_{OSC}$	—	$65 / f_{OSC}$	s	(7)
138	Data Setup Time - Synchronous Mode (Figure 36)	$t_{DATASETUP_synch}$	$48 / f_{OSC}$	—	$56 / f_{OSC}$	s	(7)
138	Data Setup Time - Double Sample Rate Mode (Figure 37)	$t_{DATASETUP_double}$	$48 / f_{OSC}$	—	$60 / f_{OSC}$	s	(7)
138	Data Setup Time - 16 Bit Resolution Mode (Figure 39)	$t_{DATASETUP_16}$	$48 / f_{OSC}$	—	$60 / f_{OSC}$	s	(7)
Programming Mode Timing							
139	Programming Mode Sync Pulse Period	$t_{S-S_PM_L}$	495	500	505	μ s	(7)
140	Programming Mode Command Timeout	$t_{PM_TIMEOUT}$	—	$4 * t_{S-S_PM}$	—	μ s	(7)
141	OTP Write Command to $V_{CC} = V_{PP}$	t_{PROG_HOLD}	—	—	20	μ s	(7)
142	OTP Write CMD Response to OTP programming start	t_{PROG_DELAY}	—	—	40	ms	(7)
143	Time to program the OTP User Array	t_{PROG_ARRAY}	70	—	—	ms	(7)

2.7 Dynamic Electrical Characteristics - Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
144	Internal Oscillator Frequency *	f_{OSC}	3.80	4	4.20	MHz	(1)
145	DSP Low-Pass Filter (Note15) Cutoff frequency LPF0 (referenced to 0 Hz) *	f_{C_LPF0}	—	400	—	Hz	(7)
146	Filter Order LPF0 *	O_{LPF0}	—	3	—	1	(7)
147	Cutoff frequency LPF1 (referenced to 0 Hz) *	f_{C_LPF1}	—	400	—	Hz	(7)
148	Filter Order LPF1 *	O_{LPF1}	—	4	—	1	(7)
149	DSP Offset Cancellation Low-Pass Filter (Note15) Offset Cancellation Low-Pass Filter Input Sample Rate	$t_{OC_SampleRate}$	—	256	—	μ s	(7)
150	Stage 1 Cutoff frequency, Startup Phase 1	f_{C_OC10}	—	10.0	—	Hz	(7)
151	Stage 1 Filter Order, Startup Phase 1	O_{OC10}	—	1	—	1	(7)
152	Stage 2 Cutoff frequency, Startup Phase 1	f_{C_OC03}	—	0.300	—	Hz	(7)
153	Stage 2 Filter Order, Startup Phase 1	O_{OC03}	—	1	—	1	(7)
154	Cutoff frequency, Option 0	f_{C_OC0}	—	0.100	—	Hz	(7)
155	Filter Order, Option 0	O_{OC0}	—	1	—	1	(7)
156	Offset Cancellation Output Update Rate (8-Bit Mode)	$t_{OFFRate_8}$	—	$f_{OSC} / 2e6$	—	s	(7)
157	Offset Cancellation Output Step Size (8-Bit Mode)	OFF_{Step_8}	—	0.125	—	LSB	(7)
158	Offset Cancellation Output Update Rate (10-Bit Mode)	$t_{OFFRate_10}$	—	$f_{OSC} / 2e6$	—	s	(7)
159	Offset Cancellation Output Step Size (10-Bit Mode)	OFF_{Step_10}	—	0.5	—	LSB	(7)
160	Offset Monitor Update Frequency	$OFFMON_{OSC}$	—	$f_{OSC} / 2000$	—	Hz	(7)
161	Offset Monitor Count Limit	$OFFMON_{CNTLIMIT}$	—	4096	—	1	(7)
162	Offset Monitor Counter Size	$OFFMON_{CNTSIZE}$	—	8192	—	1	(7)
163	Sensing Element Natural Frequency $\pm 60g$	f_{gcell_Z60}	7000	—	8000	Hz	(9)
164	$\pm 120g$	f_{gcell_Z120}	7000	—	8000	Hz	(9)
165	$\pm 240g$	f_{gcell_Z240}	13600	—	15100	Hz	(9)
166	$\pm 480g$	f_{gcell_Z480}	16289	—	17996	Hz	(9)
167	Sensing Element Roll-off Frequency (-3 db) $\pm 60g$	f_{gcell_Z60}	798	—	2211	Hz	(9)
168	$\pm 120g$	f_{gcell_Z120}	798	—	2211	Hz	(9)
169	$\pm 240g$	f_{gcell_Z240}	2000	—	4700	Hz	(9)
170	$\pm 480g$	f_{gcell_Z480}	2250	—	6350	Hz	(9)
171	Sensing Element Damping Ratio $\pm 60g$	ζ_{gcell_Z60}	1.870	—	4.610	—	(9)
172	$\pm 120g$	ζ_{gcell_Z120}	1.870	—	4.610	—	(9)
173	$\pm 240g$	ζ_{gcell_Z240}	1.750	—	3.500	—	(9)
174	$\pm 480g$	ζ_{gcell_Z480}	1.250	—	3.000	—	(9)
175	Sensing Element Delay (@100 Hz) $\pm 60g$	$f_{gcell_delay_Z60}$	77	—	200	μ s	(9)
176	$\pm 120g$	$f_{gcell_delay_Z120}$	77	—	200	μ s	(9)
177	$\pm 240g$	$f_{gcell_delay_Z240}$	40	—	86	μ s	(9)
178	$\pm 480g$	$f_{gcell_delay_Z480}$	21	—	60	μ s	(9)
179	Package Resonance Frequency	$f_{Package}$	100	—	—	kHz	(9)

2.8 Dynamic Electrical Characteristics - Supply and SPI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
180	Quiescent Current Settling Time (Power Applied to $I_q = I_{IDLE} \pm 2$ mA)	t_{SET}	—	—	5	ms	(3)
181	Reset Recovery Internal Delay (After internal POR)	t_{INT_INIT}	—	$16000 / f_{OSC}$	—	s	(7)
182	V_{CC} Micro-cut ($C_{BUF}=C_{REG}=C_{REGA}=1$ μ F) Survival Time (V_{CC} disconnect without Reset, $C_{BUF}=C_{REG}=C_{REGA}=700$ nF)	$t_{VCC_MICROCUTmin}$	30	—	—	μ s	(3)
183	Survival Time (V_{CC} disconnect without Reset, $C_{BUF}=C_{REG}=C_{REGA}=1$ μ F)	$t_{VCC_MICROCUT}$	50	—	—	μ s	(3)
184	Reset Time (V_{CC} disconnect above which Reset is guaranteed)	t_{VCC_RESET}	—	—	1000	μ s	(3)
185	V_{BUF} , Capacitor Monitor Disconnect Time (Figure 10) POR to first Capacitor Test Disconnect	$t_{POR_CAPTEST}$	—	$12000 / f_{OSC}$	—	s	(7)
186	Disconnect Time (Figure 10)	$t_{CAPTEST_TIME}$	—	1.5	5.0	μ s	(7)
187	Disconnect Delay, Asynchronous Mode (Figure 10)	$t_{CAPTEST_ADLY}$	—	$688 / f_{OSC}$	—	s	(7)
188	Disconnect Delay, Synchronous Mode (Figure 11)	$t_{CAPTEST_SDLY}$	—	$72 / f_{OSC}$	—	s	(7)
189	V_{REG} , V_{REGA} Capacitor Monitor POR to first Capacitor Test Disconnect	$t_{POR_CAPTEST}$	—	$12000 / f_{OSC}$	—	s	(7)
190	Disconnect Time	$t_{CAPTEST_TIME}$	—	$6 / f_{OSC}$	—	s	(7)
191	Disconnect Rate	$t_{CAPTEST_RATE}$	—	$256 / f_{OSC}$	—	s	(7)
192	Serial Interface Timing (See Figure 7, $C_{DOUT} \leq 80$ pF, $R_{DOUT} \geq 10$ k Ω) Clock (SCLK) period (10% of V_{CC} to 10% of V_{CC})	t_{SCLK}	320	—	—	ns	(9)
193	Clock (SCLK) high time (90% of V_{CC} to 90% of V_{CC})	t_{SCLKH}	120	—	—	ns	(9)
194	Clock (SCLK) low time (10% of V_{CC} to 10% of V_{CC})	t_{SCLKL}	120	—	—	ns	(9)
195	Clock (SCLK) rise time (10% of V_{CC} to 90% of V_{CC})	t_{SCLKR}	—	15	40	ns	(9)
196	Clock (SCLK) fall time (90% of V_{CC} to 10% of V_{CC})	t_{SCLKF}	—	15	28	ns	(9)
197	\overline{CS} asserted to SCLK high ($\overline{CS} = 10\%$ of V_{CC} to SCLK = 10% of V_{CC})	t_{LEAD}	60	—	—	ns	(9)
198	\overline{CS} asserted to D_{OUT} valid ($\overline{CS} = 10\%$ of V_{CC} to $D_{OUT} = 10/90\%$ of V_{CC})	t_{ACCESS}	—	—	60	ns	(9)
199	Data setup time ($D_{IN} = 10/90\%$ of V_{CC} to SCLK = 10% of V_{CC})	t_{SETUP}	20	—	—	ns	(9)
200	D_{IN} Data hold time (SCLK = 90% of V_{CC} to $D_{IN} = 10/90\%$ of V_{CC})	t_{HOLD_IN}	10	—	—	ns	(9)
201	D_{OUT} Data hold time (SCLK = 90% of V_{CC} to $D_{OUT} = 10/90\%$ of V_{CC})	t_{HOLD_OUT}	0	—	—	ns	(9)
202	SCLK low to data valid (SCLK = 10% of V_{CC} to $D_{OUT} = 10/90\%$ of V_{CC})	t_{VALID}	—	—	50	ns	(9)
203	SCLK low to \overline{CS} high (SCLK = 10% of V_{CC} to $\overline{CS} = 90\%$ of V_{CC})	t_{LAG}	60	—	—	ns	(9)
204	\overline{CS} high to D_{OUT} disable ($\overline{CS} = 90\%$ of V_{CC} to $D_{OUT} = Hi Z$)	$t_{DISABLE}$	—	—	60	ns	(9)
205	\overline{CS} high to \overline{CS} low ($\overline{CS} = 90\%$ of V_{CC} to $\overline{CS} = 90\%$ of V_{CC})	t_{CSN}	1000	—	—	ns	(9)

- Parameters tested 100% at final test.
- Parameters tested 100% at wafer probe.
- Verified by characterization.
- * Indicates critical characteristic.
- Verified by qualification testing.
- Parameters verified by pass/fail testing in production.
- Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
- N/A.
- Verified by simulation.
- N/A.
- Measured at V_{CC} pin; V_{SYNC} guaranteed across full V_{IDLE} range.
- Self-Test repeats on failure up to a ST_RPT_{MAX} times before transmitting Sensor Error Message.
- N/A.
- Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
- Filter cutoff frequencies are directly dependent upon the internal oscillator frequency.

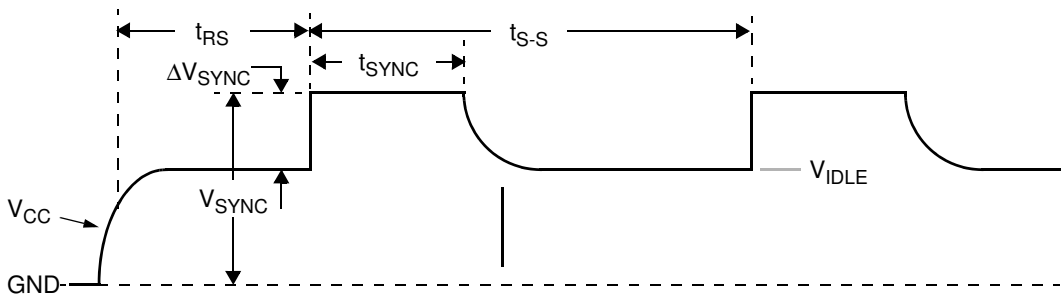


Figure 5. Sync Pulse Characteristics

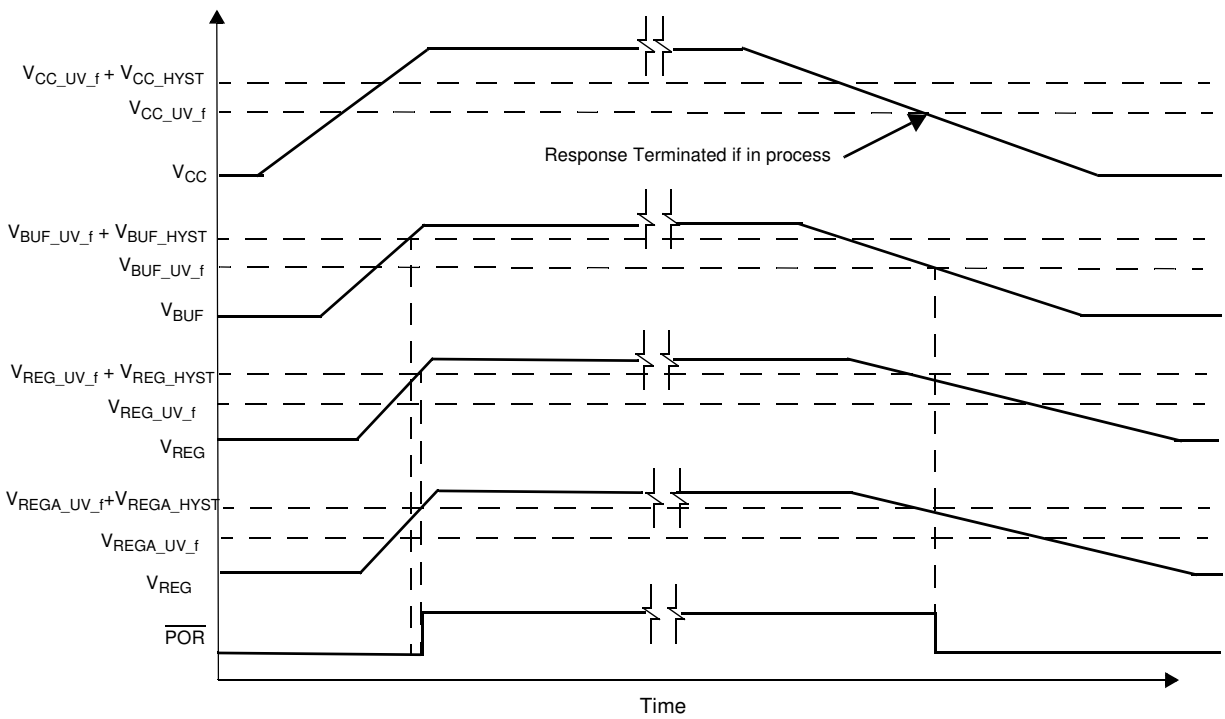


Figure 6. Powerup Timing

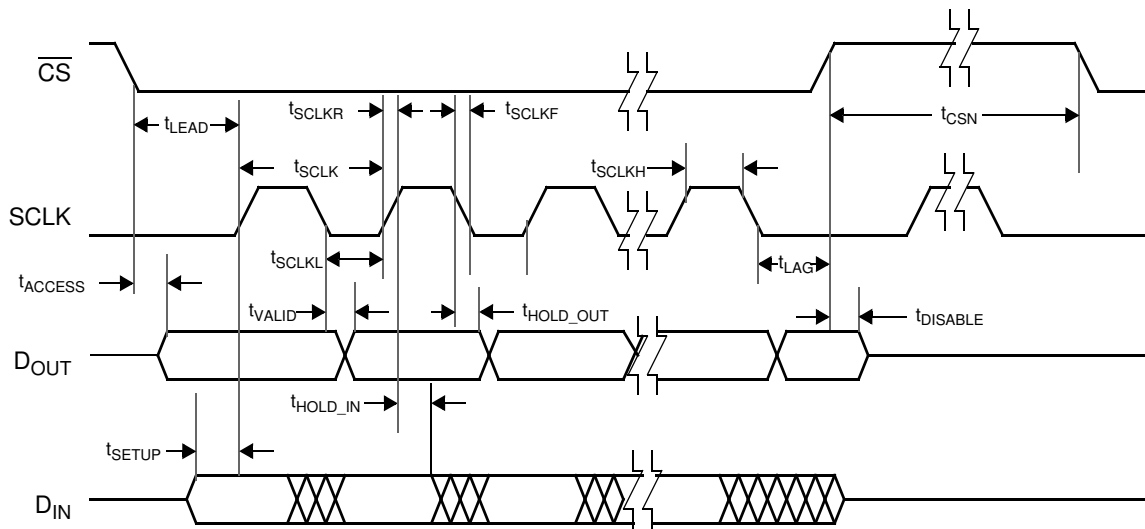


Figure 7. Serial Interface Timing

3 Functional Description

3.1 User Accessible Data Array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user programmable block, and read only registers for device status. The OTP blocks incorporate independent error detection circuitry for fault detection (reference [Section 3.2](#)). Portions of the factory programmable array are reserved for factory-programmed trim values. The user accessible data is shown in [Table 2](#).

Table 2. User Accessible Data

Byte Addr (XLong Msg)	Register	Nibble Addr (Long Msg)	Bit Function				Nibble Addr (Long Msg)	Bit Function				Type	
			7	6	5	4		3	2	1	0		
\$00	SN0	\$01	SN[7]	SN[6]	SN[5]	SN[4]	\$00	SN[3]	SN[2]	SN[1]	SN[0]	F, R	
\$01	SN1	\$03	SN[15]	SN[14]	SN[13]	SN[12]	\$02	SN[11]	SN[10]	SN[9]	SN[8]		
\$02	SN2	\$05	SN[23]	SN[22]	SN[21]	SN[20]	\$04	SN[19]	SN[18]	SN[17]	SN[16]		
\$03	SN3	\$07	SN[31]	SN[30]	SN[29]	SN[28]	\$06	SN[27]	SN[26]	SN[25]	SN[24]		
\$04	DEVCFG1	\$09	0	0	1	0	\$08	1	RNG[2]	RNG[1]	RNG[0]	U, R	
\$05	DEVCFG2	\$0B	LOCK_U	PCM	SYNC_PD	LATENCY	\$0A	DATASIZE	BLANKTIME	P_CRC	BAUD		
\$06	DEVCFG3	\$0D	TRANS_MD[1]	TRANS_MD[0]	LPF[1]	LPF[0]	\$0C	TIMESLOTB[9]	TIMESLOTB[8]	TIMESLOTA[9]	TIMESLOTA[8]		
\$07	DEVCFG4	\$0F	TIMESLOTA[7]	TIMESLOTA[6]	TIMESLOTA[5]	TIMESLOTA[4]	\$0E	TIMESLOTA[3]	TIMESLOTA[2]	TIMESLOTA[1]	TIMESLOTA[0]		
\$08	DEVCFG5	\$11	TIMESLOTB[7]	TIMESLOTB[6]	TIMESLOTB[5]	TIMESLOTB[4]	\$10	TIMESLOTB[3]	TIMESLOTB[2]	TIMESLOTB[1]	TIMESLOTB[0]		
\$09	DEVCFG6	\$13	INIT2_EXT	ASYN	U_DIR[1]	U_DIR[0]	\$12	U_REV[3]	U_REV[2]	U_REV[1]	U_REV[0]		
\$0A	DEVCFG7	\$15	MONTH[3]	MONTH[2]	MONTH[1]	MONTH[0]	\$14	YEAR[3]	YEAR[2]	YEAR[1]	YEAR[0]		
\$0B	DEVCFG8	\$17	UD[2]	UD[1]	UD[0]	DAY[4]	\$16	DAY[3]	DAY[2]	DAY[1]	DAY[0]		
\$0C	SC	\$19	0	TM_B	RESERVED	IDEN_B	\$18	OC_INIT_B	IDEF_B	OFF_B	0		R
\$0D	MFG_ID	\$1B	MFG_ID[7]	MFG_ID[6]	MFG_ID[5]	MFG_ID[4]	\$1A	MFG_ID[3]	MFG_ID[2]	MFG_ID[1]	MFG_ID[0]		U, R

Type codes

- F: Freescale programmed OTP location
- U: User programmable OTP location via PSi5
- R: Readable register via PSi5

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each device during manufacturing. The serial number is composed of the following information:

Bit Range	Content
SN[12:0]	Serial Number
SN[31:13]	Lot Number

Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the factory programmed OTP CRC verification. Reference [Section 3.2.1](#) for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Factory Configuration Register (DEVCFG1)

The factory configuration register is a factory programmed, read only register which contains user specific device configuration information. The factory configuration register is included in the factory programmed OTP CRC verification.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
\$04	DEVCFG1	0	0	1	0	1	RNG[2]	RNG[1]	RNG[0]
Factory Default		0	0	1	0	0	0	0	0

3.1.2.1 Range Indication Bits (RNG[2:0])

The range indication bits are factory programmed and indicate the full-scale range of the device as shown below.

RNG[2]	RNG[1]	RNG[0]	Full-Scale Acceleration Range	g-Cell Design	PSI5 Init Data Transmission (D9) Reference Table 12
0	0	0	Reserved	N/A	0001
0	0	1	±60g	Medium-g	0111
0	1	0	Reserved	N/A	0010
0	1	1	±120g	Medium-g	1000
1	0	0	Reserved	N/A	0011
1	0	1	±240g	High-g	1001
1	1	0	Reserved	N/A	0100
1	1	1	±480g	High-g	1010

3.1.3 Device Configuration 2 Register (DEVCFG2)

Device configuration register 2 is a user programmable OTP register that contains device configuration information.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
\$05	DEVCFG2	LOCK_U	PCM	SYNC_PD	LATENCY	DATASIZE	BLANKTIME	P_CRC	BAUD
Factory Default		0	0	0	0	0	0	0	0

3.1.3.1 User Configuration Lock Bit (LOCK_U)

The LOCK_U bit allows the user to prevent writes to the user configuration array once programming is completed.

If the LOCK_U bit is written to '1' when a PSI5 "Execute Programming of NVM" command is executed, the LOCK_U OTP bit will be programmed. Upon completion of the OTP programming, an OTP readout will be executed, locking the array from future OTP writes. The User Programmable OTP Array Error Detection is also activated (Reference [Section 3.2.2](#)).

3.1.3.2 PCM Enable Bit (PCM)

The PCM bit enables the PCM output pin. When the PCM bit is set, the PCM output pin is active and outputs a Pulse Code Modulated signal proportional to the acceleration response. Reference [Section 3.5.3.7](#) for more information regarding the PCM output. When the PCM bit is cleared, the PCM output pin is actively pulled low.

PCM	PCM Output
0	Actively Pulled Low
1	PCM Signal Enabled

3.1.3.3 Sync Pulse Pulldown Enable Bit (SYNC_PD)

The sync pulse pulldown enable bit selects if the sync pulse pulldown is enabled once a sync pulse is detected. Reference [Section 4.2.1.2](#) for more information regarding the sync pulse pulldown.

SYNC_PD	Sync Pulse Pulldown
0	Disabled
1	Enabled

If Daisy Chain Mode is enabled, the Sync Pulse Pulldown is enabled as listed below:

SYNC_PD	Daisy Chain Address Programmed	“Run Mode” Command Received	Daisy Chain Address = ‘001’	Sync Pulse Pulldown
0	x	x	x	Disabled
1	No	x	x	Enabled
1	Yes	No	x	Disabled
1	Yes	Yes	No	Disabled
1	Yes	Yes	Yes	Enabled

3.1.3.4 Latency Selection Bit (LATENCY)

The latency selection bit selects between one of two data latency methods to accommodate synchronized sampling or simultaneous sampling. Reference [Section 4.5](#) for more information regarding latency and data synchronization.

Latency	Data Latency
0	Simultaneous Sampling Mode (Latency relative to Sync Pulse)
1	Synchronous Sampling Mode (Latency relative to Time Slot)

3.1.3.5 Data Size Selection Bit (DATASIZE)

The data size selection bit selects one of two data lengths for the PSI5 response message as shown below.

DATASIZE	Data Length
0	10 Bits
1	8 Bits

3.1.3.6 PSI5 Sync Pulse Blanking Time Selection Bit (BLANKTIME)

The PSI5 sync pulse blanking time selection bit selects the timing for ignoring sync pulses after successful reception of a sync pulse. Reference [Section 4.2.1.1](#) for details regarding sync pulse detection and blanking.

BLANKTIME	Blanking Time Method
0	Maximum of $t_{\text{SYNC_OFF_500}}$ or Response Transmission Complete
1	Blanking Time determined by end of response transmission for programmed time slot

3.1.3.7 PSI5 Response Message Error Detection Selection Bit (P_CRC)

The PSI5 response message error detection selection bit selects either even parity, or a 3-Bit CRC for error detection of the PSI5 response message. Reference [Section 4.3.3](#) for details regarding response message error detection.

P_CRC	Parity or CRC
0	Parity
1	CRC

Note: The PSI5 specification recommends parity for data lengths of 10 bits or less.

3.1.3.8 Baud Rate Selection Bit (BAUD)

The baud rate selection bit selects one of two PSI5 baud rates as shown below. Reference [Section 2.6](#) for baud rate timing specifications.

BAUD	Baud Rate
0	Low Baud Rate (125 kBaud)
1	High Baud Rate (190.5 kBaud)

3.1.4 Device Configuration Registers (DEVCFG3, DEVCFG4, DEVCFG5)

Device configuration registers 3, 4, and 5 are user programmable OTP registers which contain device configuration information.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
\$06	DEVCFG3	TRANS_MD[1]	TRANS_MD[0]	LPF[1]	LPF[0]	TIMESLOTB[9]	TIMESLOTB[8]	TIMESLOTA[9]	TIMESLOTA[8]
\$07	DEVCFG4	TIMESLOTA[7]	TIMESLOTA[6]	TIMESLOTA[5]	TIMESLOTA[4]	TIMESLOTA[3]	TIMESLOTA[2]	TIMESLOTA[1]	TIMESLOTA[0]
\$08	DEVCFG5	TIMESLOTB[7]	TIMESLOTB[6]	TIMESLOTB[5]	TIMESLOTB[4]	TIMESLOTB[3]	TIMESLOTB[2]	TIMESLOTB[1]	TIMESLOTB[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.4.1 PSI5 Transmission Mode Selection Bits (TRANS_MD[1:0])

The PSI5 transmission mode selection bits select the PSI5 transmission mode as shown below.

TRANS_MD[1]	TRANS_MD[0]	Operating Mode	Reference
0	0	Normal Mode (Asynchronous or Parallel, Synchronous)	Section 4.5.1
0	1	Synchronous Double Sample Rate Mode	Section 4.5.2
1	0	16-bit Resolution Mode (Two 10-bit Responses)	Section 4.5.3
1	1	Daisy Chain Mode	Section 4.5.4

3.1.4.2 Low-Pass Filter Selection Bit (LPF[1:0])

The low-pass filter selection bits select the low-pass filter for the acceleration signal as described below:

LPF[1]	LPF[0]	Low-Pass Filter Selected
0	0	400 Hz, 3-Pole
0	1	400 Hz, 4-Pole
1	0	Reserved
1	1	Reserved

3.1.4.3 TimeSlot Selection Bits (TIMESLOTx[9:0])

The timeslot selection bits select the time slot(s) to be used for data transmission. Reference [Section 4.5](#) for details regarding PSI5 transmission modes and time slots. Accepted time slot values are 0.5 μ s to 511.5 μ s in 0.5 μ s increments. Care must be taken to prevent from programming time slots which violate the PSI5 Version 1.3 specification, or time slots which will cause data contention.

TIMESLOTx[9:0]	ASYNCR Bit	Time Slot	Reference
00 0000 0000	0	Default Time Slot ($t_{TIMESLOT_DFLT}$) from start of Sync Pulse (t_{TRIG})	Section 4.5
	1	Asynchronous Mode	Section 4.5.1.1
Non-Zero	N/A	TimeSlot Definition from start of Sync Pulse (t_{TRIG}) in 0.5 μ s Increments	Section 4.5

Note: TIMESLOTB is only used for Synchronous Double Sample Rate Mode and 16-Bit Resolution Mode.

3.1.5 Device Configuration Registers 6, 7, and 8 (DEVCFG6, DEVCFG7, DEVCFG8)

Device configuration registers 6, 7 and 8 are user programmable OTP registers which contain device configuration and user specific manufacturing information. The user specific manufacturing information bits have no impact on the performance, but are transmitted during the PSI5 initialization phase 2 in 10-bit mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
\$09	DEVCFG6	INIT2_EXT	ASYNC	U_DIR[1]	U_DIR[0]	U_REV[3]	U_REV[2]	U_REV[1]	U_REV[0]
\$0A	DEVCFG7	MONTH[3]	MONTH[2]	MONTH[1]	MONTH[0]	YEAR[3]	YEAR[2]	YEAR[1]	YEAR[0]
\$0B	DEVCFG8	UD[2]	UD[1]	UD[0]	DAY[4]	DAY[3]	DAY[2]	DAY[1]	DAY[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.5.1 Initialization Phase 2 Data Extension Bit (INIT2_EXT)

The initialization phase 2 data extension bit enables or disables data transmission in data fields D27 through D32 of PSI5 Initialization Phase 2 as shown below.

INIT2_EXT	Description
0	D27 through D32 are set to "0000"
1	D27 through D32 are transmitted as defined in Section 4.4.2.1

3.1.5.2 Asynchronous Mode Bit (ASYNC)

The asynchronous mode bit enables asynchronous data transmission as described in [Section 3.1.4.3](#).

3.1.5.3 User Sensing Direction (U_DIR[1:0])

The user sensing direction registers are user programmable OTP registers which contain the module level sensing direction. This data is transmitted to the main ECU during PSI5 initialization phase 2 in 10-bit mode, as described in [Section 4.4.2.1](#).

U_DIR[1]	U_DIR[0]	Module Sensing Direction As Defined in AKLV27	PSI5 Init Data Transmission (D8) Reference Table 12
0	0	Connector Direction (β)	0000
0	1	Bushing Direction (α)	0100
1	0	Perpendicular to α and β (γ)	1000
1	1	Not used	1100

3.1.5.4 User Product Revision (U_REV[3:0])

The user product revision registers are user programmable OTP registers which contain the module production revision. The device supports up to 16 product revisions. This data is transmitted to the main ECU during PSI5 initialization phase 2 in 10-bit mode, as described in [Section 4.4.2.1](#).

3.1.5.5 User Production Date Information (YEAR[3:0], MONTH[3:0], DAY[4:0])

The user production date information registers are user programmable OTP registers which contain the module production date. The table below shows the relationship between the stored values and the production date.

Programmed Value	Decoded Value	Julian Date Value
YEAR[3:0]	Year	JY[6:0]
0000	2009	0001001
•	•	•
•	•	•
•	•	•
1111	2024	0011000
MONTH[3:0]	Month	JM[3:0]
0000	N/A	0000
0001	January	0001
•	•	•
•	•	•
•	•	•
1100	December	1100
•	•	•
•	•	•
•	•	•
1111	N/A	N/A
DAY[4:0]	Day	JD[4:0]
00000	N/A	00000
00001	Day 1	00001
•	•	•
•	•	•
•	•	•
11111	Day 31	11111

The Julian date value is transmitted to the main ECU during PSI5 initialization phase 2 in 10-bit mode, as described in [Section 4.4.2.1](#).

3.1.5.6 User Specific Data (UD[2:0])

The user specific data bits are user programmable OTP bits. These bits have no impact on device operation or performance.

3.1.6 Status Check Register (SC)

The status check register is a read-only register containing device status information.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
\$0C	SC	0	TM_B	RESERVED	IDEN_B	OC_INIT_B	IDEF_B	OFF_B	0

3.1.6.1 Test Mode Flag (TM_B)

The test mode bit is cleared if the device is in test mode.

TM_B	Operating Mode
0	Test Mode is active
1	Test Mode is not active

3.1.6.2 Internal Data Error Flag (IDEN_B)

The internal data error bit is cleared if a register data error detection is detected in the user accessible OTP array. A device reset is required to clear the error.

IDEN_B	Error Condition
0	Error detection mismatch in user programmable OTP array
1	No error detected

3.1.6.3 Offset Cancellation Init Status Flag (OC_INIT_B)

The offset cancellation initialization status bit is set once the offset cancellation initialization process is complete, and the filter has switched to normal mode.

OC_INIT_B	Error Condition
0	Offset Cancellation in initialization
1	Offset Cancellation initialization complete (t_{OC1} and t_{OC2} expired)

3.1.6.4 Internal Factory Data Error Flag (IDEF_B)

The internal factory data error bit is cleared if a register data CRC fault is detected in the factory programmable OTP array. A device reset is required to clear the error.

IDEF_B	Error Condition
0	CRC error in factory programmable OTP array
1	No error detected

3.1.6.5 Offset Error Flag (OFF_B)

The offset error flag is cleared if the acceleration signal reaches the offset limit.

OFF_B	Error Condition
0	Offset error detected
1	No error detected

3.1.7 Manufacturer ID (MFG_ID)

The manufacturer ID register is a user programmable OTP register that contains the PSI5 manufacturer ID. The manufacturer ID register has no impact on the performance, but is transmitted during the PSI5 initialization phase 2 in 10-bit mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
\$0D	MFG_ID	MFG_ID[7]	MFG_ID[6]	MFG_ID[5]	MFG_ID[4]	MFG_ID[3]	MFG_ID[2]	MFG_ID[1]	MFG_ID[0]
Factory Default		0	0	0	0	0	0	0	0

MFG_ID	PSI5 Init Data Transmission (D\$, D5) Reference Table 10
0000 0000	D4 = 0100 D5 = 0110
Other	D4 = MFG_ID[7:4] D5 = MFG_ID[3:0]

3.2 OTP Array CRC Verification

3.2.1 Factory Programmed OTP Array CRC Verification

The Factory programmed OTP array is verified for errors with a 3-bit CRC. The CRC verification is enabled only when the factory programmed array is locked. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'.

Once the CRC verification is enabled, the CRC is continuously calculated on all bits in registers \$00, \$01, \$02, \$03, and \$04 and on the factory programmable device configuration bits with the exception of the factory lock bit. Bits are fed in from right to left (LSB first), and top to bottom (lower addresses first) in the register map. The calculated CRC is then compared against the stored 3 bit CRC. If a CRC error is detected in the OTP array, the IDEF_B bit is cleared in the SC register.

The CRC verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.2.2 User Programmable OTP Array Error Detection

The user programmable OTP array is independently verified for errors. The Error Detection is enabled only when the LOCK_U bit in the user data register array is set.

When a PSI5 Programming Mode "Execute Programming of NVM" command is received and the LOCK_U bit is set, the device calculates the error detection code and writes the code to NVM, enabling the Error Detection.

Once the error detection is enabled, the error detection code is continuously calculated on all bits in registers \$05, \$06, \$07, \$08, \$09, \$0A, \$0B and \$0D with the exception of the LOCK_U bit. The calculated code is then compared against the stored error code. If a mismatch is detected, the IDEN_B bit is cleared in the SC register.

The error detection is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.3 Voltage Regulators

The device derives its internal supply voltage from the V_{CC} and V_{SS} pins. Separate internal voltage regulators are used for the analog (V_{REGA}) and digital circuitry (V_{REG}). The analog and digital regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC and supply dropouts on V_{CC} . External filter capacitors are required, as shown in Figure 1.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the under-voltage detection thresholds. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below the under-voltage detection thresholds. A reference generator provides a reference voltage for the $\Sigma\Delta$ converter.

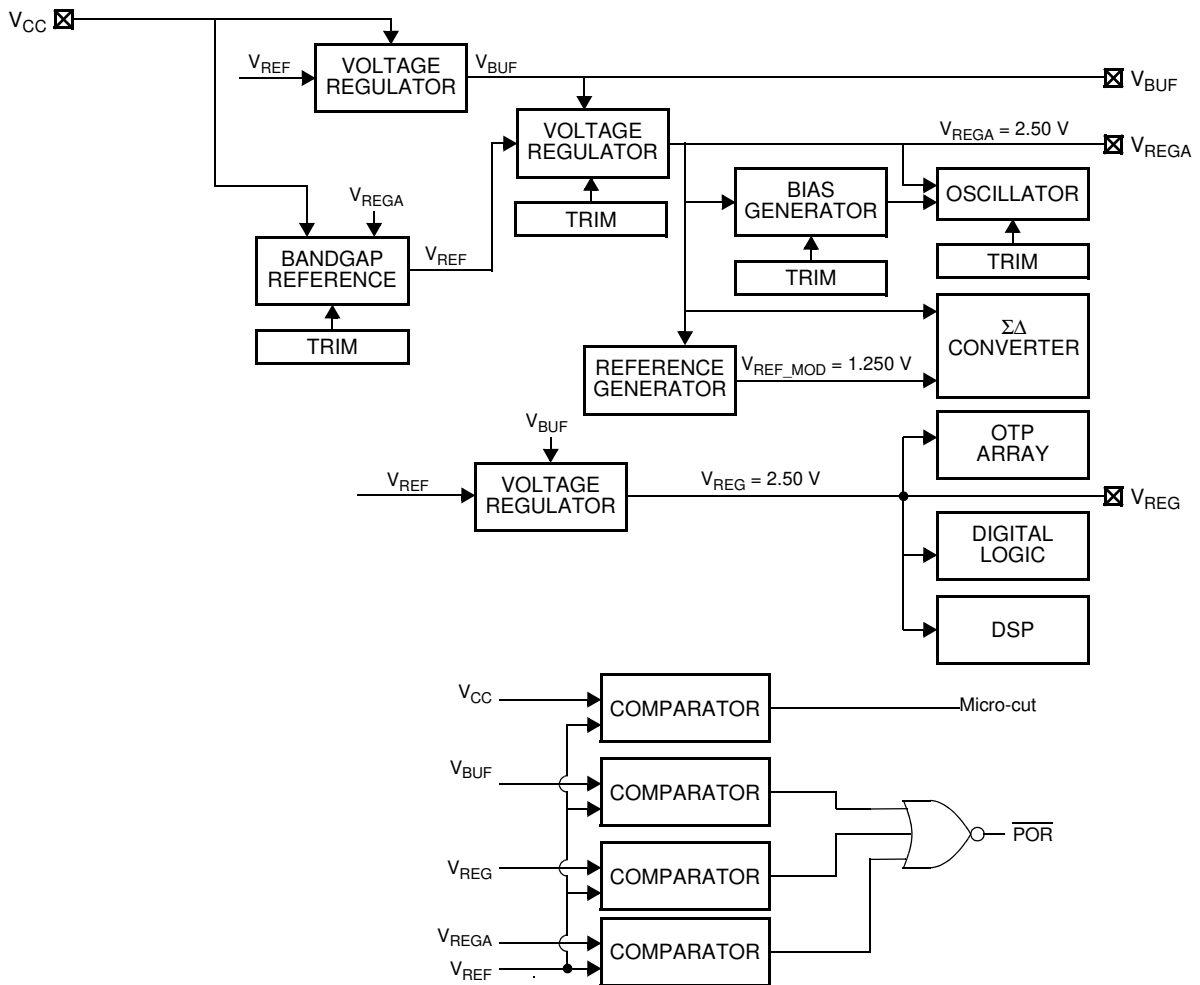


Figure 8. Voltage Regulation and Monitoring

3.3.1 V_{BUF} , V_{REG} and V_{REGA} Regulator Capacitor

The internal regulators require an external capacitor between each of the regulator pins (V_{BUF} , V_{REG} or V_{REGA}) and the associated the V_{SS} / V_{SSA} pin for stability. [Figure 1](#) shows the recommended types and values for each of these capacitors.

3.3.2 V_{CC} , V_{BUF} , V_{REG} and V_{REGA} Under-Voltage Monitor

A circuit is incorporated to monitor the supply voltage (V_{CC}) and all internally regulated voltages (V_{BUF} , V_{REG} and V_{REGA}). If any of internal regulator voltages fall below the specified under-voltage thresholds in [Section 2](#), the device will be reset. If V_{CC} falls below the specified threshold, PSI5 transmissions are terminated for the present response. Once the supply returns above the threshold, the device will respond to the next detected sync pulse. Reference [Figure 9](#).

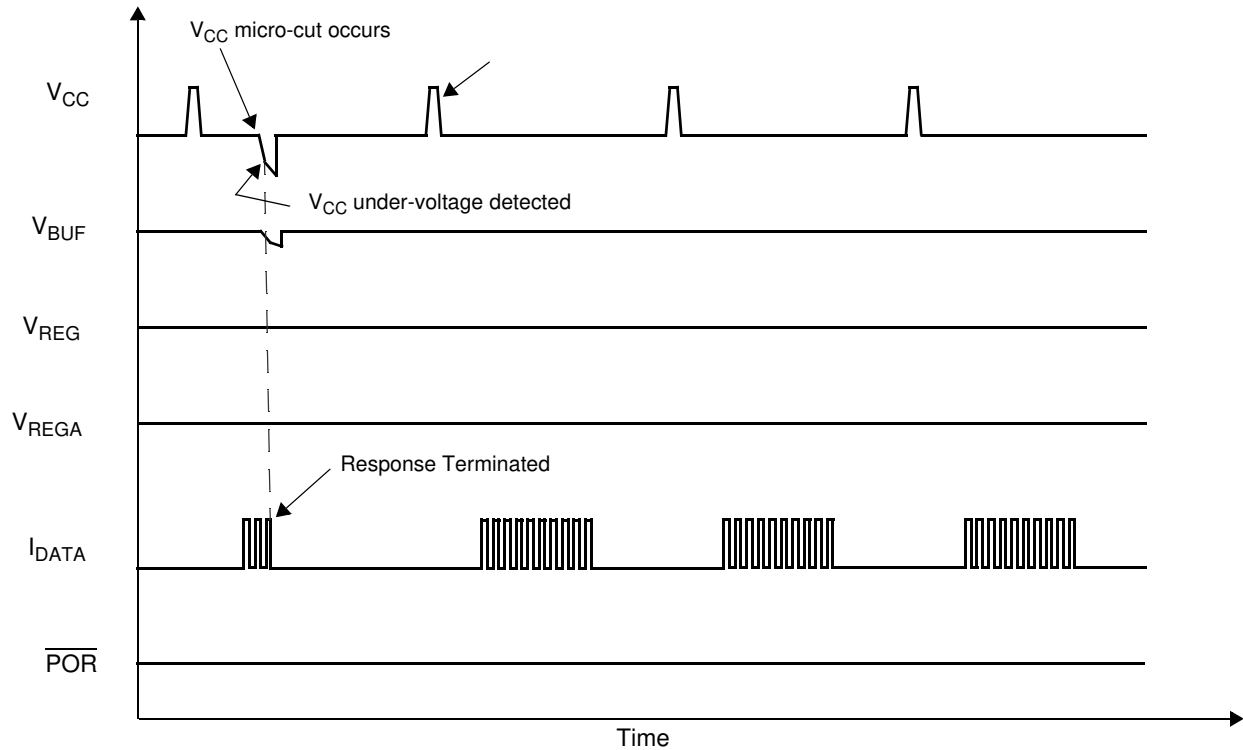


Figure 9. V_{CC} Micro-Cut Response

3.3.3 V_{BUF} , V_{REG} and V_{REGA} Capacitance Monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF} , V_{REG} , or V_{REGA} , capacitor becomes open.

In asynchronous mode, the V_{BUF} regulator is disabled $t_{CAPTEST_ADLY}$ seconds after each data transmission for a duration of $t_{CAPTEST_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

In synchronous mode, the V_{BUF} regulator is disabled $t_{CAPTEST_SDLY}$ seconds after each sync pulse for a duration of $t_{CAPTEST_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

The V_{REG} and V_{REGA} regulators are disabled at a continuous rate ($t_{CAPTEST_RATE}$), for a duration of $t_{CAPTEST_TIME}$ seconds. If either external capacitor is not present, the associated regulator voltage will fall below the internal reset threshold, forcing a device reset.

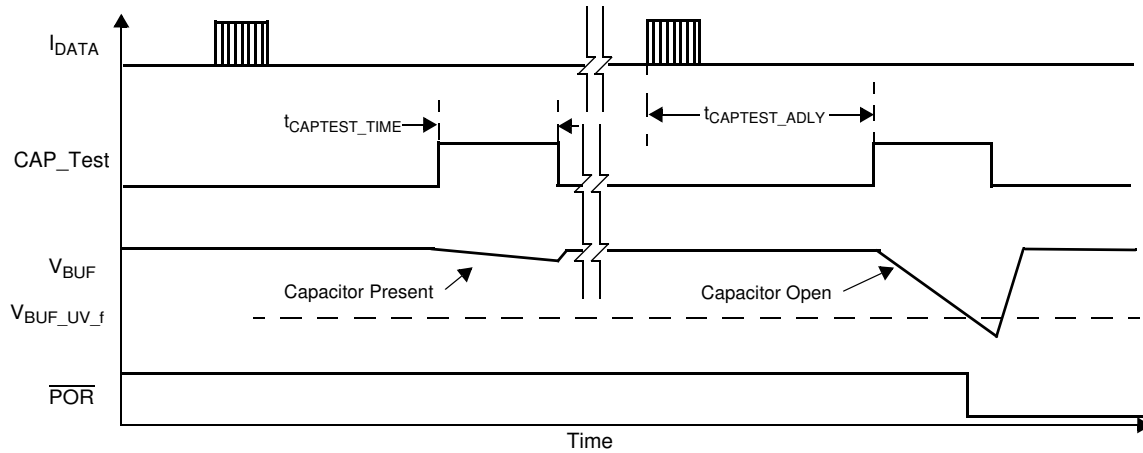


Figure 10. V_{BUF} Capacitor Monitor - Asynchronous Mode

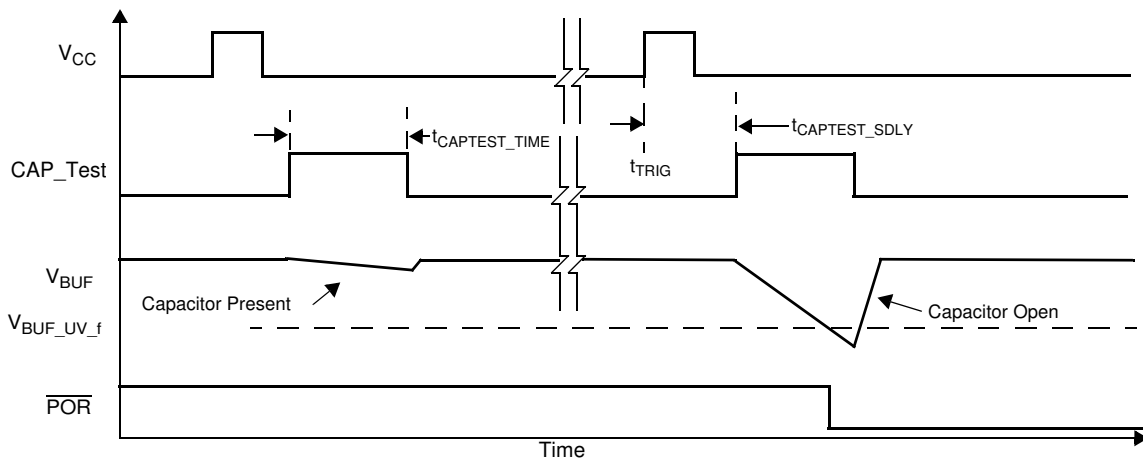


Figure 11. V_{BUF} Capacitor Monitor - Synchronous Mode

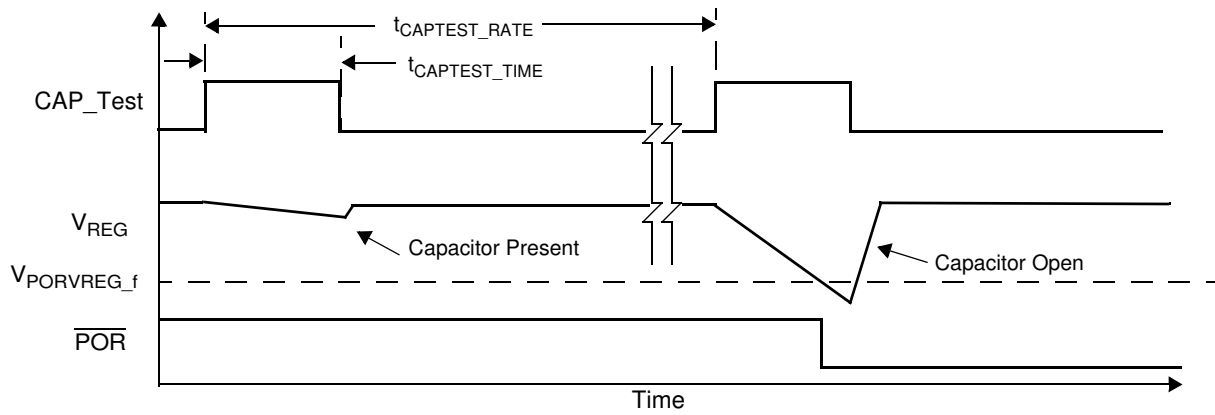


Figure 12. V_{REG} Capacitor Monitor

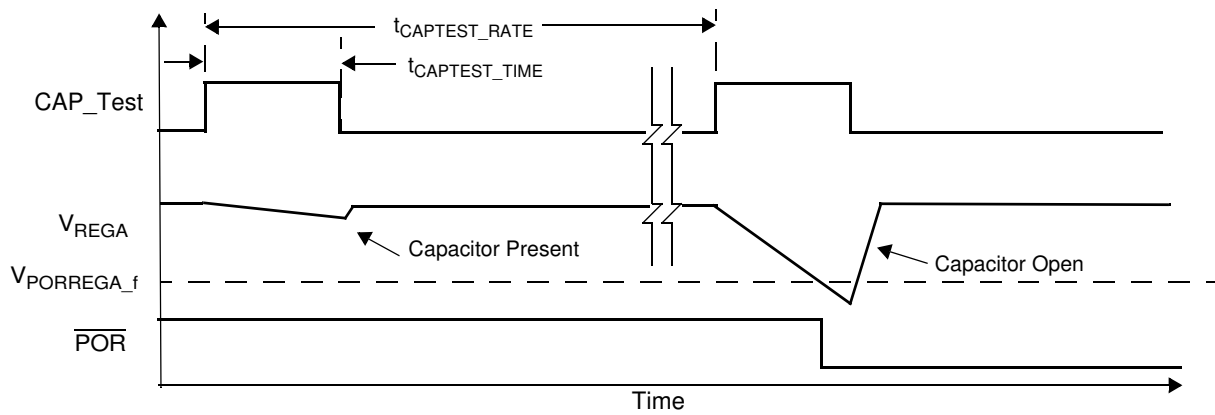


Figure 13. V_{REGA} Capacitor Monitor

3.4 Internal Oscillator

A factory trimmed oscillator is included as specified in [Section 2](#).