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Document Number: MMA52xxAKW
Rev. 0, 09/2012

RoHS

SAFE ASSURE by Freescale

Xtrinsic MMA52xxAKW PSI5 Inertial Sensor

The MMA52xxAKW family, a SafeAssure solution, includes the PSI5 Version 1.3 asynchronous mode compatible overdamped X-axis satellite accelerometers.

MMA52xxAKW

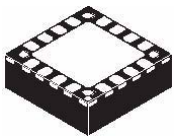
Features

- ±60g to ±480g Full-Scale Range
- 400 Hz, 3-Pole Low-Pass Filter
- Single Pole, High-Pass Filter with Fast Startup and Output Rate Limiting
- PSI5 Version 1.3 Asynchronous Mode Compatible
  - PSI5-A10P-228/1L Compatible
  - Baud Rate: 125 kBaud
  - 10-bit Data
  - Even Parity Error Detection
- 16 µs Internal Sample Rate, with Interpolation to 1 µs
- Pb-Free 16-Pin QFN, 6 by 6 Package
- Qualified AECQ100, Revision G, Grade 1 (-40°C to +125°C) (http://www.aecouncil.com/)

Typical Applications

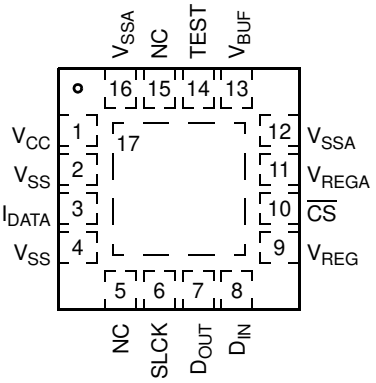
- Airbag Front and Side Crash Detection

Bottom View



16-PIN QFN
CASE 2086-01

Top View



PIN CONNECTIONS

ORDERING INFORMATION				
Device	**Axis**	**Range**	**Package**	**Shipping**
MMA5206AKW	X	60g	2086-01	Tubes
MMA5212AKW	X	120g	2086-01	Tubes
MMA5224AKW	X	240g	2086-01	Tubes
MMA5248AKW	X	480g	2086-01	Tubes
MMA5206AKWR2	X	60g	2086-01	Tape & Reel
MMA5212AKWR2	X	120g	2086-01	Tape & Reel
MMA5224AKWR2	X	240g	2086-01	Tape & Reel
MMA5248AKWR2	X	480g	2086-01	Tape & Reel

freescale Xtrinsic

Application Diagram

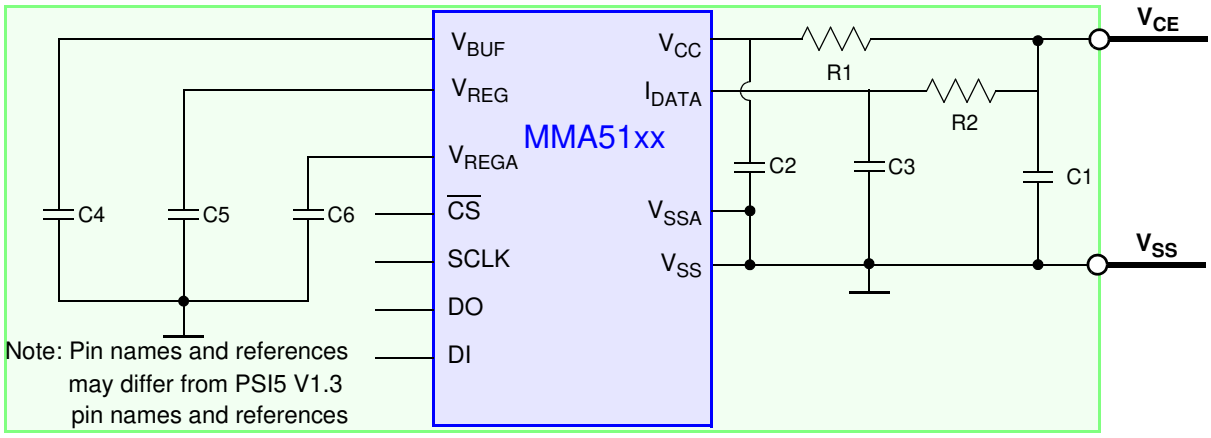


Figure 1. Application Diagram

External Component Recommendations			
Ref Des	**Type**	**Description**	**Purpose**
C1	Ceramic	2.2 nF, 10%, 50V minimum, X7R	V_{CC} Power Supply Decoupling and Signal Damping
C3	Ceramic	470 pF, 10%, 50V minimum, X7R	I_{DATA} Filtering and Signal Damping
C2	Ceramic	15 nF, 10%, 50V minimum, X7R	V_{CC} Power Supply Decoupling
C4, C5, C6	Ceramic	1 µF, 10%, 10V minimum, X7R	Voltage Regulator Output Capacitor(s)
R1	General Purpose	82Ω, 5%, 200 PPM	V_{CC} Filtering and Signal Damping
R2	General Purpose	27Ω, 5%, 200 PPM	I_{DATA} Filtering and Signal Damping

Device Orientation

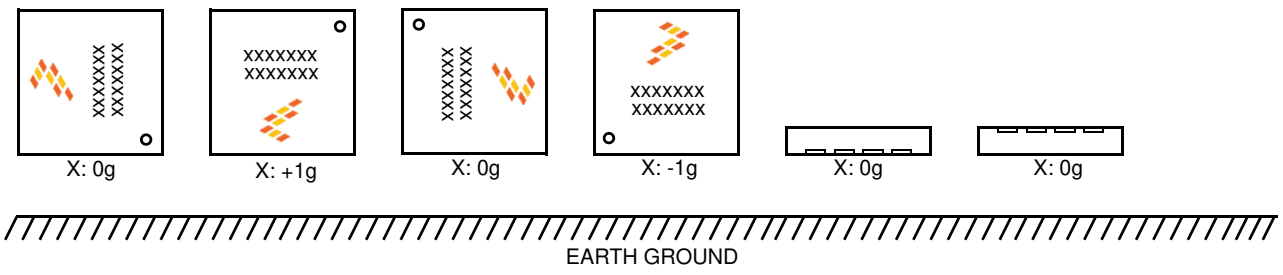


Figure 2. Device Orientation Diagram

Internal Block Diagram

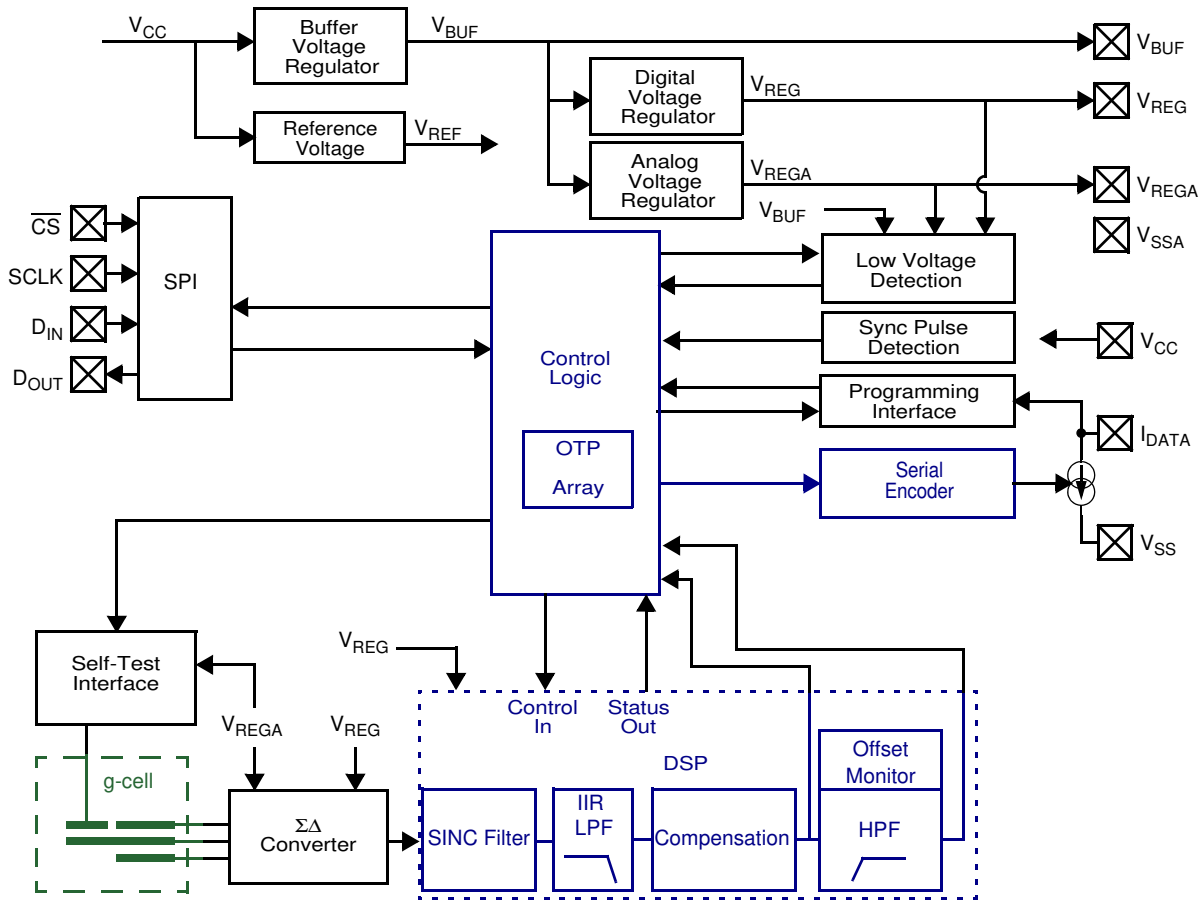


Figure 3. Block Diagram

1 Pin Connections

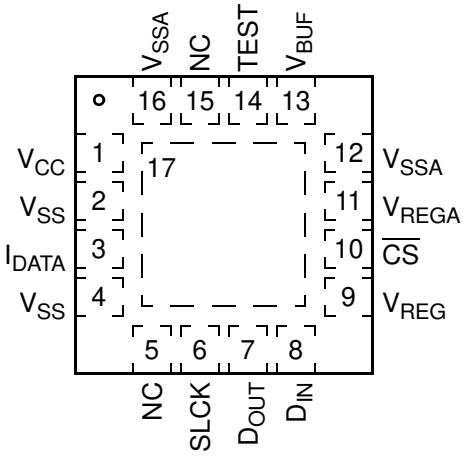


Figure 4. Top View, 16-Pin QFN Package

Table 1. Pin Description

Pin	Pin Name	Formal Name	Definition
1	V_{CC}	Supply	This pin is connected to the PSI5 power and data line through a resistor and supplies power to the device. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
2	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
3	I_{DATA}	Response Current	This pin is connected to the PSI5 power and data line through a resistor and modulates the response current for PSI5 communication. Reference Figure 1.
4	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
5	NC	Not Connected	This pin must be left unconnected in the application.
6	SCLK	SPI Clock	This input pin provides the serial clock to the SPI port for test purposes. An internal pulldown device is connected to this pin. This pin must be grounded or left unconnected in the application.
7	D_{OUT}	SPI Data Out	This pin functions as the serial data output from the SPI port for test purposes. This pin must be left unconnected in the application.
8	D_{IN}	SPI Data In	This pin functions as the serial data input to the SPI port for test purposes. An internal pulldown device is connected to this pin. This pin must be grounded or left unconnected in the application.
9	V_{REG}	Digital Supply	This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
10	CS	Chip Select	This input pin provides the chip select to the SPI port for test purposes. An internal pullup device is connected to this pin.This pin must be left unconnected in the application.
11	V_{REGA}	Analog Supply	This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V_{SSA}. Reference Figure 1.
12	VSSA	Analog GND	This pin is the power supply return node for the analog circuitry.
13	V_{BUF}	Power Supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies both the analog (V_{REGA}) and digital (V_{REG}) supplies to provide immunity from EMC and supply dropouts on V_{CC}. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
14	TEST	Test Pin	This pin is must be grounded or left unconnected in the application.
15	NC	Not Connected	This pin must be left unconnected in the application.
16	VSSA	Analog GND	This pin is the power supply return node for the analog circuitry.
17	PAD	Die Attach Pad	This pin is the die attach flag, and is internally connected to VSS.
	Corner Pads	Corner Pads	The corner pads are internally connected to V_{SS}.

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	
	Supply Voltage (V_{CC}, I_{DATA})				
1	Reverse Current ≤ 160 mA, t ≤ 80 ms	V_{CC_REV}	-0.7	V	(3)
2	Continuous	V_{CC_MAX}	+20.0	V	(3)
3	Transient (< 10 µs)	V_{CC_TRANS}	+25.0	V	(9)
4	V_{BUF}, Test		-0.3 to +4.2	V	(3)
5	V_{REG}, V_{REGA}, SCLK, $\overline{CS}$, D_{IN}, D_{OUT}		-0.3 to +3.0	V	(3)
6	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±2000	g	(3)
7	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2500	g	(3)
8	Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation)	h_{DROP}	1.2	m	(5)
	Electrostatic Discharge (per AECQ100)				
9	External Pins (V_{CC}, I_{DATA}, V_{SS}, V_{SSA}), HBM (100 pF, 1.5 kΩ)	V_{ESD}	±4000	V	(5)
10	HBM (100 pF, 1.5 kΩ)	V_{ESD}	±2000	V	(5)
11	CDM (R = 0Ω)	V_{ESD}	±1500	V	(5)
12	MM (200 pF, 0Ω)	V_{ESD}	±200	V	(5)
	Temperature Range				
13	Storage	T_{stg}	-40 to +125	°C	(3)
14	Junction	T_J	-40 to +150	°C	(9)
15	Thermal Resistance	θ_{JC}	2.5	°C/W	(9, 14)

2.2 Operating Range

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Supply Voltage		V_L		V_H		
16		V_{CC}	4.2	—	17.0	V	(1)
17		V_{CC_UV}	$V_{VCC\_UV\_F}$	—	V_L	V	(9)
	Operating Temperature Range		T_L		T_H		
18		T_A	-40	—	+105	°C	(1)
19		T_A	-40	—	+125	°C	(3)

2.3 Electrical Characteristics - Supply and I/O

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
20	Quiescent Supply Current *	I_{IDLE}	4.0	—	8.0	mA	(1)
21	Modulation Supply Current *	I_{MOD}	I_{IDLE}+ 22.0	I_{IDLE}+ 26.0	I_{IDLE}+ 30.0	mA	(1)
22	Inrush Current (Power On until V_{BUF}, V_{REG}, V_{REGA} Stable)	I_{INRUSH}	—	—	30	mA	(3)
	Internally Regulated Voltages						
23	V_{BUF} *	V_{BUF}	3.60	3.80	4.00	V	(1)
24	V_{REG} *	V_{REG}	2.425	2.50	2.575	V	(1)
25	V_{REGA} *	V_{REGA}	2.425	2.50	2.575	V	(1)
	Low Voltage Detection Threshold						
26	V_{CC} Falling	$V_{VCC\_UV\_F}$	3.40	3.70	4.0	V	(3, 6)
27	V_{BUF} Falling	$V_{BUF\_UV\_F}$	2.95	3.15	3.35	V	(3, 6)
28	V_{REG} Falling	$V_{REG\_UV\_F}$	2.15	2.25	2.35	V	(3, 6)
29	V_{REGA} Falling	$V_{REGA\_UV\_F}$	2.15	2.25	2.35	V	(3, 6)
	Hysteresis						
30	V_{CC}	V_{CC_HYST}	0.10	0.25	0.40	V	(3)
31	V_{BUF}	V_{BUF_HYST}	0.05	0.10	0.15	V	(3)
32	V_{REG}	V_{REG_HYST}	0.05	0.10	0.15	V	(3)
33	V_{REGA}	V_{REGA_HYST}	0.05	0.10	0.15	V	(3)
	External Capacitor (V_{BUF}, V_{REG}, V_{REGA})						
34	Capacitance		500	1000	1500	nF	(9)
35	ESR (including interconnect resistance)	ESR	0	—	200	mΩ	(9)
36	Output High Voltage (DO) I_{Load} = 100 µA	V_{OH}	V_{REG} - 0.1	—	—	V	(9)
37	Output Low Voltage (DO) I_{Load} = 100 µA	V_{OL}	—	—	0.1	V	(9)
38	Input High Voltage $\overline{CS}$, SCLK, DI	V_{IH}	0.7 * V_{REG}	—	—	V	(9)
39	Input Low Voltage $\overline{CS}$, SCLK, DI	V_{IL}	—	—	0.3 * V_{REG}	V	(9)
	Input Current						
40	High (at V_{IH}) (DI)	I_{IH}	-100	—	-10	µA	(9)
41	Low (at V_{IL}) ($\overline{CS}$)	I_{IL}	10	—	100	µA	(9)
42	Pulldown Resistance (SCLK)	R_{PD}	20	æ	100	kΩ	(9)

2.4 Electrical Characteristics - Sensor and Signal Chain

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	Sensitivity (10-bit output @ 100 Hz, referenced to 0 Hz)							
43	±60g Range	*	SENS	—	8	—	LSB/g	(1)
44	±120g Range	*	SENS	—	4	—	LSB/g	(1)
45	±240g Range	*	SENS	—	2	—	LSB/g	(1)
46	±480g Range	*	SENS	—	1	—	LSB/g	(1)
	Total Sensitivity Error (including non-linearity)							
47	T_A = 25°C, ≤ ±240g	*	ΔSENS_240	-5	—	+5	%	(1)
48	$T_L \le T_A \le T_H$, ≤ ±240g	*	ΔSENS_240	-7	—	+7	%	(1)
49	$T_L \le T_A \le T_H$, ≤ ±240g, $V_{VCC\_UV\_F} \le V_{CC} \le V_L$		ΔSENS_240	-7	—	+7	%	(9)
50	T_A = 25°C, > ±240g	*	ΔSENS_480	-5	—	+5	%	(1)
51	$T_L \le T_A \le T_H$, > ±240g	*	ΔSENS_480	-7	—	+7	%	(1)
52	$T_L \le T_A \le T_H$, > ±240g, $V_{VCC\_UV\_F} \le V_{CC} \le V_L$		ΔSENS_480	-7	—	+7	%	(9)
	Digital Offset Before Offset Cancellation							
53	10-bit	*	OFF_{10Bit}	-52	0	+52	LSB	(1)
54	10-bit, $T_L \le T_A \le T_H$, $V_{VCC\_UV\_F} \le V_{CC} \le V_L$		OFF_{10Bit}	-52	0	+52	LSB	(9)
	Digital Offset After Offset Cancellation							
55	10-bit, 0.3 Hz HPF or 0.1 Hz HPF	*	OFF_{10Bit}	-1	0	+1	LSB	(1)
56	10-bit, 0.04 Hz HPF	*	OFF_{10Bit}	-2	0	+2	LSB	(9)
	Continuous Offset Monitor Limit							
57	10-bit output, before compensation		OFF_{MON}	-66	—	+66	LSB	(3)
	Range of Output (10-bit Mode)							
58	Acceleration		RANGE	-480	—	+480	LSB	(3)
	Cross-Axis Sensitivity							
59	Z-axis to X-axis	*	V_{ZX}	-5	—	+5	%	(3)
60	Y-axis to X-axis	*	V_{YX}	-5	—	+5	%	(3)
61	System Output Noise Peak (10-bit Mode, 1 Hz - 1 kHz, All Ranges)	*	n_{Peak}	-4	—	+4	LSB	(3)
62	System Output Noise RMS (10-bit mode, 1 Hz - 1 kHz, All Ranges)	*	n_{RMS}	—	—	+1.0	LSB	(3)
	Non-linearity							
63	10-bit output, ≤ ±240g		NL_{OUT_240g}	-2	—	+2	%	(3)
64	10-bit output, > ±240g		NL_{OUT_480g}	-2	—	+2	%	(3)

2.5 Electrical Characteristics - Self-Test and Overload

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified.

#	Characteristic		Symbol	Min	Typ	Max	Units	
	10-Bit Output During Active Self-Test ($T_L \le T_A \le T_H$)							
65	±60g Range	*	g_{ST10_60X}	120	—	280	LSB	(3)
66	±120g Range	*	g_{ST10_120X}	40	—	160	LSB	(3)
67	±240g Range	*	g_{ST10_240X}	56	—	184	LSB	(3)
68	±480g Range	*	g_{ST10_480X}	8	—	112	LSB	(3)
69	Acceleration (without hitting internal g-cell stops) ±60g Range Positive/Negative		$g_{g\text{-}cell\_Clip60X}$	400	456	500	g	(9)
70	Acceleration (without hitting internal g-cell stops) ±120g Range Positive/Negative		$g_{g\text{-}cell\_Clip120X}$	400	456	500	g	(9)
71	Acceleration (without hitting internal g-cell stops) ±240g Range Positive/Negative		$g_{g\text{-}cell\_Clip240X}$	1750	2065	2300	g	(9)
72	Acceleration (without hitting internal g-cell stops) ±480g Range Positive/Negative		$g_{g\text{-}cell\_Clip480X}$	1750	2065	2300	g	(9)
73	ΣΔ and Sinc Filter Clipping Limit ±60g Range Positive/Negative		$g_{ADC\_Clip60X}$	191	210	233	g	(9)
74	ΣΔ and Sinc Filter Clipping Limit ±120g Range Positive/Negative		$g_{ADC\_Clip120X}$	353	380	410	g	(9)
75	ΣΔ and Sinc Filter Clipping Limit ±240g Range Positive/Negative		$g_{ADC\_Clip240X}$	928	1055	1218	g	(9)
76	ΣΔ and Sinc Filter Clipping Limit ±480g Range Positive/Negative		$g_{ADC\_Clip480X}$	1690	1879	2106	g	(9)

2.6 Dynamic Electrical Characteristics - PSI5

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Initialization Timing						
77	Phase 1	t_{PSI5_INIT1}	—	532000 / f_{OSC}	—	s	(7)
78	Phase 2 (10-Bit, Asynchronous Mode 0, k = 8)	$t_{PSI5\_INIT2\_10a0}$	—	512 * t_{ASYNC}	—	s	(7)
79	Phase 3 (10-Bit, Asynchronous Mode 0, ST_RPT = 0)	$t_{PSI5\_INIT3\_10a0}$	—	19 * t_{ASYNC}	—	s	(7, 12)
80	Offset Cancellation Stage 1 Operating Time	t_{OC1}	—	320000 / f_{OSC}	—	s	(7)
81	Offset Cancellation Stage 2 Operating Time	t_{OC2}	—	280000 / f_{OSC}	—	s	(7)
82	Self-Test Stage 1 Operating Time	t_{ST1}	—	128000 / f_{OSC}	—	s	(7)
83	Self-Test Stage 2 Operating Time	t_{ST2}	—	128000 / f_{OSC}	—	s	(7)
84	Self-Test Stage 3 Operating Time	t_{ST3}	—	128000 / f_{OSC}	—	s	(7)
85	Self-Test Repetitions	ST_RPT	0	—	5		(7, 12)
86	Programming Mode Entry Window	t_{PME}	—	300000 / f_{OSC}	—	s	(7)
87	Data Transmission Single Bit Time (PSI5 Low Bit Rate) *	t_{BIT_LOW}	7.6000	8.0000	8.4000	µs	(7)
88	Modulation Current (20% to 80% of I_{MOD} - I_{IDLE}) Rise Time	t_{RISE}	324	463	602	ns	(3)
89	Position of bit transition (PSI5 Low Baud Rate) *	$t_{Bittrans\_LowBaud}$	49	50	51	%	(7)
90	Asynchronous Response Time *	t_{ASYNC}	—	912 / f_{OSC}	—	s	(7)

2.7 Dynamic Electrical Characteristics - Signal Chain

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
91	Internal Oscillator Frequency *	f_{OSC}	3.80	4	4.20	MHz	(1)
	DSP Low-Pass Filter (Note15)						
92	Cutoff frequency LPF0 (referenced to 0 Hz) *	f_{C_LPF0}	—	400	—	Hz	(7)
93	Filter Order LPF0 *	O_{LPF0}	—	3	—	1	(7)
	DSP Offset Cancellation Low-Pass Filter (Note 15)						
94	Offset Cancellation Low-Pass Filter Input Sample Rate	$t_{OC\_SampleRate}$	—	256	—	µs	(7)
95	Stage 1 Cutoff frequency, Startup Phase 1	f_{C_OC10}	—	10.0	—	Hz	(7)
96	Stage 1 Filter Order, Startup Phase 1	O_{OC10}	—	1	—	1	(7)
97	Stage 2 Cutoff frequency, Startup Phase 1	f_{C_OC03}	—	0.300	—	Hz	(7)
98	Stage 2 Filter Order, Startup Phase 1	O_{OC03}	—	1	—	1	(7)
99	Cutoff frequency, Option 0	f_{C_OC0}	—	0.100	—	Hz	(7)
100	Filter Order, Option 0	O_{OC0}	—	1	—	1	(7)
101	Offset Cancellation Output Update Rate (10-Bit Mode)	$t_{OffRate\_10}$	—	f_{OSC} / 2e6	—	s	(7)
102	Offset Cancellation Output Step Size (10-Bit Mode)	OFF_{Step_10}	—	0.5	—	LSB	(7)
103	Offset Monitor Update Frequency	$OFFMON_{OSC}$	—	f_{OSC}/2000	—	Hz	(7)
104	Offset Monitor Count Limit	$OFFMON_{CNTLIMIT}$	—	4096	—	1	(7)
105	Offset Monitor Counter Size	$OFFMON_{CNTSIZE}$	—	8192	—	1	(7)
	Sensing Element Natural Frequency						
106	±60g	f_{gcell_X60}	12651	—	13871	Hz	(9)
107	±120g	f_{gcell_X120}	12651	—	13871	Hz	(9)
108	±240g	f_{gcell_X240}	26000	—	28700	Hz	(9)
109	±480g	f_{gcell_X480}	26000	—	28700	Hz	(9)
	Sensing Element Rolloff Frequency (-3 db)						
110	±60g	f_{gcell_X60}	938	—	2592	Hz	(9)
111	±120g	f_{gcell_X120}	938	—	2592	Hz	(9)
112	±240g	f_{gcell_X240}	3952	—	14370	Hz	(9)
113	±480g	f_{gcell_X480}	3952	—	14370	Hz	(9)
	Sensing Element Damping Ratio						
114	±60g	ζ_{gcell_X60}	2.760	—	6.770	—	(9)
115	±120g	ζ_{gcell_X120}	2.760	—	6.770	—	(9)
116	±240g	ζ_{gcell_X240}	1.260	—	3.602	—	(9)
117	±480g	ζ_{gcell_X480}	1.260	—	3.602	—	(9)
	Sensing Element Delay (@100 Hz)						
118	±60g	$f_{gcell\_delay\_X60}$	63	—	170	µs	(9)
119	±120g	$f_{gcell\_delay\_X120}$	63	—	170	µs	(9)
120	±240g	$f_{gcell\_delay\_X240}$	13	—	40	µs	(9)
121	±480g	$f_{gcell\_delay\_X480}$	13	—	40	µs	(9)
122	Package Resonance Frequency	$f_{Package}$	100	—	—	kHz	(9)

2.8 Dynamic Electrical Characteristics - Supply and SPI

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
123	Quiescent Current Settling Time (Power Applied to Iq = I_{IDLE} ± 2mA)	t_{SET}	—	—	5	ms	(3)
124	Reset Recovery Internal Delay (After internal POR)	t_{INT_INIT}	—	16000 / f_{OSC}	—	s	(7)
	V_{CC} Micro-cut (C_{BUF}=C_{REG}=C_{REGA}=1 µF)						
125	Survival Time (V_{CC} disconnect without Reset, C_{BUF}=C_{REG}=C_{REGA}=700 nF)	$t_{VCC\_MICROCUTmin}$	30	—	—	µs	(3)
126	Survival Time (V_{CC} disconnect without Reset, C_{BUF}=C_{REG}=C_{REGA}=1 µF)	$t_{VCC\_MICROCUT}$	50	—	—	µs	(3)
127	Reset Time (V_{CC} disconnect above which Reset is guaranteed)	t_{VCC_RESET}	—	—	1000	µs	(3)
	V_{BUF}, Capacitor Monitor Disconnect Time (Figure 9)						
128	POR to first Capacitor Test Disconnect	$t_{POR\_CAPTEST}$	—	12000 / f_{OSC}	—	s	(7)
129	Disconnect Delay, Asynchronous Mode (Figure 9)	$t_{CAPTEST\_ADLY}$	—	688 / f_{OSC}	—	s	(7)
	V_{REG}, V_{REGA} Capacitor Monitor						
130	POR to first Capacitor Test Disconnect	$t_{POR\_CAPTEST}$	—	12000 / f_{OSC}	—	s	(7)
131	Disconnect Rate	$t_{CAPTEST\_RATE}$	—	256 / f_{OSC}	—	s	(7)
	Serial Interface Timing (See Figure 6, $C_{DOUT} \le 80$ pF, $R_{DOUT} \ge 10$ kΩ)						
132	Clock (SCLK) period (10% of V_{CC} to 10% of V_{CC})	t_{SCLK}	320	—	—	ns	(9)
133	Clock (SCLK) high time (90% of V_{CC} to 90% of V_{CC})	t_{SCLKH}	120	—	—	ns	(9)
134	Clock (SCLK) low time (10% of V_{CC} to 10% of V_{CC})	t_{SCLKL}	120	—	—	ns	(9)
135	Clock (SCLK) rise time (10% of V_{CC} to 90% of V_{CC})	t_{SCLKR}	—	15	40	ns	(9)
136	Clock (SCLK) fall time (90% of V_{CC} to 10% of V_{CC})	t_{SCLKF}	—	15	28	ns	(9)
137	$\overline{CS}$ asserted to SCLK high ($\overline{CS}$ = 10% of V_{CC} to SCLK = 10% of V_{CC})	t_{LEAD}	60	—	—	ns	(9)
138	$\overline{CS}$ asserted to D_{OUT} valid ($\overline{CS}$ = 10% of V_{CC} to D_{OUT} = 10/90% of V_{CC})	t_{ACCESS}	—	—	60	ns	(9)
139	Data setup time (D_{IN} = 10/90% of V_{CC} to SCLK = 10% of V_{CC})	t_{SETUP}	20	—	—	ns	(9)
140	D_{IN} Data hold time (SCLK = 90% of V_{CC} to D_{IN} = 10/90% of V_{CC})	t_{HOLD_IN}	10	—	—	ns	(9)
141	D_{OUT} Data hold time (SCLK = 90% of V_{CC} to D_{OUT} = 10/90% of V_{CC})	t_{HOLD_OUT}	0	—	—	ns	(9)
142	SCLK low to data valid (SCLK = 10% of V_{CC} to D_{OUT} = 10/90% of V_{CC})	t_{VALID}	—	—	50	ns	(9)
143	SCLK low to $\overline{CS}$ high (SCLK = 10% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	t_{LAG}	60	—	—	ns	(9)
144	$\overline{CS}$ high to D_{OUT} disable ($\overline{CS}$ = 90% of V_{CC} to D_{OUT} = Hi Z)	$t_{DISABLE}$	—	—	60	ns	(9)
145	$\overline{CS}$ high to $\overline{CS}$ low ($\overline{CS}$ = 90% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	t_{CSN}	1000	—	—	ns	(9)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at wafer probe.
3. Verified by characterization
4. * Indicates critical characteristic.
5. Verified by qualification testing.
6. Parameters verified by pass/fail testing in production.
7. Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
8. N/A.
9. Verified by simulation.
10. N/A.
11. Measured at V_{CC} pin; V_{SYNC} guaranteed across full V_{IDLE} range.
12. Self-Test repeats on failure up to a ST_RPT_{MAX} times before transmitting Sensor Error Message.
13. N/A.
14. Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
15. Filter cutoff frequencies are directly dependent upon the internal oscillator frequency.

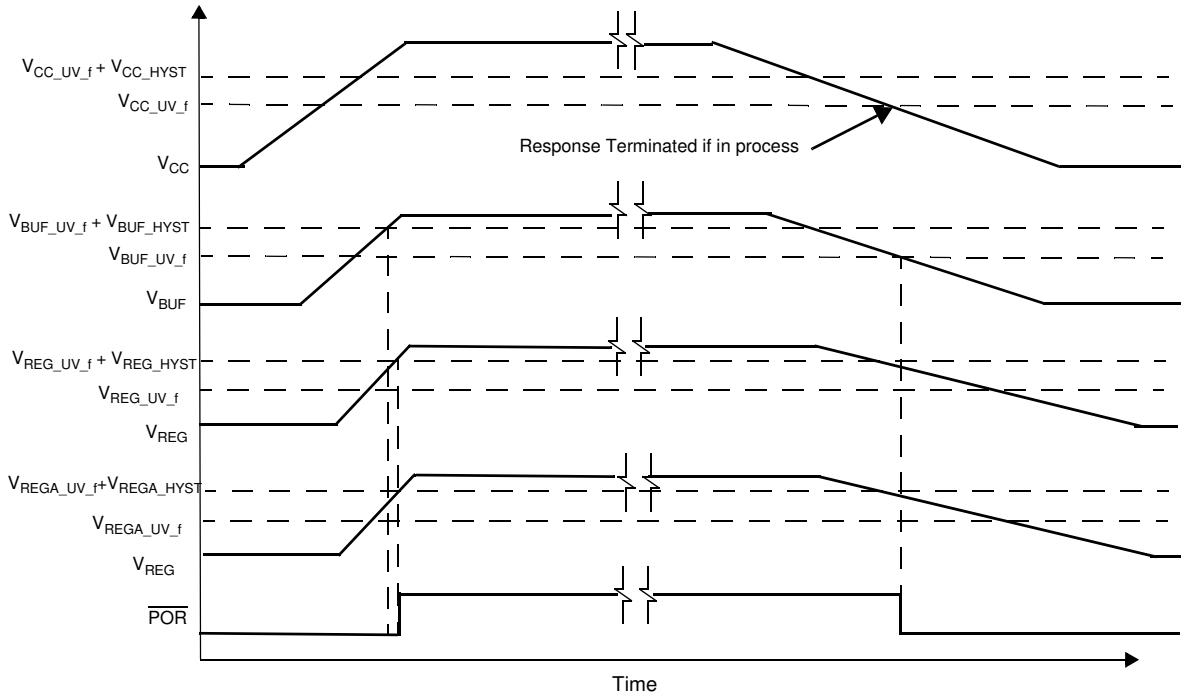


Figure 5. Powerup Timing

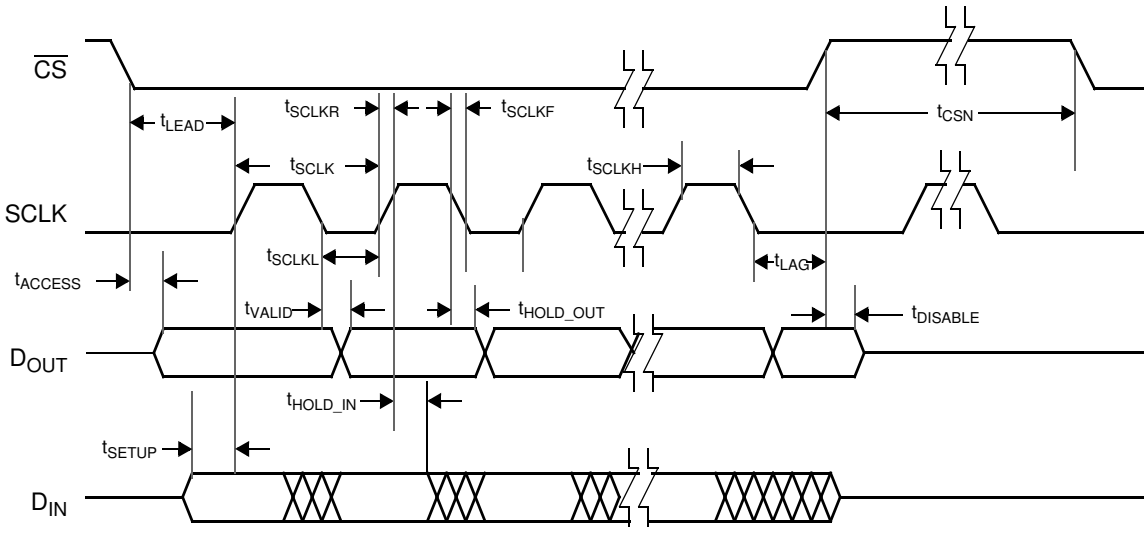


Figure 6. Serial Interface Timing

3 Functional Description

3.1 User Accessible Data Array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user programmable block, and read-only registers for device status. The OTP blocks incorporate independent error detection circuitry for fault detection (reference Section 3.2). Portions of the factory programmable array are reserved for factory-programmed trim values. The user accessible data is shown in Table 2.

Table 2. User Accessible Data

Byte Addr (XLong Msg)	Register	Nibble Addr (Long Msg)	Bit Function				Nibble Addr (Long Msg)	Bit Function				Type
			7	6	5	4		3	2	1	0	
$00	SN0	$01	SN[7]	SN[6]	SN[5]	SN[4]	$00	SN[3]	SN[2]	SN[1]	SN[0]	R
$01	SN1	$03	SN[15]	SN[14]	SN[13]	SN[12]	$02	SN[11]	SN[10]	SN[9]	SN[8]	
$02	SN2	$05	SN[23]	SN[22]	SN[21]	SN[20]	$04	SN[19]	SN[18]	SN[17]	SN[16]	
$03	SN3	$07	SN[31]	SN[30]	SN[29]	SN[28]	$06	SN[27]	SN[26]	SN[25]	SN[24]	
$04	DEVCFG1	$09	0	0	1	0	$08	0	RNG[2]	RNG[1]	RNG[0]	
$05	DEVCFG2	$0B	0	0	0	0	$0A	0	0	0	0	
$06	DEVCFG3	$0D	0	0	0	0	$0C	0	0	0	0	
$07	DEVCFG4	$0F	0	0	0	0	$0E	0	0	0	0	
$08	DEVCFG5	$11	0	0	0	0	$10	0	0	0	0	
$09	DEVCFG6	$13	0	1	0	0	$12	0	0	0	0	
$0A	DEVCFG7	$15	0	0	0	0	$14	0	0	0	0	
$0B	DEVCFG8	$17	1	0	1	0	$16	0	0	0	0	
$0C	SC	$19	0	TM_B	RESERVED	IDEN_B	$18	OC_INIT_B	IDEF_B	OFF_B	0	
$0D	MFG_ID	$1B	0	0	0	0	$1A	0	0	0	0	

Type codes

R: Readable register via PSI5

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each device during manufacturing. The serial number is composed of the following information:

Bit Range	Content
SN[12:0]	Serial Number
SN[31:13]	Lot Number

Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the factory programmed OTP CRC verification. Reference Section 3.2 for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Factory Configuration Register (DEVCFG1)

The factory configuration register is a factory programmed, read-only register which contains user specific device configuration information. The factory configuration register is included in the factory programmed OTP CRC verification.

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$04	DEVCFG1	0	0	1	0	0	RNG[2]	RNG[1]	RNG[0]
Factory Default		0	0	1	0	0	0	0	0

3.1.2.1 Range Indication Bits (RNG[2:0])

The range indication bits are factory programmed and indicate the full-scale range of the device as shown below.

RNG[2]	RNG[1]	RNG[0]	Full-Scale Acceleration Range	g-Cell Design	PSI5 Init Data Transmission (D9) Reference Table 9
0	0	0	Reserved	N/A	0001
0	0	1	±60g	Medium-g	0111
0	1	0	Reserved	N/A	0010
0	1	1	±120 g	Medium-g	1000
1	0	0	Reserved	N/A	0011
1	0	1	±240 g	High-g	1001
1	1	0	Reserved	N/A	0100
1	1	1	±480 g	High-g	1010

3.1.3 Status Check Register (SC)

The status check register is a read-only register containing device status information.

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	SC	0	TM_B	RESERVED	IDEN_B	OC_INIT_B	IDEF_B	OFF_B	0

3.1.3.1 Test Mode Flag (TM_B)

The test mode bit is cleared if the device is in test mode.

TM_B	Operating Mode
0	Test Mode is active
1	Test Mode is not active

3.1.3.2 Internal Data Error Flag (IDEN_B)

The internal data error bit is cleared if a register data error detection mismatch is detected in the user accessible OTP array. A device reset is required to clear the error.

IDEN_B	Error Condition
0	Error detection mismatch in user programmable OTP array
1	No error detected

3.1.3.3 Offset Cancellation Init Status Flag (OC_INIT_B)

The offset cancellation initialization status bit is set once the offset cancellation initialization process is complete, and the filter has switched to normal mode.

OC_INIT_B	Error Condition
0	Offset Cancellation in initialization
1	Offset Cancellation initialization complete (t_{OC1} and t_{OC2} expired)

3.1.3.4 Internal Factory Data Error Flag (IDEF_B)

The internal factory data error bit is cleared if a register data CRC fault is detected in the factory programmable OTP array. A device reset is required to clear the error.

IDEF_B	Error Condition
0	CRC error in factory programmable OTP array
1	No error detected

3.1.3.5 Offset Error Flag (OFF_B)

The offset error flag is cleared if the acceleration signal reaches the offset limit.

OFF_B	Error Condition
0	Offset error detected
1	No error detected

3.2 OTP Array Error Detection

The Factory programmed OTP array is verified for errors with a 3-bit CRC. The CRC verification is enabled only when the factory programmed array is locked. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'.

The CRC is continuously calculated on the factory programmable array with the exception of the factory lock bits. Bits are fed in from right to left (LSB first), and top to bottom (lower addresses first) in the register map. The calculated CRC is then compared against the stored 3 bit CRC. If a CRC error is detected in the OTP array, the IDEF_B bit is cleared in the SC register.

The CRC verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.3 Voltage Regulators

The device derives its internal supply voltage from the V_{CC} and V_{SS} pins. Separate internal voltage regulators are used for the analog (V_{REGA}) and digital circuitry (V_{REG}). The analog and digital regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC and supply dropouts on V_{CC}. External filter capacitors are required, as shown in Figure 1.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the undervoltage detection thresholds. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below the undervoltage detection thresholds. A reference generator provides a reference voltage for the ΣΔ converter.

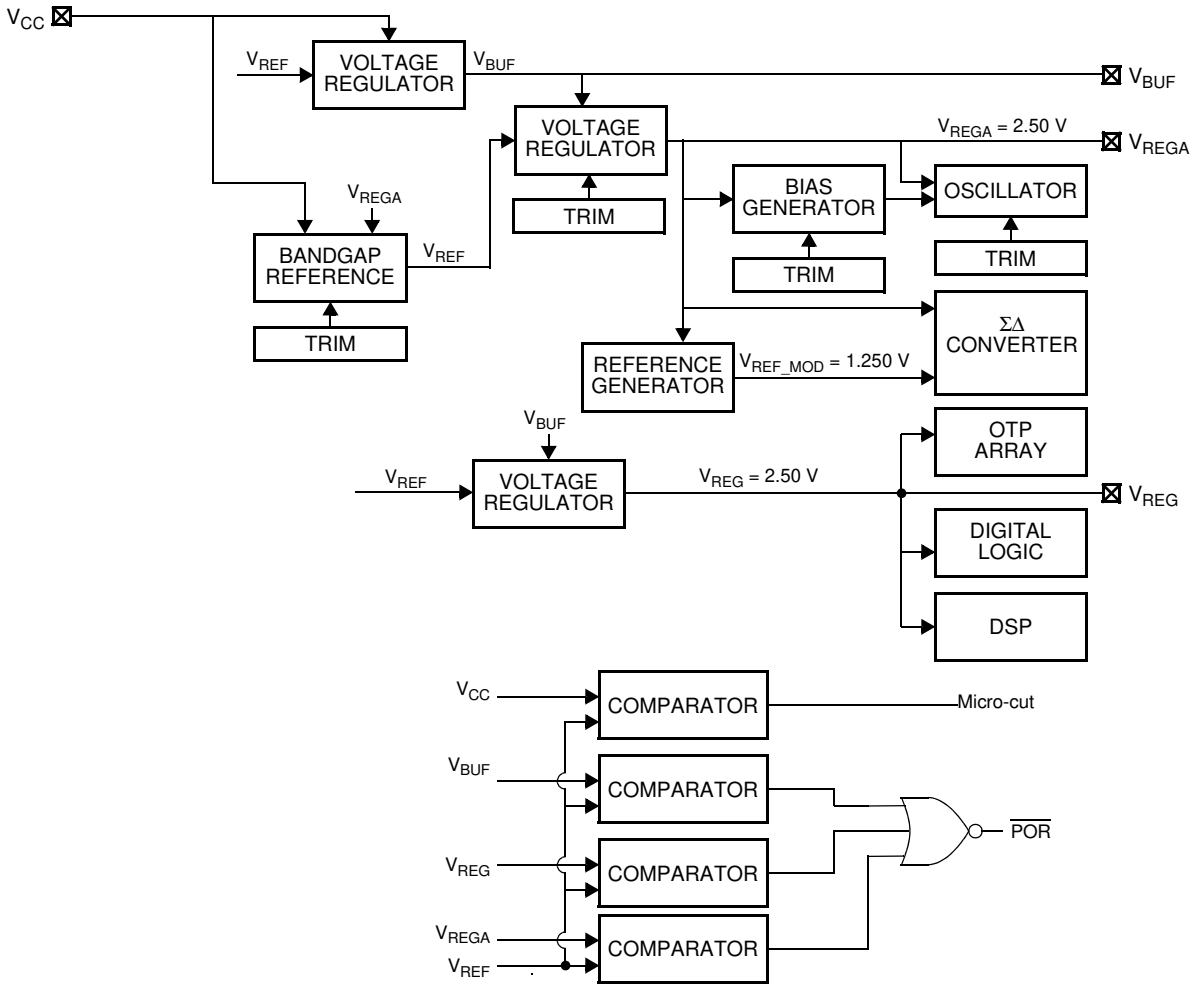


Figure 7. Voltage Regulation and Monitoring

3.3.1 V_{BUF}, V_{REG}, and V_{REGA} Regulator Capacitor

The internal regulators require an external capacitor between each of the regulator pins (V_{BUF}, V_{REG}, or V_{REGA}) and the associated the V_{SS} / V_{SSA} pin for stability. Figure 1 shows the recommended types and values for each of these capacitors.

3.3.2 V_{CC}, V_{BUF}, V_{REG}, and V_{REGA} Undervoltage Monitor

A circuit is incorporated to monitor the supply voltage (V_{CC}) and all internally regulated voltages (V_{BUF}, V_{REG}, and V_{REGA}). If any of internal regulator voltages fall below the specified undervoltage thresholds in Section 2, the device will be reset. If V_{CC} falls below the specified threshold, PSI5 transmissions are terminated for the present response. Once the supply returns above the threshold, the device will respond to the next detected sync pulse. Reference Figure 8.

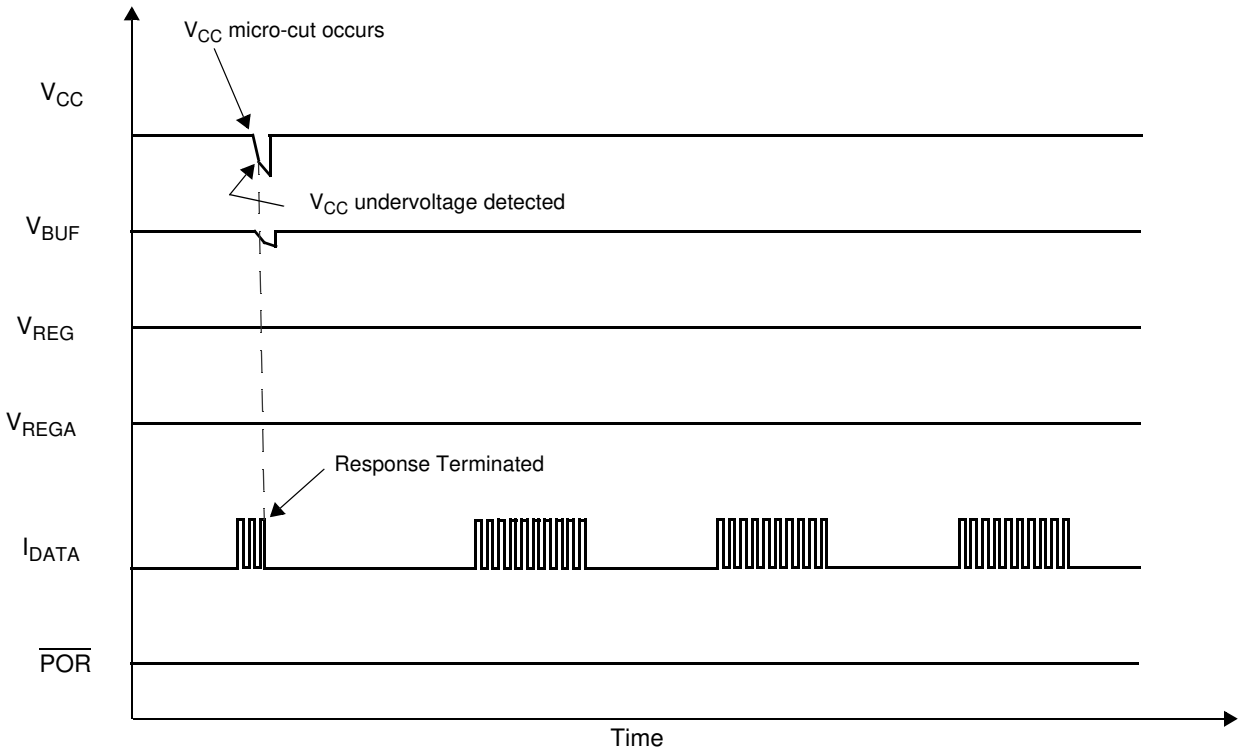


Figure 8. V_{CC} Micro-Cut Response

3.3.3 V_{BUF}, V_{REG}, and V_{REGA} Capacitance Monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF}, V_{REG}, or V_{REGA}, capacitor becomes open.

The V_{BUF} regulator is disabled $t_{CAPTEST\_ADLY}$ seconds after each data transmission for a duration of $t_{CAPTEST\_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

The V_{REG} and V_{REGA} regulators are disabled at a continuous rate ($t_{CAPTEST\_RATE}$), for a duration of $t_{CAPTEST\_TIME}$ seconds. If either external capacitor is not present, the associated regulator voltage will fall below the internal reset threshold, forcing a device reset.

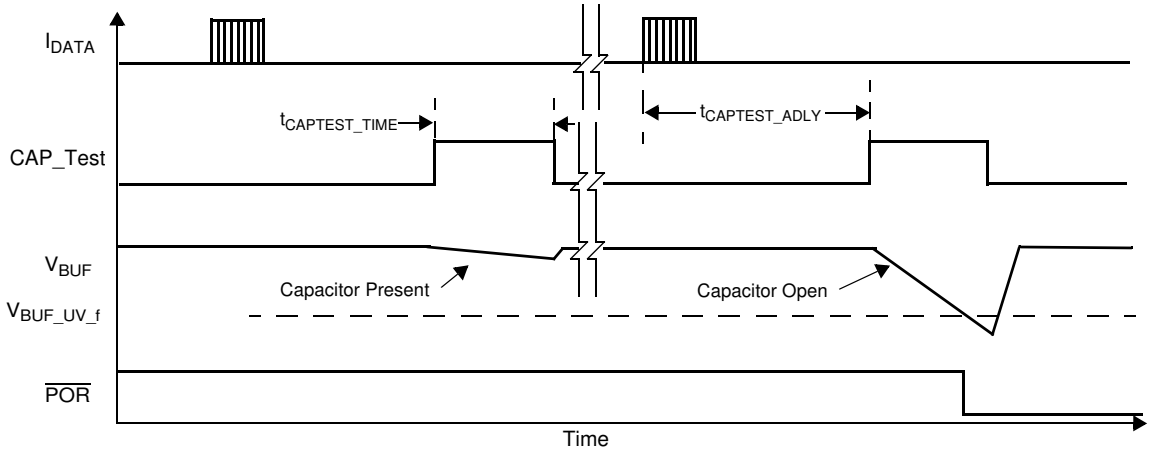


Figure 9. V_{BUF} Capacitor Monitor - Asynchronous Mode

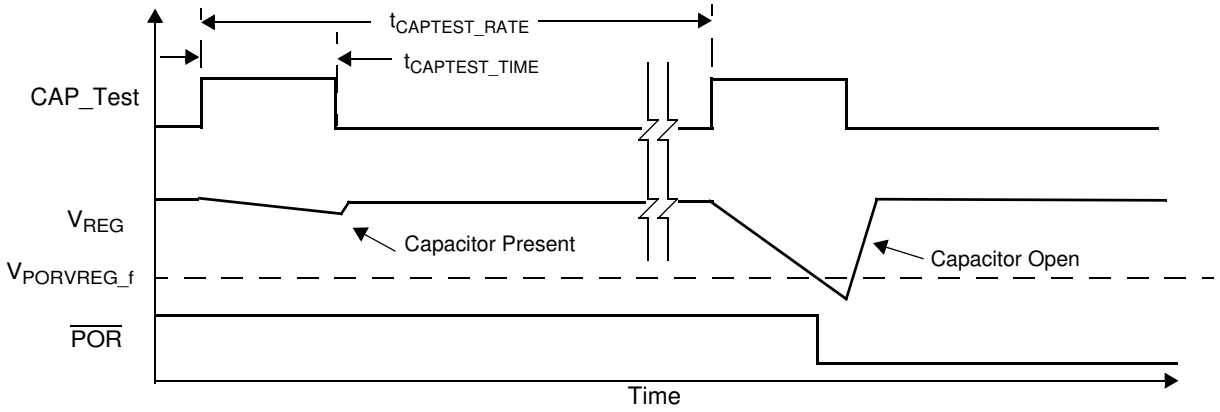


Figure 10. V_{REG} Capacitor Monitor

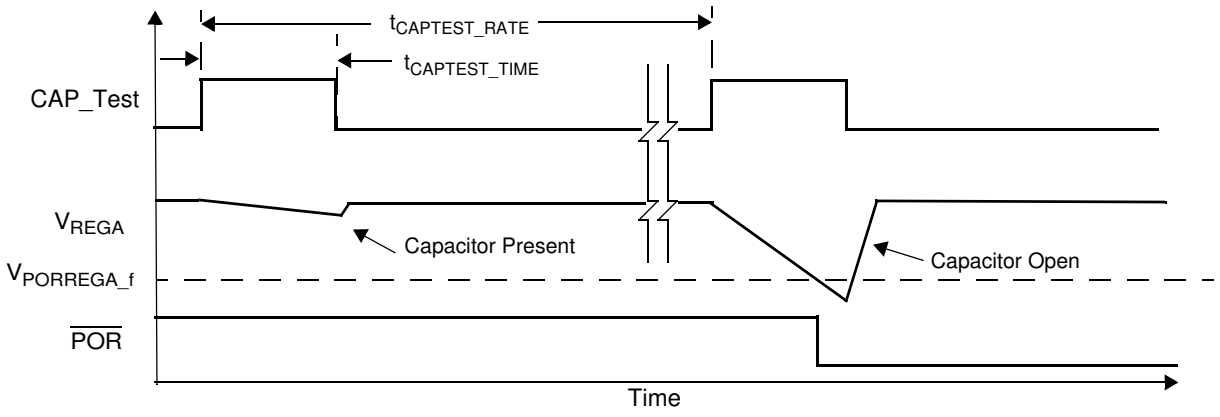


Figure 11. V_{REGA} Capacitor Monitor

3.4 Internal Oscillator

A factory trimmed oscillator is included as specified in Section 2.

3.5 Acceleration Signal Path

3.5.1 Transducer

The transducer is an overdamped mass-spring-damper system defined by the following transfer function:

where:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

ζ = Damping Ratio

ω_n = Natural Frequency = $2 * \Pi * f_n$

Reference Section 2.7 for transducer parameters.

3.5.2 ΣΔ Converter

A sigma delta modulator converts the differential capacitance of the transducer to a 1 MHz data stream that is input to the DSP block.

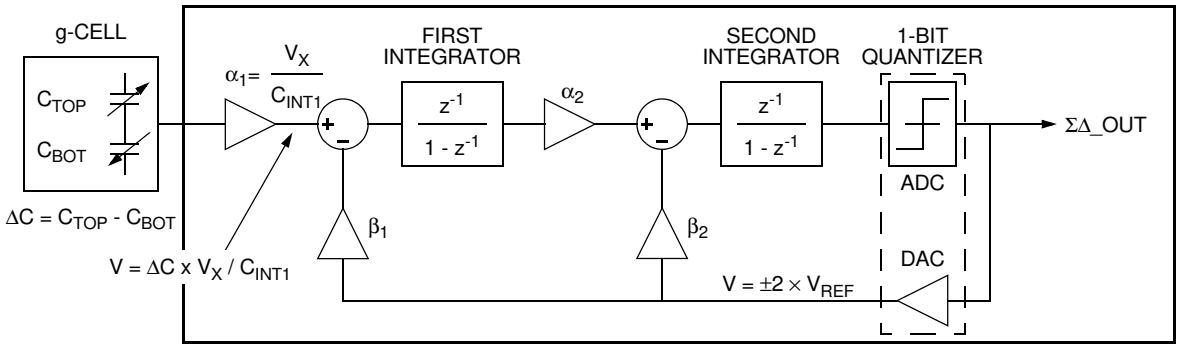


Figure 12. ΣΔ Converter Block Diagram

3.5.3 Digital Signal Processing Block

A Digital Signal Processing (DSP) block is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP block is shown in Figure 13.

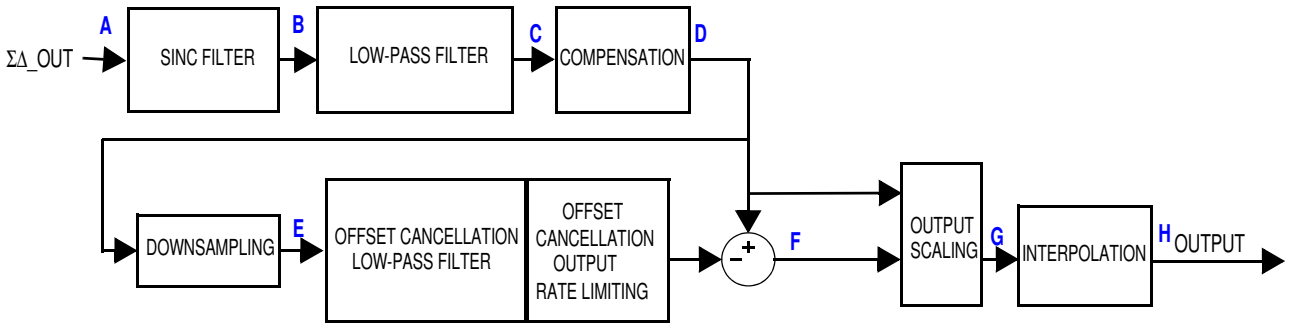


Figure 13. Signal Chain Diagram

Table 3. Signal Chain Characteristics

	Description	Sample Time (μs)	Data Width (Bits)	Over Range (Bits	Signal Width (Bits)	Signal Noise (Bits)	Signal Margin (Bits)	Typical Block Latency	Reference
A	SD	1	1		1			$203/f_{osc}$	Section 3.5.2
B	SINC Filter	16	20		13				Section 3.5.3.2
C	Low-Pass Filter	16	26	4	10	3	9	Reference Section 3.5.3.2	Section 3.5.3.2
D	Compensation	16	26	4	10	3	9	$68/f_{osc}$	
E	Down Sampling	16	26	4	10	3	9		
F	High-Pass Filter	16	26	4	10	3	9	Reference Section 3.5.3.3	Section 3.5.3.3
G	DSP Sampling 10-Bit Output Scaling	16			10			$4/f_{osc}$	Section 3.5.3.5
H	Interpolation	1			10			$64/f_{osc}$	Section 3.5.3.5

3.5.3.1 Decimation Sinc Filter

The serial data stream produced by the ΣΔ converter is decimated and converted to parallel values by a 3rd order 16:1 sinc filter with a decimation factor of 16.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})}\right]^3$$

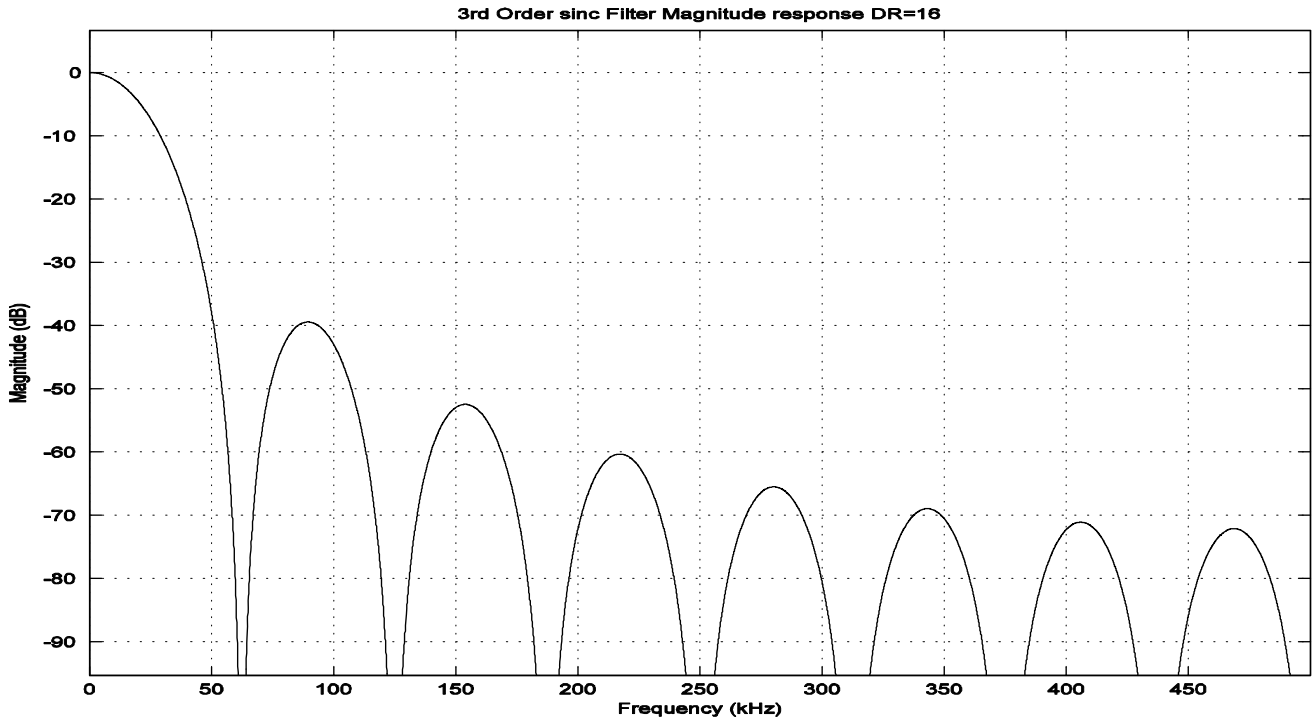


Figure 14. Sinc Filter Response, t_S = 16 μs

3.5.3.2 Low-Pass Filter

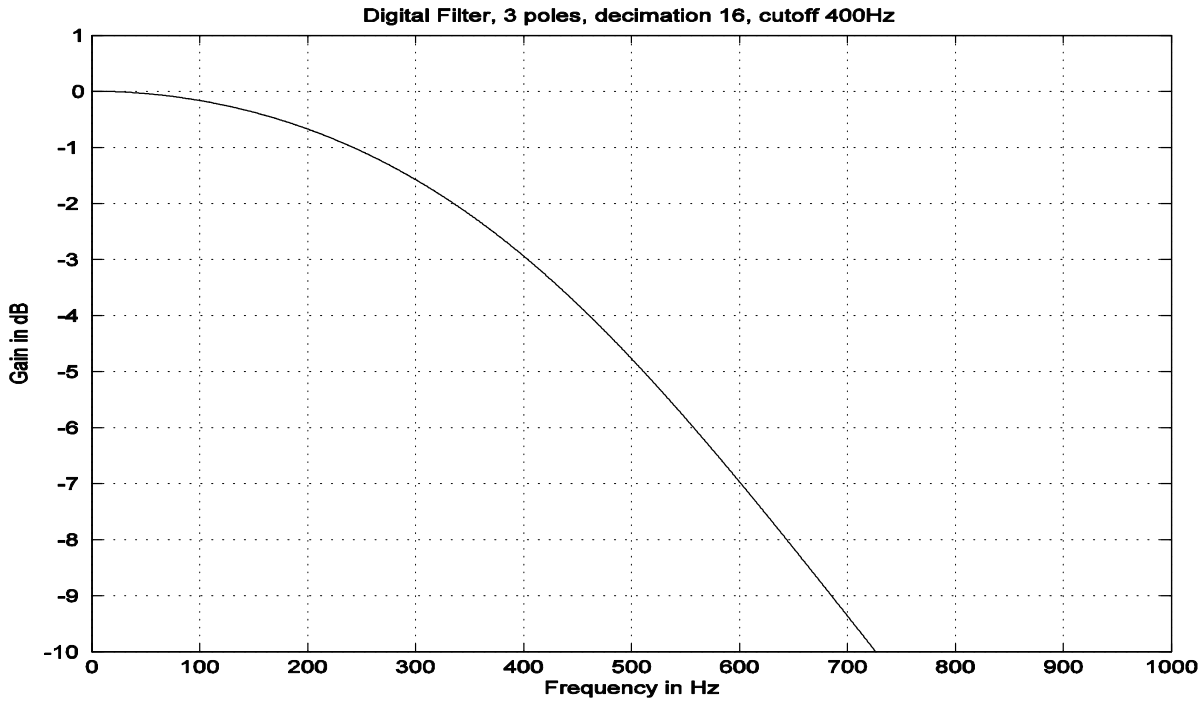
Data from the Sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})}$$

Table 4. Low-Pass Filter Coefficients

Description	Filter Coefficients				Group Delay
400 Hz, 3-Pole LPF	a_0	5.189235225042199e-02			$2816/f_{osc}$
	n_{11}	1.629077582099646e-03	d_{11}	1.0	
	n_{12}	1.630351547919014e-03	d_{12}	-9.481076477495780e-01	
	n_{13}	0	d_{13}	0	
	n_{21}	2.500977520825902e-01	d_{21}	1.0	
	n_{22}	4.999999235890745e-01	d_{22}	-1.915847097557409e+00	
	n_{23}	2.499023243303036e-01	d_{23}	9.191065266874253e-01	

Note: Low-Pass Filter values do not include g-cell frequency response.



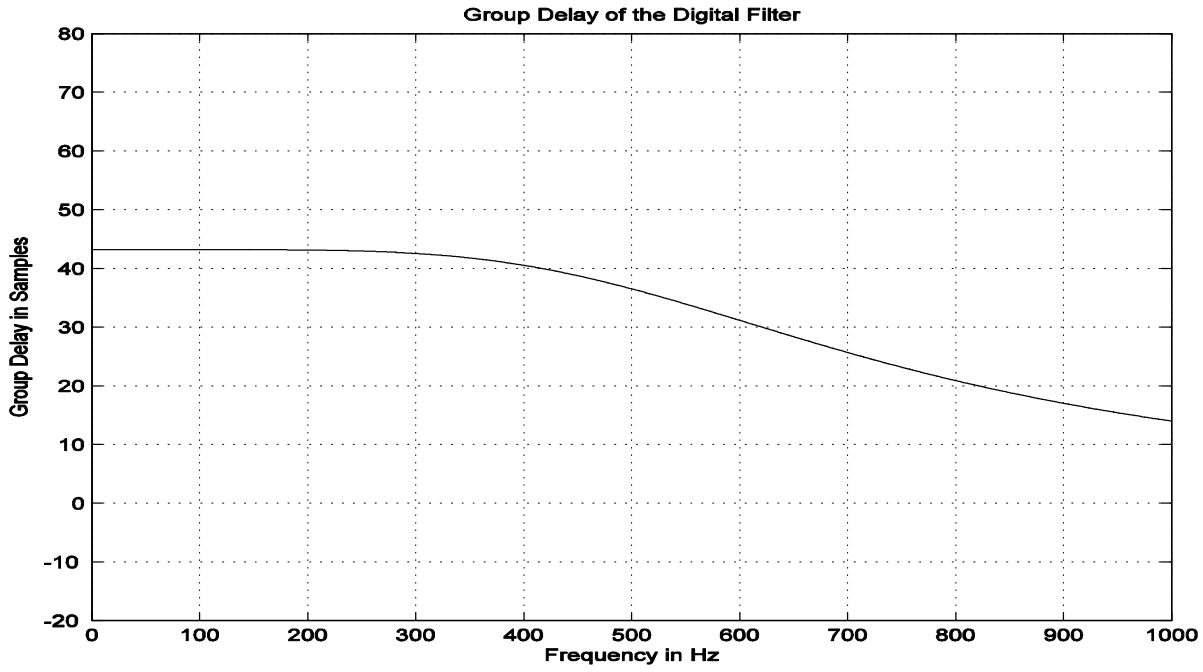


Figure 15. Low-Pass Filter Characteristics: f_C = 400 Hz, 3-Pole, t_S = 16 μs

3.5.3.3 Offset Cancellation

The device provides an offset cancellation circuit to remove internal offset error. A block diagram of the offset cancellation is shown in Figure 16.

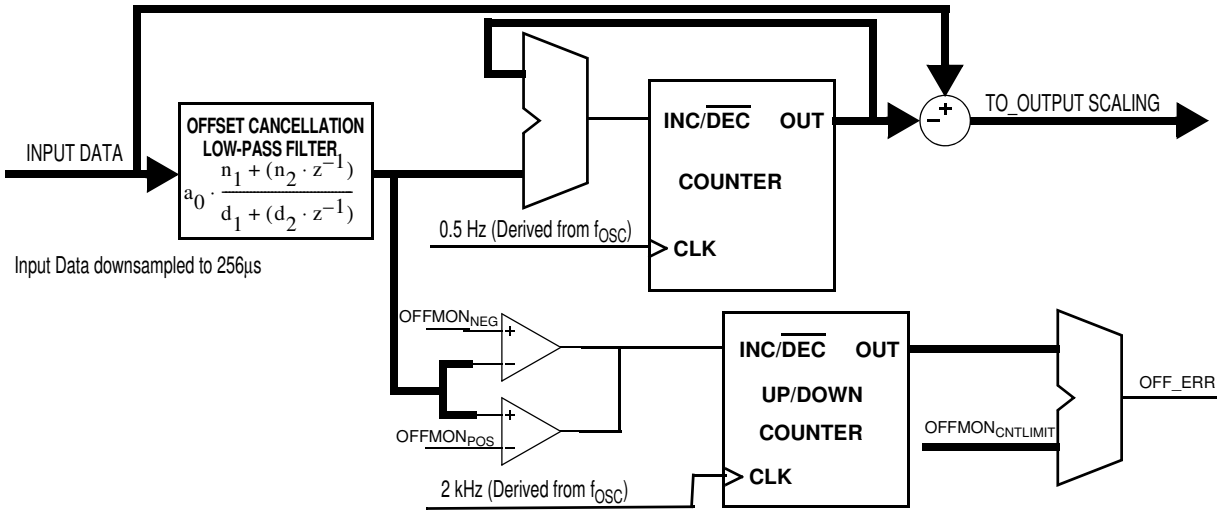


Figure 16. Offset Cancellation Block Diagram

The transfer function for the offset LPF is:

$$H(z) = ao_0 \cdot \frac{no_1 + (no_2 \cdot z^{-1})}{do_1 + (do_2 \cdot z^{-1})}$$

Response parameters are specified in Section 2 and the offset LPF coefficients are specified in Table 6.

During startup, two phases of the offset LPF are used to allow for fast convergence of the internal offset error during initialization. The timing and characteristics of each phase are shown in Table 5 and Table 6 and specified in Section 2. For more information regarding the startup timing, reference the PSI5 initialization information in Section 4.4. The offset low-pass filter used in normal operation is selected by the OC_FILT bit as shown in Table 5.

During the Initialization Self-Test phase, the offset cancellation circuit output value is frozen.

During normal operation, output rate limiting is applied to the output of the high-pass filter. Rate limiting updates the offset cancellation output by OFF_{Step_xx} LSB every $t_{OffRate\_xx}$ seconds.

Table 5. Offset Cancellation Startup Characteristics and Timing

Offset Cancellation Startup Phase	Offset LPF	Output Rate Limiting	Total Time for Phase
1	10 Hz	Bypassed	80 ms
2	0.3 Hz	Bypassed	70 ms
Self-Test	0.3 Hz	Bypassed (Frozen during ST2)	96 ms per Self-Test Sequence (up to 6 repeats)
Complete	0.1 Hz	Enabled	N/A

Table 6. High-Pass Filter Coefficients

Description	Coefficients				Group Delay
10 Hz HPF	ao_0	0.015956938266754			16.384 ms
	no_1	0.499998132328277	do_1	1.0	
	no_2	0.499998132328277	do_2	-0.984043061733246	
0.3 Hz HPF	ao_0	0.000482380390167			537.6 ms
	no_1	0.499938218213271	do_1	1.0	
	no_2	0.499938218213271	do_2	-0.999517619609833	
0.1 Hz HPF	ao_0	0.0001608133316040			1591ms
	no_1	0.4999999403953552	do_1	1.0	
	no_2	0.4999999403953552	do_2	-0.9998391270637512	

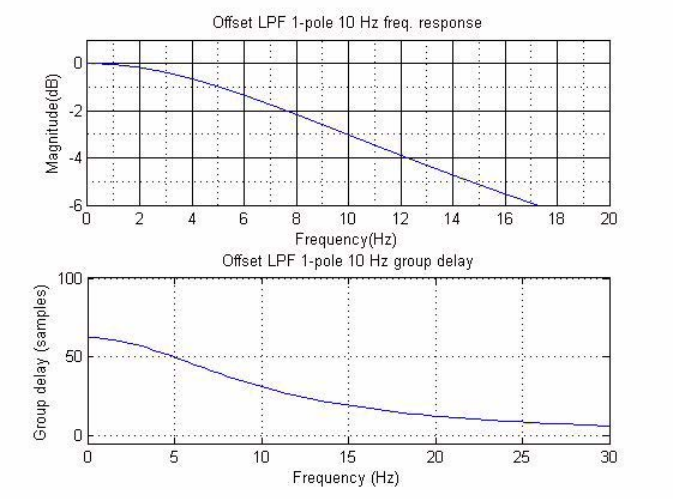


Figure 17. 10 Hz Offset Cancellation Low-Pass Filter Characteristics

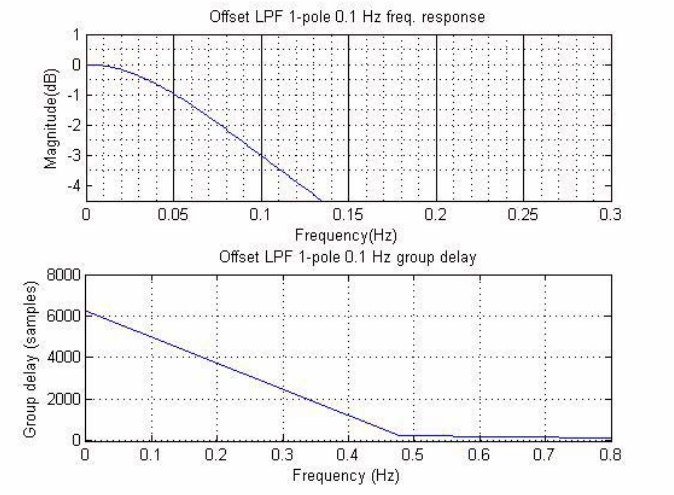


Figure 18. 0.1 Hz Offset Cancellation Low-Pass Filter Characteristics

3.5.3.4 Offset Monitor

The device includes an offset monitor circuit. The output of the single pole low-pass filter in the offset cancellation block is continuously monitored against the offset limits specified in Section 2.4. An up/down counter is employed to count up If the output exceeds the limits, and to count down if the output is within the limits. The output of the counter is compared against the count limit $OFFMON_{CNTLIMIT}$. If the counter exceeds the limit, the OFF_B flag in the SC register is cleared. The counter rails once the max counter value is reached ($OFFMON_{CNTSIZE}$). The offset monitor is disabled during Initialization Phase 1, Phase 2, and Phase 3.

3.5.3.5 Data Interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time.

3.5.3.6 Output Scaling

The 26-bit digital output from the DSP is clipped and scaled to a 10-bit word which spans the acceleration range of the device. Figure 19 shows the method used to establish the output acceleration data word from the 26-bit DSP output.

Over Range			**Signal**										**Noise**				**Margin**				
D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	...	D2	D1	D0
10-bit Data Word				D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	Using Rounding							

Figure 19. 10-Bit Output Scaling Diagram