



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





Digital Dual Axis Micromachined Accelerometer

The MMA62XXEG is a two-axis member of Freescale's family of SPI-compatible accelerometers. These devices incorporate digital signal processing for filtering, trim and data formatting.

Features

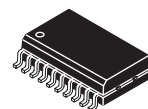
- Available in $\pm 20/20g$, $\pm 50/50g$, or $\pm 100/100g$ versions. Additional g-ranges between 20 and 100g may be available upon request
- Full-scale range is independently specified for each axis
- 400 Hz low-pass filter, 0.1 Hz high-pass filter, 4-pole, 16 μs sample time, additional filter options are available
- Ratiometric analog voltage output
- 10-bit digital signed data output
- SPI-compatible serial interface
- Capture/hold input for system-wide synchronization support
- 3.3 or 5 V single supply operation
- On-chip temperature sensor and voltage regulator
- Bidirectional internal self-test
- Minimal external component requirements
- Pb-free 20-pin SOIC package
- Automotive AEC-Q100 qualified

Typical Applications

- Crash detection (Airbag)
- Impact and vibration monitoring
- Shock detection

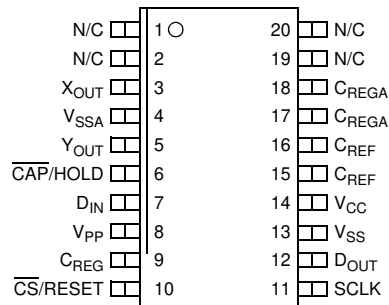
MMA6222EG
MMA6255EG
MMA621010EG

2-AXIS
SPI-COMPATIBLE
ACCELEROMETER



EG SUFFIX (Pb-free)
20-LEAD SOIC
CASE 475A-02

PIN CONNECTIONS

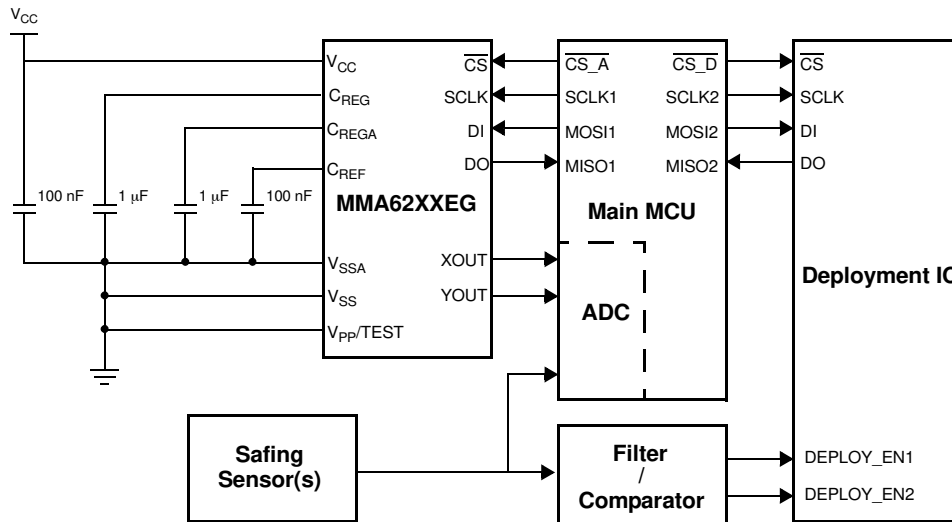


20-PIN SOIC PACKAGE

N/C: NO INTERNAL CONNECTION

ORDERING INFORMATION

| Device Name | X-Axis g-Level | Y-Axis g-Level | Temperature Range | Package | Packaging |
|---------------|----------------|----------------|-------------------|---------|-------------|
| MMA6222EG | 20 | 20 | -40 to +105°C | 475A-02 | Tubes |
| MMA6222EGR2 | 20 | 20 | -40 to +105°C | 475A-02 | Tape & Reel |
| MMA6255EG | 50 | 50 | -40 to +105°C | 475A-02 | Tubes |
| MMA6255EGR2 | 50 | 50 | -40 to +105°C | 475A-02 | Tape & Reel |
| MMA621010EG | 100 | 100 | -40 to +105°C | 475A-02 | Tubes |
| MMA621010EGR2 | 100 | 100 | -40 to +105°C | 475A-02 | Tape & Reel |



Note: If one axis of the MMA62XXEG sensor is expected to be used as a confirmation of the other axis, Freescale recommends that MMA62XXEG used in conjunction with an additional sensing/safing device for each axis.

Figure 1-1 Simplified Airbag Application Diagram

1.1 INTRODUCTION

The MMA62XXEG is intended for applications which utilize serial communications as the primary data transfer mechanism. In addition, an analog output with lower accuracy is available.

Device serial number, acceleration range, filter characteristics and status information are available along with acceleration data via the SPI interface. A pair of digital-to-analog converters is enabled to provide ratiometric voltage outputs in addition to the digital acceleration value accessible via the SPI.

1.2 BLOCK DIAGRAM

A block diagram illustrating the major components of the design is shown in [Figure 1-2](#).

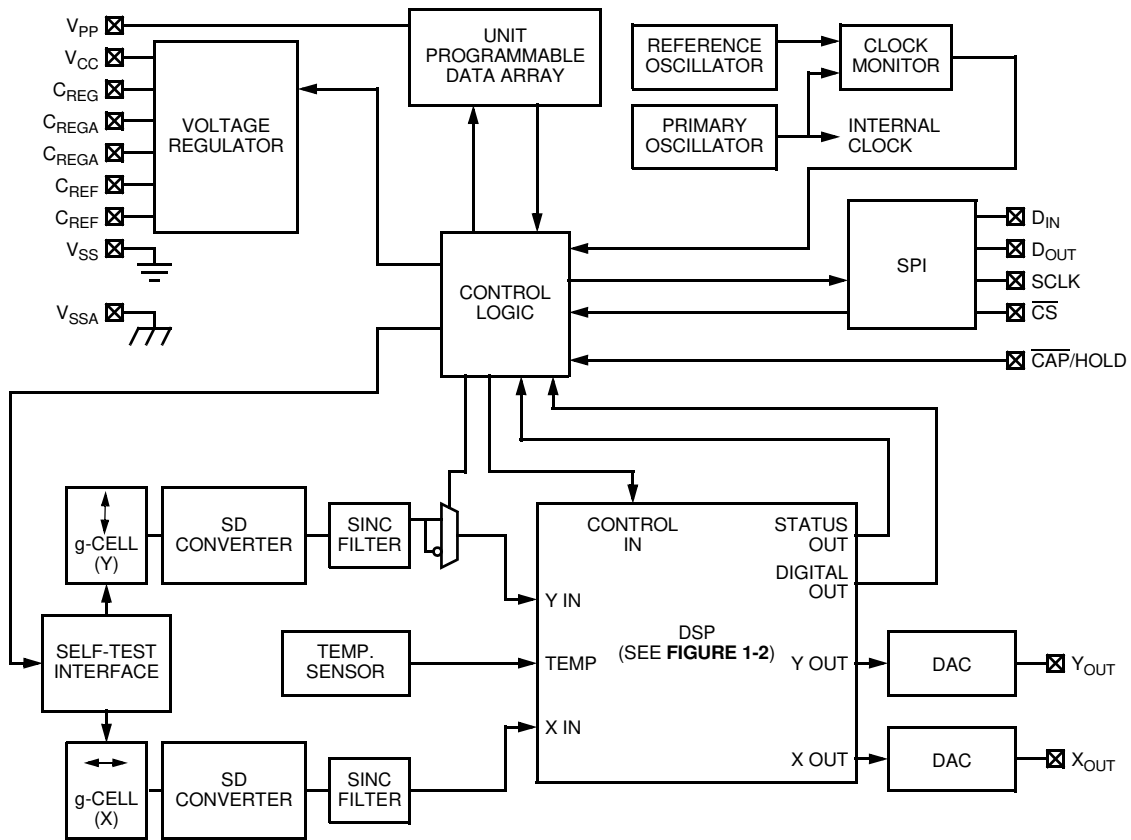


Figure 1-2 MMA62XXEG Block Diagram

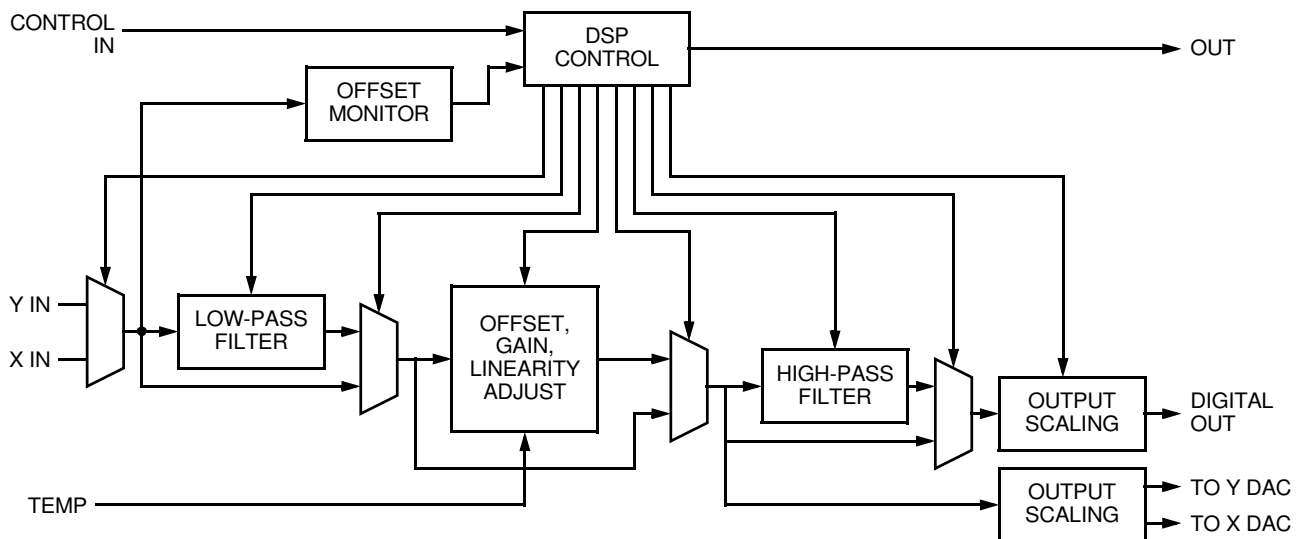
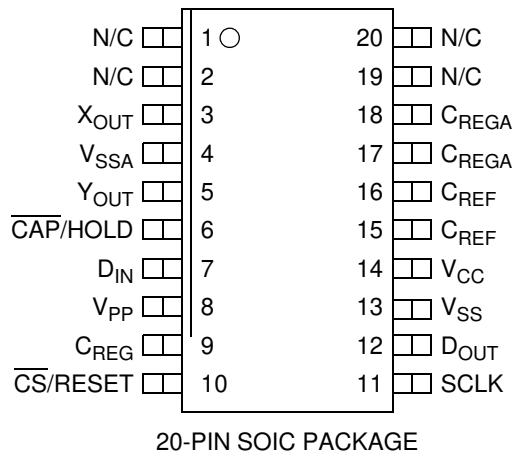


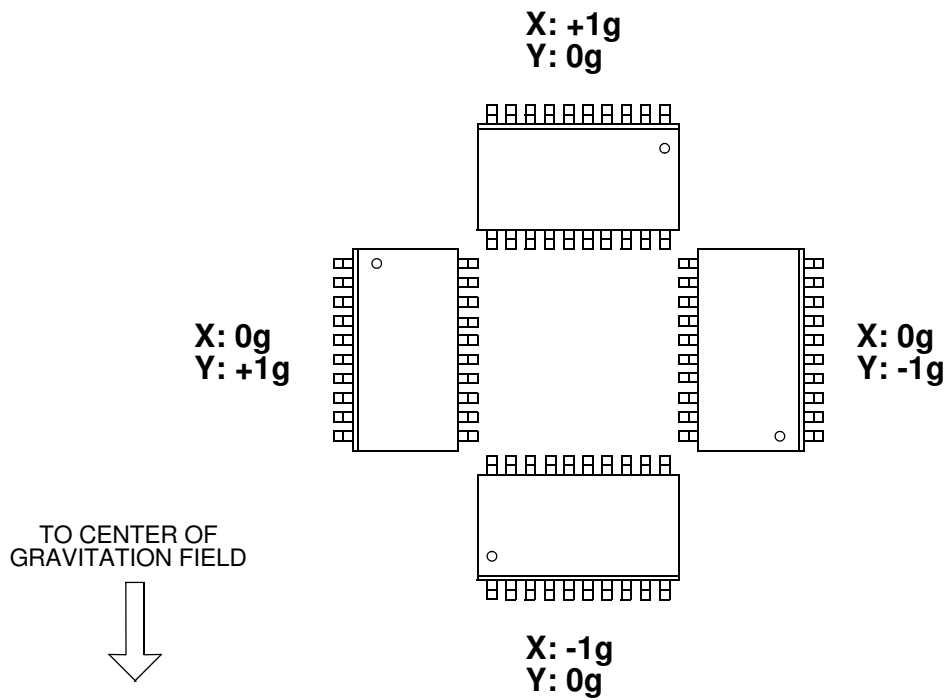
Figure 1-3 MMA62XXEG DSP Block Diagram
NOTE: Models of signal chain are available upon request.

1.3 PIN FUNCTIONS

The pinout for the MMA62XXEG device is illustrated in Figure 1-4. Pin functions are described below. When self-test is active, the output becomes more positive in both axes if ST1 is cleared, or more negative in both axes if ST1 is set, as described in Section 3.1.1.



N/C: NO INTERNAL CONNECTION



Response to static orientation within 1g field.

Figure 1-4 MMA62XXEG Pinout

1.4 PIN FUNCTION DESCRIPTIONS

1.4.1 V_{CC}

This pin supplies power to the device. Careful printed wiring board layout and capacitor placement is critical to ensure best performance. An external bypass capacitor between this pin and V_{SS} is required, as described in [Section 1.5](#).

1.4.2 V_{SS}

This pin is the power supply return node for the digital circuitry on the MMA62XXEG device.

1.4.3 V_{SSA}

This pin is the power supply return node for analog circuitry on the MMA62XXAEG device. An external bypass capacitor between this pin and V_{CC} is required, as described in [Section 1.5](#).

1.4.4 C_{REG}

This pin is connected to the internal digital circuitry power supply rail. An external filter capacitor must be connected between this pin and V_{SS} , as described in [Section 1.5](#).

1.4.5 C_{REGA}

These pins are connected in parallel to the internal analog circuitry power supply rail. One or two external filter capacitors must be connected between these pins and V_{SSA} , as described in [Section 1.5](#). Two pins are provided to support redundant connection to the printed wiring board assembly. Redundant external capacitors may be connected to these pins for maximum reliability, as described in [Section 1.5](#).

1.4.6 C_{REF}

These pins are connected in parallel to an internal reference voltage node utilized by the analog circuitry. One or two external filter capacitors must be connected between these pins and V_{SSA} , as described shown in [Section 1.5](#). Two pins are provided to support redundant connection to the printed wiring board assembly. Redundant external capacitors may be connected to these pins for maximum reliability, as described in [Section 1.5](#).

1.4.7 V_{PP}

This pin should be tied directly to V_{SS} .

1.4.8 $SCLK$

This input pin provides the serial clock to the SPI port. The state of this pin is also used as a qualifier for externally-controlled reset. An internal pull-down device is connected to this pin. This input may be left unconnected unless it is desired to initiate device reset as described in [Section 1.4.9](#).

1.4.9 $\overline{CS}/\overline{RESET}$

This pin provides two functions. When the SPI is enabled, this pin functions as the chip select input for the SPI port. The state of the D_{IN} pin during low-to-high transitions of $SCLK$ is latched internally and D_{OUT} is enabled when \overline{CS} is at a logic low level.

This pin may also be used to initiate a hardware reset. If \overline{CS} is held low and $SCLK$ is held high for 512 μs , the internal reset signal is asserted.

An internal pull-up device is connected to this pin.

1.4.10 D_{OUT}

This pin functions as the serial data output for the SPI port.

Immediately following device reset, D_{OUT} is placed in a high impedance state for approximately 800 μs . At the end of this time, D_{OUT} is driven high and a 3ms stabilization delay required by the internal circuitry begins. Reset is reported by the device so the system can be aware of potential difficulties if unexpected resets occur.

1.4.11 D_{IN}

This pin functions as the serial data input to the SPI.

1.4.12 $\overline{\text{CAP/HOLD}}$

When this input pin is low, the SPI acceleration result registers are updated by the DSP whenever a data sample becomes available. Upon a low-to-high transition of $\overline{\text{CAP/HOLD}}$, the contents of the acceleration result registers are frozen. The result registers will not be updated so long as this pin remains at a logic '1' level. This pin may be tied directly to V_{SS} if the hold function is not desired.

1.4.13 $X_{\text{OUT}}, Y_{\text{OUT}}$

Two Digital-to-Analog Converters (DACs) translate output of the DSP block into voltage levels proportional to the magnitude of the numerical result and ratiometric to V_{CC} . The DAC outputs have an inherent accuracy of about $\pm 12\%$.

1.5 EXTERNAL COMPONENTS

The connections illustrated below are recommended. Careful printed wiring board layout and component placement is essential for best performance. Low ESR capacitors must be connected to C_{REG} and C_{REGA} pins for the best performance. A grounded land area with solder mask should be placed under the package for improved shielding of the device from external effects. If a land area is not provided, no signals should be routed beneath the package. See [Figure 1-1](#).

SECTION 2 PERFORMANCE SPECIFICATION

2.1 MAXIMUM RATINGS

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep input and output voltages within the range $V_{SS} \leq V \leq V_{CC}$.

| Ref | Rating | Symbol | Value | Unit | |
|-----|---|-------------|------------------------|-------------|-----|
| 1 | Supply Voltage | V_{CC} | -0.3 to +7 | V | (1) |
| 2 | C_{REG} , C_{REGA} , C_{REF} | V_{REG} | -0.3 to +3 | V | (1) |
| 3 | V_{PP} | V_{REG} | -0.3 to +11 | V | (1) |
| 4 | $SCLK$, \overline{CS} , D_{IN} , $\overline{CAP/HOLD}$ | V_{IN} | -0.3 to $V_{CC} + 0.3$ | V | (1) |
| 5 | D_{OUT} (high impedance state) | V_{IN} | -0.3 to $V_{CC} + 0.3$ | V | (1) |
| 6 | Current Drain per Pin Excluding V_{CC} and V_{SS} | I | 10 | mA | (1) |
| 7 | Acceleration (without hitting internal g-cell stops) | g_{max} | ± 800 | g | (1) |
| 8 | Powered Shock (six sides, 0.5 ms duration) | g_{pms} | ± 1500 | g | (1) |
| 9 | Unpowered Shock (six sides, 0.5 ms duration) | g_{shock} | ± 2000 | g | (1) |
| 10 | Drop Shock (to concrete surface) | h_{DROP} | 1.2 | m | (1) |
| 11 | Electrostatic Discharge Human Body Model (HBM) | V_{ESD} | ± 2000 | V | (1) |
| 12 | Charge Device Model (CDM) | V_{ESD} | ± 500 | V | (1) |
| 13 | Machine Model (MM) | V_{ESD} | ± 200 | V | (1) |
| 14 | Storage Temperature Range | T_{stg} | -40 to +125 | $^{\circ}C$ | (1) |

Notes:

1. Verified by characterization, not tested in production.

2.2 OPERATING RANGE

The operating ratings are the limits normally expected in the application and define the range of operation.

| Ref | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|----------|-------|------|-------|-------|-----|
| 16 | Supply Voltage | | V_L | | V_H | | |
| 17 | Standard Operating Voltage, 3.3V operating range | V_{CC} | +3.15 | +3.3 | +3.45 | V | (1) |
| 17 | Standard Operating Voltage, 5V operating range | V_{CC} | +4.75 | +5.0 | +5.25 | V | (1) |
| 18 | Operating Temperature Range | T_A | T_L | — | T_H | C | (2) |

Notes:

1. Characterized at all values of V_L and V_H . Production test is conducted at typical voltage unless otherwise noted.
2. Parameters tested 100% at final test.

2.3 ELECTRICAL CHARACTERISTICS

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

| Ref | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|-----------------|----------------|---------|-------|------------|--------|
| 19 | Supply Current Drain $V_{CC} = 5.25$ V, $t_S = 16$ μ s | # I_{DD} | — | — | 9.5 | mA | (2) |
| 20 | Power-On Recovery Threshold (See Figure 2-1) V_{CC} | V_{POR_N} | 2.77 | — | 3.15 | V | (2) |
| 21 | C_{REG} | V_{POR_N} | 1.80 | — | 2.32 | V | (2) |
| 22 | C_{REGA} | V_{POR_N} | 2.18 | — | 2.50 | V | (2) |
| 23 | C_{REF} | V_{POR_N} | 1.11 | — | 1.29 | V | (2) |
| 24 | Power-On Reset Threshold (See Figure 2-1) V_{CC} | V_{POR_A} | 2.77 | — | 2.95 | V | (2) |
| 25 | C_{REG} | V_{POR_A} | 1.80 | — | 2.10 | V | (2) |
| 26 | C_{REGA} | V_{POR_A} | 2.18 | — | 2.31 | V | (2) |
| 27 | C_{REF} | V_{POR_A} | 1.11 | — | 1.19 | V | (2) |
| 28 | Hysteresis ($V_{POR_N} - V_{POR_A}$, See Figure 2-1) V_{CC} | V_{HYST} | 0 | — | 388 | mV | |
| 29 | C_{REG} | V_{HYST} | 0 | — | 300 | mV | |
| 30 | C_{REGA} | V_{HYST} | 0 | — | 261 | mV | |
| 31 | C_{REF} | V_{HYST} | 0 | — | 150 | mV | |
| 32 | Minimum Functional Voltage (See Figure 2-1) | V_{DACU} | — | — | 2.0 | V | (2) |
| 33 | Internally Regulated Voltages C_{REG} | V_{DD} | 2.42 | 2.50 | 2.58 | V | (1) |
| 34 | C_{REGA} (3) | * $V_{2.5}$ | 2.42 | 2.50 | 2.58 | V | (1) |
| 35 | C_{REF} | * V_{REF} | 1.20 | 1.25 | 1.29 | V | (1) |
| 36 | External Filter Capacitor (C_{REG} , C_{REGA}) Value | C_{REG} | 800 | 1000 | — | nF | (2) |
| 37 | ESR (including interconnect resistance) | ESR | — | — | 200 | m Ω | (2) |
| 38 | Power Supply Coupling (4) Digital output | | — | — | 0.004 | digit/mv | (2) |
| 39 | Analog output | | See Figure 2-2 | | | | (2) |
| 40 | Digital Sensitivity (D_{OUT}) 20 g Range | * SENS | — | 0.04097 | — | g/digit | (1)(5) |
| 41 | 35 g Range | * SENS | — | 0.0717 | — | g/digit | (1)(5) |
| 42 | 50 g Range | * SENS | — | 0.1024 | — | g/digit | (1)(5) |
| 43 | 100 g Range | * SENS | — | 0.2048 | — | g/digit | (1)(5) |
| 44 | Sensitivity Error $T_A = 25^\circ\text{C}$ | * Δ SENS | -4 | — | +4 | % | (1)(5) |
| 45 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | * Δ SENS | -4 | — | +4 | % | (1)(5) |

Notes:

- Parameters tested 100% at final test.
 - Verified by characterization, not tested in production.
 - Tested at $V_{CC} = V_L$ and $V_{CC} = V_H$.
 - Power supply ripple at frequencies greater than 900 kHz should be minimized to the greatest extent possible.
 - Devices are trimmed at 100 Hz with 1000 Hz low pass filter selected.
- (#) Indicates a FSL significant parameter (CPK > 1.33).
 (*) Indicates a FSL critical parameter (CPK > 1.67).

2.3 ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

| Ref | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|-----------------------|----------------------|---------------------|----------------------|------------------------|-----|
| 46 | Analog Sensitivity (X_{OUT} , Y_{OUT}) 20 g Range | * ASENS | — | 23.4 | — | mV/V/g | (1) |
| 47 | 35 g Range | * ASENS | — | 13.40 | — | mV/V/g | (1) |
| 48 | 50 g Range | * ASENS | — | 9.37 | — | mV/V/g | (1) |
| 49 | 100 g Range | * ASENS | — | 4.68 | — | mV/V/g | (1) |
| 50 | Sensitivity Error $T_A = 25^\circ\text{C}$ | * ΔSENS | -16 | — | +16 | % | (1) |
| 51 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | * ΔSENS | -16 | — | +16 | % | (1) |
| 52 | Offset at 0 g (High-pass filter disabled) 10-bits, signed | * D_{OUT} | -40 | 0 | +40 | digit | (1) |
| 53 | Analog output trimmed for digital operation | * A_{OUT} | $0.44 \times V_{CC}$ | $0.5 \times V_{CC}$ | $0.56 \times V_{CC}$ | V | (1) |
| 54 | Range of Output (D_{OUT} , 10 bits, signed) Normal | RANGE | -509 | — | 508 | digit | (5) |
| 55 | Positive Acceleration Overflow Code | OF_S | — | 510 | — | digit | (5) |
| 56 | Positive Acceleration Overrange Code | OR_S | — | 509 | — | digit | (5) |
| 57 | Negative Acceleration Underrange Code | UR_S | — | -510 | — | digit | (5) |
| 58 | Negative Acceleration Underflow Code | UF_S | — | -511 | — | digit | (5) |
| 59 | Unused Code | UNUSED | — | 511 | — | digit | (5) |
| 60 | Unused Code | UNUSED | — | -512 | — | digit | (5) |
| 61 | Output value on overrange 20 g Range | g_{OVER} | +20.0 | +20.9 | +22.1 | g | (2) |
| 62 | 35 g Range | g_{OVER} | +35.0 | +36.6 | +38.7 | g | |
| 63 | 50 g Range | g_{OVER} | +50.0 | +52.1 | +55.3 | g | (2) |
| 64 | 100 g Range | g_{OVER} | +100.1 | +104.3 | +110.5 | g | |
| 65 | Output value on underrange 20 g Range | g_{UNDER} | -20.1 | -20.9 | -22.2 | g | |
| 66 | 35 g Range | g_{UNDER} | -35.1 | -36.6 | -38.8 | g | |
| 67 | 50 g Range | g_{UNDER} | -50.0 | -52.2 | -55.4 | g | |
| 68 | 100 g Range | g_{UNDER} | -100.1 | -104.5 | -110.7 | g | |
| 69 | Maximum acceleration without saturation of internal circuitry All ranges | g_{SAT} | -200 | — | +200 | g | (2) |
| 70 | Nonlinearity | NL_{OUT} | -1 | — | 1 | % FSR | (2) |
| 71 | Noise (1Hz-1kHz) | n_{SD} | — | — | 1.1 | mg/ $\sqrt{\text{Hz}}$ | (2) |
| 72 | Positive Self Test Output Change (D_{OUT} , digital) $T_A = 25^\circ\text{C}$ | * ΔST | 67 | 72 | 77 | digit | (1) |
| 73 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | * ΔST | 62 | 72 | 82 | digit | (1) |
| 74 | (X_{OUT} , Y_{OUT} , analog) $T_A = 25^\circ\text{C}$ | * ΔST | 10 | — | 18 | % FS | (1) |
| 75 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | * ΔST | 10 | — | 18 | % FS | (1) |

Notes:

- Parameters tested 100% at final test.
- Verified by characterization, not tested in production.
5. Functionality verified 100% via scan.
- (*) Indicates a FSL critical parameter (CPK > 1.67).

2.3 ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

| Ref | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|---|-------------------|-----------------|-----|------|---------------|-----|
| 76 | Negative Self Test Output Change (D_{OUT} , digital) $T_A = 25^\circ\text{C}$ | ΔST | -78 | -72 | -66 | digit | (6) |
| 77 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | ΔST | -82 | -72 | -62 | digit | (6) |
| 78 | (X_{OUT} , Y_{OUT} , analog) $T_A = 25^\circ\text{C}$ | ΔST | -18 | — | -10 | % FS | (6) |
| 79 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | ΔST | -18 | — | -10 | % FS | (6) |
| 80 | Cross-Axis Sensitivity V_{ZX} | V_{ZX} | -4 | — | +4 | % | (6) |
| 81 | V_{YX} | V_{YX} | -4 | — | +4 | % | (6) |
| 82 | V_{ZY} | V_{ZY} | -4 | — | +4 | % | (6) |
| 83 | V_{XY} | V_{XY} | -4 | — | +4 | % | (6) |
| 84 | DAC Characteristics (X_{OUT} , Y_{OUT}) Minimum Output Level, $I_{OUT} = -200 \mu\text{A}$ | AV_{LOW} | — | — | 0.25 | V | (2) |
| 85 | Maximum Output Level, $I_{OUT} = 200 \mu\text{A}$ | AV_{HIGH} | $V_{CC} - 0.25$ | — | — | V | (2) |
| 86 | Offset Error | OFST | -0.2 | — | +0.2 | %FSR | (2) |
| 87 | Gain Error | GERR | -0.3 | — | +0.3 | %FSR | (2) |
| 88 | Differential Nonlinearity Integral Nonlinearity | DNL | -2 | — | +2 | digit | (2) |
| 89 | $T_A = 25^\circ\text{C}$ | INL | -3 | — | +3 | digit | (2) |
| 90 | $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | INL | -3.5 | — | +3.5 | digit | (6) |
| 91 | Output High Voltage D_{OUT} ($I_{Load} = -100 \mu\text{A}$) $3.15 \text{ V} \leq (V_{CC} - V_{SS}) \leq 3.45 \text{ V}$ | V_{OH} | 3.25 | — | — | V | (2) |
| 92 | $4.75 \text{ V} \leq (V_{CC} - V_{SS}) \leq 5.25 \text{ V}$ | V_{OH} | 3.75 | — | — | V | (2) |
| 93 | Output Low Voltage D_{OUT} , ($I_{Load} = 100 \mu\text{A}$) $3.15 \text{ V} \leq (V_{CC} - V_{SS}) \leq 3.45 \text{ V}$ | V_{OL} | — | — | 0.4 | V | (2) |
| 94 | $4.75 \text{ V} \leq (V_{CC} - V_{SS}) \leq 5.25 \text{ V}$ | V_{OL} | — | — | 0.4 | V | (2) |
| 95 | Output Loading (D_{OUT}) Load Resistance | Z_{OUT} | 47 | — | — | k Ω | (6) |
| 96 | Load Capacitance | C_{OUT} | — | — | 35 | pF | (6) |
| 97 | Output Loading (X_{OUT} , Y_{OUT}) Load Resistance | Z_{OUT} | 25 | — | — | k Ω | (6) |
| 98 | Load Capacitance | C_{OUT} | — | — | 60 | pF | (6) |
| 99 | Input High Voltage CS/RESET, SCLK, D_{IN}/ST , $\overline{\text{CAP}}/\text{HOLD}$ $3.15 \text{ V} \leq (V_{CC} - V_{SS}) \leq 3.45 \text{ V}$ | V_{IH} | 1.5 | — | — | V | (2) |
| 100 | $4.75 \text{ V} \leq (V_{CC} - V_{SS}) \leq 5.25 \text{ V}$ | V_{IH} | 2.5 | — | — | V | (2) |
| 101 | Input Low Voltage CS/RESET, SCLK, D_{IN}/ST , $\overline{\text{CAP}}/\text{HOLD}$ $3.15 \text{ V} \leq (V_{CC} - V_{SS}) \leq 3.45 \text{ V}$ | V_{IL} | — | — | 0.85 | V | (2) |
| 102 | $4.75 \text{ V} \leq (V_{CC} - V_{SS}) \leq 5.25 \text{ V}$ | V_{IL} | — | — | 1.0 | V | (2) |
| 103 | Input Current High (at V_{IH}) SCLK, D_{IN} , $\overline{\text{CAP}}/\text{HOLD}$ | I_{IH} | -30 | -50 | -260 | μA | (2) |
| 104 | V_{PP}/TEST (internal pulldown resistor) | R_{IN} | 190 | 270 | 350 | k Ω | (2) |
| 105 | Low (at V_{IL}) CS/RESET | I_{IL} | 30 | 50 | 260 | μA | (2) |

Notes:

- Parameters tested 100% at final test.
- Verified by characterization, not tested in production.
- Parameters tested 100% at unit probe.

2.4 CONTROL TIMING

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

| Ref | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|--------------|-------|-----|-------|---------|-----|
| 106 | DSP Low-Pass Filter (5) Cutoff frequency (6) | | 380 | 400 | 420 | Hz | (1) |
| 107 | DSP Low-Pass Filter Cutoff frequency (-3dB, referenced to 0 Hz) | | 335 | 353 | 371 | Hz | (1) |
| 108 | DSP High-Pass Filter Cutoff frequency | $f_{C(HPF)}$ | 0.095 | 0.1 | 0.105 | Hz | (1) |
| 109 | Filter Order | O_{HPF} | — | 1 | — | 1 | (1) |
| 110 | Power-On Recovery Time POR negated to CS low | t_{OP} | — | — | 840 | μ s | (1) |
| 111 | Power applied to X_{OUT} , Y_{OUT} valid | t_{XY} | — | — | 10 | ms | (2) |
| 112 | Internal Oscillator Frequency | f_{OSC} | 3.8 | 4.0 | 4.2 | MHz | (3) |
| 113 | Clock Monitor Threshold | f_{MON} | 3.6 | — | 4.4 | MHz | (1) |
| 114 | Chip Select to Internal Reset (See Figure 2-3) | t_{CSRES} | 486 | 512 | 538 | μ s | (1) |
| | Serial Interface Timing (See Figure 2-4) | | | | | | |
| 115 | Clock period | t_{SCLK} | 120 | — | — | ns | (1) |
| 116 | CS asserted to SCLK high | t_{CSCLK} | 60 | — | — | ns | (1) |
| 117 | Data setup time | t_{DC} | 20 | — | — | ns | (1) |
| 118 | Data hold time | t_{CDIN} | 10 | — | — | ns | (1) |
| 119 | SCLK low to data out | t_{CDOUT} | — | — | 50 | ns | (1) |
| 120 | SCLK high to CS negated | t_{CHCSH} | 60 | — | — | ns | (1) |
| 121 | CS negated to CS asserted | t_{CSN} | 526 | — | — | ns | (1) |
| 122 | DAC Low-Pass Filter Cutoff Frequency | f_C | 5 | 10 | 20 | kHz | (4) |
| 123 | Sensing Element Rolloff Frequency (-3 dB) | BW_{GCELL} | — | 3 | — | kHz | (2) |

Notes:

1. Functionality verified 100% via scan. Timing characteristic is directly determined by internal oscillator frequency.
2. Verified by characterization, not tested in production.
3. Parameters tested 100% at final test.
4. Parameters tested 100% at unit probe.
5. Devices are trimmed at 100 Hz with 1000 Hz low-pass filter option selected.
6. Cutoff frequencies shown are -4dB referenced to 0 Hz response, to correspond with previous specifications.

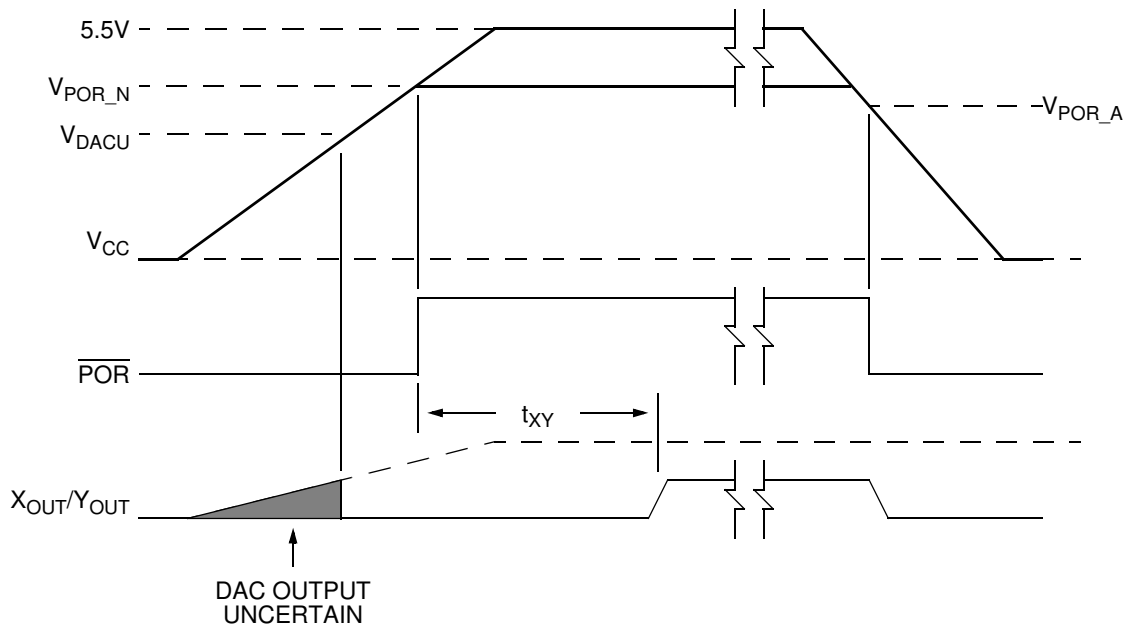


Figure 2-1 Power-Up Timing

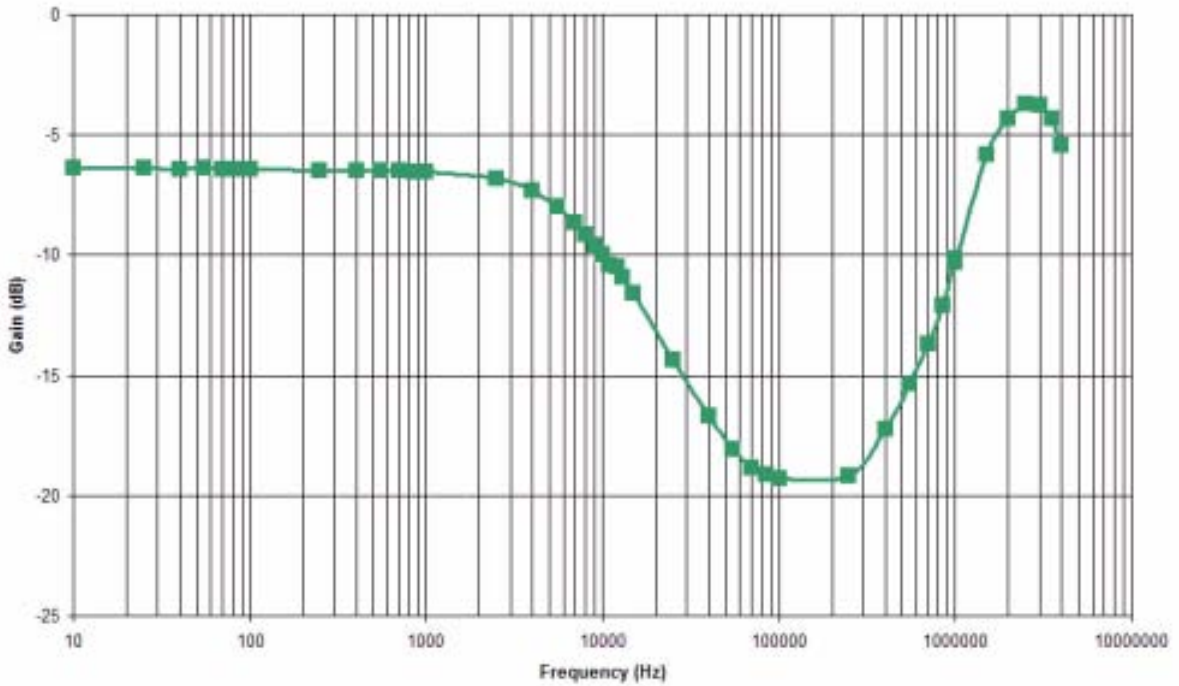


Figure 2-2 Power Supply Coupling - DAC Outputs

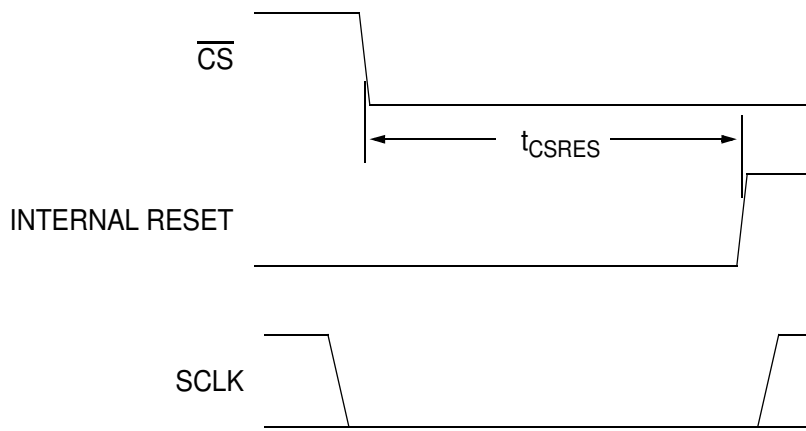


Figure 2-3 \overline{CS} Reset Timing

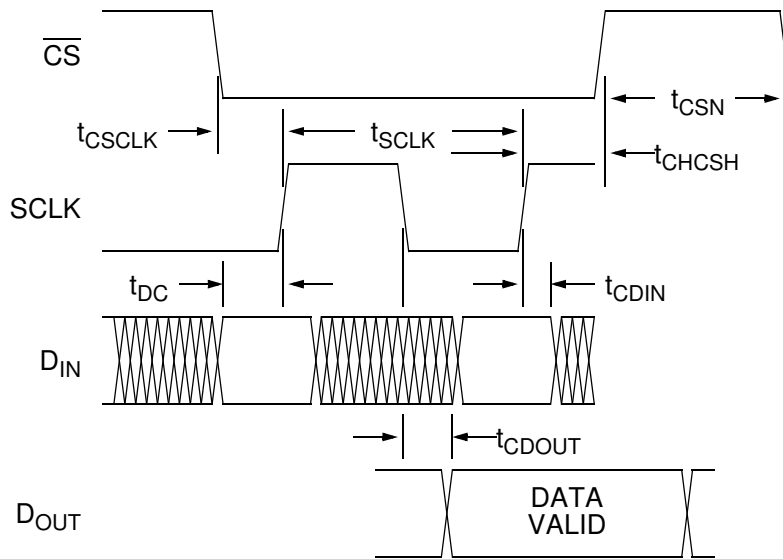


Figure 2-4 Serial Interface Timing

SECTION 3 INTERNAL MODULES

3.1 ONE-TIME PROGRAMMABLE DATA ARRAY

A 400-bit programmable data array allows each device to be customized. The array interface incorporates parity circuitry for fault detection along with a locking mechanism to prevent unintended changes. Portions of the array are reserved for factory-programmed trim values. Customer accessible data stored in the array are shown in the table below.

Addresses \$00 - \$0D are associated with the programmable data array. A writable register at address \$0E is provided for device control operations. Two read-only registers at addresses \$0F and \$10 provide status information.

Unused bits within the data array are always read as '0' values. Unprogrammed OTP bits are also read as '0' values.

Table 3-1 Customer Accessible Data

| Location | | Bit Function | | | | | | | | Type |
|----------|----------|--------------------|----------|----------|----------|----------|----------|----------|----------|------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| \$00 | SN0 | SN[7] | SN[6] | SN[5] | SN[4] | SN[3] | SN[2] | SN[1] | SN[0] | F |
| \$01 | SN1 | SN[15] | SN[14] | SN[13] | SN[12] | SN[11] | SN[10] | SN[9] | SN[8] | |
| \$02 | SN2 | SN[23] | SN[22] | SN[21] | SN[20] | SN[19] | SN[18] | SN[17] | SN[16] | |
| \$03 | SN3 | SN[31] | SN[30] | SN[29] | SN[28] | SN[27] | SN[26] | SN[25] | SN[24] | |
| \$04 | DEVCFG0 | Factory Programmed | | | | | | | | |
| \$05 | DEVCFG1 | Factory Programmed | | | | | | | | |
| \$06 | DEVCFG2 | Factory Programmed | | | | | | | | |
| \$07 | DEVCFG3 | Factory Programmed | | | | | | | | |
| \$08 | DEVCFG4 | Factory Programmed | | | | | | | | |
| \$09 | DEVCFG5 | LOCK2 | PAR2 | COMP1 | COMP0 | SPARE | DACEN | AD3 | AD2 | |
| \$0A | AXCFG_X | RNG_X[2] | RNG_X[1] | RNG_X[0] | LPF_X[4] | LPF_X[3] | LPF_X[2] | LPF_X[1] | LPF_X[0] | |
| \$0B | AXCFG_Y | RNG_Y[2] | RNG_Y[1] | RNG_Y[0] | LPF_Y[4] | LPF_Y[3] | LPF_Y[2] | LPF_Y[1] | LPF_Y[0] | |
| \$0C | | Unused | | | | | | | | N/A |
| \$0E | DEVCTL | RES_1 | RES_0 | CE | Reserved | HPFB | YINV | ST1 | ST0 | R/W |
| \$0D | DSPCFG | SPARE | SPARE | INTERP | OVL D | SD | HPFD | HPFSEL | OFMON | F |
| \$0F | TEMP | TEMP[7] | TEMP[6] | TEMP[5] | TEMP[4] | TEMP[3] | TEMP[2] | TEMP[1] | TEMP[0] | R |
| \$10 | DEVSTAT | IDE | OSCF | DEVINIT | TF | HPF | OFF_Y | OFF_X | DEVRES | |
| \$11 | COUNT | COUNT[7] | COUNT[6] | COUNT[5] | COUNT[4] | COUNT[3] | COUNT[2] | COUNT[1] | COUNT[0] | |

Type codes

F: Factory programmed OTP location

R: Read-only register

R/W: Read/write register

N/A: Not applicable

3.1.1 DEVICE CONTROL REGISTER (DEVCTL)

A read-write register at address \$0E supports a number of device control operations as described below. Reserved bits within DEVCTL are always read as logic '0' values.

Table 3-2 Device Control Register

| Address | Register | Bit | | | | | | | |
|---------|----------|------|------|----|----------|------|------|-----|-----|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$0E | DEVCTL | RES1 | RES0 | CE | Reserved | HPFB | YINV | ST1 | ST0 |

3.1.1.1 Reset Control (RES_1, RES_0)

A specific series of three write operations involving these two bits will cause the internal digital circuitry to be reset. The state of the remaining bits in the DEVCTL register do not affect the reset sequence, however any write operation involving this register in which both RES_1 and RES_0 are cleared will terminate the sequence.

To reset the internal digital circuitry, the following register write operations must be performed in the order shown:

1. Set RES1. RES0 must remain cleared.
2. Set RES1 and RES0.
3. Clear RES1 and set RES0.

RES1 and RES0 are always read as logic '0' values. After reset sequence has been completed DEVCTL register will read 0X00. It should be noted that after a reset or power-cycle sequence is completed the DEVCTL register reset to the value 0X00.

3.1.1.2 Clear Error (CE)

Setting this bit to a logic '1' state will clear transient error status conditions. It is necessary to either set this bit or perform a device reset if an error condition has been reported by the device before acceleration data transfer can be resumed. The device reset condition may be cleared only after device initialization has completed.

Error conditions and classification are described in [Section 4.2](#).

The state of this bit is always read as logic '0'.

3.1.1.3 High-Pass Filter Bypass (HPFB)

Setting this bit will remove the high-pass filter from the signal chain within the DSP block. The state of this bit is indicated when DEVCTL is read. This bit is always cleared following reset.

The state of the high-pass filter is frozen when this bit is at a logic '1' level.

3.1.1.4 Self-Test Control (ST1, ST0)

Bidirectional self-test control is provided through manipulation of these bits. ST1 controls direction while ST0 enables and disables the self-test circuitry. ST1 and ST0 are always cleared following internal reset. When ST0 is set, the high-pass filter is bypassed and the values within the high-pass filter are frozen. Both axes are affected simultaneously by the state of these bits. If the offset monitor is enabled, self-test activation in a single direction should be limited to less than 30 ms.

The state of the ST0 bit is indicated as part of all acceleration results.

3.1.1.5 Y-Axis Signal Inversion Control (YINV)

This control function is provided as a means to verify operation of the two-channel multiplexor which alternately provides X-axis and Y-axis data to the DSP. An inverter block and multiplexor at the Y-axis input to the DSP are controlled by the YINV bit. Setting this bit when ST0 is set has the effect of changing the sign of acceleration in the Y-axis. Operation of the YINV bit is illustrated in [Figure 3-1](#) below. Y-axis inversion may be selected only during self-test; the state of this bit has no effect when ST0 is cleared.

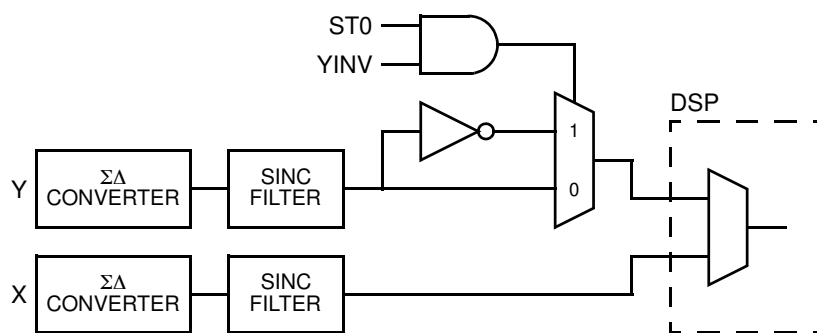


Figure 3-1 Y-Axis Inversion Function

Self-test operations controlled by YINV along with ST1 and ST0 are summarized in the following table.

Table 3-3 Self-Test Control Operations

| YINV | ST1 | ST0 | Self-Test Operation | |
|------|-----|-----|--|---------------------|
| | | | X-Axis | Y-Axis |
| X | X | 0 | Self Test Disabled, Y-Axis Signal Inversion Disabled | |
| 0 | 0 | 1 | Positive Deflection | |
| 0 | 1 | 1 | Negative Deflection | |
| 1 | 0 | 1 | Positive Deflection | Negative Deflection |
| 1 | 1 | 1 | Negative Deflection | Positive Deflection |

NOTE:

Offset correction is applied within the DSP, and is not affected by the state of the YINV bit. Consequently, inversion of the Y-axis signal may result in saturation of the Y-axis output value.

Correct operation of the DSP input multiplexor may be confirmed by performing the operations shown in [Figure 3-2](#).

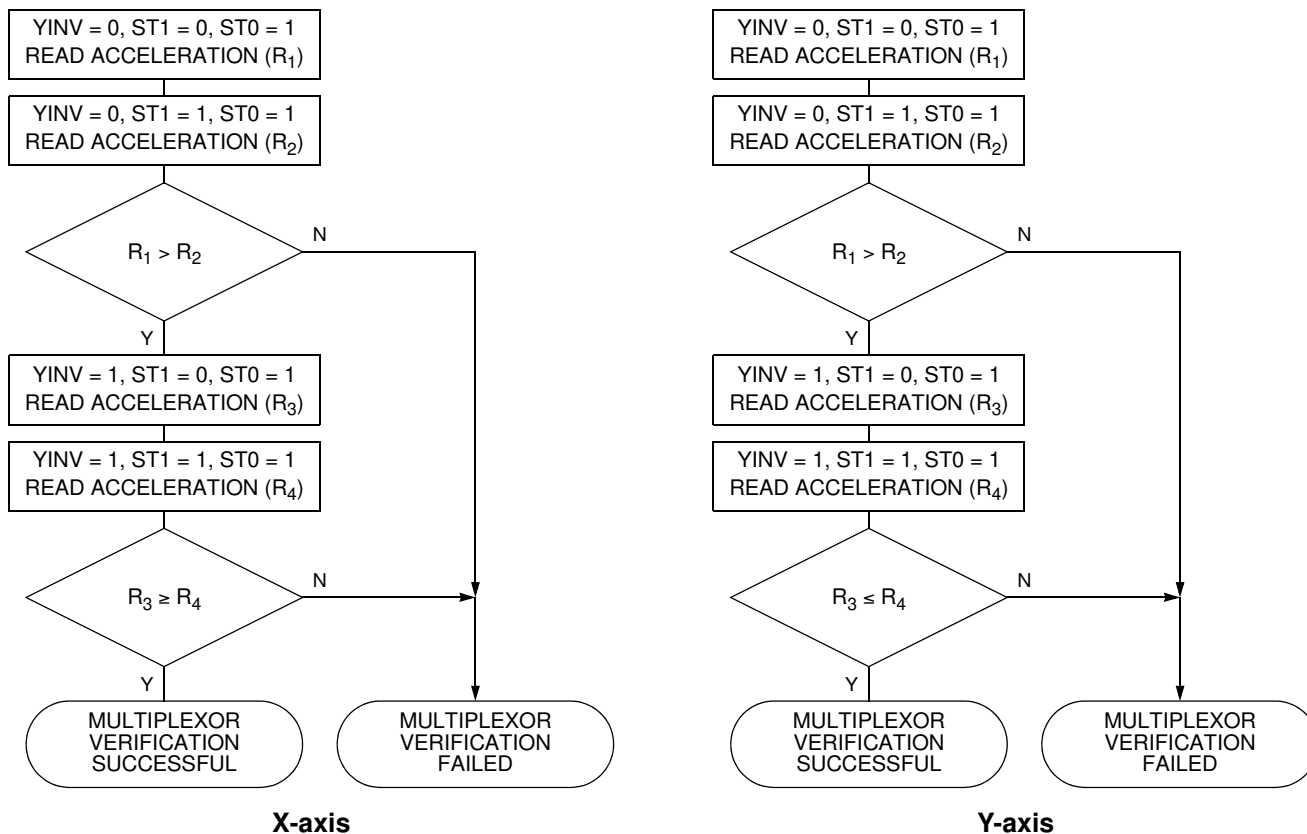


Figure 3-2 DSP Input Multiplexor Verification Flow Chart

3.1.2 Temperature Sensor Value (TEMP)

This read-only register contains a signed value which provides a relative temperature indication. The temperature sensor is uncalibrated and its output for a given temperature will vary from one device to the next. The value in this register increases with temperature.

Table 3-4 Temperature Sensor Value Register

| Location | | Bit Function | | | | | | | |
|----------|----------|--------------|---------|---------|---------|---------|---------|---------|---------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$0F | TEMP | TEMP[7] | TEMP[6] | TEMP[5] | TEMP[4] | TEMP[3] | TEMP[2] | TEMP[1] | TEMP[0] |

3.1.3 Device Status Register (DEVSTAT)

This read-only register is accessible in all modes.

Table 3-5 Device Status Register

| Location | | Bit Function | | | | | | | |
|----------|----------|--------------|------|---------|----|-----|-------|-------|--------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$10 | DEVSTAT | IDE | OSCF | DEVINIT | TF | HPF | OFF_Y | OFF_X | DEVRES |

3.1.3.1 Internal Data Error Flag (IDE)

This flag will be set if a register data parity fault or a marginally programmed fuse is detected. Device reset is required to clear this fault condition. If a parity error is associated with the data stored in the fuse array, this fault condition cannot be cleared. This flag is disabled when the device is in test mode.

3.1.3.2 Oscillator Fault Flag (OCSF)

This flag will be set if the primary oscillator and reference oscillator frequencies vary by an amount greater than the specified tolerance. In normal operating mode, an oscillator fault condition will result in D_{OUT} being driven high when \overline{CS} is asserted.

3.1.3.3 Device Initialization Flag (DEVINIT)

This flag is set during the interval between negation of internal reset and completion of device initialization. DEVINIT is cleared automatically.

3.1.3.4 Temperature Fault Flag (TF)

This flag is set if the value reported by the on-chip temperature sensor exceeds specified limits. TF may be cleared by writing a logic '1' value to the CE bit in DEVCTL, provided that the fault condition is no longer detected.

3.1.3.5 High-Pass Filter Status (HPF)

This bit is set when a high-pass filter is present in the DSP signal chain when the HPFB bit has been set.

3.1.3.6 Y-Axis Offset Error Flag (OFF_Y)

3.1.3.7 X-Axis Offset Error Flag (OFF_X)

The offset error flags are set if the associated signal reaches the specified offset limit. These flags may be cleared by writing a logic '1' value to the CE bit in DEVCTL. Offset faults are not reported for 1.5 seconds following reset.

3.1.3.8 Device Reset Flag (DEVRES)

This flag is set during device initialization. A logic '1' must be written to the CE bit in the Device Control register (DEVCTL) to clear this bit.

3.1.4 Counter Register (COUNT)

This read-only register provides the value of a free-running 8-bit counter derived from the primary oscillator. A five-bit prescaler divides the 4 MHz primary oscillator frequency by 32. Thus, the value in the register increases by one count every 8 μ s, and the counter rolls over every 2.048 ms.

Table 3-6 Counter Register

| Location | | Bit Function | | | | | | | |
|----------|----------|--------------|----------|----------|----------|----------|----------|----------|----------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$11 | COUNT | COUNT[7] | COUNT[6] | COUNT[5] | COUNT[4] | COUNT[3] | COUNT[2] | COUNT[1] | COUNT[0] |

SECTION 4 SERIAL COMMUNICATIONS

Digital data communication with MMA62XXEG is completed through synchronous serial transfers via the SPI port. Conventional SPI protocol is employed, with MMA62XXEG acting as a slave device observing CPOL = 0, CPHA = 0, MSB first. A number of data integrity features are incorporated into the transfer protocol.

4.1 SPI PROTOCOL

4.1.1 Overview

Each transfer is completed through a sequence of two operations, termed phases. During the first phase, the type of transfer and associated control information is transmitted from the SPI master to MMA62XXEG. Data from MMA62XXEG is transmitted during the second phase. Single-level queuing is employed as illustrated in Figure 4-1.

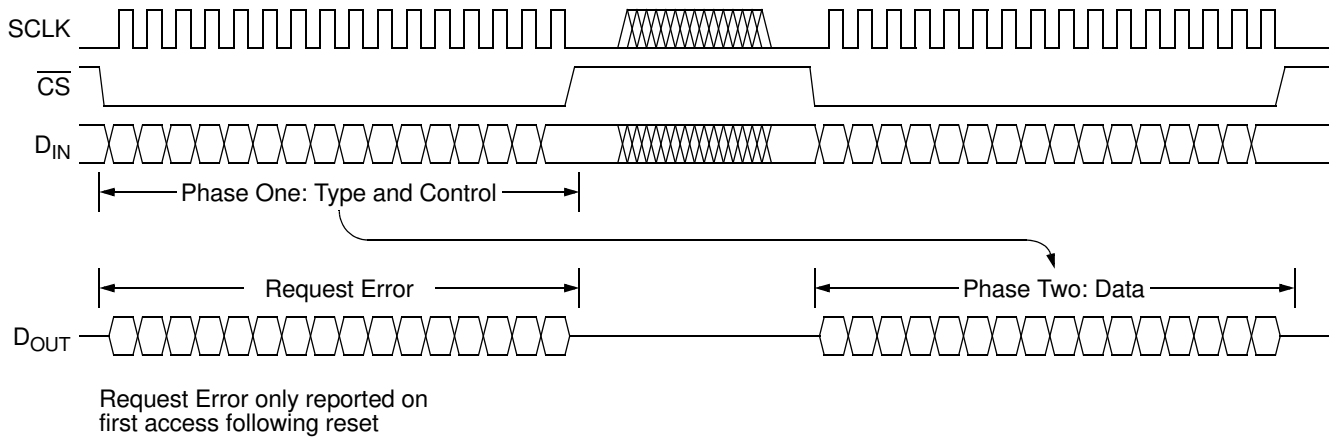


Figure 4-1 Transfer Phase Detail

Any activity on DIN or SCLK is ignored when CS is negated. Consequently, intermediate transfers involving other SPI devices may occur between Phase One and Phase Two.

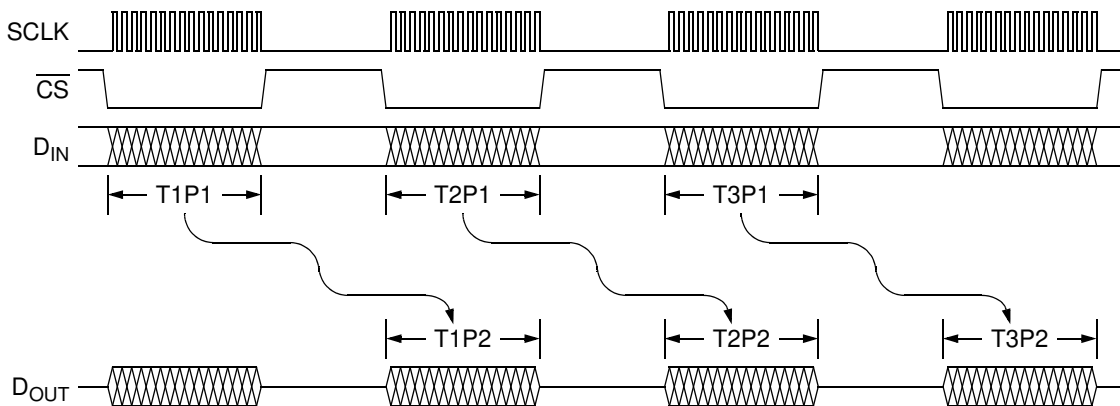


Figure 4-2 Single-Level Communications Queuing Detail

The first data transmitted by MMA62XXEG following reset is the Request Error message shown below. This occurs because MMA62XXEG transmits during Phase Two and there is no corresponding Phase One for the first transfer.

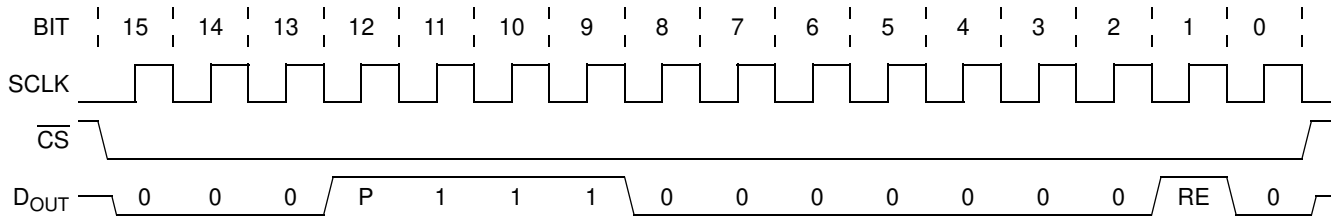


Figure 4-3 Request Error Frame

4.1.2 Command Format

The following abbreviations are used in the following figures.

| Bit Name | Description | Bit Address | |
|----------|-----------------------------|-----------------|------------------|
| | | D _{IN} | D _{OUT} |
| A[4:0] | Register address | 12:8 | 12:8 |
| D[9:0] | 10-bit acceleration data | N/A | 9:0 |
| Acc | Acceleration data indicator | 13 | 13 |
| AXIS | Axis specifier | 14 | 14 |
| P | Parity | N/A | 12 |
| S[1:0] | Status | N/A | 11:10 |

Commands are transferred from the SPI master to MMA62XXEG. Commands fall into three categories: acceleration data requests, register operations and device test. Acceleration data requests are initiated when bit 13 from the master is set to a logic '1' state. Register operations and device test are when bit 13 is set to logic '0' and are further distinguished by the states of bits 15 and 14.

4.1.3 Acceleration Data Transfers

Acceleration data requests are initiated when bit 15 from the master is set to a logic '0' state and bit 13 is set to a logic '1' state. The axis associated with the acceleration to be transferred is determined by D_{IN} bit 14.

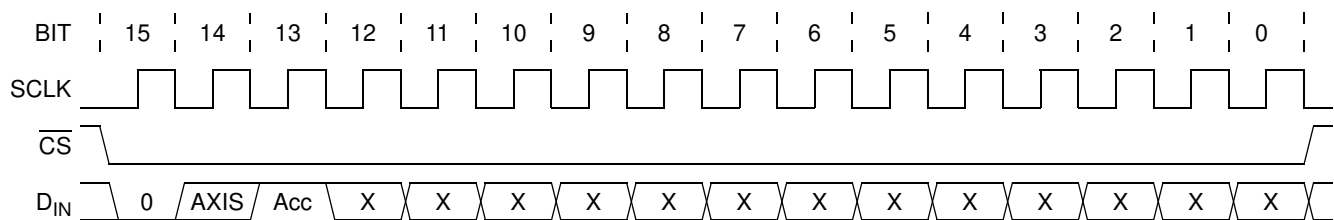


Figure 4-4 Acceleration Command Format

Acceleration data is returned as illustrated below. In addition to the acceleration value, the axis associated with the measurement is indicated in bit 13, while bits 11 and 10 provide status information.

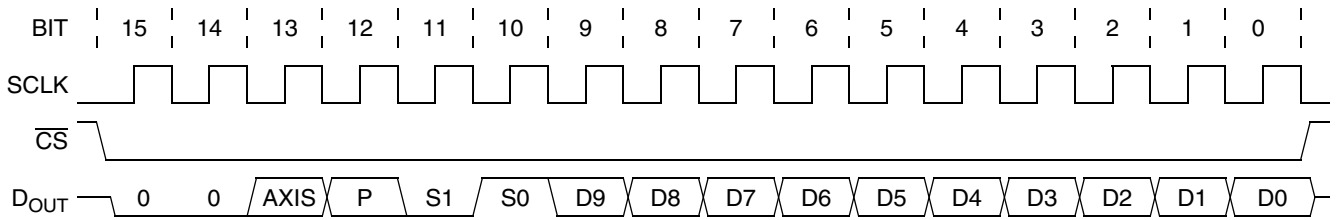


Figure 4-5 Acceleration Command Response

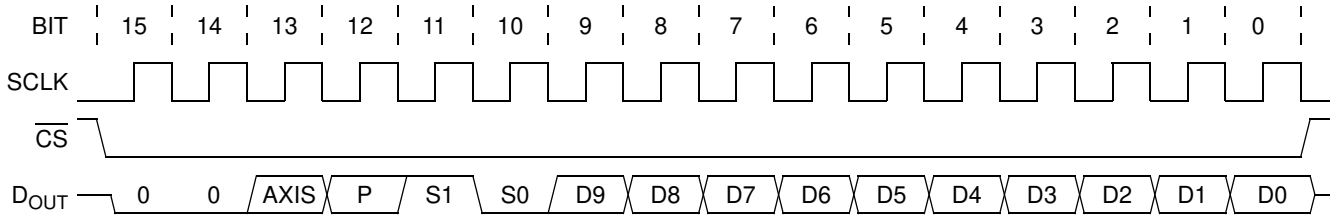


Figure 4-6 Acceleration Command Response, Self-Test Active

4.1.4 AXIS Bit

Bit 13 indicates the axis associated with acceleration data, as shown below.

Table 4-1 AXIS Bit Definitions

| AXIS | Selected Axis |
|------|---------------|
| 0 | X |
| 1 | Y |

4.1.5 Status Bits

Data bits 11 and 10 convey additional information regarding the acceleration data being transmitted. If an error condition is indicated, bits D9 through D0 contain flags which further describe the nature of the error.

Table 4-2 STATUS Bit Definitions

| Status Bit | | Definition |
|------------|----|-------------------|
| S1 | S0 | |
| 0 | 0 | Not Applicable |
| 0 | 1 | Acceleration Data |
| 1 | 0 | Self-test Data |
| 1 | 1 | Error |

The combination S1 = 0, S0 = 0 is never transmitted by MMA62XXEG in response to an acceleration data command.

4.1.6 Acceleration Response Error Status

Several error conditions may be detected and reported in response to an acceleration data command.

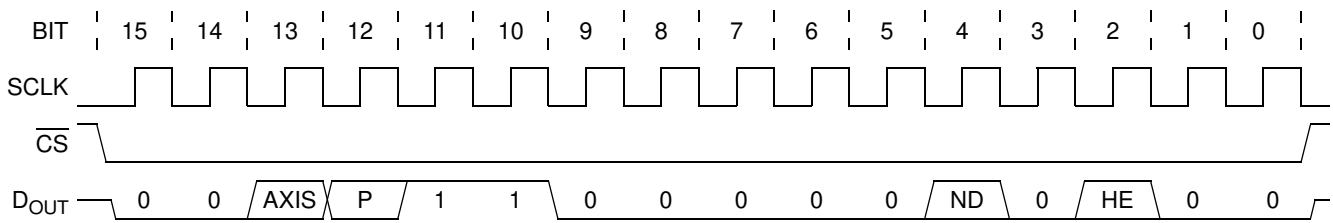


Figure 4-7 ND/HE Error Frame

4.1.6.1 ND - No Data Available

Bit 4 will be set to indicate a “No Data” condition if acceleration data is requested while the device is undergoing device initialization following reset. To ensure that an unexpected device reset will always be detectable regardless of the interval at which the sensor is accessed, “No Data” status will be returned in response to the first acceleration data request following device initialization.

4.1.6.2 HE - Hardware Error

A fault has been detected within the MMA62XXEG device. Detectable fault conditions are listed below

- Device over-temperature
- Offset error
- Internal parity error

Specific error conditions are indicated in the device status register. The contents of this register are returned in response to a device test operation, as described in Section 4.1.10. Oscillator fault status will be reported only if the internal oscillator is functional but frequency comparison between the primary and reference oscillators fails. If an oscillator fault condition exists, the device will respond as described in Section 4.2.2.2.

4.1.6.3 CNC - Conditions Not Correct

Acceleration data will not be provided when bit 15 of command is detected as logic ‘1’. The response to such requests is illustrated below. Should a No Data Available or Hardware Error condition also exist, it will be reported as well.

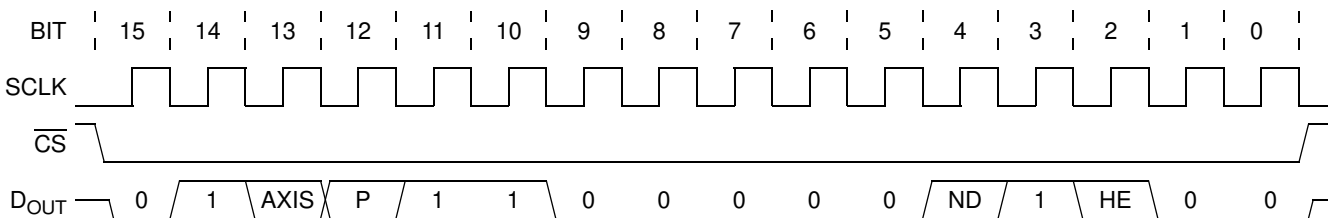


Figure 4-8 CNC Error Frame

4.1.7 Non-Acceleration Transfers

Three different types of non-acceleration transfers are supported; register write, register read and device test. Non-acceleration data transfers are initiated when bit 13 from the master is set to a logic ‘0’ state. The operation to be performed is indicated by bits 15 and 14.

Table 4-3 Non-Acceleration Operations

| Bit 15 | Bit 14 | Operation |
|--------|--------|----------------|
| 0 | 0 | Unused |
| 0 | 1 | Register Write |
| 1 | 0 | Register Read |
| 1 | 1 | Device Test |

Non-acceleration transfers will always succeed except in the case of oscillator fault, SPI error or request error conditions. Only oscillator failure, SPI error or request error conditions are reported in response to non-acceleration commands. Other error conditions are reported as hardware errors in response to acceleration data requests.

4.1.8 Register Write Operations

Register write operations are initiated when bits 15 and 13 from the master is set to a logic '0' and bit 14 is set to a logic '1'. Bits 12 through 8 contain a five-bit address, while the last eight bits contain the data value to be written. Only the DEVCTL register is writable. If an attempt is made to write to any register other than DEVCTL, a request error response (see Figure 4-15) will occur.

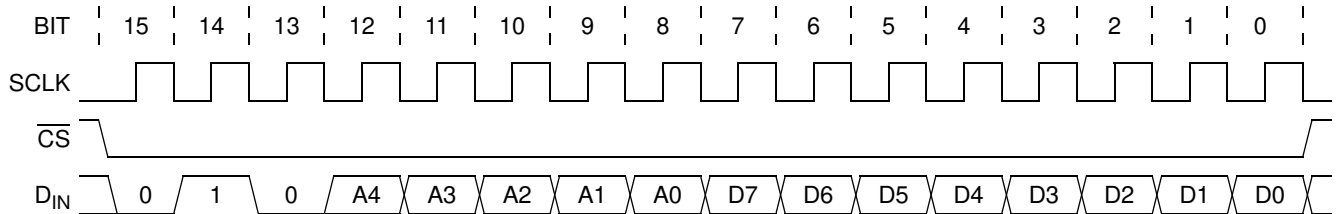


Figure 4-9 Register Write Command

Response to a register write operation is illustrated below. DEVCTL bits which can be read as logic '1' (HPFB, ST1 and ST0) will be indicated during the last eight clock cycles, as shown.

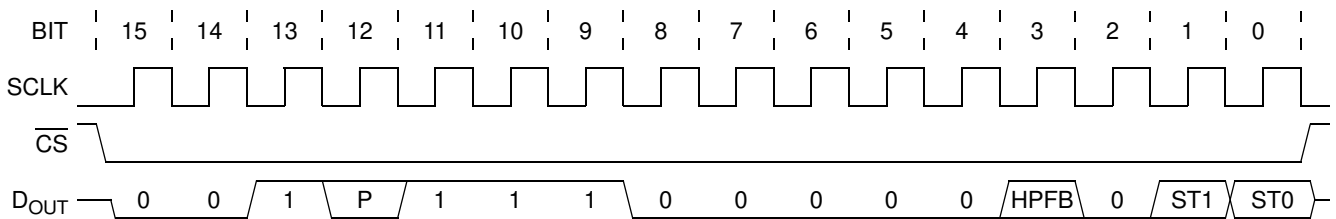


Figure 4-10 Register Write Command Response

4.1.9 Register Read Operations

Register read operations are initiated when bit 15 from the master is set to a logic '1' state and bits 14 and 13 are driven to a logic low level. The address of the register to be accessed is contained in bits 12 through 8. D_{IN} bits 7 through 0 are ignored by MMA62XXEG during register read command transfers.

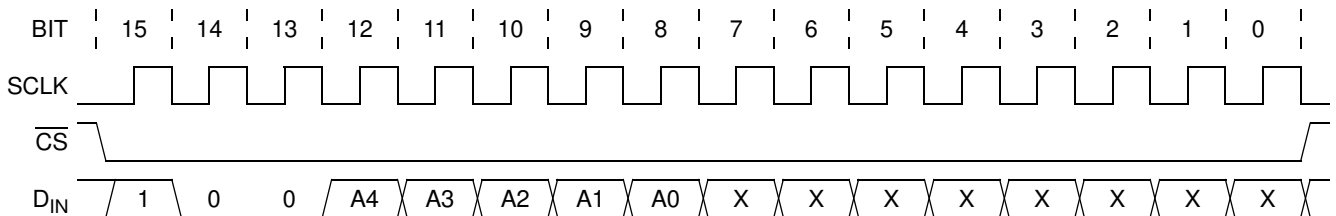


Figure 4-11 Register Read Command

Data read from the selected register is returned in bits 7 through 0, as shown below.

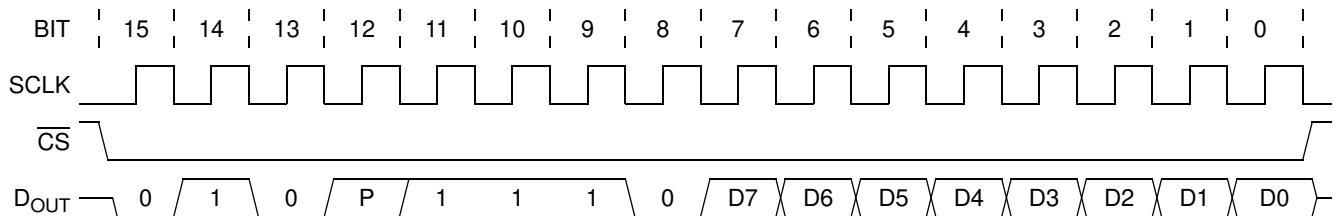


Figure 4-12 Register Read Command Response

4.1.10 Device Test Operation

A device test operation is conducted when D_{IN} bits 15 and 14 are at a logic high level and bit 13 is driven to a logic low level.

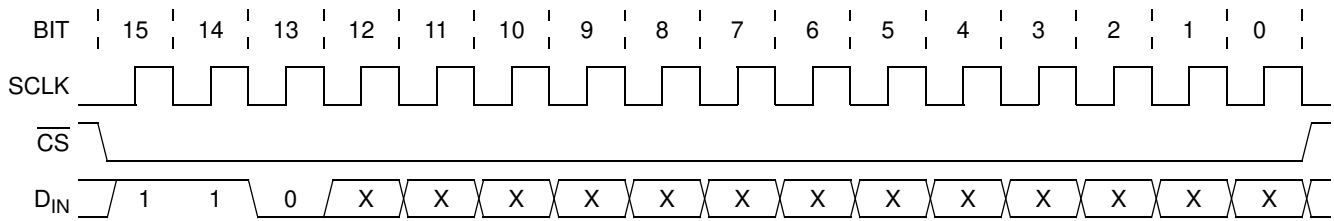


Figure 4-13 Device Test Command

The content of the device status register are transmitted in bits D7 through D0 in response to a device test operation. Refer to [Section 3.1.3](#) for details regarding the device status register

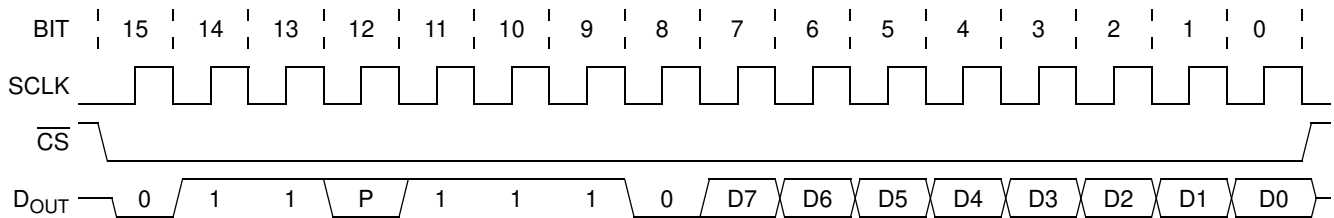


Figure 4-14 Device Test Command Response

Status register bit 0 is set following any device reset. This bit will remain set until explicitly cleared by writing the CE bit in the device control register, as described in [Section 3.1.1](#).

4.1.11 Non-Acceleration Request Error

An error condition is indicated if a non-acceleration command is detected and D_{IN} bits 15 and 14 are both zero, as no operation is specified for this combination.

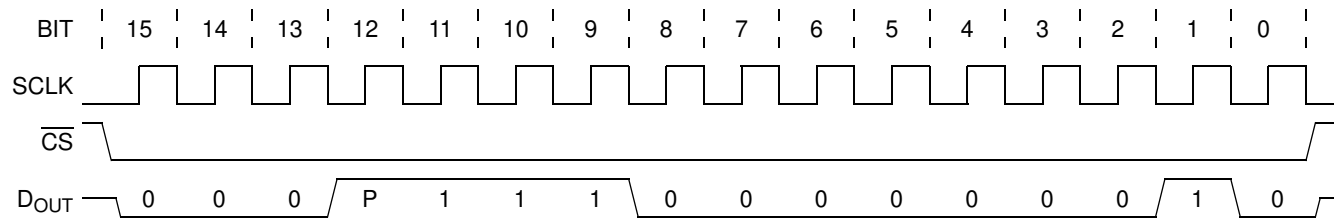


Figure 4-15 Non-Acceleration Request Error

4.1.12 SPI Error Response

The following conditions detected at D_{IN} will result in a SPI error. Since the error condition likely indicate a corrupted transfer, the response frame is the same regardless of the state of bit 13 at D_{IN} .

- SCLK high when \overline{CS} asserted
- Fewer than 16 rising edges of SCLK detected while \overline{CS} is asserted
- Greater than 16 rising edges of SCLK detected while \overline{CS} is asserted
- SCLK high when \overline{CS} negated

The response to a SPI error condition is shown below.

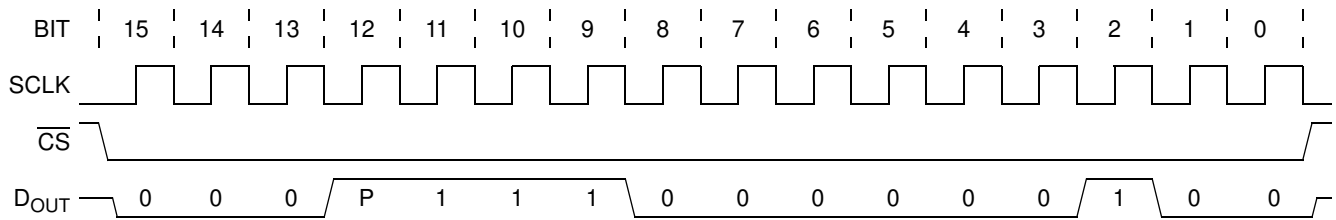


Figure 4-16 SPI Error Response

4.1.13 Initial Response

During initialization phase one, the device does not respond to SPI access attempts. During the second initialization phase, register operations complete normally, however the device will respond to sensor data requests with No Data (ND) status. The first acceleration request following completion of device initialization will also result in a No Data response. This ensures that an unexpected reset will always be detectable, even in systems which poll the device at longer intervals than required for device initialization.

4.2 ERROR CONDITIONS

A number of error conditions may be detected. If an error condition is detected, MMA62XXEG will always transmit an error indicator in place of acceleration data. Error indicators are defined in the following sections.

4.2.1 Error Condition Classification

Error conditions fall into five classes, as described below.

4.2.1.1 Critical Errors

Error condition affects device operation. Critical errors are always reported regardless of other error conditions which may be detected.

4.2.1.2 Initialization

Initialization is a special case condition which occurs after reset until internal circuitry is ready to provide accurate acceleration results. The duration of the initialization period depends upon whether a high-pass filter has been selected or not. If no high-pass filter has been selected, initialization requires approximately 3 ms after power-up. If a high-pass filter has been selected, an additional 200 ms is required. During the device initialization period, this status is reported in response to any acceleration data request, however normal register access operations may be performed.

Device initialization status is cleared automatically.

4.2.1.3 Reset

Reset is also a special case condition. Reset will occur at power-on, as the result of a temporary undervoltage condition, or in response to explicit actions taken by the controller. Upon negation of the internal reset signal, the DEVRES flag in the device status (DEVSTAT) register is set. Because it is critically important that the system can detect any unintended reset condition, this flag may only be cleared by writing a logic '1' to the CE bit in the device control register (DEVCTL) after device initialization has completed.

4.2.1.4 Transient Errors

An error condition which may be the result of a condition which precludes an accurate acceleration measurement but which may not persist. Transient errors are reported in response to acceleration data transfer requests. If a transient error condition has been detected, a logic '1' may be written to the clear error (CE) bit in the device control (DEVCTL) register to clear the associated flag. Should the error condition still exist, the flag will only be cleared momentarily.