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Document Number: MMA685x
Rev 4, 12/2011

RoHS

Single-Axis SPI Inertial Sensor

MMA685x is a SPI-based, single-axis, medium-g, over-damped lateral accelerometer designed for use in automotive airbag systems.

Features

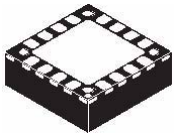
- ±20g to ±120g full-scale range
- 3.3V or 5V single supply operation
- SPI-compatible serial interface
- 10-bit digital signed or unsigned SPI data output
- Programmable arming functions
- 12 low-pass filter options, ranging from 50 Hz to 1000 Hz
- Optional offset cancellation with > 6s averaging period and < 0.25 LSB/s slew rate
- Pb-Free 16-Pin QFN-6 by 6 Package

Referenced Documents

- AECQ100, Revision G, dated May 14, 2007 (http://www.aecouncil.com/)

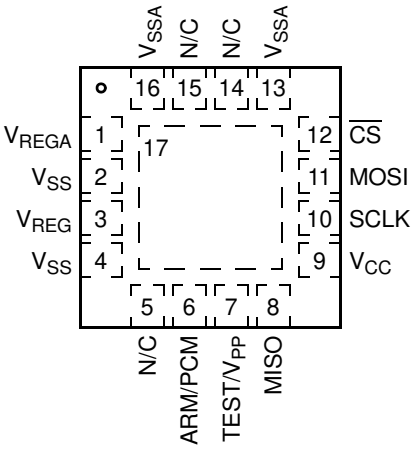
MMA685x

Bottom View



16 LEAD QFN
6 mm by 6 mm
CASE 2086-01

Top View



Pin Connections

ORDERING INFORMATION			
Device	**Axis**	**Axis Range**	**Shipping**
MMA6851BKW	X	±25g	Tubes
MMA6853BKW	X	±50g	Tubes
MMA6855BKW	X	±120g	Tubes
MMA6856BKW	X	±60g	Tubes
MMA6851BKWR2	X	±25g	Tape & Reel
MMA6853BKWR2	X	±50g	Tape & Reel
MMA6855BKWR2	X	±120g	Tape & Reel
MMA6856BKWR2	X	±60g	Tape & Reel

freescale Xtrinsic

Application Diagram

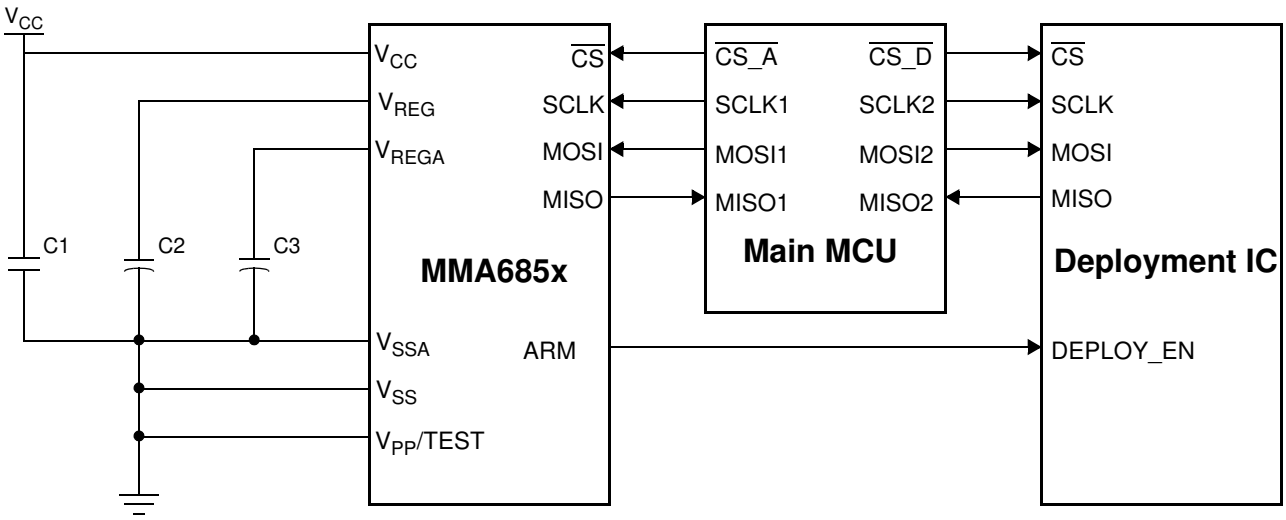


Figure 1. Application Diagram

Table 1. External Component Recommendations

Ref Des	Type	Description	Purpose
C1	Ceramic	0.1 µF, 10%, 10V Minimum, X7R	V_{CC} Power Supply Decoupling
C2	Ceramic	1 µF, 10%, 10V Minimum, X7R	Voltage Regulator Output Capacitor (C_{REG})
C3	Ceramic	1 µF, 10%, 10V Minimum, X7R	Voltage Regulator Output Capacitor (C_{REGA})

Device Orientation

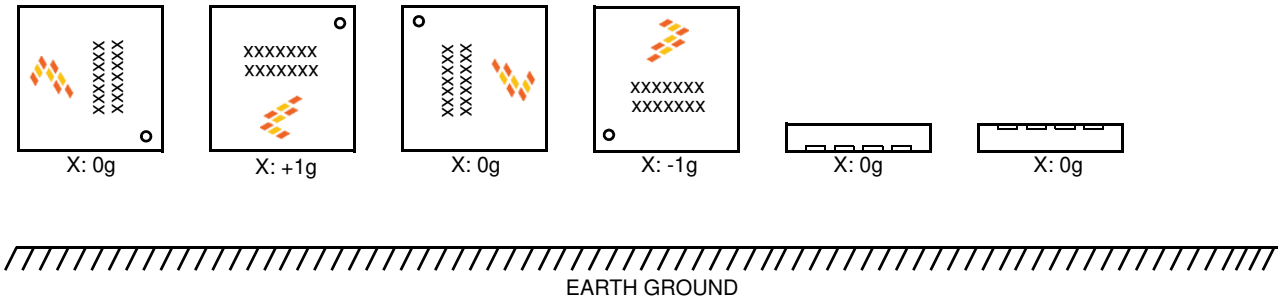


Figure 2. Device Orientation Diagram

Internal Block Diagram

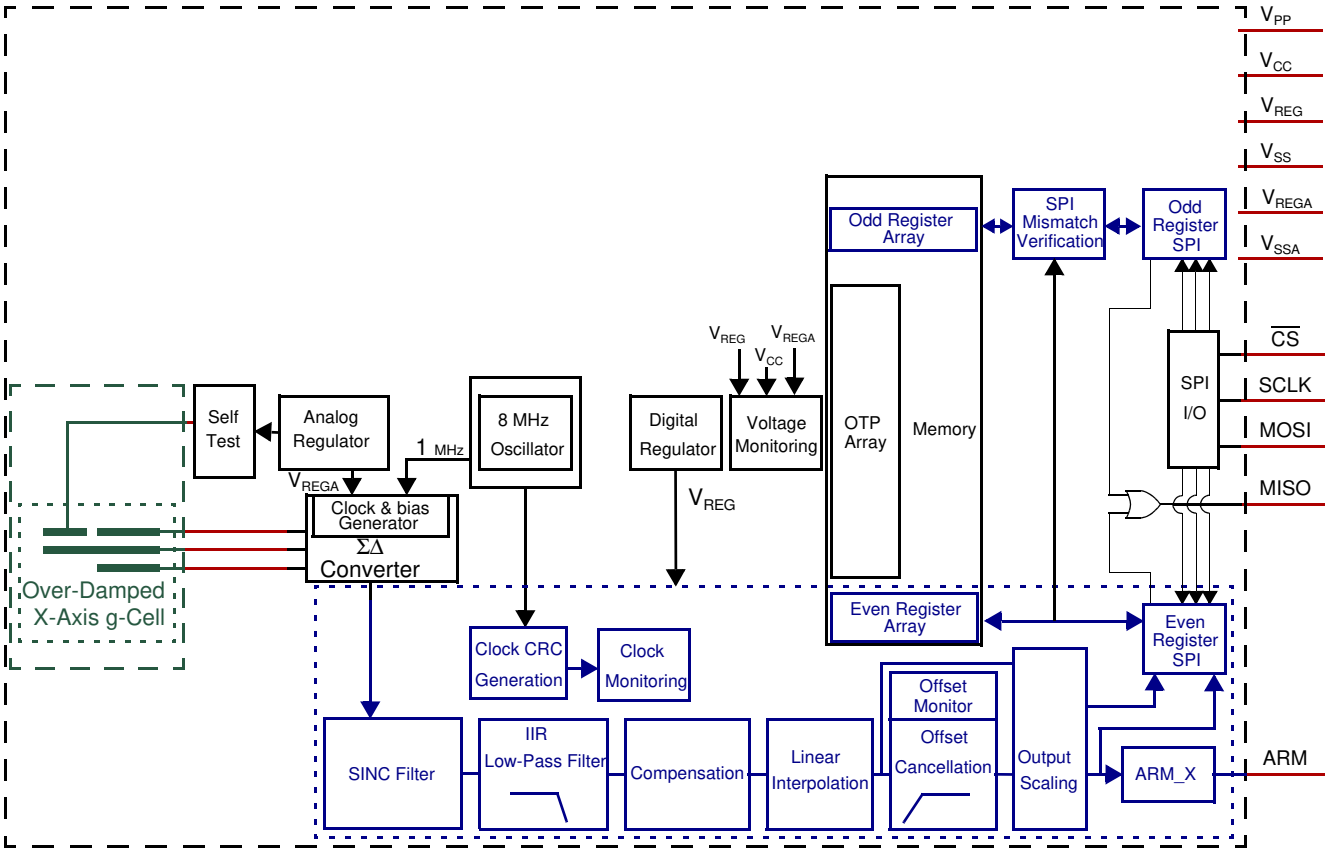


Figure 3. Block Diagram

1 Pin Connections

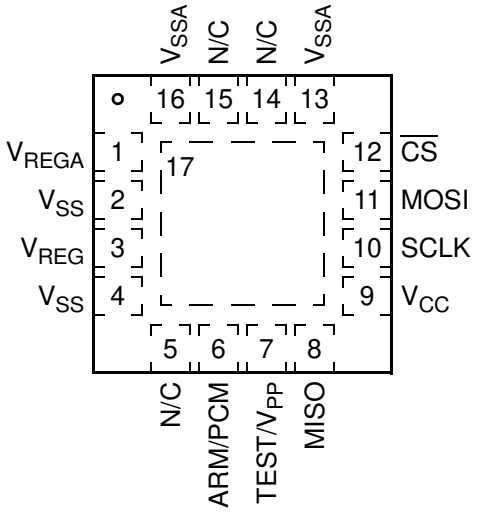


Figure 4. 16-Pin QFN Package, Top View

Table 2. Pin Description

Pin	Pin Name	Formal Name	Definition
1	V_{REGA}	Analog Supply	This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V_{SSA}. Reference Figure 1.
2	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
3	V_{REG}	Digital Supply	This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
4	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
5	N/C	No Connect	No Connection
6	ARM/ PCM	Arm Output / PCM Output	The function of this pin is configurable via the DEVCFG register as described in Section 3.1.6.5. When the arming output is selected, ARM can be configured as an open drain, active low output with a pullup current; or an open drain, active high output with a pulldown current. Alternatively, this pin can be configured as a digital output with a PCM signal proportional to the acceleration data. Reference Section 3.8.9 and Section 3.8.10. If unused, this pin must be left unconnected.
7	TEST/ V_{PP}	Programming Voltage	This pin provides the power for factory programming of the OTP registers. This pin must be connected to V_{SS} in the application.
8	MISO	SPI Data Out	This pin functions as the serial data output for the SPI port.
9	V_{CC}	Supply	This pin supplies power to the device. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
10	SCLK	SPI Clock	This input pin provides the serial clock to the SPI port. An internal pulldown device is connected to this pin.
11	MOSI	SPI Data In	This pin functions as the serial data input to the SPI port. An internal pulldown device is connected to this pin.
12	CS	Chip Select	This input pin provides the chip select for the SPI port. An internal pullup device is connected to this pin.
13	V_{SSA}	Analog GND	This pin is the power supply return node for analog circuitry.
14	N/C	No Connect	No Connection
15	N/C	No Connect	No Connection
16	V_{SSA}	Analog GND	This pin is the power supply return node for analog circuitry.
17	PAD	Die Attach Pad	This pin is the die attach flag, and is internally connected to V_{SS}.
	Corner Pads	Corner Pads	The corner pads are internally connected to V_{SS}.

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	
1	Supply Voltage	V_{CC}	-0.3 to +7.0	V	(3)
2	C_{REG}, C_{REGA}	V_{REG}	-0.3 to +3.0	V	(3)
3	SCLK, $\overline{CS}$, MOSI,V_{PP}/TEST	V_{IN}	-0.3 to V_{CC} + 0.3	V	(3)
4	ARM	V_{IN}	-0.3 to V_{CC} + 0.3	V	(3)
5	MISO (high impedance state)	V_{IN}	-0.3 to V_{CC} + 0.3	V	(3)
6	Acceleration without hitting internal g-cell stops	g_{gcell_Clip}	±500	g	(3, 18)
7	Acceleration without saturation of internal circuitry	g_{ADC_Clip}	±375	g	(3)
8	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±1500	g	(5, 18)
9	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2000	g	(5, 18)
10	Drop Shock (to concrete surface)	h_{DROP}	1.2	m	(5)
	Electrostatic Discharge				
11	Human Body Model (HBM)	V_{ESD}	±2000	V	(5)
12	Charge Device Model (CDM)	V_{ESD}	±750	V	(5)
13	Machine Model (MM)	V_{ESD}	±200	V	(5)
14	Storage Temperature Range	T_{stg}	-40 to +125	°C	(5)
15	Thermal Resistance - Junction to Case	q_{JC}	2.5	°C/W	(14)

2.2 Operating Range

The operating ratings are the limits normally expected in the application and define the range of operation.

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Supply Voltage		V_L	V_{TYP}	V_H		
16	Standard Operating Voltage, 3.3V	V_{CC}	+3.135	+3.3	+5.25	V	(15)
17	Standard Operating Voltage, 5.0V			+5.0		V	(15)
	Operating Ambient Temperature Range		T_L		T_H		
18	Verified by 100% Final Test	T_A	-40	—	+105	C	(1)
20	Power-on Ramp Rate (V_{CC})	V_{CC_r}	0.000033	—	3300	V/µs	(19)

2.3 Electrical Characteristics - Power Supply and I/O

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	
21	Supply Current	*	I_{DD}	3.0	—	7.0	mA	(1)
	Power Supply Monitor Thresholds (See Figure 8)							
22	V_{CC} Undervoltage (Falling)	*	$V_{CC\_UV\_f}$	2.74	—	3.02	V	(3, 6)
23	V_{REG} Undervoltage (Falling)	*	$V_{REG\_UV\_f}$	2.10	—	2.25	V	(3, 6)
24	V_{REG} Overvoltage (Rising)	*	$V_{REG\_OV\_r}$	2.65	—	2.85	V	(3, 6)
25	V_{REGA} Undervoltage (Falling)	*	$V_{REGA\_UV\_f}$	2.20	—	2.35	V	(3, 6)
26	V_{REGA} Overvoltage (Rising)	*	$V_{REGA\_OV\_r}$	2.65	—	2.85	V	(3, 6)
	Power Supply Monitor Hysteresis							
27	V_{CC} Undervoltage (Falling)		V_{HYST}	65	100	110	mV	(3)
28	V_{REG} Undervoltage, V_{REG} Overvoltage		V_{HYST}	20	100	210	mV	(3)
29	V_{REGA} Undervoltage, V_{REGA} Overvoltage		V_{HYST}	20	100	150	mV	(3)
	Power Supply RESET Thresholds (See Figure 5, and Figure 8)							
30	V_{REG} Undervoltage RESET (Falling)	*	$V_{REG\_UVR\_f}$	1.764	—	2.024	V	(3, 6)
31	V_{REG} Undervoltage RESET (Rising)	*	$V_{REG\_UVR\_r}$	1.876	—	2.152	V	(3, 6)
32	V_{REG} RESET Hysteresis		V_{HYST}	80	—	140	mV	(3)
	Internally Regulated Voltages							
33	V_{REG}	*	V_{REG}	2.42	2.50	2.58	V	(1, 3)
34	V_{REGA}	*	V_{REGA}	2.42	2.50	2.58	V	(1, 3)
	External Filter Capacitor (C_{REG}, C_{REGA})							
35	Value		C_{REG}	700	1000	1500	nF	(19)
36	ESR (including interconnect resistance)		ESR	—	—	400	mΩ	(19)
	Power Supply Coupling							
37	50 kHz ≤ f_n ≤ 300 kHz			—	—	0.004	LSB/mv	(19)
38	4 MHz ≤ f_n ≤ 100 MHz			—	—	0.004	LSB/mv	(19)
	Output High Voltage (MISO, PCM)							
39	3.15V ≤ (V_{CC} - V_{SS}) ≤ 3.45V (I_{Load} = -1 mA)	*	V_{OH_3}	V_{CC} - 0.2	—	—	V	(2, 3)
40	4.75V ≤ (V_{CC} - V_{SS}) ≤ 5.25V (I_{Load} = -1 mA)	*	V_{OH_5}	V_{CC} - 0.4	—	—	V	(2, 3)
	Output Low Voltage (MISO, PCM)							
41	3.15V ≤ (V_{CC} - V_{SS}) ≤ 3.45V (I_{Load} = 1 mA)	*	V_{OL_3}	—	—	0.2	V	(2, 3)
42	4.75V ≤ (V_{CC} - V_{SS}) ≤ 5.25V (I_{Load} = 1 mA)	*	V_{OL_5}	—	—	0.4	V	(2, 3)
	Open Drain Output High Voltage (ARM)							
43	3.15V ≤ (V_{CC} - V_{SS}) ≤ 3.45V (I_{ARM} = -1 mA)	*	V_{ODH_3}	V_{CC} - 0.2	—	—	V	(2, 3)
44	4.75V ≤ (V_{CC} - V_{SS}) ≤ 5.25V (I_{ARM} = -1 mA)	*	V_{ODH_5}	V_{CC} - 0.4	—	—	V	(2, 3)
	Open Drain Output Pulldown Current (ARM)							
45	3.15V ≤ (V_{CC} - V_{SS}) ≤ 3.45V (V_{ARM} = 1.5 V)	*	I_{ODPD_3}	50	—	100	µA	(2, 3)
46	4.75V ≤ (V_{CC} - V_{SS}) ≤ 5.25V (V_{ARM} = 1.5 V)	*	I_{ODPD_5}	50	—	100	µA	(2, 3)
	Open Drain Output Low Voltage (ARM)							
47	3.15V ≤ (V_{CC} - V_{SS}) ≤ 3.45V (I_{ARM} = 1 mA)	*	V_{ODH_3}	—	—	0.2	V	(2, 3)
48	4.75V ≤ (V_{CC} - V_{SS}) ≤ 5.25V (I_{ARM} = 1 mA)	*	V_{ODH_5}	—	—	0.4	V	(2, 3)
	Open Drain Output Pullup Current (ARM)							
49	3.15V ≤ (V_{CC} - V_{SS}) ≤ 3.45V (V_{ARM} = 1.5 V)	*	I_{ODPU_3}	-100	—	-50	µA	(2, 3)
50	4.75V ≤ (V_{CC} - V_{SS}) ≤ 5.25V (V_{ARM} = 1.5 V)	*	I_{ODPU_5}	-100	—	-50	µA	(2, 3)
51	Input High Voltage $\overline{CS}$, SCLK, MOSI	*	V_{IH}	2.0	—	—	V	(3, 6)
52	Input Low Voltage $\overline{CS}$, SCLK, MOSI	*	V_{IL}	—	—	1.0	V	(3, 6)
53	Input Voltage Hysteresis $\overline{CS}$, SCLK, MOSI	*	V_{I_HYST}	0.125	—	0.500	V	(19)
	Input Current							
54	High (at V_{IH}) (SCLK, MOSI)	*	I_{IH}	-260	-50	-30	µA	(2, 3)
55	Low (at V_{IL}) ($\overline{CS}$)	*	I_{IL}	30	50	260	µA	(2, 3)

2.4 Electrical Characteristics - Sensor and Signal Chain

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	
	Digital Sensitivity (SPI, 10-Bit Output)							
56	25g (MMA6851)	*	SENS	—	20.479	—	LSB/g	(1, 9)
57	50g (MMA6853)	*	SENS	—	9.766	—	LSB/g	(1, 9)
58	60g (MMA6856)	*	SENS	—	8.192	—	LSB/g	(1, 9)
59	120g (MMA6855)	*	SENS	—	4.096	—	LSB/g	(1, 9)
	Sensitivity Error							
60	T_A = 25°C	*	ΔSENS	-4	—	+4	%	(1)
61	-40°C ≤ T_A ≤ 105°C	*	ΔSENS	-5	—	+5	%	(1)
67	-40°C ≤ T_A ≤ 105°C, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		ΔSENS	-5	—	+5	%	(3)
	Offset at 0g (No Offset Cancellation)							
68	10-Bits, unsigned	*	OFFSET	452	512	572	LSB	(1)
69	10-Bits, signed	*	OFFSET	-60	0	+60	LSB	(1)
70	10-Bits, unsigned, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		OFFSET	452	512	572	LSB	(3)
71	10-Bits, signed, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		OFFSET	-60	0	+60	LSB	(3)
	Offset Monitor Thresholds							
72	Positive Threshold (10-Bits, unsigned)		$OFFTHR_{POS}$	—	612	—	LSB	(7)
73	Negative Threshold (10-Bits, unsigned)		$OFFTHR_{NEG}$	—	412	—	LSB	(7)
	Range of Output (SPI, 10-Bits, unsigned)							
74	Normal		RANGE	32	—	992	LSB	(7)
75	Fault Response Code		FAULT	—	0	—	LSB	(7)
76	Unused Codes		UNUSED	1	—	31	LSB	(7)
77	Unused Codes		UNUSED	993	—	1023	LSB	(7)
	Range of Output (SPI, 10-Bits, signed)							
78	Normal		RANGE	-480	—	480	LSB	(7)
79	Fault Response Code		FAULT	—	-512	—	LSB	(7)
80	Unused Codes		UNUSED	-511	—	-481	LSB	(7)
81	Unused Codes		UNUSED	481	—	511	LSB	(7)
82	Nonlinearity	*	NL_{OUT}	-1	—	1	% FSR	(3)
	System Output Noise							
83	RMS (10-Bit, All Ranges, 400 Hz, 4-pole LPF)		n_{RMS}	—	—	0.5	LSB	(3)
84	Peak to Peak (10-Bit, All Ranges, 400 Hz, 4-pole LPF)		n_{P-P}	—	—	1.0	LSB	(3)
	Cross-Axis Sensitivity							
85	V_{ZX}	*	V_{ZX}	-4	—	+4	%	(3)
86	V_{YX}	*	V_{YX}	-4	—	+4	%	(3)
	Self-Test Output Change (Ref Section 3.6)			ΔST_{MIN}	ΔST_{NOM}	ΔST_{MAX}		
87	STMAG = 0, T_A = 25°C	*	ΔST_{Low25}	11.25	15	18.75	g	(1)
88	STMAG = 0, -40°C ≤ T_A ≤ 105°C	*	ΔST_{Low}	10.68	15	19.69	g	(1)
89	STMAG = 1, T_A = 25°C	*	ΔST_{HI25}	22.5	30	37.5	g	(1)
90	STMAG = 1, -40°C ≤ T_A ≤ 105°C	*	ΔST_{HI}	21.37	30	39.38	g	(1)
91	STMAG = 0, -40°C ≤ T_A ≤ 105°C, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		ΔST_{Low}	10.68	15	19.69	g	(3)
92	STMAG = 1, -40°C ≤ T_A ≤ 105°C, $V_{CC\_UV\_f} \le V_{CC} - V_{SS} \le V_L$		ΔST_{HI}	21.37	30	39.38	g	(3)
	Acceleration (without hitting internal g-cell stops)							
93	Any Range Positive/Negative		$g_{g\text{-}cell\_Clip}$	500	560	600	g	(19)

2.5 Dynamic Electrical Characteristics - Signal Chain

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	
94	DSP Sample Rate (LPF 0,1,2,3,4,5)		t_S	—	$64/f_{OSC}$	—	s	(7)
95	DSP Sample Rate (LPF 8,9,10,11,12,13)		t_S	—	$128/f_{OSC}$	—	s	(7)
96	Interpolation Sample Rate		t_{INTERP}	—	$t_S/2$	—	s	(7)
	Datapath Latency (excluding g-cell and Low Pass Filter)							
97	$T_S = 64/f_{OSC}$	*	$t_{DataPath\_8}$	33.0	34.8	36.5	µs	(7, 16)
98	$T_S = 128/f_{OSC}$	*	$t_{DataPath\_16}$	51.9	54.6	57.4	µs	(7, 16)
	Low-Pass Filter (t_s = 8 µs)							
99	Cutoff frequency 0: 100 Hz, 4-pole	*	$f_{C0(LPF)}$	95	100	105	Hz	(3, 7, 17)
100	Cutoff frequency 1: 300 Hz, 4-pole	*	$f_{C1(LPF)}$	285	300	315	Hz	(7, 17)
101	Cutoff frequency 2: 400 Hz, 4-pole	*	$f_{C2(LPF)}$	380	400	420	Hz	(7, 17)
102	Cutoff frequency 3: 800 Hz, 4-pole	*	$f_{C3(LPF)}$	760	800	840	Hz	(7, 17)
103	Cutoff frequency 4: 1000 Hz, 4-pole	*	$f_{C4(LPF)}$	950	1000	1050	Hz	(7, 17)
104	Cutoff frequency 5: 400 Hz, 3-pole	*	$f_{C5(LPF)}$	380	400	420	Hz	(7, 17)
	Low-Pass Filter (t_s = 16µs)							
105	Cutoff frequency 8: 50 Hz, 4-pole	*	$f_{C8(LPF)}$	47.5	50	52.5	Hz	(7, 17)
106	Cutoff frequency 9: 150 Hz, 4-pole	*	$f_{C9(LPF)}$	142.5	150	157.5	Hz	(7, 17)
107	Cutoff frequency 10: 200 Hz, 4-pole	*	$f_{C10(LPF)}$	190	200	210	Hz	(7, 17)
108	Cutoff frequency 11: 400 Hz, 4-pole	*	$f_{C11(LPF)}$	380	400	420	Hz	(7, 17)
109	Cutoff frequency 12: 500 Hz, 4-pole	*	$f_{C12(LPF)}$	475	500	525	Hz	(7, 17)
110	Cutoff frequency 13: 200 Hz, 3-pole	*	$f_{C13(LPF)}$	190	200	210	Hz	(7, 17)
	Offset Cancellation (Normal Mode, 10-Bit Output)							
111	Offset Averaging Period	*	OFF_{AVEPER}	—	6.291456	—	s	(7)
112	Offset Slew Rate	*	OFF_{SLEW}	—	0.2384	—	LSB/s	(7)
113	Offset Update Rate	*	OFF_{RATE}	—	1049	—	ms	(7)
114	Offset Correction Value per Update Positive	*	OFF_{CORRP}	—	0.25	—	LSB	(7)
115	Offset Correction Value per Update Negative	*	OFF_{CORRN}	—	-0.25	—	LSB	(7)
116	Offset Correction Threshold Positive	*	OFF_{THP}	—	0.125	—	LSB	(7)
117	Offset Correction Threshold Negative	*	OFF_{THN}	—	0.125	—	LSB	(7)
118	Offset Monitor Bypass Time after Self-Test Deactivation		t_{ST_OMB}	—	320	—	t_S	(3, 7)
119	Time Between Acceleration Data Requests		t_{ACC_REQ}	15	—	—	µs	(3, 7, 20)
	Arming Output Activation Time (ARM, I_{ARM} = 200 µA)							
120	Moving Average and Count Arming Modes (2,3,4,5)		t_{ARM}	0	—	1.05	µs	(3, 12)
121	Unfiltered Mode Activation Delay (Reference Figure 28)		$t_{ARM\_UF\_DLY}$	0	—	1.05	µs	(3, 12)
122	Unfiltered Mode Arm Assertion Time (Reference Figure 28)		$t_{ARM\_UF\_ASSERT}$	5.00	—	6.579	µs	(3)
123	Sensing Element Natural Frequency (-40°C ≤ T_A ≤ 105°C)		f_{gcell}	10791	—	15879	Hz	(19)
124	Sensing Element Cutoff Frequency (-3 dB ref. to 0 Hz, -40°C ≤ T_A ≤ 105°C)		f_{gcell}	0.851	—	2.29	kHz	(19)
125	Sensing Element Damping Ratio (-40°C ≤ T_A ≤ 105°C)		ζ_{gcell}	2.46	—	9.36	—	(19)
126	Sensing Element Delay (@100 Hz, -40°C ≤ T_A ≤ 105°C)		f_{gcell_delay}	70	—	187	µs	(19)
127	Package Resonance Frequency		$f_{Package}$	100	—	—	kHz	(19)
128	Package Quality Factor		$q_{Package}$	1	—	5		(19)

2.6 Dynamic Electrical Characteristics - Supply and SPI

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 25$ K/min unless otherwise specified

#	Characteristic		Symbol	Min	Typ	Max	Units	
129	Power-On Recovery Time (VCC = VCCMIN to first SPI access)		t_{OP}	—	—	10	ms	(3)
130	Power-On Recovery Time (Internal POR to first SPI access)		t_{OP}	—	—	840	µs	(3, 7)
131	Internal Oscillator Frequency	*	f_{OSC}	7.6	8	8.4	MHz	(7)
132	Test Frequency - Divided from Internal Oscillator		f_{OSCTST}	0.95	1	1.05	MHz	(1)
	Serial Interface Timing (See Figure 6, $C_{MISO} \le 80$ pF, $R_{MISO} \ge 10$ kΩ)							
133	Clock (SCLK) period (10% of V_{CC} to 10% of V_{CC})	*	t_{SCLK}	120	—	—	ns	(3)
134	Clock (SCLK) high time (90% of V_{CC} to 90% of V_{CC})	*	t_{SCLKH}	40	—	—	ns	(3)
135	Clock (SCLK) low time (10% of V_{CC} to 10% of V_{CC})	*	t_{SCLKL}	40	—	—	ns	(3)
136	Clock (SCLK) rise time (10% of V_{CC} to 90% of V_{CC})		t_{SCLKR}	—	15	40	ns	(19)
137	Clock (SCLK) fall time (90% of V_{CC} to 10% of V_{CC})		t_{SCLKF}	—	15	28	ns	(19)
138	$\overline{CS}$ asserted to SCLK high ($\overline{CS}$ = 10% of V_{CC} to SCLK = 10% of V_{CC})	*	t_{LEAD}	60	—	—	ns	(3)
139	$\overline{CS}$ asserted to MISO valid ($\overline{CS}$ = 10% of V_{CC} to MISO = 10/90% of V_{CC})	*	t_{ACCESS}	—	—	60	ns	(3)
140	Data setup time (MOSI = 10/90% of V_{CC} to SCLK = 10% of V_{CC})	*	t_{SETUP}	20	—	—	ns	(3)
141	MOSI Data hold time (SCLK = 90% of V_{CC} to MOSI = 10/90% of V_{CC})	*	t_{HOLD_IN}	10	—	—	ns	(3)
142	MISO Data hold time (SCLK = 90% of V_{CC} to MISO = 10/90% of V_{CC})	*	t_{HOLD_OUT}	0	—	—	ns	(3)
143	SCLK low to data valid (SCLK = 10% of V_{CC} to MISO = 10/90% of V_{CC})	*	t_{VALID}	—	—	40	ns	(3)
144	SCLK low to $\overline{CS}$ high (SCLK = 10% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	*	t_{LAG}	60	—	—	ns	(3)
145	$\overline{CS}$ high to MISO disable ($\overline{CS}$ = 90% of V_{CC} to MISO = Hi Z)	*	$t_{DISABLE}$	—	—	60	ns	(3)
146	$\overline{CS}$ high to $\overline{CS}$ low ($\overline{CS}$ = 90% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	*	t_{CSN}	526	—	—	ns	(3)
147	SCLK low to $\overline{CS}$ low (SCLK = 10% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	*	t_{CLKCS}	60	—	—	ns	(3)
148	$\overline{CS}$ high to SCLK high ($\overline{CS}$ = 90% of V_{CC} to SCLK = 90% of V_{CC})		t_{CSCLK}	60	—	—	ns	(19)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at wafer probe.
3. Parameters verified by characterization
4. (*) Indicates a critical characteristic.
5. Verified by qualification testing.
6. Parameters verified by pass/fail testing in production.
7. Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
8. N/A
9. Devices are trimmed at 100 Hz with 1000 Hz low-pass filter option selected. Response is corrected to 0 Hz response.
10. Low-pass filter cutoff frequencies shown are -3dB referenced to 0 Hz response.
11. Power supply ripple at frequencies greater than 900 kHz should be minimized to the greatest extent possible.
12. Time from falling edge of $\overline{CS}$ to ARM output valid.
13. N/A
14. Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
15. Device characterized at all values of V_L and V_H. Production test is conducted at all typical voltages (V_{TYP}) unless otherwise noted.
16. Data path Latency is the signal latency from g-cell to SPI output disregarding filter group delays.
17. Filter characteristics are specified independently, and do not include g-cell frequency response.
18. Electrostatic Deflection Test completed during wafer probe.
19. Verified by simulation.
20. Acceleration Data Request timing constraint only applies for proper operation of the Arming Function.

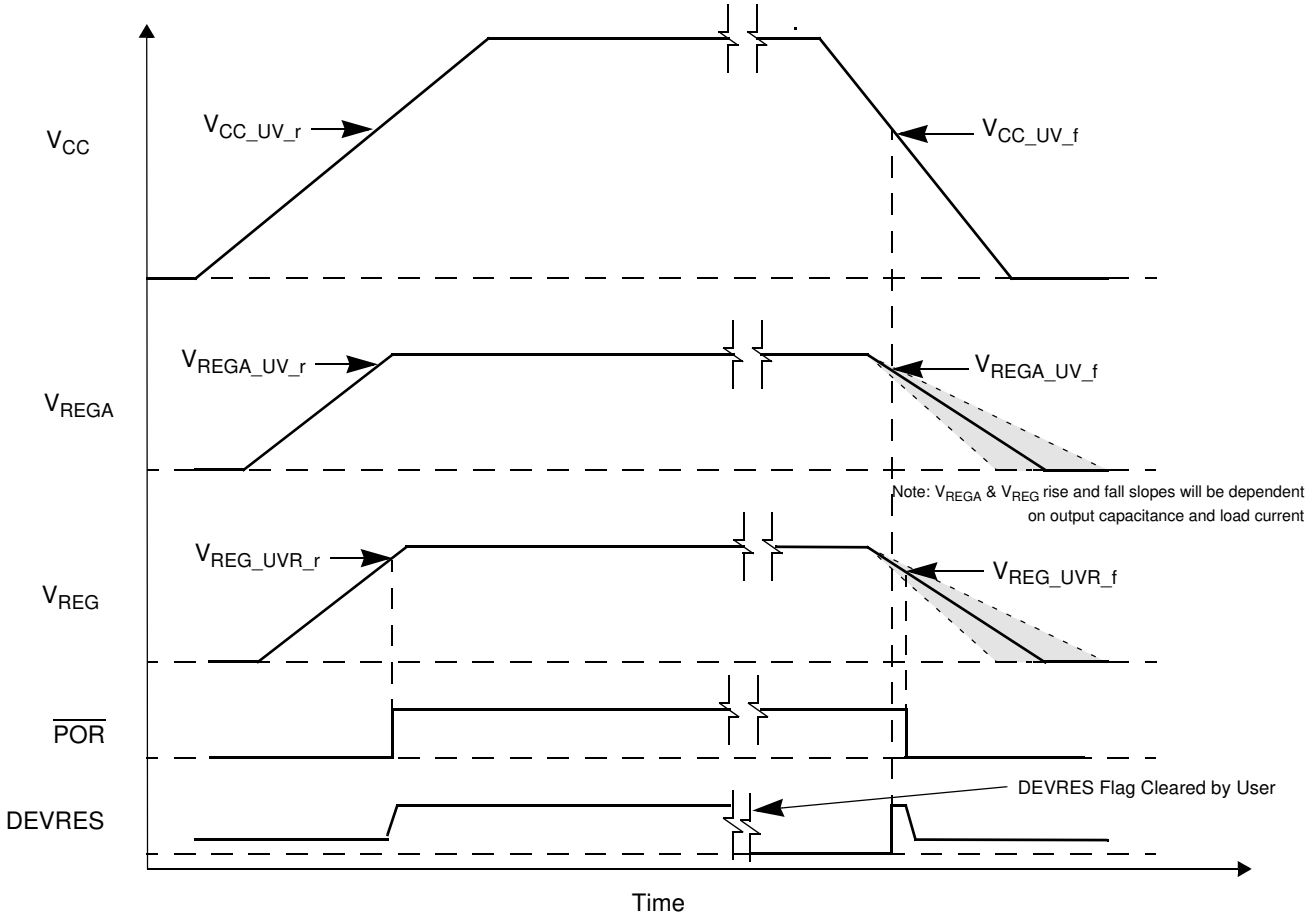


Figure 5. Power-Up Timing

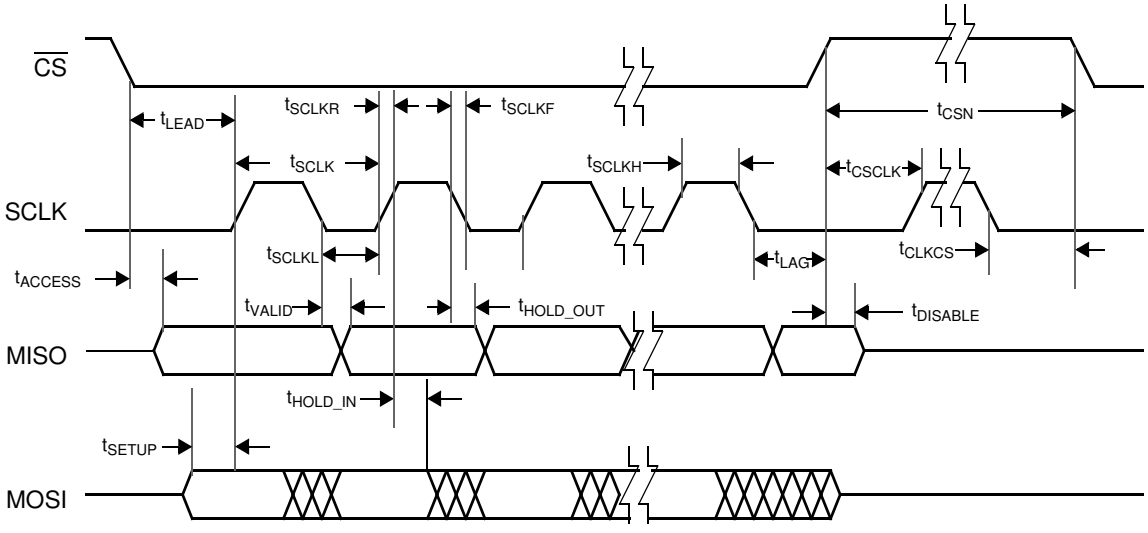


Figure 6. Serial Interface Timing

3 Functional Description

3.1 Customer Accessible Data Array

A customer accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block and read/write registers for device programmability and status. The OTP and writable register blocks incorporate independent CRC circuitry for fault detection (reference Section 3.2). The writable register block includes a locking mechanism to prevent unintended changes during normal operation. Portions of the array are reserved for factory-programmed trim values. The customer accessible data is shown in Table 3.

Table 3. Customer Accessible Data

Location		Bit Function								Type
Addr	Register	7	6	5	4	3	2	1	0	
$00	SN0	SN[7]	SN[6]	SN[5]	SN[4]	SN[3]	SN[2]	SN[1]	SN[0]	F
$01	SN1	SN[15]	SN[14]	SN[13]	SN[12]	SN[11]	SN[10]	SN[9]	SN[8]	
$02	SN2	SN[23]	SN[22]	SN[21]	SN[20]	SN[19]	SN[18]	SN[17]	SN[16]	
$03	SN3	SN[31]	SN[30]	SN[29]	SN[28]	SN[27]	SN[26]	SN[25]	SN[24]	
$04	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
$05	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
$06	FCTCFG	STMAG	0	0	0	0	0	0	0	
$07	Invalid Address: “Invalid Register Request”									
$08	PN	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]	
$09	Invalid Address: “Invalid Register Request”									
$0A	DEVCTL	RES_1	RES_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/W
$0B	DEVCFG	Reserved	Reserved	ENDINIT	$\overline{SD}$	OFMON	A_CFG[2]	A_CFG[1]	A_CFG[0]	
$0C	DEVCFG_X	ST	Reserved	Reserved	Reserved	LPF[3]	LPF[2]	LPF[1]	LPF[0]	
$0D	Invalid Address: “Invalid Register Request”									
$0E	ARMCFG	Reserved	Reserved	APS[1]	APS[0]	AWS_N[1]	AWS_N[0]	AWS_P[1]	AWS_P[0]	
$0F	Invalid Address: “Invalid Register Request”									
$10	ARMT_P	AT_P[7]	AT_P[6]	AT_P[5]	AT_P[4]	AT_P[3]	AT_P[2]	AT_P[1]	AT_P[0]	
$11	Invalid Address: “Invalid Register Request”									
$12	ARMT_N	AT_N[7]	AT_N[6]	AT_N[5]	AT_N[4]	AT_N[3]	AT_N[2]	AT_N[1]	AT_N[0]	
$13	Invalid Address: “Invalid Register Request”									
$14	DEVSTAT	UNUSED	IDE	SDOV	DEVINIT	MISOERR	0	OFFSET	DEVRES	R
$15	COUNT	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]	
$16	OFFCORR_X	OFFCORR_X[7]	OFFCORR_X[6]	OFFCORR_X[5]	OFFCORR_X[4]	OFFCORR_X[3]	OFFCORR_X[2]	OFFCORR_X[1]	OFFCORR_X[0]	
$17	Invalid Address: “Invalid Register Request”									
$1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
$1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	

Type codes
F: Factory programmed OTP location
R/W: Read/write register
R: Read-only register
N/A: Not applicable

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each MMA685x device during manufacturing. The serial number is composed of the following information:

Bit Range	Content
S12 - S0	Serial Number
S31 - S13	Lot Number

Serial numbers begin at 1 for all produced devices in each lot, and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the OTP shadow register array CRC verification. Reference Section 3.2.1 for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Reserved Registers

These reserved registers are read-only and have no impact on device operation or performance.

Table 4. Reserved Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$04	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$05	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

3.1.3 Factory Configuration Registers

The factory configuration register is a one time programmable, read only register which contains customer specific device configuration information that is programmed by Freescale.

Table 5. Factory Configuration Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$06	FCTCFG	STMAG	0	0	0	0	0	0	0

3.1.3.1 Self-Test Magnitude Selection Bits (STMAG)

The self-test magnitude selection bits indicate if the nominal self-test deflection value is set to the low or high value as shown in the table below.

STMAG	Full-Scale Acceleration Range	Nominal Self-Test Deflection Value (Reference Section 2.4)
0	≤ 60g	ΔST_{Low}
1	> 60g	ΔST_{HI}

3.1.4 Part Number Register (PN)

The part number register is a one time programmable, read only register which contains two digits of the device part number to identify the axis and range information. The contents of this register have no impact on device operation or performance.

Table 6. Part Number Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$08	PN	PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]

PN Register Value		Range Reference Section 2.4
Decimal	**HEX**	
51	$33	20
52	$34	35
53	$35	50
54	$36	75
55	$37	100
56	$38	60

3.1.5 Device Control Register (DEVCTL)

The device control register is a read-write register which contains device control operations that can be applied during both initialization and normal operation.

Table 7. Device Control Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0A	DEVCTL	RES_1	RES_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value		0	0	0	0	0	0	0	0

3.1.5.1 Reset Control (RES_1, RES_0)

A series of three consecutive register write operations to the reset control bits in the DEVCTL register will cause a device reset. To reset the internal digital circuitry, the following register write operations must be performed in the order shown below. The register write operations must be consecutive SPI commands in the order shown or the device will not be reset.

Register Write to DEVCTL	RES_1	RES_0	Effect
SPI Register Write 1	0	0	No Effect
SPI Register Write 2	1	1	No Effect
SPI Register Write 3	0	1	Device RESET

The response to the Register Write returns ‘0’ for RES_1 and RES_0. A Register Read of RES_1 and RES_0 returns ‘0’ and terminates the reset sequence.

3.1.5.2 Reserved Bits (DEVCTL[5:0])

Bits 5 through 0 of the DEVCTL register are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

3.1.6 Device Configuration Register (DEVCFG)

The device configuration register is a read/write register which contains data for general device configuration. The register can be written during initialization but is locked once the ENDINIT bit is set. This register is included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 8. Device Configuration Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0B	DEVCFG	Reserved	Reserved	ENDINIT	$\overline{SD}$	OFMON	A_CFG[2]	A_CFG[1]	A_CFG[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.6.1 Reserved Bits (Reserved)

Bits 6 and 7 of the DEVCFG register are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

3.1.6.2 End of Initialization Bit (ENDINIT)

The ENDINIT bit is a control bit used to indicate that the user has completed all device and system level initialization tests, and that MMA685x will operate in normal mode. Once the ENDINIT bit is set, writes to all writable register bits are inhibited except for the DEVCTL register. Once written, the ENDINIT bit can only be cleared by a device reset. The writable register CRC check (reference Section 3.2.2) is only enabled when the ENDINIT bit is set.

3.1.6.3 $\overline{SD}$ Bit

The $\overline{SD}$ bit determines the format of acceleration data results. If the $\overline{SD}$ bit is set to a logic ‘1’, unsigned results are transmitted, with the zero-g level represented by a nominal value of 512. If the $\overline{SD}$ bit is cleared, signed results are transmitted, with the zero-g level represented by a nominal value of 0.

$\overline{SD}$	Operating Mode
1	Unsigned Data Output
0	Signed Data Output

3.1.6.4 OFMON Bit

The OFMON bit determines if the offset monitor circuit is enabled. If the OFMON bit is set to a logic ‘1’, the offset monitor is enabled. Refer to Section 3.8.5 for more information. If the OFMON bit is cleared, the offset monitor is disabled.

OFMON	Operating Mode
1	Offset Monitor Circuit Enabled
0	Offset Monitor Circuit Disabled

3.1.6.5 ARM Configuration Bits (A_CFG[2:0])

The ARM Configuration Bits (A_CFG[2:0]) select the mode of operation for the ARM/PCM pins.

Table 9. Arming Output Configuration

A_CFG[2]	A_CFG[1]	A-CFG[0]	Operating Mode	Output Type	Reference
0	0	0	Arm Output Disabled	Hi Impedance	
0	0	1	PCM Output	Digital Output	Section 3.8.10
0	1	0	Moving Average Mode	Active High with Pulldown Current	Section 3.8.9.1
0	1	1	Moving Average Mode	Active Low with Pullup Current	Section 3.8.9.1
1	0	0	Count Mode	Active High with Pulldown Current	Section 3.8.9.2
1	0	1	Count Mode	Active Low with Pullup Current	Section 3.8.9.2
1	1	0	Unfiltered Mode	Active High with Pulldown Current	Section 3.8.9.3
1	1	1	Unfiltered Mode	Active Low with Pullup Current	Section 3.8.9.3

3.1.7 Axis Configuration Register (DEVCFG_X)

The Axis configuration register is a read/write register which contains axis specific configuration information. This register can be written during initialization, but is locked once the ENDINIT bit is set. This register is included in the writable register CRC check. Refer to Section 3.2.2 for details

Table 10. Axis Configuration Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	DEVCFG_X	ST	Reserved	Reserved	Reserved	LPF[3]	LPF[2]	LPF[1]	LPF[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.7.1 Self-Test Control (ST)

The ST bit enables and disables the self-test circuitry. Self-test circuitry is enabled if a logic ‘1’ is written to ST and the ENDINIT bit has not been set. Enabling the self-test circuitry results in a positive acceleration value. Self-test deflection values are specified in Section 2.4. ST is always cleared following internal reset.

When the self-test circuitry is active, the offset cancellation block and the offset monitor status are suspended, and the status bits in the Acceleration Data Request Response will indicate “Self-Test Active”. Reference Section 3.8.4 and Section 4.2 for details. When the self-test circuitry is disabled by clearing the ST bit, the offset monitor remains disabled until the time t_{ST_OMB} specified in Section 2.4 expires. However, the status bits in the Acceleration Data Request Response will immediately indicate that self-test has been deactivated.

3.1.7.2 Reserved Bits (Reserved)

Bits 6 through 4 of the DEVCFG_X register are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

3.1.7.3 Low-Pass Filter Selection Bits (LPF[3:0])

The Low Pass Filter selection bit selects a low-pass filter as shown in Table 11. Refer to Section 3.8.3 for details regarding filter configurations.

Table 11. Low Pass Filter Selection Bits

LPF[3]	LPF[2]	LPF[1]	LPF[0]	Low Pass Filter Selected	Nominal Sample Rate (μs)
0	0	0	0	100 Hz, 4-pole	8
0	0	0	1	300 Hz, 4-Pole	8
0	0	1	0	400 Hz, 4-Pole	8
0	0	1	1	800 Hz, 4-Pole	8
0	1	0	0	1000 Hz, 4-Pole	8
0	1	0	1	400 Hz, 3-Pole	8
0	1	1	0	Reserved	Reserved
0	1	1	1	Reserved	Reserved
1	0	0	0	50 Hz, 4-Pole	16
1	0	0	1	150 Hz, 4-Pole	16
1	0	1	0	200 Hz, 4-Pole	16
1	0	1	1	400 Hz, 4-Pole	16
1	1	0	0	500 Hz, 4-Pole	16
1	1	0	1	200 Hz, 3-Pole	16
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

Note: Filter characteristics do not include g-cell frequency response.

3.1.8 Arming Configuration Registers (ARMCFG)

The arming configuration register contains configuration information for the arming function. The values in this register are only relevant if the arming function is operating in moving average mode, or count mode.

This register can be written during initialization but is locked once the ENDINIT bit is set. Refer to Section 3.1.6.2. This register is included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 12. Arming Configuration Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0E	ARMCFG	Reserved	Reserved	APS[1]	APS[0]	AWS_N[1]	AWS_N[0]	AWS_P[1]	AWS_P[0]
Reset Value		0	0	0	0	1	1	1	1

3.1.8.1 Reserved Bits (Reserved)

Bits 7 through 6 of the ARMCFG register are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

3.1.8.2 Arming Pulse Stretch (APS[1:0])

The APS[1:0] bit sets the programmable pulse stretch time for the arming outputs. Refer to Section 3.8.9 for more details regarding the arming function.

Table 13. Arming Pulse Stretch Definitions

APS[1]	APS[0]	Pulse Stretch Time[1] (Typical Oscillator)
0	0	0 mS
0	1	16.256 ms - 16.384 ms
1	0	65.408 ms - 65.536 ms
1	1	261.888 ms - 262.016 ms

1.Pulse stretch times are derived from the internal oscillator, so the tolerance on this oscillator applies.

3.1.8.3 Arming Window Size (AWS_x[1:0])

The AWS_x[1:0] bit has a different function depending on the state of the A_CFG bits in the DEVCFG register.

If the arming function is set to moving average mode, the AWS bits set the number of acceleration samples used for the arming function moving average. The number of samples is set independently for polarity. If the arming function is set to count mode, the AWS bits set the sample count limit for the arming function. The sample count limit is set independently.

Refer to Section 3.8.9 for more details regarding the arming function.

Table 14. Positive Arming Window Size Definitions (Moving Average Mode)

AWS_P[1]	AWS_P[0]	Positive Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Table 15. Negative Arming Window Size Definitions (Moving Average Mode)

AWS_N[1]	AWS_N[0]	Negative Window Size
0	0	2
0	1	4
1	0	8
1	1	16

Table 16. Arming Count Limit Definitions (Count Mode)

AWS_N[1]	AWS_N[0]	AWS_P[1]	AWS_P[0]	Sample Count Limit
Don't Care	Don't Care	0	0	1
Don't Care	Don't Care	0	1	3
Don't Care	Don't Care	1	0	7
Don't Care	Don't Care	1	1	15

3.1.9 Arming Threshold Registers (ARMT_P, ARMT_N)

These registers contain the positive and negative thresholds to be used by the arming function. Refer to Section 3.8.9 for more details regarding the arming function.

These registers can be written during initialization but are locked once the ENDINIT bit is set. Refer to Section 3.1.6.2. These registers are included in the writable register CRC check. Refer to Section 3.2.2 for details.

Table 17. Arming Threshold Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$10	ARMT_P	AT_P[7]	AT_P[6]	AT_P[5]	AT_P[4]	AT_P[3]	AT_P[2]	AT_P[1]	AT_P[0]
$12	ARMT_N	AT_N[7]	AT_N[6]	AT_N[5]	AT_N[4]	AT_N[3]	AT_N[2]	AT_N[1]	AT_N[0]
Reset Value		0	0	0	0	0	0	0	0

The values programmed into the threshold registers are the threshold values used for the arming function as described in Section 3.8.9. The threshold registers hold independent unsigned 8-bit values for polarity. Each threshold increment is equivalent to one output LSB. Table 18 shows examples of some threshold register values and the corresponding threshold.

Table 18. Threshold Register Value Examples

Axis Type		Programmed Thresholds			
Range (g)	**Sensitivity (g/LSB)**	**Positive (Decimal)**	**Negative (Decimal)**	**Positive Threshold (g)**	**Negative Threshold (g)**
20	0.04097	100	50	4.10	-2.05
20	0.04097	255	0	10.45	Disabled
50	0.1024	50	20	5.12	-2.05
120	0.24414	20	10	4.88	-2.44

If either the positive or negative threshold is programmed to $00, comparisons are disabled for only that polarity. The arming function still operates for the opposite polarity. If both the positive and negative arming thresholds are programmed to $00, the Arming function is disabled, and the output pin is disabled, regardless of the value of the A_CFG bits in the DEVCFG register.

3.1.10 Device Status Register (DEVSTAT)

The device status register is a read-only register. A read of this register clears the status flags affected by transient conditions. Reference Section 4.5 for details on the MMA685x response for each status condition.

Table 19. Device Status Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$14	DEVSTAT	UNUSED	IDE	SDOV	DEVINIT	MISOERR	0	OFFSET	DEVRES

3.1.10.1 Unused Bit (UNUSED)

The unused bit has no impact on operation or performance. When read this bit may be ‘1’ or ‘0’.

3.1.10.2 Internal Data Error Flag (IDE)

The internal data error flag is set if a customer or OTP register data CRC fault or other internal fault is detected as defined in Section 4.5.5. The internal data error flag is cleared by a read of the DEVSTAT register. If the error is associated with a CRC fault in the writable register array, the fault will be re-asserted and will require a device reset to clear. If the error is associated with the data stored in the fuse array, the fault will be re-asserted even after a device reset.

3.1.10.3 Sigma Delta Modulator Over Range Flag (SDOV)

The sigma delta modulator over range flag is set if the sigma delta modulator becomes saturated. The SDOV flag is cleared by a read of the DEVSTAT register.

3.1.10.4 Device Initialization Flag (DEVINIT)

The device initialization flag is set during the interval between negation of internal reset and completion of internal device initialization. DEVINIT is cleared automatically. The device initialization flag is not affected by a read of the DEVSTAT register.

3.1.10.5 SPI MISO Data Mismatch Error Flag (MISOERR)

The MISO data mismatch flag is set when a MISO Data mismatch fault occurs as specified in Section 4.5.2. The MISOERR flag is cleared by a read of the DEVSTAT register.

3.1.10.6 Offset Monitor Over Range Flags (OFFSET)

The offset monitor over range flag is set if the acceleration signal reaches the specified offset limit. The offset monitor over range flags are cleared by a read of the DEVSTAT register.

3.1.10.7 Device Reset Flag (DEVRES)

The device reset flag is set during device initialization following a device reset. The device reset flag is cleared by a read of the DEVSTAT register.

3.1.11 Count Register (COUNT)

The count register is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit pre-scaler divides the primary oscillator frequency by 1024. Thus, the value in the register increases by one count every 128 µs and the counter rolls over every 32.768 ms.

Table 20. Count Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$15	COUNT	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.12 Offset Correction Value Registers (OFFCORR)

The offset correction value register is a read-only register which contain the most recent offset correction increment / decrement value from the offset cancellation circuit. The value stored in this register indicates the amount of offset correction being applied to the SPI output data. The values have a resolution of 1 LSB.

Table 21. Offset Correction Value Register

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$16	OFFCORR_X	OFFCORR_X[7]	OFFCORR_X[6]	OFFCORR_X[5]	OFFCORR_X[4]	OFFCORR_X[3]	OFFCORR_X[2]	OFFCORR_X[1]	OFFCORR_X[0]
Reset Value		0	0	0	0	0	0	0	0

3.1.13 Reserved Registers (Reserved)

Registers $1C and $1D are reserved. A write to the reserved bits must always be logic ‘0’ for normal device operation and performance.

Table 22. Reserved Registers

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$1C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$1D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value		0	0	0	0	0	0	0	0

3.2 Customer Accessible Data Array CRC Verification

3.2.1 OTP Shadow Register Array CRC Verification

The OTP shadow register array is verified for errors using a 3-bit CRC. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'. If a CRC error is detected in the OTP array, the IDE bit is set in the DEVSTAT register.

3.2.2 Writable Register CRC Verification

The writable registers in the data array are verified for errors using a 3-bit CRC. The CRC verification is enabled only when the ENDINIT bit is set in the DEVCFG register. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'. If a CRC error is detected in the writable register array, the IDE bit is set in the DEVSTAT register.

3.3 Voltage Regulators

Separate internal voltage regulators supply the analog and digital circuitry. External filter capacitors are required, as shown in Figure 1. The voltage regulator module includes voltage monitoring circuitry which indicates a device reset until the external supply and all internal regulated voltages are within predetermined limits. A reference generator provides a stable voltage which is used by the ΣΔ converters.

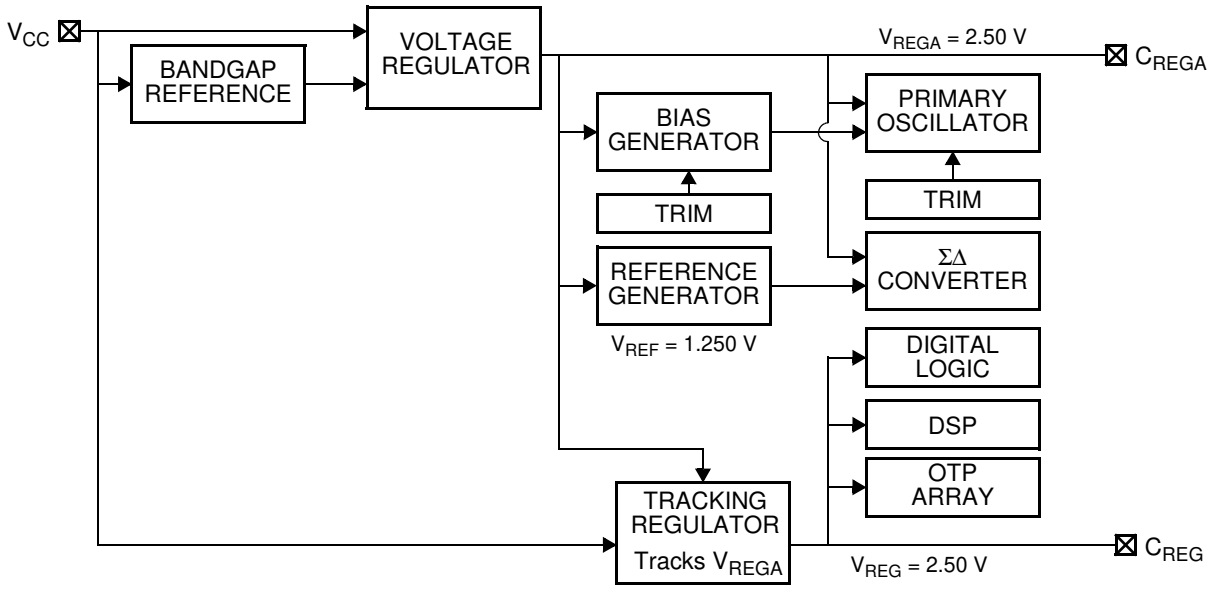


Figure 7. Power Supply

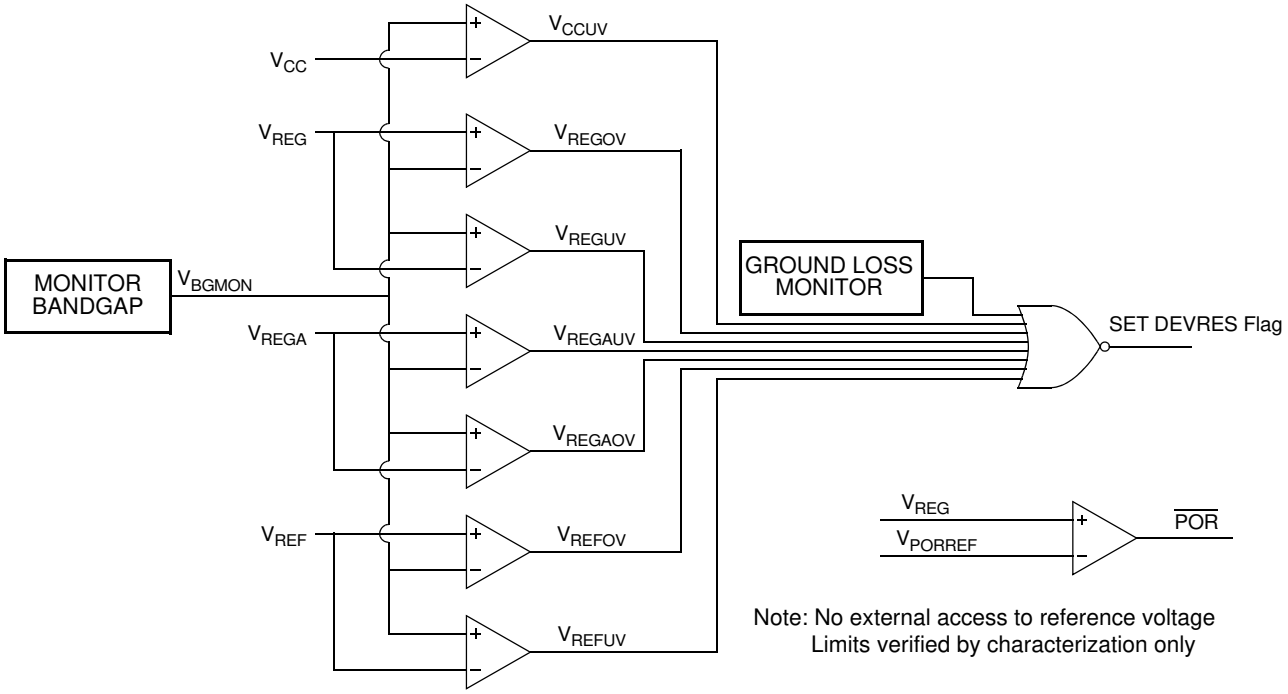


Figure 8. Voltage Monitoring

3.3.1 C_{REG} Failure Detection

The digital supply voltage regulator is designed to be unstable with low capacitance. If the connection to the V_{REG} capacitor becomes open, the digital supply voltage will oscillate and cause either an undervoltage, or overvoltage failure within one internal sample time. This failure will result in one of the following:

1. The DEVRES flag in the DEVSTAT register will be set. MMA685x will respond to SPI acceleration requests as defined in Table 27.
2. MMA685x will be held in RESET and be non-responsive to SPI requests.

3.3.2 C_{REGA} Failure Detection

The analog supply voltage regulator is designed to be unstable with low capacitance. If the connection to the V_{REGA} capacitor becomes open, the analog supply voltage will oscillate and cause either an undervoltage, or overvoltage failure within one internal sample time. The DEVRES flag in the DEVSTAT register will be set. MMA685xMMA685x will respond to SPI acceleration requests as defined in Table 27.

Note: This feature is only supported with a V_{CC} supply voltage in the range of 4.75V to 5.25V.

3.3.3 V_{SS} and V_{SSA} Ground Loss Monitor

MMA685x detects the loss of ground connection to either V_{SS} or V_{SSA}. A loss of ground connection to V_{SS} will result in a V_{REG} overvoltage failure. A loss of ground connection to V_{SSA} will result in a V_{REG} undervoltage failure. Both failures result in a device reset.

3.3.4 SPI Initiated Reset

In addition to voltage monitoring, a device reset can be initiated by a specific series of three write operations involving the RES_1 and RES_0 bits in the DEVCTL register. Reference Section 3.1.5.1. for details regarding the SPI initiated reset.

3.4 Internal Oscillator

MMA685x includes a factory trimmed oscillator as specified in Section 2.6.

3.4.1 Oscillator Monitor

The COUNT register in the customer accessible array is a read-only register which provides the current value of a free-running 8-bit counter derived from the primary oscillator. A 10-bit pre-scaler divides the primary oscillator by 1024. Thus, the value in the COUNT register increases by one count every 128µs, and the register rolls over every 32.768 ms. The SPI master can periodically read the COUNT register, and verify the difference between subsequent register reads against the system time base.

1. The SPI access rates and deviations must be taken into account for this oscillator verification.

3.5 Transducer

The MMA685x transducer is an overdamped mass-spring-damper system described by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

where:

ζ = Damping Ratio

ω_n = Natural Frequency = $2 * \Pi * f_n$

Reference Section 2.4 for transducer parameters.

3.6 Self-Test Interface

The self-test interface applies a voltage to the g-cell, causing deflection of the proof mass. The self-test interface is controlled through SPI write operations to the DEVCFG_X register described in Section 3.1.7. The ENDINIT bit in the DEVCFG register must also be low to enable self-test. A diagram of the self-test interface is shown in Figure 9.

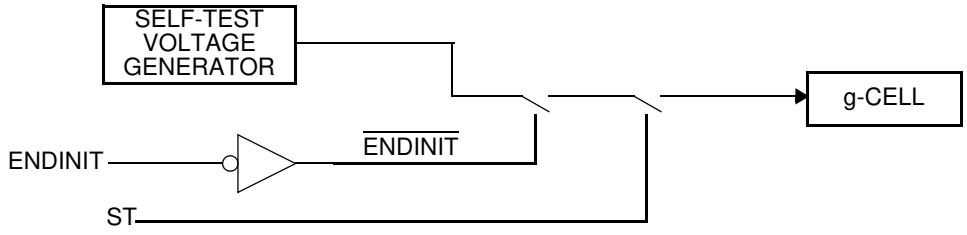


Figure 9. Self-Test Interface

The raw self-test deflection can be verified against raw self-test limits using the following equations:

$$\Delta ST_{MINLIMIT} = FLOOR \cdot (\Delta ST_{MIN}) \cdot [SENS \cdot (1 - \Delta SENS)]$$

$$\Delta ST_{MAXLIMIT} = CEIL \cdot (\Delta ST_{MAX}) \cdot [SENS \cdot (1 + \Delta SENS)]$$

where:

ΔST_{MIN}	The minimum self-test deflection over temperature as specified in Section 2.4.
ΔST_{MAX}	The maximum self-test deflection over temperature as specified in Section 2.4.
SENS	The sensitivity of the device
ΔSENS	The sensitivity tolerance

3.7 ΣΔ Converters

Two sigma delta converters provide the interface between the g-cell and the DSP. The output of each ΣΔ converter is a data stream at a nominal frequency of 1 MHz.

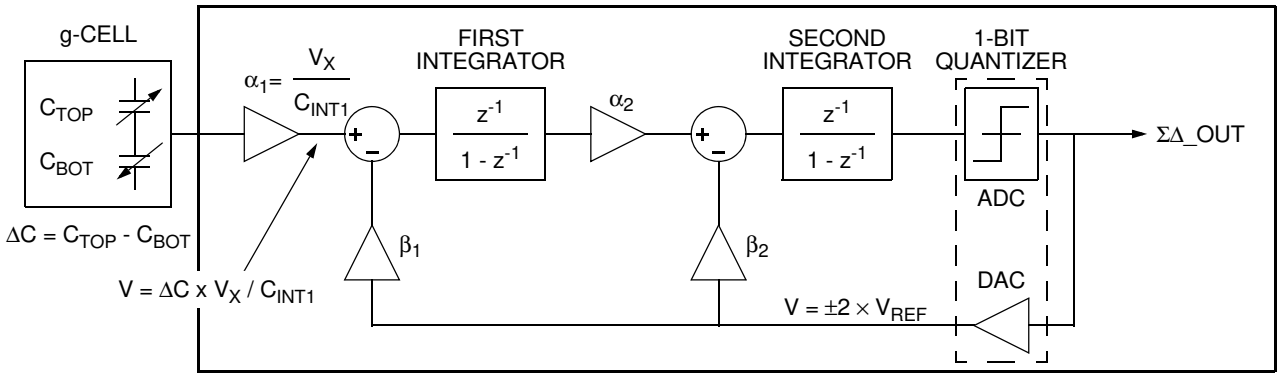


Figure 10. ΣΔ Converter Block Diagram

3.8 Digital Signal Processing Block

A digital signal processing (DSP) block is used to perform signal filtering and compensation operations. A diagram illustrating the signal processing flow is shown in Figure 11.

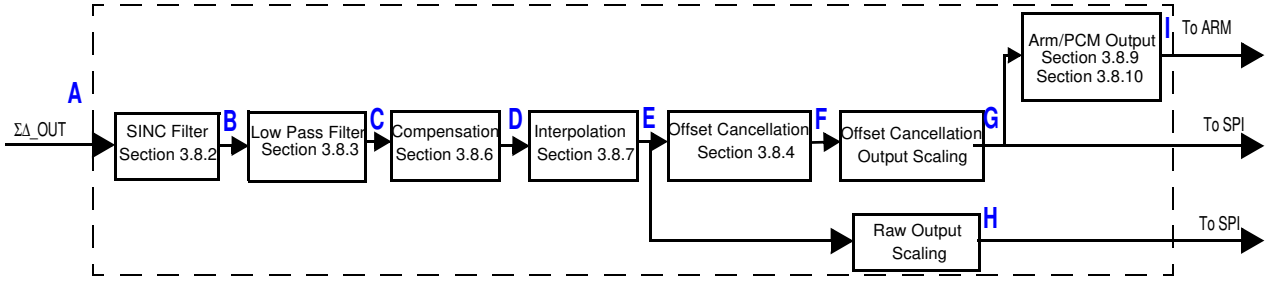


Figure 11. Signal Chain Diagram

Table 23. MMA685x Signal Chain Characteristics

	Description	Sample Time (μs)	Data Width Bits	Over Bits	Effective Bits	Rounding Resolution Bits	Typical Block Latency	Reference
A	ΣΔ	1	1		1	—	3.2 μs	Section 3.7
B	SINC Filter	8	14		13	—	11.2 μs	Section 3.8.2
C	Low Pass Filter	8/16	20	6	10	4	Reference Section 3.8.3	Section 3.8.3
D	Compensation	8/16	20	6	10	4	7.875 μs	Section 3.8.6
E	Interpolation	4/8	20	6	10	4	t_s / 2	Section 3.8.7
F	Offset Cancellation	256	20	6	10	4	N/A	Section 3.8.4
G, H	SPI Output	4/8	—	—	10	—	t_s / 2	—
I	PCM Output	4/8	—	—	9	—	—	Section 3.8.10

3.8.1 DSP Clock

The DSP is clocked at 8 MHz, with an effective 6MHz operating frequency. The clock to the DSP is disabled for 1 clock prior to each edge of the ΣΔ modulator clock to minimize noise during data conversion. The bit streams from the two ΣΔ converters are processed through independent data paths within the DSP.

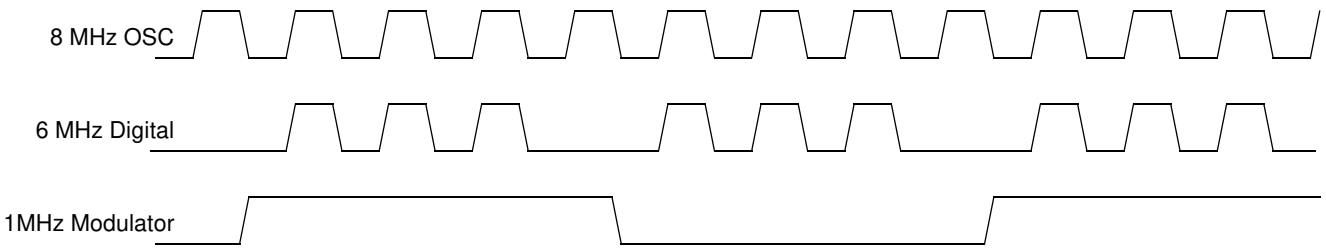


Figure 12. Clock Generation

3.8.2 Decimation Sinc Filter

The serial data stream produced by the ΣΔ converter is decimated and converted to parallel values by a 3rd order 16:1 sinc filter with a decimation factor of 8 or 16, depending on the Low Pass Filter selected.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})}\right]^3$$

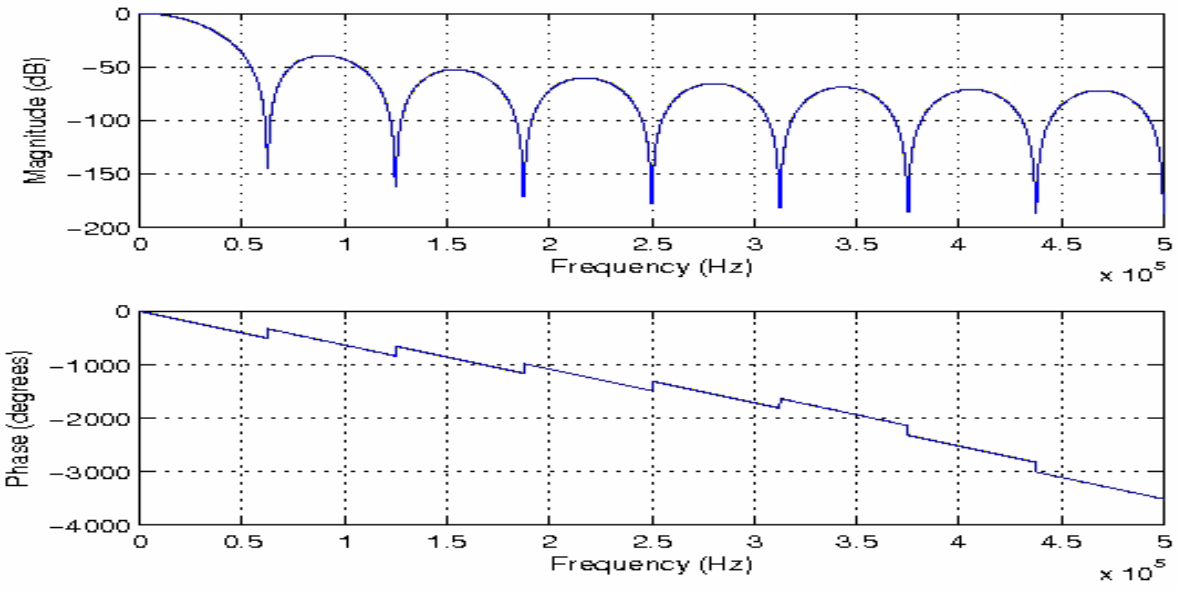


Figure 13. Sinc Filter Response, t_S = 8 μs