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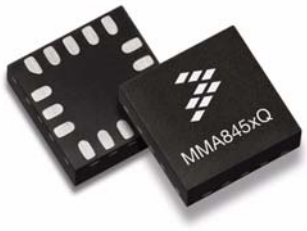
Xtrinsic MMA8451Q 3-Axis, 14-bit/8-bit Digital Accelerometer

MMA8451Q

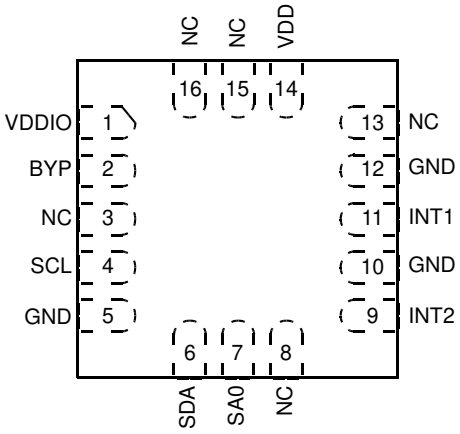
The MMA8451Q is a smart, low-power, three-axis, capacitive, micromachined accelerometer with 14 bits of resolution. This accelerometer is packed with embedded functions with flexible user programmable options, configurable to two interrupt pins. Embedded interrupt functions allow for overall power savings relieving the host processor from continuously polling data. There is access to both low-pass filtered data as well as high-pass filtered data, which minimizes the data analysis required for jolt detection and faster transitions. The device can be configured to generate inertial wakeup interrupt signals from any combination of the configurable embedded functions allowing the MMA8451Q to monitor events and remain in a low-power mode during periods of inactivity. The MMA8451Q is available in a 3 mm by 3 mm by 1 mm QFN package.

Top and Bottom View



16 PIN QFN
3 mm by 3 mm by 1 mm
CASE 2077-02

Top View



Pin Connections

Features

- 1.95V to 3.6V supply voltage
- 1.6V to 3.6V interface voltage
- ±2g/±4g/±8g dynamically selectable full-scale
- Output Data Rates (ODR) from 1.56 Hz to 800 Hz
- 99 µg/√Hz noise
- 14-bit and 8-bit digital output
- I^2C digital output interface (operates to 2.25 MHz with 4.7 kΩ pullup)
- Two programmable interrupt pins for seven interrupt sources
- Three embedded channels of motion detection
- Freefall or Motion Detection: 1 channel
- Pulse Detection: 1 channel
- Jolt Detection: 1 channel
- Orientation (Portrait/Landscape) detection with programmable hysteresis
- Automatic ODR change for Auto-WAKE and return to SLEEP
- 32-sample FIFO
- High-Pass Filter Data available per sample and through the FIFO
- Self-Test
- RoHS compliant
- Current Consumption: 6 µA to 165 µA

Typical Applications

- E-Compass applications
- Static orientation detection (Portrait/Landscape, Up/Down, Left/Right, Back/Front position identification)
- Notebook, e-reader, and Laptop Tumble and Freefall Detection
- Real-time orientation detection (virtual reality and gaming 3D user position feedback)
- Real-time activity analysis (pedometer step counting, freefall drop detection for HDD, dead-reckoning GPS backup)
- Motion detection for portable product power saving (Auto-SLEEP and Auto-WAKE for cell phone, PDA, GPS, gaming)
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)
- User interface (menu scrolling by orientation change, tap detection for button replacement)

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
MMA8451QT	-40°C to +85°C	QFN-16	Tray
MMA8451QR1	-40°C to +85°C	QFN-16	Tape and Reel

freescale Xtrinsic

Contents

Related Documentation

The MMA8451Q device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA8451Q.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Block Diagram and Pin Description

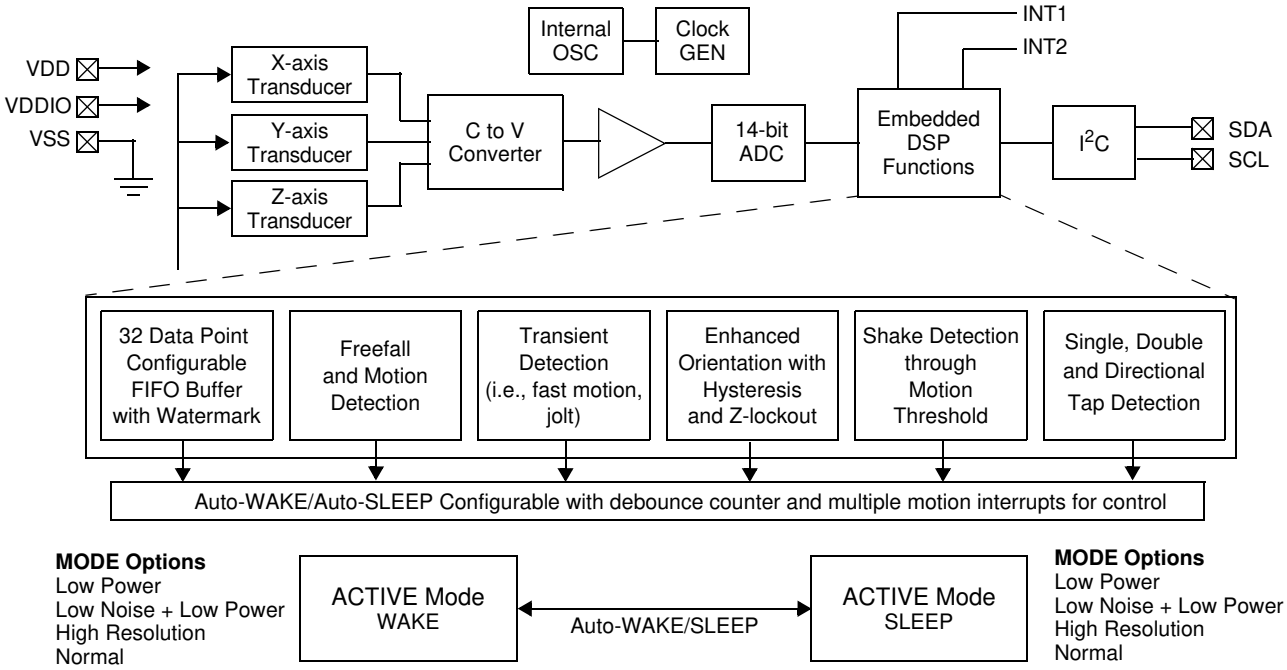


Figure 1. Block Diagram

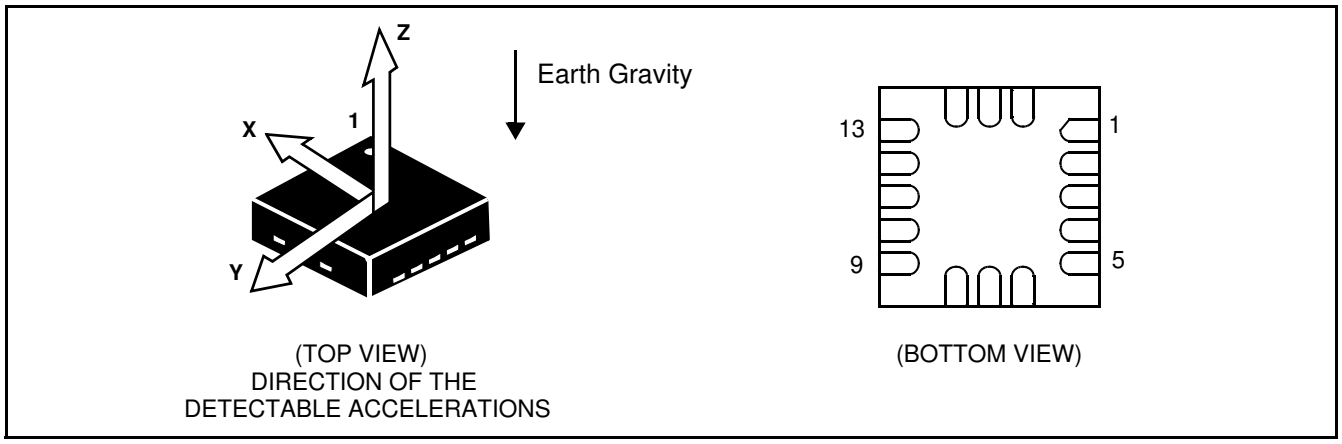


Figure 2. Direction of the Detectable Accelerations

Figure 3 shows the device configuration in the 6 different orientation modes. These orientations are defined as the following: PU = Portrait Up, LR = Landscape Right, PD = Portrait Down, LL = Landscape Left, BACK and FRONT side views. There are several registers to configure the orientation detection and are described in detail in the register setting section.

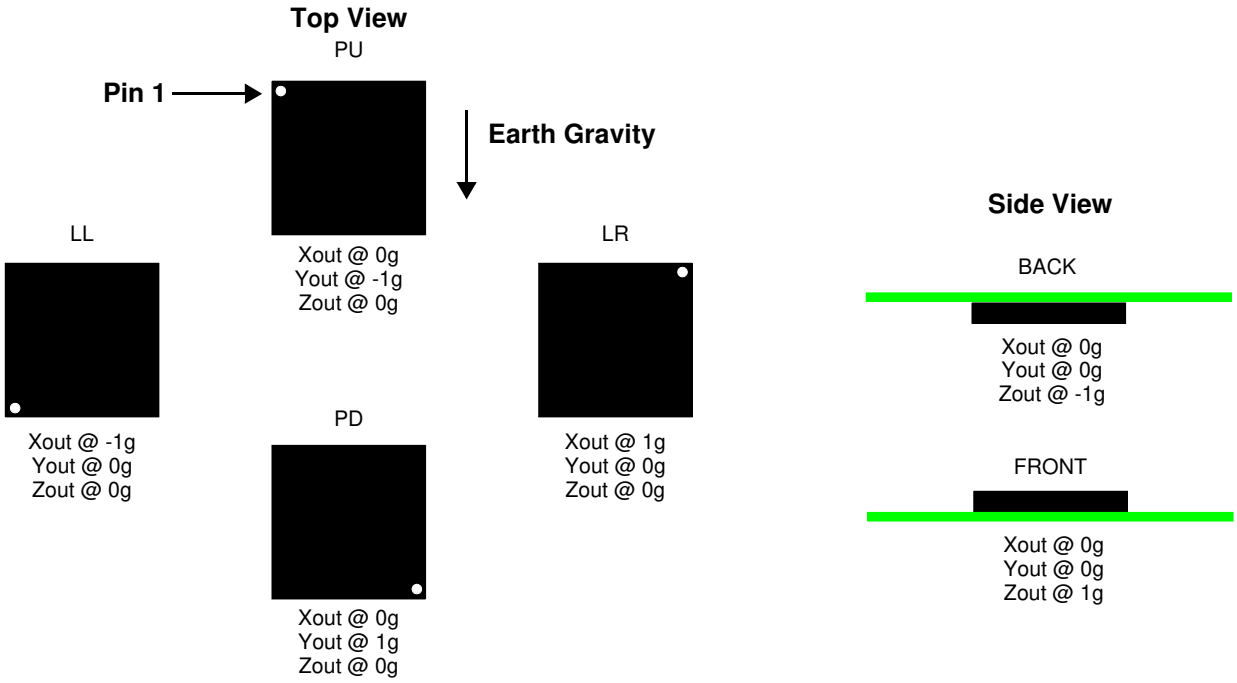


Figure 3. Landscape/Portrait Orientation

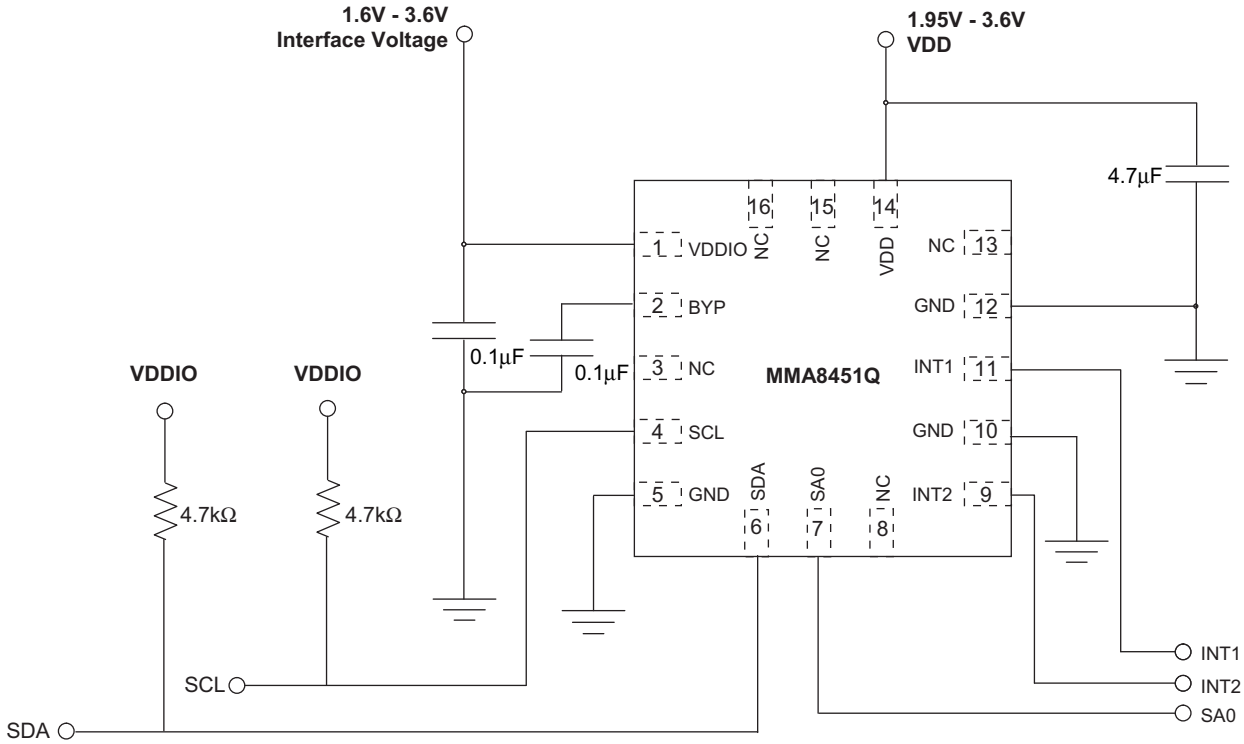


Figure 4. Application Diagram

Table 1. Pin Description

Pin #	Pin Name	Description	Pin Status
1	VDDIO	Internal Power Supply (1.62V - 3.6V)	Input
2	BYP	Bypass capacitor (0.1 µF)	Input
3	NC	Leave open. Do not connect	Open
4	SCL	I^2C Serial Clock	Open Drain
5	GND	Connect to Ground	Input
6	SDA	I^2C Serial Data	Open Drain
7	SA0	I^2C Least Significant Bit of the Device I^2C Address	Input
8	NC	Internally not connected (can be GND or VDD)	Input
9	INT2	Inertial Interrupt 2	Output
10	GND	Connect to Ground	Input
11	INT1	Inertial Interrupt 1	Output
12	GND	Connect to Ground	Input
13	NC	Internally not connected (can be GND or VDD)	Input
14	VDD	Power Supply (1.95V to 3.6V)	Input
15	NC	Internally not connected (can be GND or VDD)	Input
16	NC	Internally not connected (can be GND or VDD)	Input

The device power is supplied through VDD line. Power supply decoupling capacitors (100 nF ceramic plus 4.7 µF bulk, or a single 4.7 µF ceramic) should be placed as near as possible to the pins 1 and 14 of the device.

The control signals SCL, SDA, and SA0 are not tolerant of voltages more than VDDIO + 0.3V. If VDDIO is removed, the control signals SCL, SDA, and SA0 will clamp any logic signals with their internal ESD protection diodes.

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) are user programmable through the I^2C interface. The SDA and SCL I^2C connections are open drain and therefore require a pullup resistor as shown in the application diagram in Figure 4.

1.1 Soldering Information

The QFN package is compliant with the RoHS standard. Please refer to AN4077.

2 Mechanical and Electrical Specifications

2.1 Mechanical Characteristics

Table 2. Mechanical Characteristics @ VDD = 2.5V, VDDIO = 1.8V, T = 25°C unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Measurement Range(1)	FS[1:0] set to 00 2g Mode	FS		±2		g
	FS[1:0] set to 01 4g Mode			±4		
	FS[1:0] set to 10 8g Mode			±8		
Sensitivity	FS[1:0] set to 00 2g Mode	So		4096		counts/g
	FS[1:0] set to 01 4g Mode			2048		
	FS[1:0] set to 10 8g Mode			1024		
Sensitivity Accuracy(2)		Soa		±2.64		%
Sensitivity Change vs. Temperature	FS[1:0] set to 00 2g Mode	TCSo		±0.008		%/°C
	FS[1:0] set to 01 4g Mode					
	FS[1:0] set to 10 8g Mode					
Zero-g Level Offset Accuracy(3)	FS[1:0] 2g, 4g, 8g	TyOff		±17		mg
Zero-g Level Offset Accuracy Post Board Mount(4)	FS[1:0] 2g, 4g, 8g	TyOffPBM		±20		mg
Zero-g Level Change vs. Temperature	-40°C to 85°C	TCOff		±0.15		mg/°C
Self-Test Output Change(5) X Y Z	FS[1:0] set to 0 4g Mode	Vst		 +181 +255 +1680		LSB
ODR Accuracy 2 MHz Clock				±2		%
Output Data Bandwidth		BW	ODR/3		ODR/2	Hz
Output Noise	Normal Mode ODR = 400 Hz	Noise		126		µg/√Hz
Output Noise Low Noise Mode(1)	Normal Mode ODR = 400 Hz	Noise		99		µg/√Hz
Operating Temperature Range		Top	-40		+85	°C

1. Dynamic Range is limited to 4g when the Low Noise bit in Register 0x2A, bit 2 is set.
2. Sensitivity remains in spec as stated, but changing Oversampling mode to Low Power causes 3% sensitivity shift. This behavior is also seen when changing from 800 Hz to any other data rate in the Normal, Low Noise + Low Power or High Resolution mode.
3. Before board mount.
4. Post Board Mount Offset Specifications are based on an 8 Layer PCB, relative to 25°C.
5. Self-Test is one direction only.

2.2 Electrical Characteristics

Table 3. Electrical Characteristics @ VDD = 2.5V, VDDIO = 1.8V, T = 25°C unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD(1)	1.95	2.5	3.6	V
Interface Supply Voltage		VDDIO(1)	1.62	1.8	3.6	V
Low Power Mode	ODR = 1.56 Hz	I_{dd}LP		6		µA
	ODR = 6.25 Hz			6		
	ODR = 12.5 Hz			6		
	ODR = 50 Hz			14		
	ODR = 100 Hz			24		
	ODR = 200 Hz			44		
	ODR = 400 Hz			85		
	ODR = 800 Hz			165		
Normal Mode	ODR = 1.56 Hz	I_{dd}		24		µA
	ODR = 6.25 Hz			24		
	ODR = 12.5 Hz			24		
	ODR = 50 Hz			24		
	ODR = 100 Hz			44		
	ODR = 200 Hz			85		
	ODR = 400 Hz			165		
	ODR = 800 Hz			165		
Current during Boot Sequence, 0.5 mSec max duration using recommended Bypass Cap	VDD = 2.5V	Idd Boot			1	mA
Value of Capacitor on BYP Pin	-40°C 85°C	Cap	75	100	470	nF
STANDBY Mode Current @25°C	VDD = 2.5V, VDDIO = 1.8V STANDBY Mode	I_{dd}Stby		1.8	5	µA
Digital High Level Input Voltage SCL, SDA, SA0		VIH	0.75*VDDIO			V
Digital Low Level Input Voltage SCL, SDA, SA0		VIL			0.3*VDDIO	V
High Level Output Voltage INT1, INT2	I_O = 500 µA	VOH	0.9*VDDIO			V
Low Level Output Voltage INT1, INT2	I_O = 500 µA	VOL			0.1*VDDIO	V
Low Level Output Voltage SDA	I_O = 500 µA	VOLS			0.1*VDDIO	V
Power on Ramp Time			0.001		1000	ms
Time from VDDIO on and VDD > Vmin until I^2C ready for operation	Cbyp = 100 nF	BT	—	350	500	µs
Turn-on time (STANDBY to ACTIVE)		Ton		2/ODR + 1 ms		s
Turn-on time (Power Down to ACTIVE Mode)		Ton		2/ODR + 2 ms		s
Operating Temperature Range		Top	-40		+85	°C

1. There is no requirement for power supply sequencing. The VDDIO input voltage can be higher than the VDD input voltage.

2.3 I²C interface characteristics

Table 4. I²C slave timing values(1)

Parameter	Symbol	I²C Fast Mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0	400	kHz
Bus-free time between STOP and START condition	t_{BUF}	1.3		µs
(Repeated) START hold time	$t_{HD;STA}$	0.6		µs
Repeated START setup time	$t_{SU;STA}$	0.6		µs
STOP condition setup time	$t_{SU;STO}$	0.6		µs
SDA data hold time	$t_{HD;DAT}$	0.05	0.9 (2)	µs
SDA setup time	$t_{SU;DAT}$	100		ns
SCL clock low time	t_{LOW}	1.3		µs
SCL clock high time	t_{HIGH}	0.6		µs
SDA and SCL rise time	t_r	20 + 0.1 C_b(3)	300	ns
SDA and SCL fall time	t_f	20 + 0.1 C_b(3)	300	ns
SDA valid time (4)	$t_{VD;DAT}$		0.9 (2)	µs
SDA valid acknowledge time (5)	$t_{VD;ACK}$		0.9 (2)	µs
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	ns
Capacitive load for each bus line	Cb		400	pF

1.All values referred to $V_{IH(min)}$ (0.3V_{DD}) and $V_{IL(max)}$ (0.7V_{DD}) levels.
2.This device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3.C_b = total capacitance of one bus line in pF.
4.$t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5.$t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

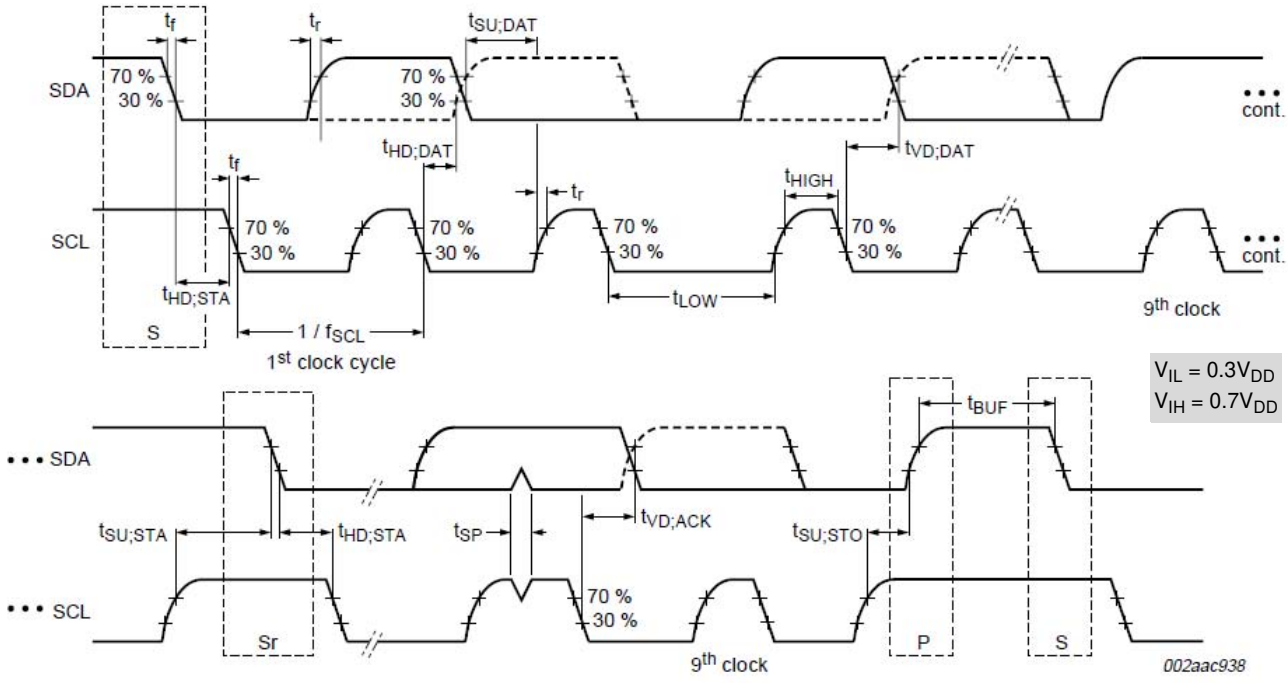


Figure 5. I²C slave timing diagram

2.4 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Acceleration (all axes, 100 μs)	g_{max}	5,000	g
Supply Voltage	VDD	-0.3 to + 3.6	V
Input voltage on any control pin (SA0, SCL, SDA)	Vin	-0.3 to VDDIO + 0.3	V
Drop Test	D_{drop}	1.8	m
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +125	°C

Table 6. ESD and Latchup Protection Characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latchup Current at T = 85°C	—	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage of the part or cause the part to otherwise fail.

This device is sensitive to ESD, improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

The sensitivity is represented in counts/g. In 2g mode the sensitivity is 4096 counts/g. In 4g mode the sensitivity is 2048 counts/g and in 8g mode the sensitivity is 1024 counts/g.

3.2 Zero-g Offset

Zero-g Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if the sensor is stationary. A sensor stationary on a horizontal surface will measure 0g in X-axis and 0g in Y-axis whereas the Z-axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT Registers 0x00, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress on the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

3.3 Self-Test

Self-Test checks the transducer functionality without external mechanical stimulus. When Self-Test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case, the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When Self-Test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

4 Modes of Operation

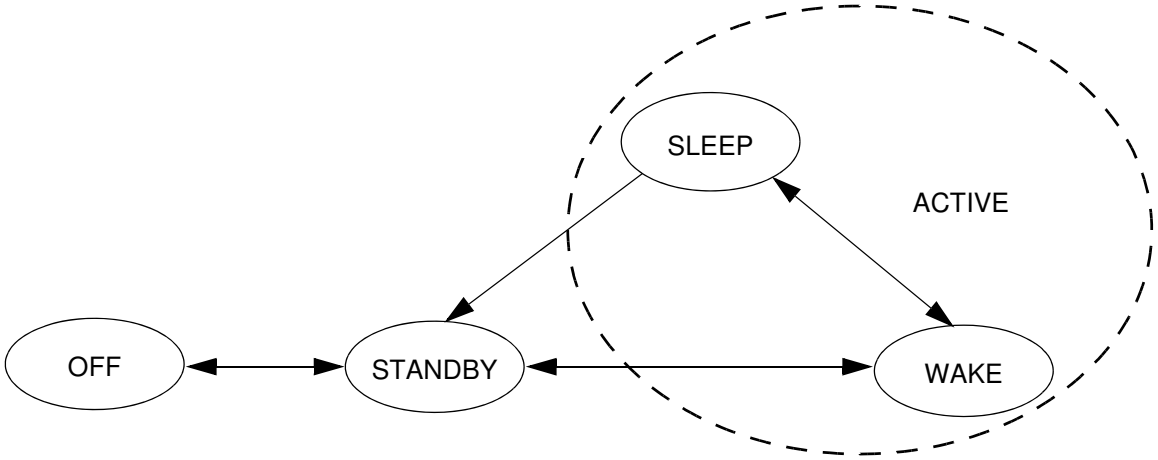


Figure 6. MMA8451Q Mode Transition Diagram

Table 7. Mode of Operation Description

Mode	I^2C Bus State	VDD	VDDIO	Function Description
OFF	Powered Down	<1.8V	VDDIO Can be > VDD	The device is powered off. All analog and digital blocks are shutdown. I^2C bus inhibited.
STANDBY	I^2C communication with MMA8451Q is possible	ON	VDDIO = High VDD = High ACTIVE bit is cleared	Only digital blocks are enabled. Analog subsystem is disabled. Internal clocks disabled.
ACTIVE (WAKE/SLEEP)	I^2C communication with MMA8451Q is possible	ON	VDDIO = High VDD = High ACTIVE bit is set	All blocks are enabled (digital, analog).

All register contents are preserved when transitioning from ACTIVE to STANDBY mode. Some registers are reset when transitioning from STANDBY to ACTIVE. These are all noted in the device memory map register table. The SLEEP and WAKE modes are ACTIVE modes. For more information on how to use the SLEEP and WAKE modes and how to transition between these modes, please refer to the functionality section of this document.

5 Functionality

The MMA8451Q is a low-power, digital output 3-axis linear accelerometer with a I^2C interface and embedded logic used to detect events and notify an external microprocessor over interrupt lines. The functionality includes the following:

- 8-bit or 14-bit data, High-Pass Filtered data, 8-bit or 14-bit configurable 32 sample FIFO
- Four different oversampling options for compromising between resolution and current consumption based on application requirements
- Additional Low Noise mode that functions independently of the Oversampling modes for higher resolution
- Low Power and Auto-WAKE/SLEEP modes for conservation of current consumption
- Single/Double tap with directional information 1 channel
- Motion detection with directional information or Freefall 1 channel
- Transient/Jolt detection based on a high-pass filter and settable threshold for detecting the change in acceleration above a threshold with directional information 1 channel
- Flexible user configurable portrait landscape detection algorithm addressing many use cases for screen orientation

All functionality is available in 2g, 4g or 8g dynamic ranges. There are many configuration settings for enabling all the different functions. Separate application notes have been provided to help configure the device for each embedded functionality.

Table 8. Features of the MMA845xQ devices

Feature List	MMA8451	MMA8452	MMA8453
Digital Resolution (Bits)	14	12	10
Digital Sensitivity (Counts/g)	4096	1024	256
Data-Ready Interrupt	Yes	Yes	Yes
Single-Pulse Interrupt	Yes	Yes	Yes
Double-Pulse Interrupt	Yes	Yes	Yes
Directional-Pulse Interrupt	Yes	Yes	Yes
Auto-WAKE	Yes	Yes	Yes
Auto-SLEEP	Yes	Yes	Yes
Freefall Interrupt	Yes	Yes	Yes
32 Level FIFO	Yes	No	No
High-Pass Filter	Yes	Yes	Yes
Low-Pass Filter	Yes	Yes	Yes
Orientation Detection Portrait/Landscape = 30°, Landscape to Portrait = 60°, and Fixed 45° Threshold	Yes	Yes	Yes
Programmable Orientation Detection	Yes	No	No
Motion Interrupt with Direction	Yes	Yes	Yes
Transient Detection with High-Pass Filter	Yes	Yes	Yes
Low Power Mode	Yes	Yes	Yes

5.1 Device Calibration

The device interface is factory calibrated for sensitivity and Zero-g offset for each axis. The trim values are stored in Non Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the circuitry. In normal use, further calibration in the end application is not necessary. However, the MMA8451Q allows the user to adjust the Zero-g offset for each axis after power-up, changing the default offset values. The user offset adjustments are stored in 6 volatile registers. For more information on device calibration, refer to Freescale application note, AN4069.

5.2 8-bit or 14-bit Data

The measured acceleration data is stored in the OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB registers as 2's complement 14-bit numbers. The most significant 8-bits of each axis are stored in OUT_X (Y, Z)_MSB, so applications needing only 8-bit results can use these 3 registers and ignore OUT_X,Y, Z_LSB. To do this, the F_READ bit in CTRL_REG1 must be set. When the F_READ bit is cleared, the fast read mode is disabled.

When the full-scale is set to 2g, the measurement range is -2g to +1.99975g, and each count corresponds to 1g/4096 (0.25 mg) at 14-bits resolution. When the full-scale is set to 8g, the measurement range is -8g to +7.999g, and each count corresponds to 1g/1024 (0.98 mg) at 14-bits resolution. The resolution is reduced by a factor of 64 if only the 8-bit results are used. For more information on the data manipulation between data formats and modes, refer to Freescale application.

5.3 Internal FIFO Data Buffer

MMA8451Q contains a 32 sample internal FIFO data buffer minimizing traffic across the I^2C bus. The FIFO can also provide power savings of the system by allowing the host processor/MCU to go into a SLEEP mode while the accelerometer independently stores the data, up to 32 samples per axis. The FIFO can run at all output data rates. There is the option of accessing the full 14-bit data or for accessing only the 8-bit data. When access speed is more important than high resolution the 8-bit data read is a better option.

The FIFO contains four modes (Fill Buffer Mode, Circular Buffer Mode, Trigger Mode, and Disabled Mode) described in the F_SETUP Register 0x09. Fill Buffer Mode collects the first 32 samples and asserts the overflow flag when the buffer is full and another sample arrives. It does not collect any more data until the buffer is read. This benefits data logging applications where all samples must be collected. The Circular Buffer Mode allows the buffer to be filled and then new data replaces the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This benefits situations where the processor is waiting for an specific interrupt to signal that the data must be flushed to analyze the event. The trigger mode will hold the last data up to the point when the trigger occurs and can be set to keep a selectable number of samples after the event occurs.

The MMA8451Q FIFO Buffer has a configurable watermark, allowing the processor to be triggered after a configurable number of samples has filled in the buffer (1 to 32).

For details on the configurations for the FIFO buffer as well as more specific examples and application benefits, refer to Freescale application note, AN4073.

5.4 Low Power Modes vs. High Resolution Modes

The MMA8451Q can be optimized for lower power modes or for higher resolution of the output data. High resolution is achieved by setting the LNOISE bit in Register 0x2A. This improves the resolution but be aware that the dynamic range is limited to 4g when this bit is set. This will affect all internal functions and reduce noise. Another method for improving the resolution of the data is by oversampling. One of the oversampling schemes of the data can activated when MODS = 10 in Register 0x2B which will improve the resolution of the output data only. The highest resolution is achieved at 1.56 Hz.

There is a trade-off between low power and high resolution. Low Power can be achieved when the oversampling rate is reduced. The lowest power is achieved when MODS = 11 or when the sample rate is set to 1.56 Hz. For more information on how to configure the MMA8451Q in Low Power mode or High Resolution mode and to realize the benefits, refer to Freescale application note, AN4075.

5.5 Auto-WAKE/SLEEP Mode

The MMA8451Q can be configured to transition between sample rates (with their respective current consumption) based on four of the interrupt functions of the device. The advantage of using the Auto-WAKE/SLEEP is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the SLEEP mode (lower current) when the device does not require higher sampling rates. Auto-WAKE refers to the device being triggered by one of the interrupt functions to transition to a higher sample rate. This may also interrupt the processor to transition from a SLEEP mode to a higher power mode.

SLEEP mode occurs after the accelerometer has not detected an interrupt for longer than the user definable time-out period. The device will transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode to save on current during this period of inactivity.

The Interrupts that can WAKE the device from SLEEP are the following: Tap Detection, Orientation Detection, Motion/Freefall, and Transient Detection. The FIFO can be configured to hold the data in the buffer until it is flushed if the FIFO Gate bit is set in Register 0x2C but the FIFO cannot WAKE the device from SLEEP.

The interrupts that can keep the device from falling asleep are the same interrupts that can wake the device with the addition of the FIFO. If the FIFO interrupt is enabled and data is being accessed continually servicing the interrupt then the device will remain in the WAKE mode. Refer to AN4074, for more detailed information for configuring the Auto-WAKE/SLEEP.

5.6 Freefall and Motion Detection

MMA8451Q has flexible interrupt architecture for detecting either a Freefall or a Motion. Freefall can be enabled where the set threshold must be less than the configured threshold, or motion can be enabled where the set threshold must be greater than the threshold. The motion configuration has the option of enabling or disabling a high-pass filter to eliminate tilt data (static offset). The freefall does not use the high-pass filter. For details on the Freefall and Motion detection with specific application examples and recommended configuration settings, refer to Freescale application note, AN4070.

5.6.1 Freefall Detection

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is **below** a user specified threshold for a user definable amount of time. Normally, the usable threshold ranges are between ±100 mg and ±500 mg.

5.6.2 Motion Detection

Motion is often used to simply alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event. The motion detection function can analyze static acceleration changes or faster jolts. For example, to detect that an object is spinning, all three axes would be enabled with a threshold detection of > 2g. This condition would need to occur for a minimum of 100 ms to ensure that the event wasn't just noise. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to determine whether the condition exists for configurable set of time (i.e., 100 ms or longer). There is also directional data available in the source register to detect the direction of the motion. This is useful for applications such as directional shake or flick, which assists with the algorithm for various gesture detections.

5.7 Transient Detection

The MMA8451Q has a built-in high-pass filter. Acceleration data goes through the high-pass filter, eliminating the offset (DC) and low frequencies. The high-pass filter cutoff frequency can be set by the user to four different frequencies which are dependent on the Output Data Rate (ODR). A higher cutoff frequency ensures the DC data or slower moving data will be filtered out, allowing only the higher frequencies to pass. The embedded Transient Detection function uses the high-pass filtered data allowing the user to set the threshold and debounce counter. The transient detection feature can be used in the same manner as the motion detection by bypassing the high-pass filter. There is an option in the configuration register to do this. This adds more flexibility to cover various customer use cases.

Many applications use the accelerometer’s static acceleration readings (i.e., tilt) which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered with a low-pass filter where high frequency data is considered noise. However, there are many functions where the accelerometer must analyze dynamic acceleration. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the acceleration. It is simpler to interpret these functions dependent on dynamic acceleration data when the static component has been removed. The Transient Detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 register (0x2E). Registers 0x1D – 0x20 are the dedicated Transient Detection configuration registers. The source register contains directional data to determine the direction of the acceleration, either positive or negative. For details on the benefits of the embedded Transient Detection function along with specific application examples and recommended configuration settings, please refer to Freescale application note, AN4071.

5.8 Tap Detection

The MMA8451Q has embedded single/double and directional tap detection. This function has various customizing timers for setting the pulse time width and the latency time between pulses. There are programmable thresholds for all three axes. The tap detection can be configured to run through the high-pass filter and also through a low-pass filter, which provides more customizing and tunable tap detection schemes. The status register provides updates on the axes where the event was detected and the direction of the tap. For more information on how to configure the device for tap detection please refer to Freescale application note, AN4072.

5.9 Orientation Detection

The MMA8451Q incorporates an advanced algorithm for orientation detection (ability to detect all 6 orientations) with configurable trip points. The embedded algorithm allows the selection of the mid point with the desired hysteresis value.

The MMA8451Q Orientation Detection algorithm confirms the reliability of the function with a configurable Z-lockout angle. Based on known functionality of linear accelerometers, it is not possible to rotate the device about the Z-axis to detect change in acceleration at slow angular speeds. The angle at which the device no longer detects the orientation change is referred to as the "Z-Lockout angle". The device operates down to 14° from the flat position.

For further information on the configuration settings of the orientation detection function, including recommendations for configuring the device to support various application use cases, refer to Freescale application note, AN4068.

Figure 8 shows the definitions of the trip angles going from Landscape to Portrait (A) and then also from Portrait to Landscape (B).

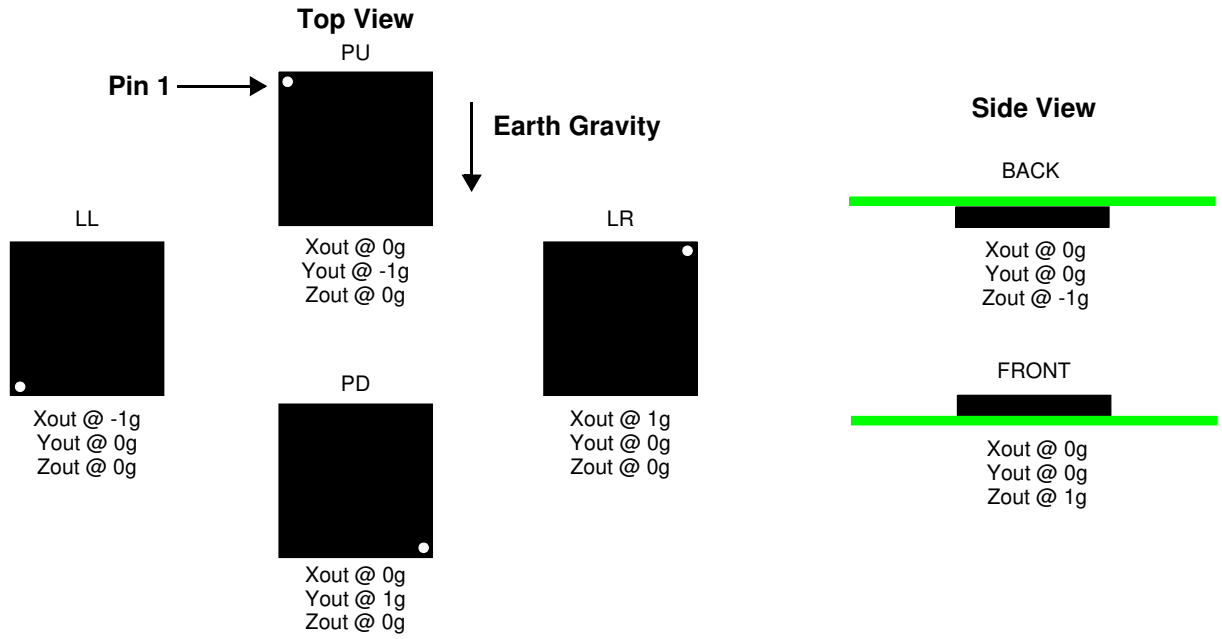


Figure 7. Landscape/Portrait Orientation

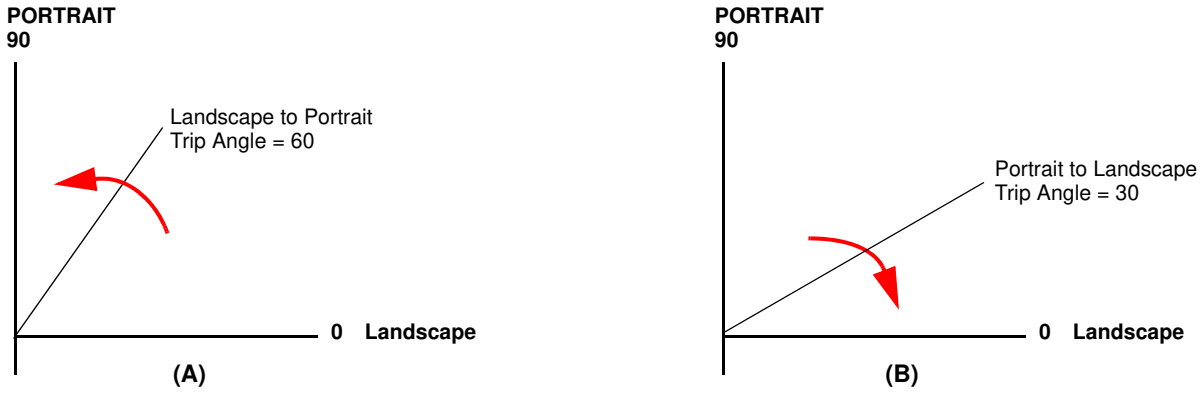


Figure 8. Illustration of Landscape to Portrait Transition (A) and Portrait to Landscape Transition (B)

Figure 9 illustrates the Z-angle lockout region. When lifting the device upright from the flat position it will be active for orientation detection as low as14° from flat. This is user configurable. The default angle is 29° but it can be set as low as 14°.
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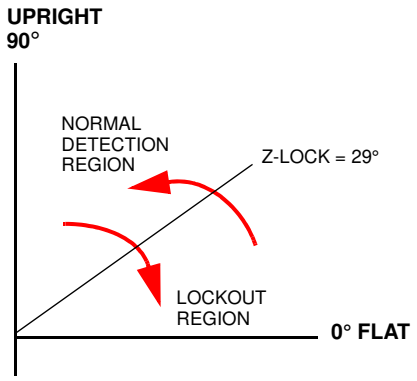

Figure 9. Illustration of Z-Tilt Angle Lockout Transition

5.10 Interrupt Register Configurations

There are seven configurable interrupts in the MMA8451Q: Data Ready, Motion/Freefall, Tap (Pulse), Orientation, Transient, FIFO and Auto-SLEEP events. These seven interrupt sources can be routed to one of two interrupt pins. The interrupt source must be enabled and configured. If the event flag is asserted because the event condition is detected, the corresponding interrupt pin, INT1 or INT2, will assert.

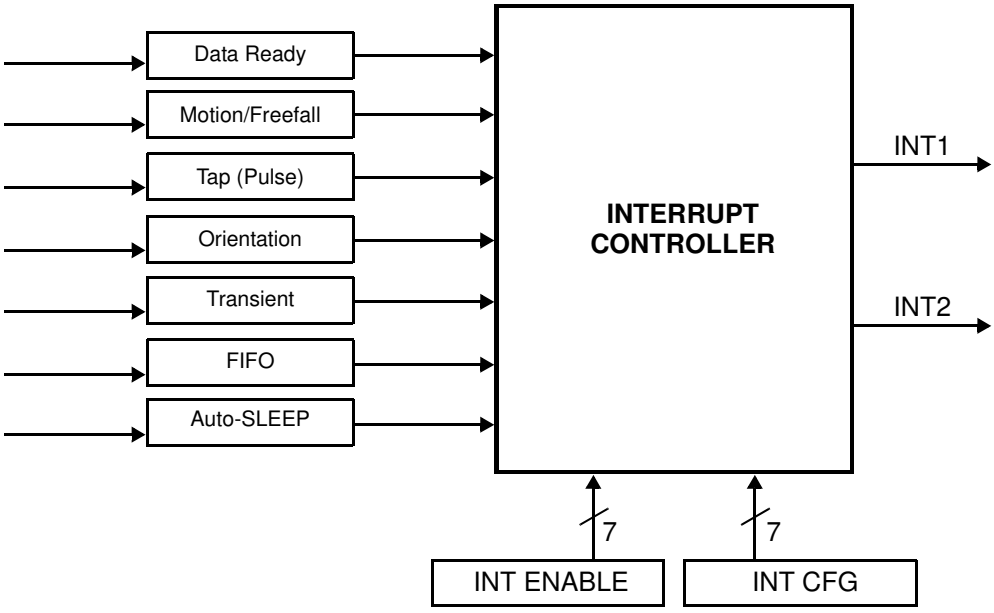

Figure 10. System Interrupt Generation Block Diagram

5.11 Serial I²C Interface

Acceleration data may be accessed through an I²C interface thus making the device particularly suitable for direct interfacing with a microcontroller. The MMA8451Q features an interrupt signal which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device. The MMA8451Q may also be configured to generate other interrupt signals accordingly to the programmable embedded functions of the device for Motion, Freefall, Transient, Orientation, and Tap.

The registers embedded inside the MMA8451Q are accessed through the I²C serial interface (Table 9). To enable the I²C interface, VDDIO line must be tied high (i.e., to the interface supply voltage). If VDD is not present and VDDIO is present, the

MMA8451Q is in off mode and communications on the I²C interface are ignored. The I²C interface may be used for communications between other I²C devices and the MMA8451Q does not affect the I²C bus.

Table 9. Serial Interface Pin Description

Pin Name	Pin Description
SCL	I²C Serial Clock
SDA	I²C Serial Data
SA0	I²C least significant bit of the device address

There are two signals associated with the I²C bus; the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are expected for SDA and SCL. When the bus is free both the lines are high. The I²C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I²C standards (Table 4).

5.11.1 I²C Operation

The transaction on the bus is started through a start condition (START) signal. START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After START has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master. The 9th clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

A LOW to HIGH transition on the SDA line while the SCL line is high is defined as a stop condition (STOP). A data transfer is always terminated by a STOP. A Master may also issue a repeated START during a data transfer. The MMA8451Q expects repeated STARTs to be used to randomly read from specific registers.

The MMA8451Q's standard slave address is a choice between the two sequential addresses 0011100 and 0011101. The selection is made by the high and low logic level of the SA0 (pin 7) input respectively. The slave addresses are factory programmed and alternate addresses are available at customer request. The format is shown in Table 10.

Table 10. I²C Address Selection Table

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0011100 (0x1C)	0011101 (0x1D)	Factory Default

Single Byte Read

The MMA8451Q has an internal ADC that can sample, convert and return sensor data on request. The transmission of an 8-bit command begins on the falling edge of SCL. After the eight clock cycles are used to send the command, note that the data returned is sent with the MSB first once the data is received. Figure 11 shows the timing diagram for the accelerometer 8-bit I²C read operation. The Master (or MCU) transmits a start condition (ST) to the MMA8451Q, slave address ($1D), with the R/W bit set to “0” for a write, and the MMA8451Q sends an acknowledgement. Then the Master (or MCU) transmits the address of the register to read and the MMA8451Q sends an acknowledgement. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8451Q ($1D) with the R/W bit set to “1” for a read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

Multiple Byte Read

When performing a multi-byte read or “burst read”, the MMA8451Q automatically increments the received register address commands after a read command is received. Therefore, after following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8451Q acknowledgment (AK) is received until a no acknowledge (NAK) occurs from the Master followed by a stop condition (SP) signaling an end of transmission.

Single Byte Write

To start a write command, the Master transmits a start condition (ST) to the MMA8451Q, slave address ($1D) with the R/W bit set to “0” for a write, the MMA8451Q sends an acknowledgement. Then the Master (MCU) transmits the address of the register to write to, and the MMA8451Q sends an acknowledgement. Then the Master (or MCU) transmits the 8-bit data to write to the designated register and the MMA8451Q sends an acknowledgement that it has received the data. Since this transmission is

complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA8451Q is now stored in the appropriate register.

Multiple Byte Write

The MMA8451Q automatically increments the received register address commands after a write command is received. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA8451Q acknowledgment (ACK) is received.

Table 11. I²C Device Address Sequence

Command	[6:1] Device Address	[0] SA0	[6:0] Device Address	R/W	8-bit Final Value
Read	001110	0	0x1C	1	0x39
Write	001110	0	0x1C	0	0x38
Read	001110	1	0x1D	1	0x3B
Write	001110	1	0x1D	0	0x3A

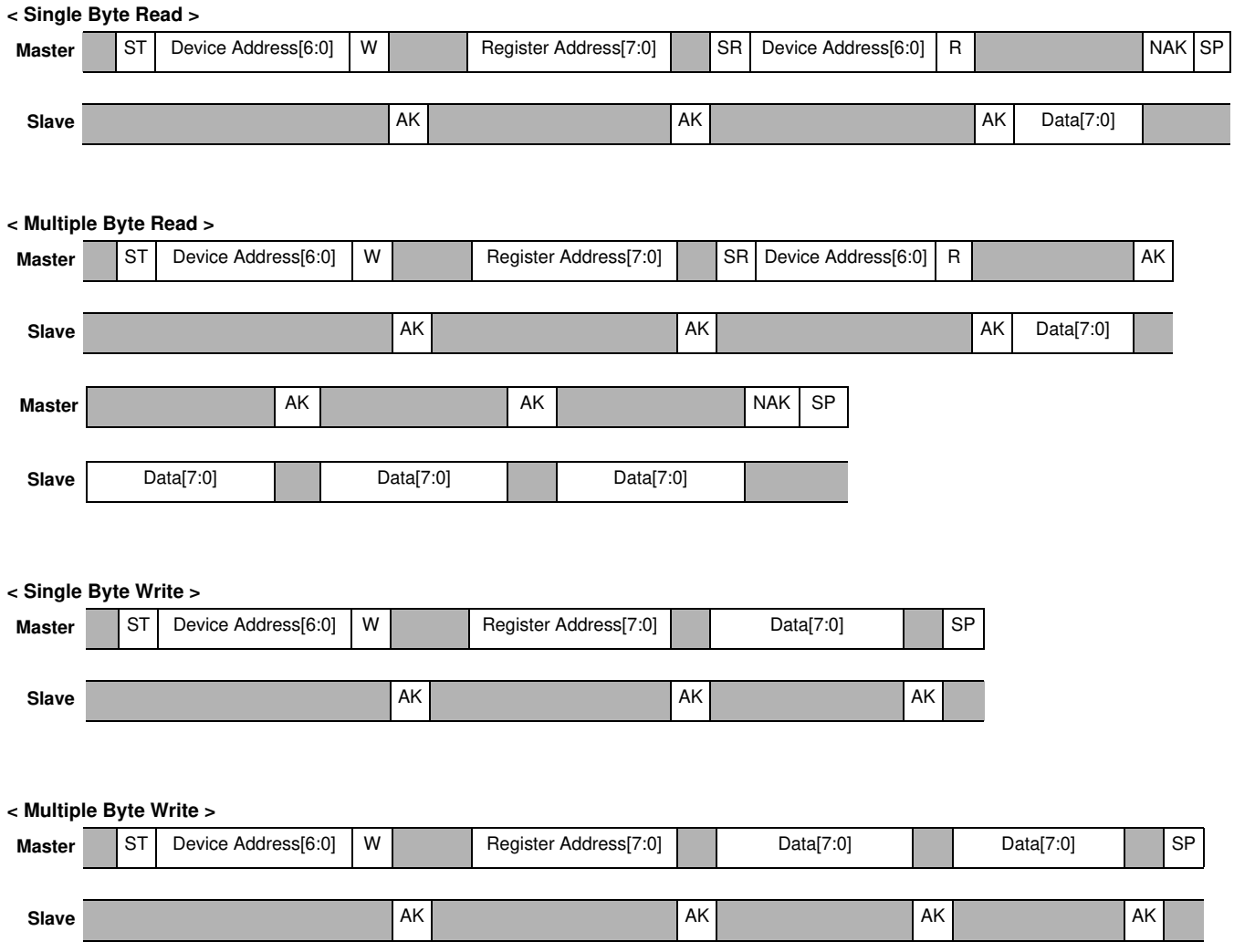

Figure 11. I²C Timing Diagram

6 Register Descriptions

Table 12. Register Address Map

Name	Type	Register Address	Auto-Increment Address				Default	Hex Value	Comment
			FMODE = 0 F_READ = 0	FMODE > 0 F_READ = 0	FMODE = 0 F_READ = 1	FMODE > 0 F_READ = 1			
STATUS/F_STATUS(1)(2)	R	0x00	0x01				00000000	0x00	FMODE = 0, real time status FMODE > 0, FIFO status
OUT_X_MSB(1)(2)	R	0x01	0x02	0x01	**0x03**	**0x01**	Output	—	[7:0] are 8 MSBs of 14-bit sample. / Root pointer to XYZ FIFO data.
OUT_X_LSB(1)(2)	R	0x02	0x03		**0x00**		Output	—	[7:2] are 6 LSBs of 14-bit real-time sample
OUT_Y_MSB(1)(2)	R	0x03	0x04		**0x05**	**0x00**	Output	—	[7:0] are 8 MSBs of 14-bit real-time sample
OUT_Y_LSB(1)(2)	R	0x04	0x05		**0x00**		Output	—	[7:2] are 6 LSBs of 14-bit real-time sample
OUT_Z_MSB(1)(2)	R	0x05	0x06		**0x00**		Output	—	[7:0] are 8 MSBs of 14-bit real-time sample
OUT_Z_LSB(1)(2)	R	0x06	**0x00**				Output	—	[7:2] are 6 LSBs of 14-bit real-time sample
Reserved	R	0x07	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x08	—	—	—	—	—	—	Reserved. Read return 0x00.
F_SETUP(1)(3)	R/W	0x09	0x0A				00000000	0x00	FIFO setup
TRIG_CFG(1)(4)	R/W	0x0A	0x0B				00000000	0x00	Map of FIFO data capture events
SYSMOD(1)(2)	R	0x0B	0x0C				00000000	0x00	Current System Mode
INT_SOURCE(1)(2)	R	0x0C	0x0D				00000000	0x00	Interrupt status
WHO_AM_I(1)	R	0x0D	0x0E				00011010	0x1A	Device ID (0x1A)
XYZ_DATA_CFG(1)(4)	R/W	0x0E	0x0F				00000000	0x00	Dynamic Range Settings
HP_FILTER_CUTOFF(1)(4)	R/W	0x0F	0x10				00000000	0x00	Cutoff frequency is set to 16 Hz @ 800 Hz
PL_STATUS(1)(2)	R	0x10	0x11				00000000	0x00	Landscape/Portrait orientation status
PL_CFG (1)(4)	R/W	0x11	0x12				10000000	0x80	Landscape/Portrait configuration.
PL_COUNT(1)(3)	R/W	0x12	0x13				00000000	0x00	Landscape/Portrait debounce counter
PL_BF_ZCOMP(1)(4)	R/W	0x13	0x14				01000100	0x44	Back/Front, Z-Lock Trip threshold
P_L_THS_REG(1)(4)	R/W	0x14	0x15				10000100	0x84	Portrait to Landscape Trip Angle is 29°
FF_MT_CFG(1)(4)	R/W	0x15	0x16				00000000	0x00	Freefall/Motion functional block configuration
FF_MT_SRC(1)(2)	R	0x16	0x17				00000000	0x00	Freefall/Motion event source register
FF_MT_THS(1)(3)	R/W	0x17	0x18				00000000	0x00	Freefall/Motion threshold register
FF_MT_COUNT(1)(3)	R/W	0x18	0x19				00000000	0x00	Freefall/Motion debounce counter
Reserved	R	0x19	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x1A	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x1B	—	—	—	—	—	—	Reserved. Read return 0x00.
Reserved	R	0x1C	—	—	—	—	—	—	Reserved. Read return 0x00.
TRANSIENT_CFG(1)(4)	R/W	0x1D	0x1E				00000000	0x00	Transient functional block configuration
TRANSIENT_SCR(1)(2)	R	0x1E	0x1F				00000000	0x00	Transient event status register

Table 12. Register Address Map

TRANSIENT_THS[1][3]	R/W	0x1F	0x20	00000000	0x00	Transient event threshold
TRANSIENT_COUNT[1][3]	R/W	0x20	0x21	00000000	0x00	Transient debounce counter
PULSE_CFG[1][4]	R/W	0x21	0x22	00000000	0x00	ELE, Double_XYZ or Single_XYZ
PULSE_SRC[1][2]	R	0x22	0x23	00000000	0x00	EA, Double_XYZ or Single_XYZ
PULSE_THSX[1][3]	R/W	0x23	0x24	00000000	0x00	X pulse threshold
PULSE_THSY[1][3]	R/W	0x24	0x25	00000000	0x00	Y pulse threshold
PULSE_THSZ[1][4]	R/W	0x25	0x26	00000000	0x00	Z pulse threshold
PULSE_TMLT[1][4]	R/W	0x26	0x27	00000000	0x00	Time limit for pulse
PULSE_LTCY[1][4]	R/W	0x27	0x28	00000000	0x00	Latency time for 2nd pulse
PULSE_WIND[1][4]	R/W	0x28	0x29	00000000	0x00	Window time for 2nd pulse
ASLP_COUNT[1][4]	R/W	0x29	0x2A	00000000	0x00	Counter setting for Auto-SLEEP
CTRL_REG1[1][4]	R/W	0x2A	0x2B	00000000	0x00	ODR = 800 Hz, STANDBY Mode.
CTRL_REG2[1][4]	R/W	0x2B	0x2C	00000000	0x00	Sleep Enable, OS Modes, RST, ST
CTRL_REG3[1][4]	R/W	0x2C	0x2D	00000000	0x00	Wake from Sleep, IPOL, PP_OD
CTRL_REG4[1][4]	R/W	0x2D	0x2E	00000000	0x00	Interrupt enable register
CTRL_REG5[1][4]	R/W	0x2E	0x2F	00000000	0x00	Interrupt pin (INT1/INT2) map
OFF_X[1][4]	R/W	0x2F	0x30	00000000	0x00	X-axis offset adjust
OFF_Y[1][4]	R/W	0x30	0x31	00000000	0x00	Y-axis offset adjust
OFF_Z[1][4]	R/W	0x31	**0x0D**	00000000	0x00	Z-axis offset adjust
Reserved (do not modify)		0x40 – 7F	—	—	—	Reserved. Read return 0x00.

1. Register contents are preserved when transition from ACTIVE to STANDBY mode occurs.
2. Register contents are reset when transition from STANDBY to ACTIVE mode occurs.
3. Register contents can be modified anytime in STANDBY or ACTIVE mode. A write to this register will cause a reset of the corresponding internal system debounce counter.
4. Modification of this register's contents can only occur when device is STANDBY mode except CTRL_REG1 ACTIVE bit and CTRL_REG2 RST bit.

Note: Auto-increment addresses which are not a simple increment are highlighted in **bold**. The auto-increment addressing is only enabled when device registers are read using I^2C burst read mode. Therefore the internal storage of the auto-increment address is cleared whenever a stop-bit is detected.

6.1 Data Registers

The following are the data registers for the MMA8451Q. For more information on data manipulation of the MMA8451Q, refer to application note, AN4076.

When the F_MODE bits found in Register 0x09 (F_SETUP), bits 7 and 6 are both cleared (the FIFO is not on). Register 0x00 reflects the real-time status information of the X, Y and Z sample data. When the F_MODE value is greater than zero the FIFO is on (in either Fill, Circular or Trigger mode). In this case Register 0x00 will reflect the status of the FIFO. It is expected when the FIFO is on that the user will access the data from Register 0x01 (X_MSB) for either the 14-bit or 8-bit data. When accessing the 8-bit data the F_READ bit (Register 0x2A) is set which modifies the auto-incrementing to skip over the LSB data. When F_READ bit is cleared the 14-bit data is read accessing all 6 bytes sequentially (X_MSB, X_LSB, Y_MSB, Y_LSB, Z_MSB, Z_LSB).

F_MODE = 00: 0x00 STATUS: Data Status Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Table 13. STATUS Description

ZYXOW	X, Y, Z-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous X, Y, or Z data was overwritten by new X, Y, or Z data before it was read
ZOW	Z-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous Z-axis data was overwritten by new Z-axis data before it was read
YOW	Y-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous Y-axis data was overwritten by new Y-axis data before it was read
XOW	X-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred 1: Previous X-axis data was overwritten by new X-axis data before it was read
ZYXDR	X, Y, Z-axis new Data Ready. Default value: 0 0: No new set of data ready 1: A new set of data is ready
ZDR	Z-axis new Data Available. Default value: 0 0: No new Z-axis data is ready 1: A new Z-axis data is ready
YDR	Y-axis new Data Available. Default value: 0 0: No new Y-axis data ready 1: A new Y-axis data is ready
XDR	X-axis new Data Available. Default value: 0 0: No new X-axis data ready 1: A new X-axis data is ready

ZYXOW is set whenever a new acceleration data is produced before completing the retrieval of the previous set. This event occurs when the content of at least one acceleration data register (i.e., OUT_X, OUT_Y, OUT_Z) has been overwritten. ZYXOW is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the active channels are read.

ZOW is set whenever a new acceleration sample related to the Z-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. ZOW is cleared anytime OUT_Z_MSB register is read.

YOW is set whenever a new acceleration sample related to the Y-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. YOW is cleared anytime OUT_Y_MSB register is read.

XOW is set whenever a new acceleration sample related to the X-axis is generated before the retrieval of the previous sample. When this occurs the previous sample is overwritten. XOW is cleared anytime OUT_X_MSB register is read.

ZYXDR signals that a new sample for any of the enabled channels is available. ZYXDR is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the enabled channels are read.

ZDR is set whenever a new acceleration sample related to the Z-axis is generated. ZDR is cleared anytime OUT_Z_MSB register is read.

YDR is set whenever a new acceleration sample related to the Y-axis is generated. YDR is cleared anytime OUT_Y_MSB register is read.

XDR is set whenever a new acceleration sample related to the X-axis is generated. XDR is cleared anytime OUT_X_MSB register is read.

Data Registers: 0x01 OUT_X_MSB, 0x02 OUT_X_LSB, 0x03 OUT_Y_MSB, 0x04 OUT_Y_LSB, 0x05 OUT_Z_MSB, 0x06 OUT_Z_LSB

These registers contain the X-axis, Y-axis, and Z-axis14-bit output sample data expressed as 2's complement numbers.

Note: The sample data output registers store the current sample data if the FIFO data output register driver is disabled, but if the FIFO data output register driver is enabled (F_MODE > 00) the sample data output registers point to the head of the FIFO buffer (Register 0x01 X_MSB) which contains the previous 32 X, Y, and Z data samples. Data Registers F_MODE = 00

0x01: OUT_X_MSB: X_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD13	XD12	XD11	XD10	XD9	XD8	XD7	XD6

0x02: OUT_X_LSB: X_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD5	XD4	XD3	XD2	XD1	XD0	0	0

0x03: OUT_Y_MSB: Y_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD13	YD12	YD11	YD10	YD9	YD8	YD7	YD6

0x04: OUT_Y_LSB: Y_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD5	YD4	YD3	YD2	YD1	YD0	0	0

0x05: OUT_Z_MSB: Z_MSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6

0x06: OUT_Z_LSB: Z_LSB Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD5	ZD4	ZD3	ZD2	ZD1	ZD0	0	0

OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x01 to 0x06 to reduce reading the status followed by 14-bit axis data to 7 bytes. If the F_READ bit is set (0x2A bit 1), auto increment will skip over LSB registers. This will shorten the data acquisition from 7 bytes to 4 bytes. The LSB registers can only be read immediately following the read access of the corresponding MSB register. A random read access to the LSB registers is not possible. Reading the MSB register and then the LSB register in sequence ensures that both bytes (LSB and MSB) belong to the same data sample, even if a new data sample arrives between reading the MSB and the LSB byte.

6.2 32 Sample FIFO

The following registers are used to configure the FIFO. For more information on the FIFO please refer to AN4073.

F_MODE > 0 0x00: F_STATUS FIFO Status Register

When F_MODE > 0, Register 0x00 becomes the FIFO Status Register which is used to retrieve information about the FIFO. This register has a flag for the overflow and watermark. It also has a counter that can be read to obtain the number of samples stored in the buffer when the FIFO is enabled.

0x00: F_STATUS: FIFO STATUS Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_OVF	F_WMRK_FLAG	F_CNT5	F_CNT4	F_CNT3	F_CNT2	F_CNT1	F_CNT0

Table 14. FIFO Flag Event Description

F_OVF	F_WMRK_FLAG	Event Description
0	—	No FIFO overflow events detected.
1	—	FIFO event detected; FIFO has overflowed.
—	0	No FIFO watermark events detected.
—	1	FIFO Watermark event detected. FIFO sample count is greater than watermark value. If F_MODE = 11, Trigger Event detected.

The F_OVF and F_WMRK_FLAG flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit flag in the interrupt source register (INT_SOURCE) by reading the F_STATUS register. In this case, the SRC_FIFO bit in the INT_SOURCE register will be set again when the next data sample enters the FIFO. Therefore the F_OVF bit flag will remain asserted while the FIFO has overflowed and the F_WMRK_FLAG bit flag will remain asserted while the F_CNT value is equal to or greater than then F_WMRK value. If the FIFO overflow flag is cleared and if F_MODE = 11 then the FIFO overflow flag will remain 0 before the trigger event even if the FIFO is full and overflows. If the FIFO overflow flag is set and if F_MODE is = 11, the FIFO has stopped accepting samples.

Table 15. FIFO Sample Count Description

F_CNT[5:0]	FIFO sample counter. Default value: 00_0000. (00_0001 to 10_0000 indicates 1 to 32 samples stored in FIFO

F_CNT[5:0] bits indicate the number of acceleration samples currently stored in the FIFO buffer. Count 000000 indicates that the FIFO is empty.

0x09: F_SETUP FIFO Setup Register

0x09 F_SETUP: FIFO Setup Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_MODE1	F_MODE0	F_WMRK5	F_WMRK4	F_WMRK3	F_WMRK2	F_WMRK1	F_WMRK0

Table 16. F_SETUP Description

BITS	Description
F_MODE[1:0](1)(2)	FIFO buffer overflow mode. Default value: 0. **00:** FIFO is disabled. **01:** FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample. **10:** FIFO stops accepting new samples when overflowed. **11:** Trigger mode. The FIFO will be in a circular mode up to the number of samples in the watermark. The FIFO will be in a circular mode until the trigger event occurs after that the FIFO will continue to accept samples for 32-WMRK samples and then stop receiving further samples. This allows data to be collected both before and after the trigger event and it is definable by the watermark setting. The FIFO is flushed whenever the FIFO is disabled, during an automatic ODR change (Auto-WAKE/SLEEP), or transitioning from STANDBY mode to ACTIVE mode. Disabling the FIFO (F_MODE = 00) resets the F_OVF, F_WMRK_FLAG, F_CNT to zero. A FIFO overflow event (i.e., F_CNT = 32) will assert the F_OVF flag and a FIFO sample count equal to the sample count watermark (i.e., F_WMRK) asserts the F_WMRK_FLAG event flag.
F_WMRK[5:0](2)	FIFO Event Sample Count Watermark. Default value: 00_0000. These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag is raised when FIFO sample count F_CNT[5:0] ≥ F_WMRK[5:0] watermark. Setting the F_WMRK[5:0] to 00_0000 will disable the FIFO watermark event flag generation. Also used to set the number of pre-trigger samples in Trigger mode.

1. Bit field can be written in ACTIVE mode.
2. Bit field can be written in STANDBY mode.

The FIFO mode can be changed while in the active state. The mode must first be disabled F_MODE = 00 then the mode can be switched between Fill mode, Circular mode and Trigger mode.

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data. The FIFO update rate is dictated by the selected system ODR. In ACTIVE mode the ODR is set by the DR bits in the CTRL_REG1 register. When Auto-SLEEP is active the ODR is set by the ASLP_RATE field in the CTRL_REG1 register.

When a byte is read from the FIFO buffer the oldest sample data in the FIFO buffer is returned and also deleted from the front of the FIFO buffer, while the FIFO sample count is decremented by one. It is assumed that the host application shall use the I^2C multi-byte read transaction to empty the FIFO.

0x0A: TRIG_CFG

In the trigger configuration register the bits that are set (logic ‘1’) control which function may trigger the FIFO to its interrupt and conversely bits that are cleared (logic ‘0’) indicate which function has not asserted its interrupt.

The bits set are rising edge sensitive, and are set by a low to high state change and reset by reading the appropriate source register.

0x0A: TRIG_CFG Trigger Configuration Register (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	Trig_TRANS	Trig_LNDPRT	Trig_PULSE	Trig_FF_MT	—	—

Table 17. Trigger Configuration Description

INT_SOURCE	Description
Trig_TRANS	Transient interrupt trigger bit. Default value: 0
Trig_LNDPRT	Landscape/Portrait Orientation interrupt trigger bit. Default value: 0
Trig_PULSE	Pulse interrupt trigger bit. Default value: 0
Trig_FF_MT	Freefall/Motion trigger bit. Default value: 0

0x0B: SYSMOD System Mode Register

The System mode register indicates the current device operating mode. Applications using the Auto-SLEEP/WAKE mechanism should use this register to synchronize the application with the device operating mode transitions. The System mode register also indicates the status of the FIFO gate error and number of samples since the gate error occurred.

0x0B: SYSMOD: System Mode Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FGERR	FGT_4	FGT_3	FGT_2	FGT_1	FGT_0	SYSMOD1	SYSMOD0

Table 18. SYSMOD Description

FGERR	FIFO Gate Error. Default value: 0. 0: No FIFO Gate Error detected. 1: FIFO Gate Error was detected. Emptying the FIFO buffer clears the FGERR bit in the SYS_MOD register. See section 0x2C: CTRL_REG3 Interrupt Control Register for more information on configuring the FIFO Gate function.
FGT[4:0]	Number of ODR time units since FGERR was asserted. Reset when FGERR Cleared. Default value: 0_0000
SYSMOD[1:0]	System Mode. Default value: 00. 00: STANDBY mode 01: WAKE mode 10: SLEEP mode

0x0C: INT_SOURCE System Interrupt Status Register

In the interrupt source register the status of the various embedded features can be determined. The bits that are set (logic '1') indicate which function has asserted an interrupt and conversely the bits that are cleared (logic '0') indicate which function has not asserted or has deasserted an interrupt. **The bits are set by a low to high transition and are cleared by reading the appropriate interrupt source register.** The SRC_DRDY bit is cleared by reading the X, Y and Z data. It is not cleared by simply reading the Status Register (0x00).

0x0C: INT_SOURCE: System Interrupt Status Register (Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT	—	SRC_DRDY

Table 19. INT_SOURCE Description

INT_SOURCE	Description
SRC_ASLP	Auto-SLEEP/WAKE interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt event that can cause a WAKE to SLEEP or SLEEP to WAKE system mode transition has occurred. Logic '0' indicates that no WAKE to SLEEP or SLEEP to WAKE system mode transition interrupt event has occurred. **WAKE to SLEEP** transition occurs when no interrupt occurs for a time period that exceeds the user specified limit (ASLP_COUNT). This causes the system to transition to a user specified low ODR setting. **SLEEP to WAKE** transition occurs when the user specified interrupt event has woken the system; thus causing the system to transition to a user specified high ODR setting. Reading the SYSMOD register clears the SRC_ASLP bit.
SRC_FIFO	FIFO interrupt status bit. Default value: 0. Logic '1' indicates that a FIFO interrupt event such as an overflow event or watermark has occurred. Logic '0' indicates that no FIFO interrupt event has occurred. FIFO interrupt event generators: FIFO Overflow, or (Watermark: F_CNT = F_WMRK) and the interrupt has been enabled. This bit is cleared by reading the F_STATUS register.
SRC_TRANS	Transient interrupt status bit. Default value: 0. Logic '1' indicates that an acceleration transient value greater than user specified threshold has occurred. Logic '0' indicates that no transient event has occurred. This bit is asserted whenever "EA" bit in the TRANS_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the TRANS_SRC register.
SRC_LNDPRT	Landscape/Portrait Orientation interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt was generated due to a change in the device orientation status. Logic '0' indicates that no change in orientation status was detected. This bit is asserted whenever "NEWLP" bit in the PL_STATUS is asserted and the interrupt has been enabled. This bit is cleared by reading the PL_STATUS register.
SRC_PULSE	Pulse interrupt status bit. Default value: 0. Logic '1' indicates that an interrupt was generated due to single and/or double pulse event. Logic '0' indicates that no pulse event was detected. This bit is asserted whenever "EA" bit in the PULSE_SRC is asserted and the interrupt has been enabled. This bit is cleared by reading the PULSE_SRC register.
SRC_FF_MT	Freefall/Motion interrupt status bit. Default value: 0. Logic '1' indicates that the Freefall/Motion function interrupt is active. Logic '0' indicates that no Freefall or Motion event was detected. This bit is asserted whenever "EA" bit in the FF_MT_SRC register is asserted and the FF_MT interrupt has been enabled. This bit is cleared by reading the FF_MT_SRC register.
SRC_DRDY	Data Ready Interrupt bit status. Default value: 0. Logic '1' indicates that the X, Y, Z data ready interrupt is active indicating the presence of new data and/or data overrun. Otherwise if it is a logic '0' the X, Y, Z interrupt is not active. This bit is asserted when the ZYXOW and/or ZYXDR is set and the interrupt has been enabled. This bit is cleared by reading the X, Y, and Z data.