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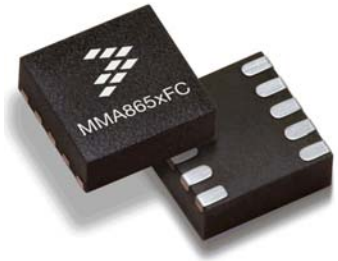
RoHS

MMA8652FC, 3-Axis, 12-bit, Digital Accelerometer

MMA8652FC

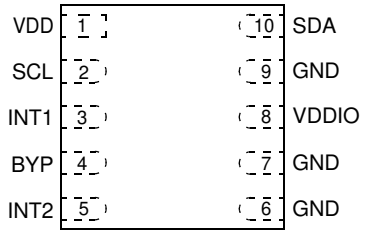
The MMA8652FC is an intelligent, low-power, three-axis, capacitive micromachined accelerometer with 12 bits of resolution. This accelerometer is packed with embedded functions with flexible user-programmable options, configurable to two interrupt pins. Embedded interrupt functions enable overall power savings, by relieving the host processor from continuously polling data. There is access to either low-pass or high-pass filtered data, which minimizes the data analysis required for jolt detection and faster transitions. The device can be configured to generate inertial wake-up interrupt signals from any combination of the configurable embedded functions, enabling the MMA8652FC to monitor inertial events while remaining in a low-power mode during periods of inactivity. The MMA8652FC is available in a small 10-pin DFN package (2 mm x 2 mm x 1 mm).

Top and Bottom View



10-pin DFN
2 mm x 2 mm x 1 mm
Case 98ASA00301D

Top View



Pin Connections

Features

- 1.95 V to 3.6 V supply voltage
- 1.62 V to 3.6 V digital interface voltage
- ±2 g, ±4 g, and ±8 g dynamically selectable full-scale ranges
- Output Data Rates (ODR) from 1.56 Hz to 800 Hz
- 12-bit digital output
- I^2C digital output interface with programmable interrupts
- Four embedded channels of configurable motion detection (Freefall, Motion, Pulse, Transient)
- Orientation (Portrait/Landscape) detection with programmable hysteresis
- Configurable automatic ODR change triggered by the Auto-Wake/Sleep state change
- 32-sample FIFO
- High-Pass Filter Data available per sample and through the FIFO
- Self-Test

Typical applications

- Tilt compensation in e-compass applications
- Static orientation detection (Portrait/Landscape, Up/Down, Left/Right, Back/Front position identification)
- Notebook, tablet, e-reader, and laptop tumble and freefall detection
- Real-time orientation detection (virtual reality and gaming 3D user orientation feedback)
- Real-time activity analysis (pedometer step counting, freefall drop detection for HDD, dead-reckoning GPS backup)
- Motion detection for portable product power saving (Auto-SLEEP and Auto-WAKE for cell phone, PDA, GPS, gaming)
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)
- User interface (tilt menu scrolling, tap detection for button replacement)

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
MMA8652FCR1	-40°C to +85°C	DFN-10	Tape and Reel

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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Table 1. Feature comparison of the MMA865xFC devices

Feature	MMA8652FC	MMA8653FC
ADC Resolution (bits)	12	10
Digital Sensitivity in 2 g mode (counts/g)	1024	256
Low-Power Mode	Yes	Yes
Auto-WAKE	Yes	Yes
Auto-SLEEP	Yes	Yes
32-Level FIFO	Yes	No
Low-Pass Filter	Yes	Yes
High-Pass Filter	Yes	No
Transient Detection with High-Pass Filter	Yes	No
Fixed Orientation Detection	No	Yes
Programmable Orientation Detection	Yes	No
Data-Ready Interrupt	Yes	Yes
Single-Tap Interrupt	Yes	No
Double-Tap Interrupt	Yes	No
Directional Tap Interrupt	Yes	No
Freefall Interrupt	Yes	Yes
Motion Interrupt with Direction	Yes	No

Contents

Related Documentation

The MMA8652FC device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA8652FC.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Block Diagram and Pin Descriptions

1.1 Block diagram

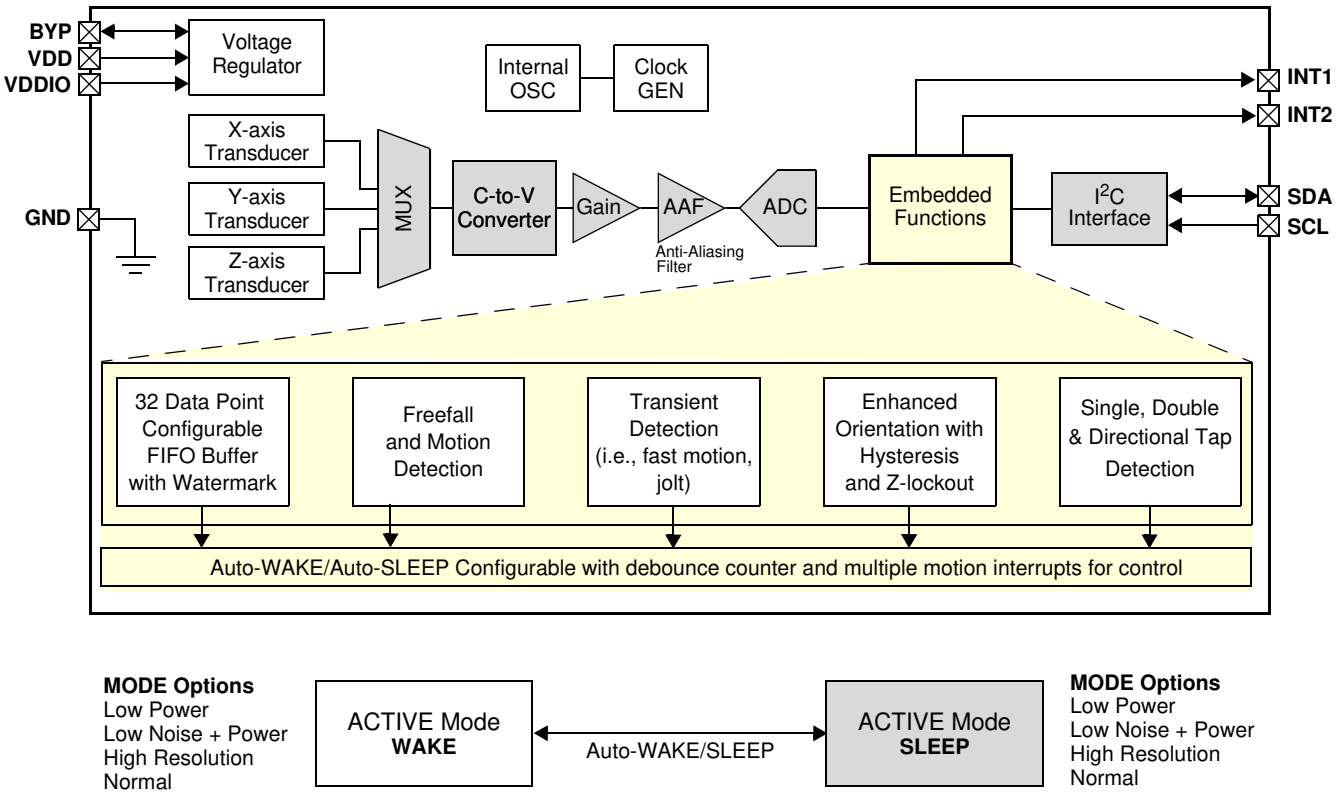


Figure 1. MMA8652FC block diagram

1.2 Pin descriptions

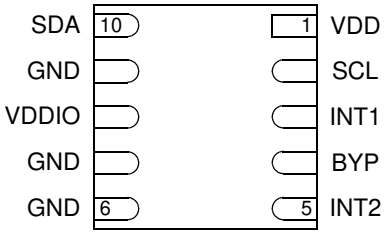


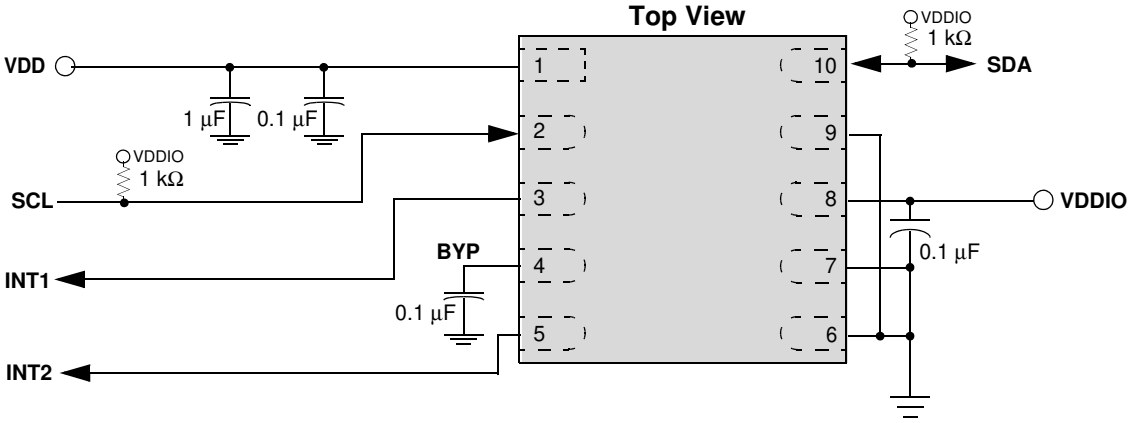
Figure 2. Pin connections (bottom view)

Table 1. Pin descriptions

Pin #	Pin Name	Description	Notes
1	VDD	Power supply	Device power is supplied through the VDD line. Power supply decoupling capacitors should be placed as close as possible to pin 1 and pin 8 of the device.
2	SCL(1)	I^2C Serial Clock	7-bit I^2C device address is 0x1D.
3	INT1	Interrupt 1 output	The interrupt source and pin settings are user-programmable through the I^2C interface.
4	BYP	Internal regulator output capacitor connection	
5	INT2	Interrupt 2 output	See INT1.
6	GND	Ground	
7	GND	Ground	
8	VDDIO	Digital Interface Power supply	
9	GND	Ground	
10	SDA(1)	I^2C Serial Data	See SCL.

1. The control signals SCL and SDA are not tolerant of voltages higher than VDDIO + 0.3 V. If VDDIO is removed, then the control signals SCL and SDA will clamp any logic signals with their internal ESD protection diodes. The SDA and SCL I^2C connections are open drain, and therefore require a pullup resistor to VDDIO.

1.3 Typical application circuit



Note: 4.7 kΩ Pullup resistors on INT1/INT2 can be added for open-drain operation.

Figure 3. Typical application circuit

2 Mechanical and Electrical Specifications

2.1 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Maximum ratings

Rating	Symbol	Value	Unit
Maximum acceleration (all axes, 100 µs)	g_{max}	10,000	g
Supply voltage	VDD	–0.3 to +3.6	V
Input voltage on any control pin (SCL, SDA)	Vin	–0.3 to VDDIO + 0.3	V
Drop test	D_{drop}	1.8	m
Operating temperature range	T_{OP}	–40 to +85	°C
Storage temperature range	T_{STG}	–40 to +125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human body model	HBM	±2000	V
Machine model	MM	±200	V
Charge device model	CDM	±500	V
Latch-up current at T = 85°C	I_{LU}	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part.

This part is ESD-sensitive. Improper handling can cause permanent damage to the part.

2.2 Mechanical characteristics

Table 4. Mechanical characteristics at VDD = 2.5 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Full-Scale measurement range	FS	FS[1:0] set to 00 ±2 g mode		±2		g
		FS[1:0] set to 01 ±4 g mode		±4		
		FS[1:0] set to 10 ±8 g mode		±8		
Sensitivity	So	FS[1:0] set to 00 ±2 g mode		1024		LSB/g
		FS[1:0] set to 01 ±4 g mode		512		
		FS[1:0] set to 10 ±8 g mode		256		
Sensitivity accuracy	Soa			±2.5		%
Sensitivity change vs. temperature	TCS	–40°C to 85°C		±0.0074		%/°C
Zero-g level offset accuracy (1)	TyOff			±25		mg
Zero-g level offset accuracy, post-board mount (2)	TyOffPBM			±33.5		mg
Zero-g level change vs. temperature	TCO	–40°C to 85°C		±0.27		mg/°C
Self-Test output change (±2 g mode)	STOC	x		+90		LSB
		y		+104		
		z		+782		
ODR accuracy	ODRa			±3.1		%
Output data bandwidth	BW		ODR/3		ODR/2	Hz
Output noise	RMS	Normal mode ODR = 400 Hz		182		µg/√Hz
Operating temperature range	T_{AGOC}		–40		85	°C

1. Before board mount.
2. Post-board mount offset specifications are based on an 8-layer PCB, relative to 25°C.

2.3 Electrical characteristics

Table 5. Electrical characteristics at VDD = 2.5 V, VDDIO = 1.8 V, T = 25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply voltage	VDD		1.95	2.5	3.6	V
Interface supply voltage	VDDIO		1.62	1.8	3.6	V
Low Power mode	$I_{dd}LP$	ODR = 1.563 Hz		6.5		µA
		ODR = 6.25 Hz		6.5		
		ODR = 12.5 Hz		6.5		
		ODR = 50 Hz		15		
		ODR = 100 Hz		26		
		ODR = 200 Hz		49		
		ODR = 400 Hz		94		
		ODR = 800 Hz		184		
Normal mode	I_{dd}	ODR = 1.563 Hz		27		µA
		ODR = 6.25 Hz		27		
		ODR = 12.5 Hz		27		
		ODR = 50 Hz		27		
		ODR = 100 Hz		49		
		ODR = 200 Hz		94		
		ODR = 400 Hz		184		
		ODR = 800 Hz		184		
Boot-Up current	I_{ddBoot}	VDD = 2.5 V, the current during the Boot sequence is integrated over 0.5 ms, using a recommended bypass cap			1	mA
Value of capacitor on BYP pin	Cap	–40°C to 85°C	75	100	470	nF
Standby current	I_{ddStby}	25°C		1.4	5	µA
Digital high-level input voltage SCL, SDA	VIH	VDD = 3.6 V, VDDIO = 3.6 V	0.7*VDDIO			V
Digital low-level input voltage SCL, SDA	VIL	VDD = 1.95 V, VDDIO = 1.62 V			0.3*VDDIO	V
High-level output voltage INT1, INT2	VOH	VDD = 3.6 V, VDDIO = 3.6 V, I_O = 500 µA	0.9*VDDIO			V
Low-level output voltage INT1, INT2	VOL	VDD = 1.95 V, VDDIO = 1.62 V, I_O = 500 µA			0.1*VDDIO	V
Low-level output voltage SDA	VOLS	I_O = 3 mA			0.4	V
Output source current INT1, INT2	I_{source}	Voltage high level VOUT = 0.9 x VDDIO		2		mA
Output sink current INT1, INT2	I_{sink}	Voltage high level VOUT = 0.9 x VDDIO		3		mA
Power-on ramp time	Tpr		0.001		1000	ms
Boot time	Tbt	Time from VDDIO on and VDD > VDD min until I^2C is ready for operation, Cbyp = 100 nf		350	500	µs
Turn-on time	Ton1	Time to obtain valid data from Standby mode to Active mode			2/ODR + 1 ms	-
Turn-on time	Ton2	Time to obtain valid data from valid voltage applied			2/ODR + 2 ms	-
Operating temperature range	T_{AGOC}		–40		85	°C

2.4 I²C interface characteristic

Table 6. I²C slave timing values (1)

Parameter	Symbol	I²C Fast Mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0	400	kHz
Bus-free time between STOP and START condition	t_{BUF}	1.3		µs
(Repeated) START hold time	$t_{HD;STA}$	0.6		µs
Repeated START setup time	$t_{SU;STA}$	0.6		µs
STOP condition setup time	$t_{SU;STO}$	0.6		µs
SDA data hold time	$t_{HD;DAT}$	0.05	0.9 (2)	µs
SDA setup time	$t_{SU;DAT}$	100		ns
SCL clock low time	t_{LOW}	1.3		µs
SCL clock high time	t_{HIGH}	0.6		µs
SDA and SCL rise time	t_r	20 + 0.1 C_b (3)	300	ns
SDA and SCL fall time	t_f	20 + 0.1 C_b (3)	300	ns
SDA valid time (4)	$t_{VD;DAT}$		0.9 (2)	µs
SDA valid acknowledge time (5)	$t_{VD;ACK}$		0.9 (2)	µs
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	ns
Capacitive load for each bus line	Cb		400	pF

1. All values referred to VIH(min) (0.3 VDD) and VIL(max) (0.7 VDD) levels.
2. This device does not stretch the LOW period (tLOW) of the SCL signal.
3. C_b = total capacitance of one bus line in pF.
4. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

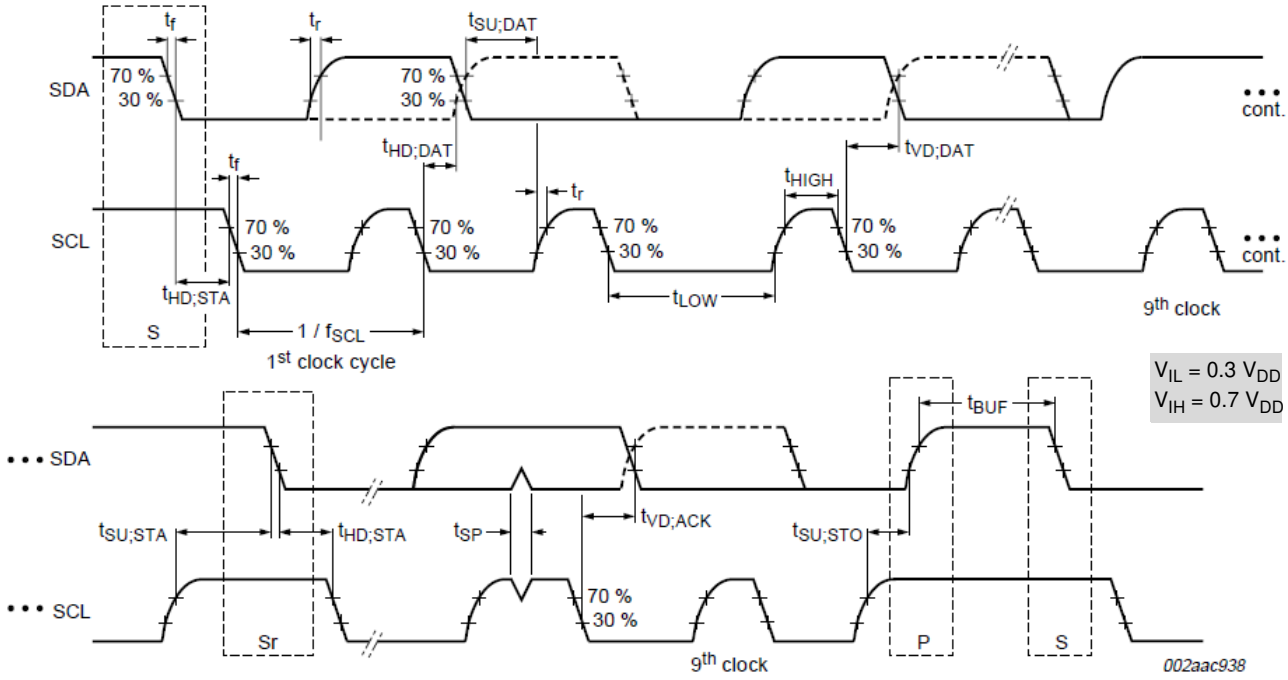


Figure 4. I²C slave timing diagram

3 Terminology

3.1 Sensitivity

The sensitivity is represented in counts/g.

- In ±2 g mode, sensitivity = 1024counts/g.
- In ±4 g mode, sensitivity = 512counts/g.
- In ±8 g mode, sensitivity = 256counts/g.

3.2 Zero-g offset

Zero-g Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if the sensor is stationary. A sensor stationary on a horizontal surface will measure 0 g in X-axis and 0 g in Y-axis, whereas the Z-axis will measure 1 g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT Registers 0x00, data expressed as a 2's complement number). A deviation from ideal value in this case is called Zero-g offset.

Offset is to some extent a result of stress on the MEMS sensor, and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress.

3.3 Self-Test

Self-Test can be used to verify the transducer and signal chain functionality without the need to apply external mechanical stimulus.

When Self-Test is activated:

- An electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case, the sensor outputs will exhibit a change in their DC levels which, are related to the selected full scale through the device sensitivity.
- The device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

4 Modes of Operation

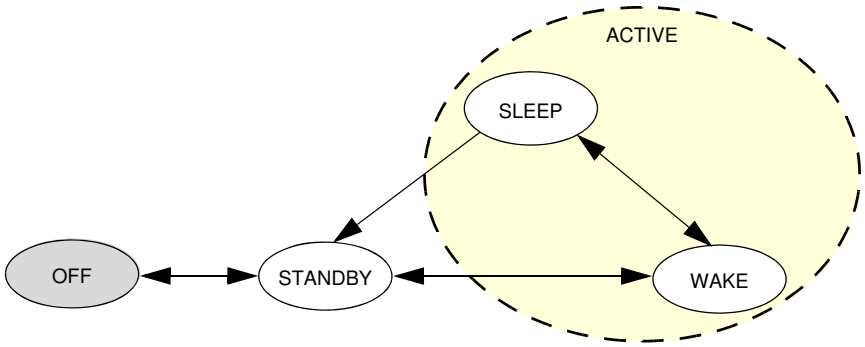


Figure 5. Operating modes for MMA8652FC

Table 7. Operating modes

Mode	I^2C Bus State	VDD	VDDIO	Description
OFF	Powered down	<1.8 V	VDDIO can be > VDD	• The device is powered off. • All analog and digital blocks are shutdown. • I^2C bus inhibited.
STANDBY	I^2C communication with MMA8652FC is possible	ON	VDDIO = High VDD = High ACTIVE bit is cleared	• Only digital blocks are enabled. • Analog subsystem is disabled. • Internal clocks disabled.
ACTIVE (WAKE/SLEEP)	I^2C communication with MMA8652FC is possible	ON	VDDIO = High VDD = High ACTIVE bit is set	All blocks are enabled (digital, analog).

Some registers are reset when transitioning from STANDBY to ACTIVE. These registers are all noted in the device memory map register table.

The SLEEP and WAKE modes are ACTIVE modes. For more information about how to use the SLEEP and WAKE modes and how to transition between these modes, see Section 5.

5 Functionality

The MMA8652FC is a low-power, digital output 3-axis linear accelerometer with a I^2C interface with embedded logic used to detect events and notify an external microprocessor over interrupt lines.

- 8-bit or 12-bit data, high-pass filtered data, 8-bit or 12-bit configurable 32-sample FIFO
- Four different oversampling options that allow for the optimum resolution vs. current consumption trade-off to be made for a given application
- Low-power and auto-WAKE/SLEEP modes for reducing current consumption
- Single/double tap with directional information (one channel)
- Motion detection with directional information or Freefall (one channel)
- Transient/jolt detection based on a high-pass filter, with a settable threshold for detecting the change in acceleration above a threshold with directional information (one channel)
- Flexible user-configurable portrait landscape detection algorithm, for addressing screen orientation
- Two independent interrupt output pins that are programmable among seven interrupt sources (Data Ready, Motion/Freefall, Tap, Orientation, Transient, FIFO, Auto-WAKE)

All functionality is available in ±2 g, ±4 g or ±8 g dynamic measurement ranges. There are many configuration settings for enabling all of the different functions. Separate application notes are available to help configure the device for each embedded functionality.

5.1 Device calibration

The device is factory calibrated for sensitivity and Zero-g offset for each axis. The trim values are stored in Non-Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the circuitry. In normal use, further calibration in the end application is not necessary. However, the MMA8652FC allows you to adjust the offset for each axis after power-up, by changing the default offset values. The user offset adjustments are stored in three volatile 8-bit registers (OFF_X, OFF_Y, OFF_Z).

5.2 8-bit or 12-bit

The measured acceleration data is stored in the following registers as 2's complement 12-bit:

- OUT_X_MSB, OUT_X_LSB
- OUT_Y_MSB, OUT_Y_LSB
- OUT_Z_MSB, OUT_Z_LSB

The most significant eight bits of each axis are stored in OUT_X (Y, Z)_MSB, so applications needing only 8-bit results can use these three registers (and ignore the OUT_X/Y/Z_LSB registers). To use only 8-bit results, the F_READ bit in CTRL_REG1 must be set. When the F_READ bit is cleared, the fast read mode is disabled.

- **When the full-scale is set to ±2 g**, the measurement range is –2 g to +1.999 g, and each count corresponds to (1/1024) g (0.98 mg) at 12-bit resolution.
- **When the full-scale is set to ±4 g**, the measurement range is –4 g to +3.998 g, and each count corresponds to (1/512) g
- (1.96 mg) at 12-bit resolution.
- **When the full-scale is set to ±8 g**, the measurement range is –8 g to +7.996 g, and each count corresponds to (1/256) g (3.9 mg) at 12-bit resolution.
- **If only the 8-bit results are used**, then the resolution is reduced by a factor of 16.

For more information about the data manipulation between data formats and modes, see application note AN4083, *Data Manipulation and Basic Settings for Xtrinsic MMA865xFC Accelerometers*. There is a device driver available that can be used with the Sensor Toolbox demo board (LFSTBEB865xFC) with this application note.

Table 8. Accelerometer 12-bit output data

12-bit data	Range ±2 g (1 mg/LSB)	Range ±4 g (2 mg/LSB)	Range ±8 g (4 mg/LSB)
0111 1111 1111	1.999 g	+3.998 g	+7.996 g
0111 1111 1110	1.998 g	+3.996 g	+7.992 g
…	…	…	…
0000 0000 0001	0.001 g	+0.002 g	+0.004 g
0000 0000 0000	0.0000 g	0.0000 g	0.0000 g
1111 1111 1111	–0.001 g	–0.002 g	–0.004 g

Table 8. Accelerometer 12-bit output data (Continued)

12-bit data	Range ±2 g (1 mg/LSB)	Range ±4 g (2 mg/LSB)	Range ±8 g (4 mg/LSB)
…	…	…	…
1000 0000 0001	–1.999 g	–3.998 g	–7.996 g
1000 0000 0000	–2.0000 g	–4.0000 g	–8.0000 g

Table 9. Accelerometer 8-bit output data

8-bit Data	Range ±2 g (15.6 mg/LSB)	Range ±4 g (31.25 mg/LSB)	Range ±8 g (62.5 mg/LSB)
0111 1111	1.9844 g	+3.9688 g	+7.9375 g
0111 1110	1.9688 g	+3.9375 g	+7.8750 g
…	…	…	…
0000 0001	+0.0156 g	+0.0313 g	+0.0625 g
0000 0000	0.000 g	0.0000 g	0.0000 g
1111 1111	–0.0156 g	–0.0313 g	–0.0625 g
…	…	…	…
1000 0001	–1.9844 g	–3.9688 g	–7.9375 g
1000 0000	–2.0000 g	–4.0000 g	–8.0000 g

5.3 Internal FIFO data buffer

MMA8652FC contains a 32-sample internal FIFO data buffer, which helps minimize traffic across the I^2C bus. The FIFO can also save system power, by allowing the host processor/MCU to go into a SLEEP mode while the accelerometer independently stores the data (up to 32 samples per axis).

The FIFO can run at all output data rates. There are options for accessing the full 12-bit data or for accessing only the 8-bit data. When access speed is more important than high resolution, the 8-bit data read is a better option.

The FIFO contains four modes (Fill Buffer mode, Circular Buffer mode, Trigger mode, and Disabled mode), which are described in F_SETUP Register 0x09.

- **Fill Buffer mode** collects the first 32 samples and asserts the overflow flag when the buffer is full and another sample arrives. It does not collect any more data until the buffer is read. This benefits data logging applications where all samples must be collected.
- **Circular Buffer mode** allows the buffer to be filled and then new data replaces the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This benefits situations where the processor is waiting for an specific interrupt to signal that the data must be flushed to analyze the event.
- **Trigger mode** will hold the last data up to the point when the trigger occurs, and can be set to keep a selectable number of samples after the event occurs.

The MMA8652FC FIFO Buffer has a configurable watermark, allowing the processor to be triggered after a configurable number of samples has filled in the buffer (1 to 32).

5.4 Low power modes vs. high resolution modes

The MMA8652FC can be optimized for lower power modes or for higher resolution of the output data. One of the oversampling schemes of the data can be activated when MODS = 10 in Register 0x2B, which will improve the resolution of the output data only. The highest resolution is achieved at 1.56 Hz.

There is a trade-off between low power and high resolution. Low power can be achieved when the oversampling rate is reduced. When MODS = 11, the lowest power is achieved. The lowest power is achieved when the sample rate is set to 1.56 Hz.

5.5 Auto-WAKE/SLEEP mode

The MMA8652FC can be configured to transition between sample rates (with their respective current consumption) based on four of the interrupt functions of the device. The advantage of using the Auto-WAKE/SLEEP is that the system can automatically transition to a higher sample rate (higher current consumption) when needed, but spends the majority of the time in the SLEEP mode (lower current) when the device does not require higher sampling rates.

- **Auto-WAKE** refers to the device being triggered by one of the interrupt functions to transition to a higher sample rate. This may also interrupt the processor to transition from a SLEEP mode to a higher power mode.
- **SLEEP mode** occurs after the accelerometer has not detected an interrupt for longer than the user-definable timeout period. The device will transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode, to save on current during this period of inactivity.

The Interrupts that can WAKE the device from SLEEP are the following: Tap Detection, Orientation Detection, Motion/Freefall, and Transient Detection. The FIFO can be configured to hold the data in the buffer until it is flushed, if the FIFO Gate bit is set (in Register 0x2C) and if the FIFO cannot WAKE the device from SLEEP.

The interrupts that can keep the device from falling asleep are the same interrupts that can wake the device—with the addition of the FIFO. If the FIFO interrupt is enabled and data is being accessed continually servicing the interrupt, then the device will remain in WAKE mode.

5.6 Freefall and motion detection

MMA8652FC has a flexible interrupt architecture for detecting either a Freefall or a Motion.

- Freefall can be enabled where the set threshold *must be less than* the configured threshold.
- Motion can be enabled where the set threshold *must be greater than* the configured threshold.

The motion configuration has the option of enabling or disabling a high-pass filter to eliminate tilt data (static offset); the freefall configuration does not use the high-pass filter.

5.6.1 Freefall detection

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is *below a user-specified threshold for a user-definable amount of time*. Usable threshold levels are typically between ±100 mg and ±500 mg.

5.6.2 Motion detection

Motion is often used to simply alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold, the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event.

- The motion detection function can analyze static acceleration changes or faster jolts. For example, to detect that an object is spinning, all three axes would be enabled with a threshold detection of > 2 g. This condition would need to occur for a minimum of 100 ms to ensure that the event was not just noise. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to determine whether the condition exists for configurable set of time (like 100 ms or longer).
- To detect the direction of the motion, there is also directional data available in the source register. This is useful for applications such as directional shake or flick, which assists with the algorithm for various gesture detections.

5.7 Transient detection

The MMA8652FC has a built-in, high-pass filter. Acceleration data goes through the high pass filter, eliminating the offset (DC) and low frequencies. The high-pass filter cutoff frequency can be set to four different frequencies, which depends on the Output Data Rate (ODR). A higher cutoff frequency ensures that the DC data (or slower moving data) will be filtered out, allowing only the higher frequencies to pass. The embedded transient detection function uses the high-pass filtered data, allowing you to set the threshold and debounce counter. The transient detection feature can be used in the same manner as the motion detection feature, by bypassing the high-pass filter. There is an option in the configuration register to do this, which adds more flexibility to accommodate various use cases.

Many applications use the accelerometer’s **static acceleration readings** (like tilt), which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered with a low-pass filter where high frequency data is considered noise. However, there are many functions where the accelerometer must analyze **dynamic acceleration**. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the acceleration. It is simpler to interpret these functions (which are dependent on dynamic acceleration data) when the static component has been removed.

The Transient Detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 register (0x2E). Registers 0x1D – 0x20 are the dedicated Transient Detection configuration registers. The source register contains directional data to determine the direction of the acceleration (either positive or negative).

5.8 Tap detection

The MMA8652FC has embedded single/double and directional tap detection.

- The tap detection function has various customizing timers, for setting the pulse time width and the latency time between pulses. There are programmable thresholds for all three axes.
- The tap detection can be configured to run through the high-pass filter and also through a low-pass filter, which provides more customizing and tunable tap detection schemes.
- The status register provides updates on the axes where the event was detected and the direction of the tap.

5.9 Orientation detection

The MMA8652FC incorporates an advanced orientation detection algorithm with the ability to detect all six orientations shown in Figure 6. The embedded algorithm uses configurable trip points, allowing the selection of the desired midpoint and hysteresis value (see Figure 7).

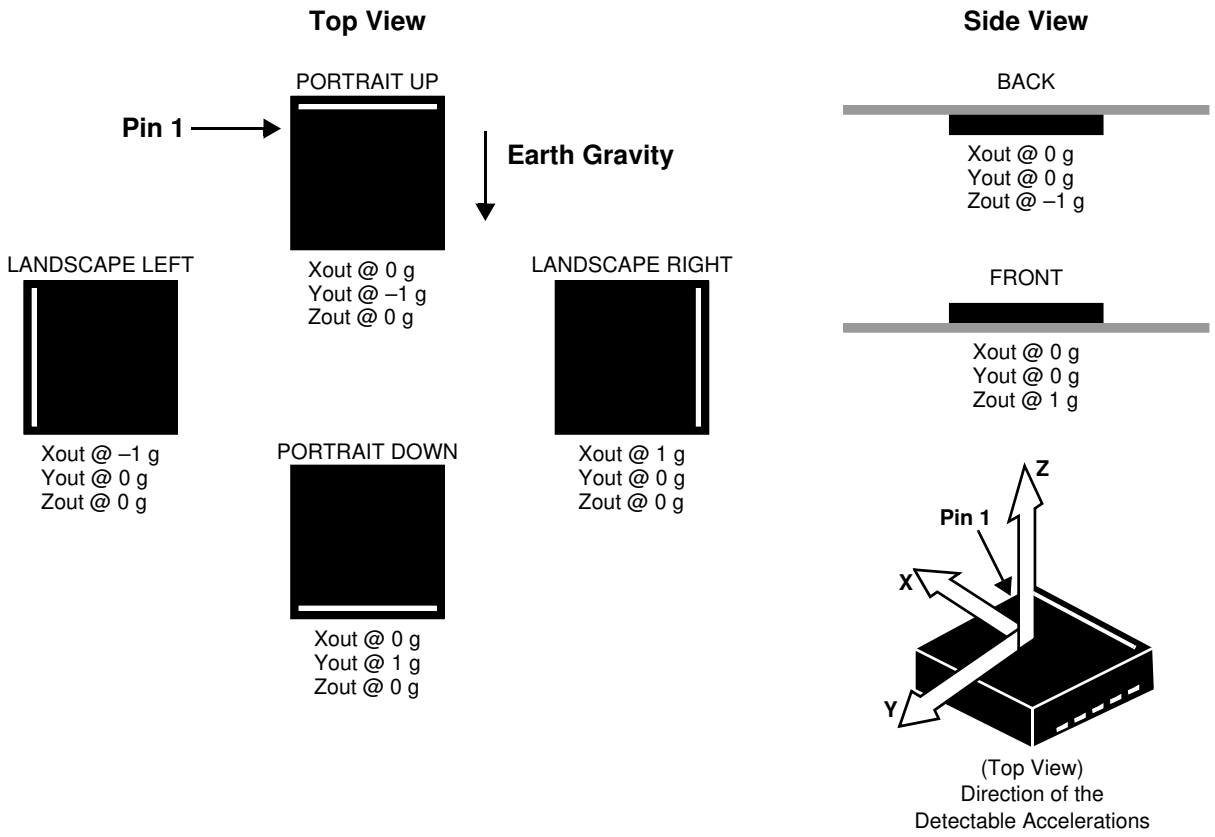


Figure 6. Sensitive axes orientation

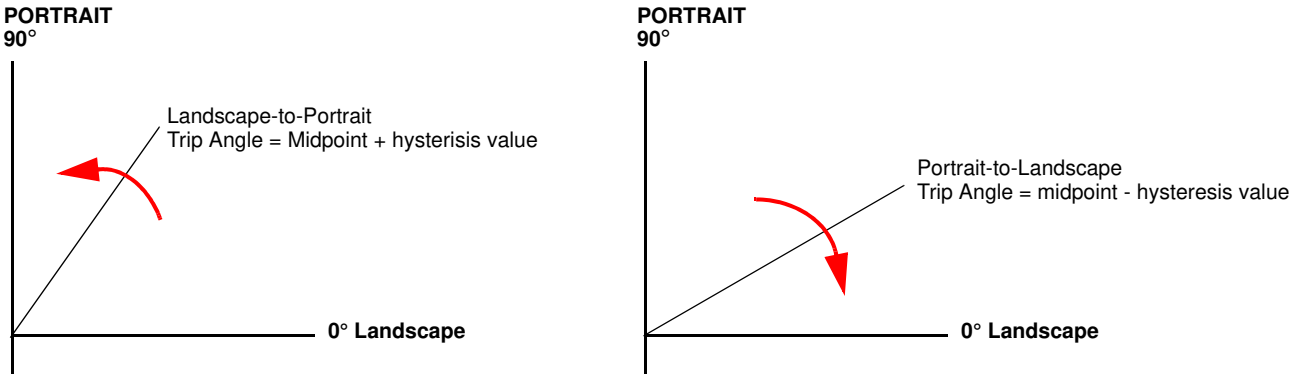


Figure 7. Landscape-to-Portrait transition trip angles

The MMA8652FC orientation detection algorithm confirms the reliability of the function with a configurable Z-lockout angle. Based on the known functionality of linear accelerometers, it is not possible to rotate the device about the Z-axis, to detect change in acceleration at slow angular speeds. The angle at which the device no longer detects the orientation change is referred to as the “Z-lockout angle” (see Figure 8). The device operates down to 14° from the flat position.

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When lifting the device upright from the flat position, orientation detection will be active for orientation angles greater than a user-configurable value.

The default angle is 29° from flat, but the angle can be set as low as 14°.

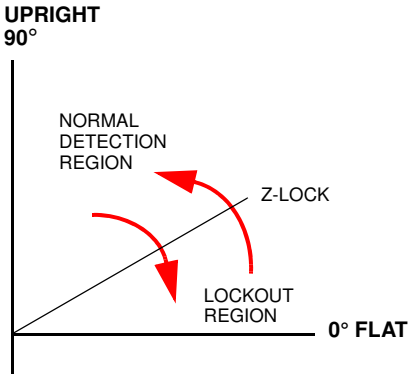

Figure 8. Z-Tilt angle lockout transition

5.10 Interrupt register configurations

There are seven configurable interrupts in the MMA8652FC: Data Ready, Motion/Freefall, Tap (Pulse), Orientation, Transient, FIFO events, and Auto-SLEEP events.

These seven interrupt sources can be routed to one of two interrupt pins.

The interrupt source must be enabled and configured.

If the event flag is asserted because the event condition is detected, then the corresponding interrupt pin (INT1 or INT2) will assert.

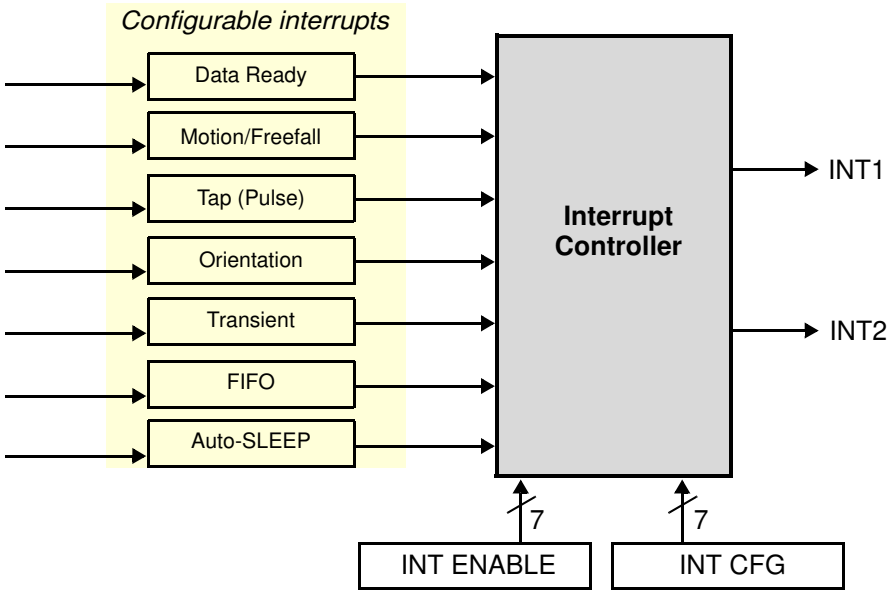

Figure 9. System interrupt generation

- The MMA8652FC features an interrupt signal that indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.
- The MMA8652FC may also be configured to generate *other interrupt signals* accordingly, to the programmable embedded functions of the device for Motion, Freefall, Transient, Orientation, and Tap.

5.11 Serial I²C interface

Acceleration data may be accessed through an I²C interface, thus making the device particularly suitable for direct interfacing to a microcontroller. The acceleration data and configuration registers embedded inside the MMA8652FC are accessed through the I²C serial interface (Table 10).

- To enable the I²C interface, VDDIO line must be tied high (to the interface supply voltage). If VDD is not present and VDDIO is present, then the MMA8652FC is in OFF mode—and communications on the I²C interface are ignored.
- The I²C interface may be used for communications between other I²C devices; the MMA8652FC does not affect the I²C bus.

Table 10. Serial Interface pins

Pin Name	Pin Description	Notes
SCL	I²C Serial Clock	**There are two signals associated with the I²C bus; the Serial Clock Line (SCL) and the Serial Data line (SDA).** • SDA is a bidirectional line used for sending and receiving the data to/from the interface. • External pullup resistors connected to VDDIO are expected for SDA and SCL. When the bus is free, both SCL and SDA lines are high.
SDA	I²C Serial Data	

The I²C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I²C standards (Table 11).

I²C operation:

1. The transaction on the bus is started through a start condition (START) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After START has been transmitted by the Master, the bus is considered busy.
2. The next byte of data transmitted after START contains the slave address in the first seven bits. The eighth bit tells whether the Master is *receiving data from the slave* or is *transmitting data to the slave*.
3. After a start condition and when an address is sent, each device in the system compares the first seven bits with its address. If the device's address matches the sent address, then the device considers itself addressed by the Master.

4. The 9th clock pulse following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low, so that it remains stable low during the high period of the acknowledge clock period.
5. A Master may also issue a repeated START during a data transfer. The MMA8652FC expects repeated STARTs to be used to randomly read from specific registers.
6. A low-to-high transition on the SDA line *while the SCL line is high* is defined as a stop condition (STOP). A data transfer is always terminated by a STOP.

The MMA8652FC's standard slave address is 0011101 or 0x01D.

Table 11. I²C Device address sequence

Command	[6:0] Device address	[6:0] Device address	R/W	8-bit final value
Read	0011101	0x1D	1	0x3B
Write	0011101	0x1D	0	0x3A

5.11.1 Single-byte read

1. The transmission of an 8-bit command begins on the falling edge of SCL. After the eight clock cycles are used to send the command, note that *the data returned* is sent with the MSB first after the data is received. Figure 10 shows the timing diagram for the accelerometer 8-bit I²C read operation.
2. The Master (or MCU) transmits a start condition (ST) to the MMA8652FC [slave address (0x1D), with the R/W bit set to “0” for a write], and the MMA8652FC sends an acknowledgement.
3. Next the Master (or MCU) transmits the address of the register to read, and the MMA8652FC sends an acknowledgement.
4. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8652FC (0x1D), with the R/W bit set to “1” for a read from the previously selected register.
5. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

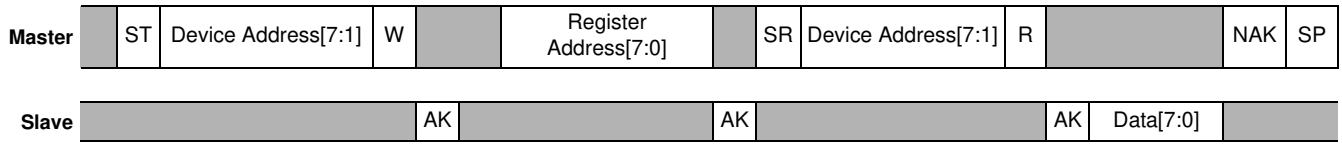

Figure 10. Single-Byte Read timing (I²C)

NOTE

For the following subsections, use the following legend.

Legend

ST: Start Condition	SP: Stop Condition	NAK: No Acknowledge	W: Write = 0
SR: Repeated Start Condition	AK: Acknowledge	R: Read = 1	

5.11.2 Multiple byte read

(See Table 11 for next auto-increment address.)

1. When performing a multi-byte read or “burst read”, the MMA8652FC automatically increments the received register address commands after a read command is received.
2. After following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8652FC acknowledgment (AK) is received,
3. Until a no acknowledge (NAK) occurs from the Master,
4. Followed by a stop condition (SP), which signals the end of transmission.

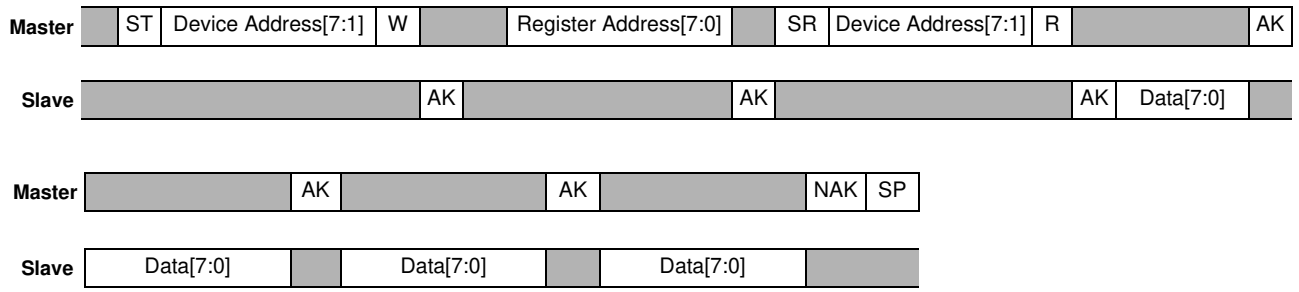

Figure 11. Multiple Byte Read timing (I^2C)

5.11.3 Single byte write

1. To start a write command, the Master transmits a start condition (ST) to the MMA8652FC, slave address ($1D) with the R/W bit set to “0” for a write,
2. The MMA8652FC sends an acknowledgement.
3. Next the Master (MCU) transmits the address of the register to write to, and the MMA8652FC sends an acknowledgement.
4. Then the Master (or MCU) transmits the 8-bit data to write to the designated register, and the MMA8652FC sends an acknowledgement that it has received the data. Because this transmission is complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA8652FC is now stored in the appropriate register.

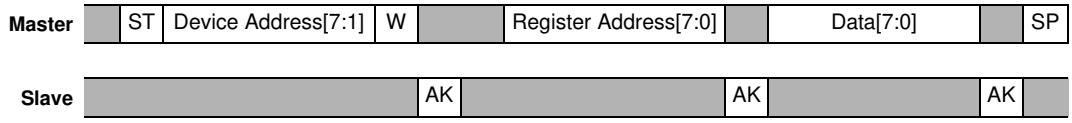

Figure 12. Single Byte Write timing (I^2C)

5.11.4 Multiple byte write

(See Table 11 for next auto-increment address.)

1. After a write command is received, the MMA8652FC *automatically increments* the received register address commands.
2. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA8652FC acknowledgment (ACK) is received.

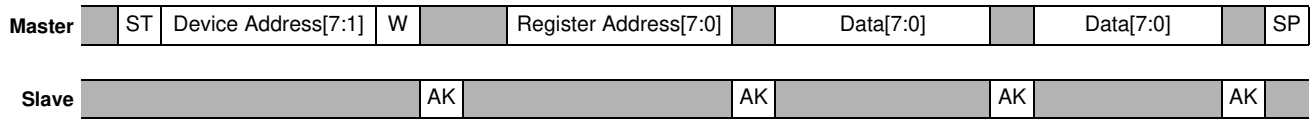

Figure 13. Multiple Byte Write timing (I^2C)

6 Register Descriptions

6.1 Register address map

Table 12. MMA8652FC register address map

Name	Type	Register Address	Auto-Increment Address				Default	Hex Value	Comment
			FMODE = 0 F_READ = 0	FMODE > 0 F_READ = 0	FMODE = 0 F_READ = 1	FMODE > 0 F_READ = 1			
STATUS/ F_STATUS(1)(2)	R	0x00	0x01				00000000	0x00	FMODE = 0, real time status FMODE > 0, FIFO status
OUT_X_MSB(1)(2)	R	0x01	0x02	0x01	**0x03**	**0x01**	Output	—	[7:0] are 8 MSBs of 12-bit sample. / Root pointer to XYZ FIFO data.
OUT_X_LSB(1)(2)	R	0x02	0x03		**0x00**		Output	—	[7:4] are 4 LSBs of 12-bit real-time sample
OUT_Y_MSB(1)(2)	R	0x03	0x04		**0x05**	**0x00**	Output	—	[7:0] are 8 MSBs of 12-bit real-time sample
OUT_Y_LSB(1)(2)	R	0x04	0x05		**0x00**		Output	—	[7:4] are 4 LSBs of 12-bit real-time sample
OUT_Z_MSB(1)(2)	R	0x05	0x06		**0x00**		Output	—	[7:0] are 8 MSBs of 12-bit real-time sample
OUT_Z_LSB(1)(2)	R	0x06	**0x00**				Output	—	[7:4] are 4 LSBs of 12-bit real-time sample
Reserved	R	0x07 0x08	—	—	—	—	—	—	Reserved. Read return 0x00.
F_SETUP(1)(3)	R/W	0x09	0x0A				00000000	0x00	FIFO setup
TRIG_CFG(1)(4)	R/W	0x0A	0x0B				00000000	0x00	Map of FIFO data capture events
SYSMOD(1)(2)	R	0x0B	0x0C				00000000	0x00	Current System mode
INT_SOURCE(1)(2)	R	0x0C	0x0D				00000000	0x00	Interrupt status
WHO_AM_I(1)	R	0x0D	0x0E				01001010	0x4A	Device ID (0x4A)
XYZ_DATA_CFG(1)(4)	R/W	0x0E	0x0F				00000000	0x00	Dynamic Range Settings
HP_FILTER_CUTOFF(1)(4)	R/W	0x0F	0x10				00000000	0x00	High-Pass Filter Selection
PL_STATUS(1)(2)	R	0x10	0x11				00000000	0x00	Landscape/Portrait orientation status
PL_CFG(1)(4)	R/W	0x11	0x12				10000000	0x80	Landscape/Portrait configuration.
PL_COUNT(1)(3)	R/W	0x12	0x13				00000000	0x00	Landscape/Portrait debounce counter
PL_BF_ZCOMP(1)(4)	R/W	0x13	0x14				01000100	0x44	Back/Front, Z-Lock Trip threshold
P_L_THS_REG(1)(4)	R/W	0x14	0x15				10000100	0x84	Portrait/Landscape Threshold and Hysteresis
FF_MT_CFG(1)(4)	R/W	0x15	0x16				00000000	0x00	Freefall/Motion functional block configuration
FF_MT_SRC(1)(2)	R	0x16	0x17				00000000	0x00	Freefall/Motion event source register
FF_MT_THS(1)(3)	R/W	0x17	0x18				00000000	0x00	Freefall/Motion threshold register
FF_MT_COUNT(1)(3)	R/W	0x18	0x19				00000000	0x00	Freefall/Motion debounce counter
Reserved	R	0x19 0x1A 0x1B 0x1C	—	—	—	—	—	—	Reserved. Read return 0x00.

Table 12. MMA8652FC register address map (Continued)

Name	Type	Register Address	Auto-Increment Address				Default	Hex Value	Comment
			FMODE = 0 F_READ = 0	FMODE > 0 F_READ = 0	FMODE = 0 F_READ = 1	FMODE > 0 F_READ = 1			
TRANSIENT_CFG(1)(4)	R/W	0x1D	0x1E				00000000	0x00	Transient functional block configuration
TRANSIENT_SRC(1)(2)	R	0x1E	0x1F				00000000	0x00	Transient event status register
TRANSIENT_THS(1)(3)	R/W	0x1F	0x20				00000000	0x00	Transient event threshold
TRANSIENT_COUNT(1)(3)	R/W	0x20	0x21				00000000	0x00	Transient debounce counter
PULSE_CFG(1)(4)	R/W	0x21	0x22				00000000	0x00	Pulse enable configuration
PULSE_SRC(1)(2)	R	0x22	0x23				00000000	0x00	Pulse detection source
PULSE_THSX(1)(3)	R/W	0x23	0x24				00000000	0x00	X pulse threshold
PULSE_THSY(1)(3)	R/W	0x24	0x25				00000000	0x00	Y pulse threshold
PULSE_THSZ(1)(3)	R/W	0x25	0x26				00000000	0x00	Z pulse threshold
PULSE_TMLT(1)(4)	R/W	0x26	0x27				00000000	0x00	Time limit for pulse
PULSE_LTCY(1)(4)	R/W	0x27	0x28				00000000	0x00	Latency time for 2nd pulse
PULSE_WIND(1)(4)	R/W	0x28	0x29				00000000	0x00	Window time for 2nd pulse
ASLP_COUNT(1)(4)	R/W	0x29	0x2A				00000000	0x00	Counter setting for Auto-SLEEP
CTRL_REG1(1)(4)	R/W	0x2A	0x2B				00000000	0x00	Data rates and modes setting
CTRL_REG2(1)(4)	R/W	0x2B	0x2C				00000000	0x00	Sleep Enable, OS modes, RST, ST
CTRL_REG3(1)(4)	R/W	0x2C	0x2D				00000000	0x00	Wake from Sleep, IPOL, PP_OD
CTRL_REG4(1)(4)	R/W	0x2D	0x2E				00000000	0x00	Interrupt enable register
CTRL_REG5(1)(4)	R/W	0x2E	0x2F				00000000	0x00	Interrupt pin (INT1/INT2) map
OFF_X(1)(4)	R/W	0x2F	0x30				00000000	0x00	X-axis offset adjust
OFF_Y(1)(4)	R/W	0x30	0x31				00000000	0x00	Y-axis offset adjust
OFF_Z(1)(4)	R/W	0x31	**0x0D**				00000000	0x00	Z-axis offset adjust

1. Register contents are preserved when a transition from ACTIVE to STANDBY mode occurs.
2. Register contents are reset when a transition from STANDBY to ACTIVE mode occurs.
3. Register contents can be modified at any time in either STANDBY or ACTIVE mode. A write to this register will cause a reset of the corresponding internal system debounce counter.
4. Register contents can only be modified while the device is in STANDBY mode; the only exceptions to this are the CTRL_REG1[ACTIVE] and CTRL_REG2[RST] bits.

NOTE

Auto-increment addresses that are not a simple increment are highlighted in **bold**. The auto-increment addressing is only enabled when device registers are read using I^2C *burst read mode*. The *internally stored* auto-increment address is cleared whenever an I^2C STOP condition is detected.

6.2 Register bit map

Table 13. MMA8652FC register bit map

Reg	Name	Definition	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	STATUS/F_STATUS	Data Status	R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
01	OUT_X_MSB	12-bit X Data	R	XD11	XD10	XD9	XD8	XD7	XD6	XD5	XD4
02	OUT_X_LSB	12-bit X Data	R	XD3	XD2	XD1	XD0	0	0	0	0
03	OUT_Y_MSB	12-bit Y Data	R	YD11	YD10	YD9	YD8	YD7	YD6	YD5	YD4
04	OUT_Y_LSB	12-bit Y Data	R	YD3	YD2	YD1	YD0	0	0		0
05	OUT_Z_MSB	12-bit Z Data	R	ZD11	ZD10	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4
06	OUT_Z_LSB	12-bit Z Data	R	ZD3	ZD2	ZD1	ZD0	0	0	0	0
09	F_SETUP	FIFO Setup	R/W	F_MODE1	F_MODE0	F_WMRK5	F_WMRK4	F_WMRK3	F_WMRK2	F_WMRK1	F_WMRK0
0A	TRIG_CFG	FIFO Triggers	R/W	—	—	Trig_TRANS	Trig_LNDPRT	Trig_PULSE	Trig_FF_MT	—	—
0B	SYSMOD	System mode	R	FGERR	FGT_4	FGT_3	FGT_2	FGT_1	FGT_0	SYSMOD1	SYSMOD0
0C	INT_SOURCE	Interrupt Status	R	SRC_ASLP	SRC_FIFO	SRC_TRANS	SRC_LNDPRT	SRC_PULSE	SRC_FF_MT	—	SRC_DRDY
0D	WHO_AM_I	ID Register	R	0	1	0	0	1	0	1	0
0E	XYZ_DATA_CFG	Data Config	R/W	—	—	—	HPF_Out	—	—	FS1	FS0
0F	HP_FILTER_CUTOFF	HP Filter Setting	R/W	—	—	Pulse_HPF_BYP	Pulse_LPF_EN	—	—	SEL1	SEL0
10	PL_STATUS	PL Status	R	NEWLP	LO	—	—	—	LAPO[1]	LAPO[0]	BAFRO
11	PL_CFG	PL Configuration	R/W	DBCNTM	PL_EN	—	—	—	—	—	—
12	PL_COUNT	PL DEBOUNCE	R/W	DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE[2]	DBNCE[1]	DBNCE[0]
13	PL_BF_ZCOMP	PL Back/Front Z Comp	R/W	BKFR[1]	BKFR[0]	—	—	—	ZLOCK[2]	ZLOCK[1]	ZLOCK[0]
14	P_L_THS_REG	PL THRESHOLD	R/W	P_L_THS[4]	P_L_THS[3]	P_L_THS[2]	P_L_THS[1]	P_L_THS[0]	HYS[2]	HYS[1]	HYS[0]
15	FF_MT_CFG	Freefall/Motion Config	R/W	ELE	OAE	ZEFE	YEFE	XEFE	—	—	—
16	FF_MT_SRC	Freefall/Motion Source	R	EA	—	ZHE	ZHP	YHE	YHP	XHE	XHP
17	FF_MT_THS	Freefall/Motion Threshold	R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
18	FF_MT_COUNT	Freefall/Motion Debounce	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1D	TRANSIENT_CFG	Transient Config	R/W	—	—	—	ELE	ZTEFE	YTEFE	XTEFE	HPF_BYP
1E	TRANSIENT_SRC	Transient Source	R	—	EA	ZTRANSE	Z_Trans_Pol	YTRANSE	Y_Trans_Pol	XTRANSE	X_Trans_Pol
1F	TRANSIENT_THS	Transient Threshold	R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
20	TRANSIENT_COUNT	Transient Debounce	R/W	D7	D6	D5	D4	D3	D2	D1	D0
21	PULSE_CFG	Pulse Config	R/W	DPA	ELE	ZDPEFE	ZSPEFE	YDPEFE	YSPEFE	XDPEFE	XSPEFE
22	PULSE_SRC	Pulse Source	R	EA	AxZ	AxY	AxX	DPE	Pol_Z	Pol_Y	Pol_X
23	PULSE_THSX	Pulse X Threshold	R/W	—	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0
24	PULSE_THSY	Pulse Y Threshold	R/W	—	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0
25	PULSE_THSZ	Pulse Z Threshold	R/W	—	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
26	PULSE_TMLT	Pulse First Timer	R/W	TMLT7	TMLT6	TMLT5	TMLT4	TMLT3	TMLT2	TMLT1	TMLT0
27	PULSE_LTCY	Pulse Latency	R/W	LTCY7	LTCY6	LTCY5	LTCY4	LTCY3	LTCY2	LTCY1	LTCY0
28	PULSE_WIND	Pulse 2nd Window	R/W	WIND7	WIND6	WIND5	WIND4	WIND3	WIND2	WIND1	WIND0
29	ASLP_COUNT	Auto-SLEEP Counter	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2A	CTRL_REG1	Control Reg1	R/W	ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	—	F_READ	ACTIVE
2B	CTRL_REG2	Control Reg2	R/W	ST	RST	—	SMODS1	SMODS0	SLPE	MODS1	MODS0
2C	CTRL_REG3	Control Reg3 (WAKE Interrupts from SLEEP)	R/W	FIFO_GATE	WAKE_TRANS	WAKE_LNDPRT	WAKE_PULSE	WAKE_FF_MT	—	IPOL	PP_OD
2D	CTRL_REG4	Control Reg4 (Interrupt Enable Map)	R/W	INT_EN_ASLP	INT_EN_FIFO	INT_EN_TRANS	INT_EN_LNDPRT	INT_EN_PULSE	INT_EN_FF_MT	—	INT_EN_DRDY

Table 13. MMA8652FC register bit map (Continued)

Reg	Name	Definition	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2E	CTRL_REG5	Control Reg5 (Interrupt Configuration)	R/W	INT_CFG_ASLP	INT_CFG_FIFO	INT_CFG_TRANS	INT_CFG_LNDPRT	INT_CFG_PULSE	INT_CFG_FF_MT	—	INT_CFG_DRDY
2F	OFF_X	X-axis 0 g offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30	OFF_Y	Y-axis 0 g offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31	OFF_Z	Z-axis 0 g offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0

6.3 Data registers

The following are the data registers for the MMA8652FC device. For more information about data manipulation in the MMA8652FC, see application note AN4083, *Data Manipulation and Basic Settings for Xtrinsic MMA865xFC Accelerometers.*

- When the F_MODE bits (F_SETUP register 0x09, bit 6 and 7) are cleared, the FIFO is not ON. Register 0x00 reflects the real-time status information of the X, Y and Z sample data.
- When the F_MODE value is greater than zero, then the FIFO is ON (in either Fill, Circular, or Trigger mode). In this case, register 0x00 will reflect the status of the FIFO. It is expected that when the FIFO is ON, the user will access the data from register 0x01 (X_MSB) for either the 12-bit or 8-bit data.
- When accessing the 8-bit data, the F_READ bit (register 0x2A) is set, which modifies the auto-incrementing to skip over the LSB data.
- When the F_READ bit is cleared, the 12-bit data is read, accessing all 6 bytes sequentially (X_MSB, X_LSB, Y_MSB, Y_LSB, Z_MSB, Z_LSB).

6.3.1 0x00: STATUS Data Status register (F_MODE = 00)

When F_MODE = 0, register 0x00 reflects the real-time status information of the X, Y and Z sample data; it contains the X, Y, and Z data overwrite and data ready flag.

These registers contain the X-axis, Y-axis, and Z-axis 12-bit output sample data (expressed as 2's complement numbers).

Table 14. F_MODE = 00: 0x00 STATUS: Data Status register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Table 15. STATUS register bits

Bit(s)	Field	Description	Notes
7	ZYXOW	**X, Y, Z-axis data overwrite** • Set whenever a new acceleration data is produced *before completing the retrieval of the previous set.* This event occurs when the content of at least one acceleration data register (i.e., OUT_X, OUT_Y, OUT_Z) has been overwritten. • Cleared when the high bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the channels are read. 0 No data overwrite has occurred (default) 1 Previous X, Y, or Z data was overwritten by new X, Y, or Z data before it (the previous X, Y, or Z data) was read	
6	ZOW	**Z-axis data overwrite**	***For # = Z, Y, or X:*** • Set whenever a new acceleration sample *related to the #-axis* is generated *before the retrieval of the previous sample.* When this occurs, the previous sample is overwritten. • Cleared whenever the OUT_#_MSB register is read. 0 No data overwrite has occurred (default) 1 Previous Z-axis data was overwritten by new #-axis data before it (the previous #-axis data) was read
5	YOW	**Y-axis data overwrite**	
4	XOW	**X-axis data overwrite**	
3	ZYXDR	**X, Y, Z-axis new data ready** • Set when a new sample for any of the enabled channels is available. • Cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the channels are read. 0 No new set of data ready (default) 1 A new set of data is ready	
2	ZDR	**Z-axis new data available**	For # = Z, Y, or X • Set whenever a new acceleration sample *related to the #-axis* is generated. • Cleared whenever the OUT_#_MSB register is read. 0 No new #-axis data ready (default) 1 New #-axis data is ready
1	YDR	**Y-axis new data available**	
0	XDR	**X-axis new data available**	

- OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x01 – 0x06, to reduce reading the status followed by 12-bit axis data to 7 bytes. If the F_READ bit is set (0x2A bit 1), then auto-increment will skip over LSB registers (to access the MSB data only). This will shorten the data acquisition from seven bytes to four bytes.