Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Freescale Semiconductor
Data Sheet: Technical Data
An Energy-Efficient Solution by Freescale

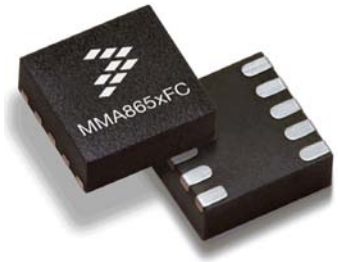
Document Number: MMA8653FC
Rev. 1.0, 02/2013

Xtrinsic MMA8653FC 3-Axis, 10-bit Digital Accelerometer

MMA8653FC

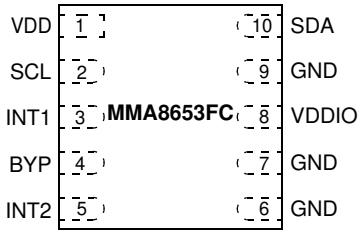
The MMA8653FC is an intelligent, low-power, three-axis, capacitive micromachined accelerometer with 10 bits of resolution. This accelerometer is packed with embedded functions with flexible user-programmable options, configurable to two interrupt pins. Embedded interrupt functions enable overall power savings, by relieving the host processor from continuously polling data. There is access to either low-pass or high-pass filtered data, which minimizes the data analysis required for jolt detection and faster transitions. The device can be configured to generate inertial wake-up interrupt signals from any combination of the configurable embedded functions, enabling the MMA8653FC to monitor inertial events while remaining in a low-power mode during periods of inactivity. The MMA8653FC is available in a small 10-pin DFN package (2 mm x 2 mm x 1 mm).

Top and Bottom View



10-PIN DFN
2 mm x 2 mm x 1 mm
CASE 2162

Top View



Pin Connections

Features

- 1.95 V to 3.6 V supply voltage
- 1.62 V to 3.6 V digital interface voltage
- ±2 g, ±4 g, and ±8 g dynamically selectable full-scale ranges
- Output Data Rates (ODR) from 1.56 Hz to 800 Hz
- 10-bit digital output
- I^2C digital output interface with programmable interrupts
- One embedded channel of configurable motion detection (Freefall)
- Orientation (Portrait/Landscape) detection with fixed hysteresis of 15°.
- Configurable automatic ODR change triggered by the Auto-Wake/Sleep state change
- Self-Test

Typical applications

- Tilt compensation in e-compass applications
- Static orientation detection (Portrait/Landscape, Up/Down, Left/Right, Back/Front position identification)
- Notebook, tablet, e-reader, and laptop tumble and freefall detection
- Real-time orientation detection (virtual reality and gaming 3D user orientation feedback)
- Real-time activity analysis (pedometer step counting, freefall drop detection for HDD, dead-reckoning GPS backup)
- Motion detection for portable product power saving (Auto-SLEEP and Auto-WAKE for cell phone, PDA, GPS, gaming)
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)
- User interface (tilt menu scrolling)

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
MMA8653FCR1	-40°C to +85°C	DFN-10	Tape and Reel

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Table 1. Feature comparison of the MMA865xFC devices

Feature	MMA8652FC	MMA8653FC
ADC Resolution (bits)	12	10
Digital Sensitivity in 2 g mode (counts/g)	1024	256
Low-Power Mode	Yes	Yes
Auto-WAKE	Yes	Yes
Auto-SLEEP	Yes	Yes
32-Level FIFO	Yes	No
Low-Pass Filter	Yes	Yes
High-Pass Filter	Yes	No
Transient Detection with High-Pass Filter	Yes	No
Fixed Orientation Detection	No	Yes
Programmable Orientation Detection	Yes	No
Data-Ready Interrupt	Yes	Yes
Single-Tap Interrupt	Yes	No
Double-Tap Interrupt	Yes	No
Directional Tap Interrupt	Yes	No
Freefall Interrupt	Yes	Yes
Motion Interrupt with Direction	Yes	No

Contents

Related Documentation

The MMA8653FC device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA8653FC.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Block Diagram and Pin Descriptions

1.1 Block diagram

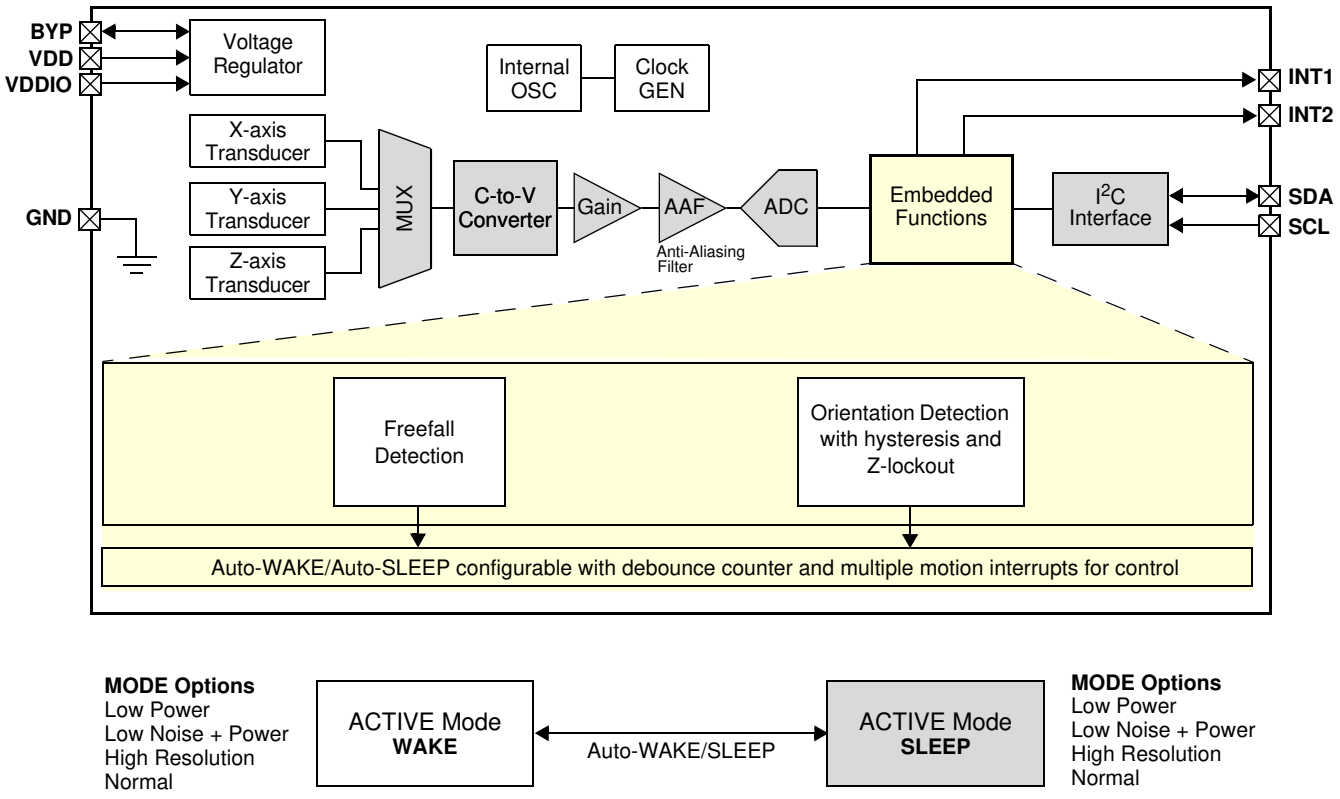


Figure 1. MMA8653 block diagram

1.2 Pin descriptions

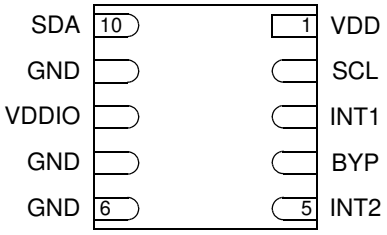


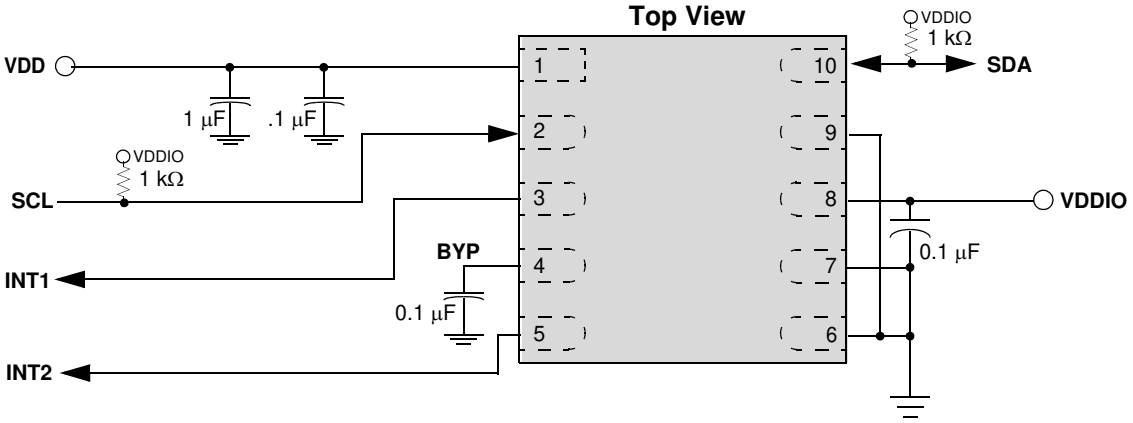
Figure 2. Pin connections (bottom view)

Table 1. Pin descriptions

Pin #	Pin Name	Description	Notes
1	VDD	Power supply	Device power is supplied through the VDD line. Power supply decoupling capacitors should be placed as close as possible to pin 1 and pin 8 of the device.
2	SCL(1)	I^2C Serial Clock	7-bit I^2C device address is 0x1D.
3	INT1	Interrupt 1	The interrupt source and pin settings are user-programmable through the I^2C interface.
4	BYP	Internal regulator output capacitor connection	
5	INT2	Interrupt 2	See INT1.
6	GND	Ground	
7	GND	Ground	
8	VDDIO	Digital Interface Power supply	
9	GND	Ground	
10	SDA(1)	I^2C Serial Data	See SCL.

1. The control signals SCL and SDA are not tolerant of voltages higher than VDDIO + 0.3 V. If VDDIO is removed, then the control signals SCL and SDA will clamp any logic signals with their internal ESD protection diodes. The SDA and SCL I^2C connections are open drain, and therefore require a pullup resistor to VDDIO.

1.3 Typical application circuit



Note: 4.7 kΩ Pullup resistors on INT1/INT2 can be added for open-drain operation.

Figure 3. Typical application circuit

2 Mechanical and Electrical Specifications

2.1 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Maximum ratings

Rating	Symbol	Value	Unit
Maximum acceleration (all axes, 100 μs)	g_{max}	10,000	g
Supply voltage	VDD	–0.3 to +3.6	V
Input voltage on any control pin (SCL, SDA)	Vin	–0.3 to VDDIO + 0.3	V
Drop test	D_{drop}	1.8	m
Operating temperature range	T_{OP}	–40 to +85	°C
Storage temperature range	T_{STG}	–40 to +125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human body model	HBM	±2000	V
Machine model	MM	±200	V
Charge device model	CDM	±500	V
Latch-up current at T = 85°C	I_{LU}	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part.

This part is ESD-sensitive. Improper handling can cause permanent damage to the part.

2.2 Mechanical characteristics

Table 4. Mechanical characteristics at VDD = 2.5 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Full-Scale measurement range	FS	FS[1:0] set to 00 ±2 g mode		±2		g
		FS[1:0] set to 01 ±4 g mode		±4		
		FS[1:0] set to 10 ±8 g mode		±8		
Sensitivity	So	FS[1:0] set to 00 ±2 g mode		256		LSB/g
		FS[1:0] set to 01 ±4 g mode		128		
		FS[1:0] set to 10 ±8 g mode		64		
Sensitivity accuracy	Soa			±2.5		%
Sensitivity change vs. temperature	TCS	–40°C to 85°C		±0.0074		%/°C
Zero-g level offset accuracy (1)	TyOff			±25		mg
Zero-g level offset accuracy, post-board mount (2)	TyOffPBM			±33.5		mg
Zero-g level change vs. temperature	TCO	–40°C to 85°C		±0.27		mg/°C
Self-Test output change (±2 g mode)	STOC	x		+22.5		LSB
		y		+26		
		z		+195.5		
ODR accuracy	ODRa			±3.1		%
Output data bandwidth	BW		ODR/3		ODR/2	Hz
Output noise	RMS	Normal mode ODR = 400 Hz		182		µg/√Hz
Operating temperature range	T_{AGOC}		–40		85	°C

1. Before board mount.
2. Post-board mount offset specifications are based on an 8-layer PCB, relative to 25°C.

2.3 Electrical characteristics

Table 5. Electrical characteristics at VDD = 2.5 V, VDDIO = 1.8 V, T = 25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply voltage	VDD		1.95	2.5	3.6	V
Interface supply voltage	VDDIO		1.62	1.8	3.6	V
Low Power mode	$I_{dd}LP$	ODR = 1.563 Hz		6.5		µA
		ODR = 6.25 Hz		6.5		
		ODR = 12.5 Hz		6.5		
		ODR = 50 Hz		15		
		ODR = 100 Hz		26		
		ODR = 200 Hz		49		
		ODR = 400 Hz		94		
		ODR = 800 Hz		184		
Normal mode	I_{dd}	ODR = 1.563 Hz		27		µA
		ODR = 6.25 Hz		27		
		ODR = 12.5 Hz		27		
		ODR = 50 Hz		27		
		ODR = 100 Hz		49		
		ODR = 200 Hz		94		
		ODR = 400 Hz		184		
		ODR = 800 Hz		184		
Boot-Up current	I_{ddBoot}	VDD = 2.5 V, the current during the Boot sequence is integrated over 0.5 ms, using a recommended bypass cap			1	mA
Value of capacitor on BYP pin	Cap	–40°C to 85°C	75	100	470	nF
Standby current	I_{ddStby}	25°C		1.4	5	µA
Digital high-level input voltage SCL, SDA	VIH	VDD = 3.6 V, VDDIO = 3.6 V	0.7*VDDIO			V
Digital low-level input voltage SCL, SDA	VIL	VDD = 1.95 V, VDDIO = 1.62 V			0.3*VDDIO	V
High-level output voltage INT1, INT2	VOH	VDD = 3.6 V, VDDIO = 3.6 V, I_O = 500 µA	0.9*VDDIO			V
Low-level output voltage INT1, INT2	VOL	VDD = 1.95 V, VDDIO = 1.62 V, I_O = 500 µA			0.1*VDDIO	V
Low-level output voltage SDA	VOLS	I_O = 3 mA			0.4	V
Output source current INT1, INT2	I_{source}	Voltage high level VOUT = 0.9 x VDDIO		2		mA
Output sink current INT1, INT2	I_{sink}	Voltage high level VOUT = 0.9 x VDDIO		3		mA
Power-on ramp time	Tpr		0.001		1000	ms
Boot time	Tbt	Time from VDDIO on and VDD > VDD min until I^2C is ready for operation, Cbyp = 100 nf		350	500	µs
Turn-on time	Ton1	Time to obtain valid data from Standby mode to Active mode			2/ODR + 1 ms	-
Turn-on time	Ton2	Time to obtain valid data from valid voltage applied			2/ODR + 2 ms	-
Operating temperature range	T_{AGOC}		–40		85	°C

2.4 I²C interface characteristic

Table 6. I²C slave timing values (1)

Parameter	Symbol	I²C Fast Mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0	400	kHz
Bus-free time between STOP and START condition	t_{BUF}	1.3		µs
(Repeated) START hold time	$t_{HD;STA}$	0.6		µs
Repeated START setup time	$t_{SU;STA}$	0.6		µs
STOP condition setup time	$t_{SU;STO}$	0.6		µs
SDA data hold time	$t_{HD;DAT}$	0.05	0.9 (2)	µs
SDA setup time	$t_{SU;DAT}$	100		ns
SCL clock low time	t_{LOW}	1.3		µs
SCL clock high time	t_{HIGH}	0.6		µs
SDA and SCL rise time	t_r	20 + 0.1 C_b (3)	300	ns
SDA and SCL fall time	t_f	20 + 0.1 C_b (3)	300	ns
SDA valid time (4)	$t_{VD;DAT}$		0.9 (2)	µs
SDA valid acknowledge time (5)	$t_{VD;ACK}$		0.9 (2)	µs
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	ns
Capacitive load for each bus line	Cb		400	pF

1. All values referred to VIH(min) (0.3 VDD) and VIL(max) (0.7 VDD) levels.
2. This device does not stretch the LOW period (tLOW) of the SCL signal.
3. C_b = total capacitance of one bus line in pF.
4. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

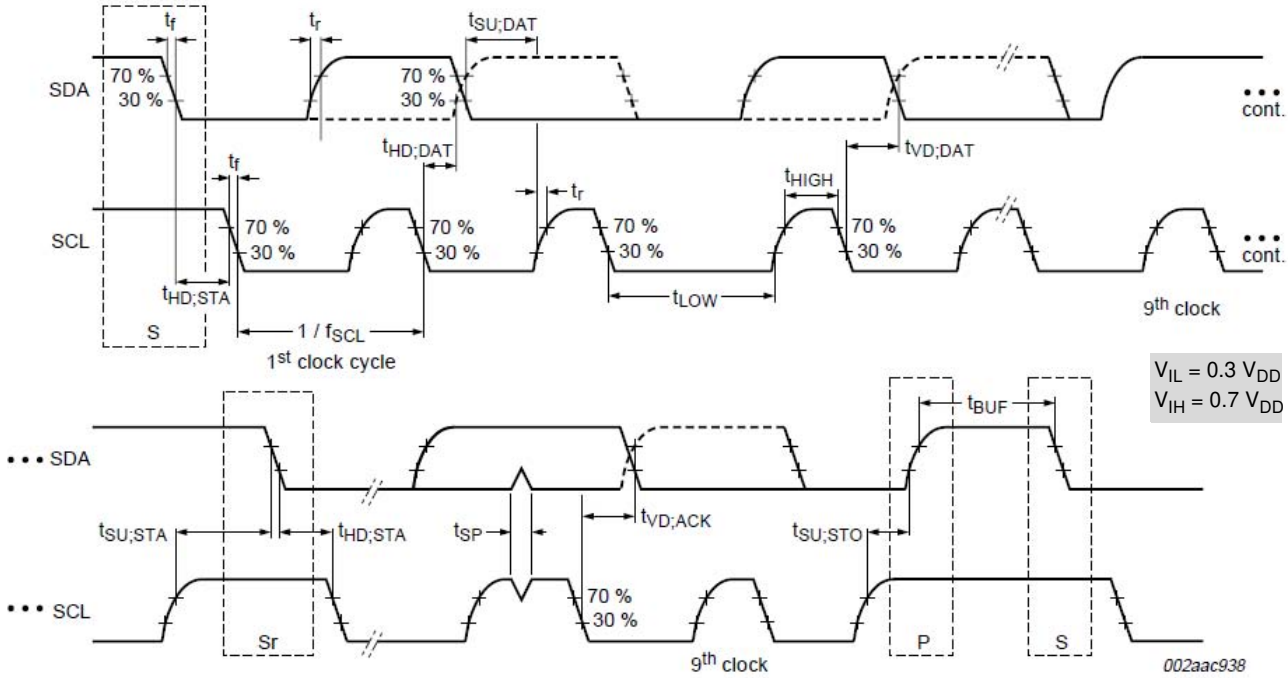


Figure 4. I²C slave timing diagram

MMA8653FC

3 Terminology

3.1 Sensitivity

The sensitivity is represented in counts/g.

- In ±2 g mode, sensitivity = 256 counts/g.
- In ±4 g mode, sensitivity = 128 counts/g.
- In ±8 g mode, sensitivity = 64 counts/g.

3.2 Zero-g offset

Zero-g Offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if the sensor is stationary. A sensor stationary on a horizontal surface will measure 0 g in X-axis and 0 g in Y-axis, whereas the Z-axis will measure 1 g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT Registers 0x00, data expressed as a 2's complement number). A deviation from ideal value in this case is called Zero-g offset.

Offset is to some extent a result of stress on the MEMS sensor, and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress.

3.3 Self-Test

Self-Test can be used to verify the transducer and signal chain functionality without the need to apply external mechanical stimulus.

When Self-Test is activated:

- An electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case, the sensor outputs will exhibit a change in their DC levels which, are related to the selected full scale through the device sensitivity.
- The device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

4 Modes of Operation

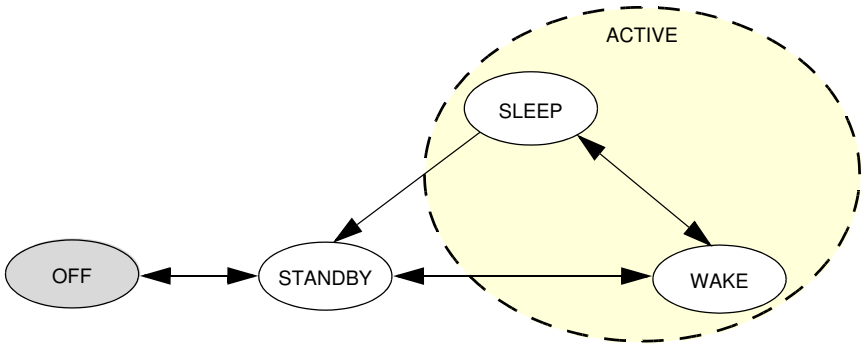


Figure 5. Operating modes for MMA8653FC

Table 7. Operating modes

Mode	I^2C Bus State	VDD	VDDIO	Description
OFF	Powered down	<1.8 V	VDDIO can be > VDD	• The device is powered off. • All analog and digital blocks are shutdown. • I^2C bus inhibited.
STANDBY	I^2C communication with MMA8653FC is possible	ON	VDDIO = High VDD = High ACTIVE bit is cleared	• Only digital blocks are enabled. • Analog subsystem is disabled. • Internal clocks disabled.
ACTIVE (WAKE/SLEEP)	I^2C communication with MMA8653FC is possible	ON	VDDIO = High VDD = High ACTIVE bit is set	All blocks are enabled (digital, analog).

Some registers are reset when transitioning from STANDBY to ACTIVE. These registers are all noted in the device memory map register table.

The SLEEP and WAKE modes are ACTIVE modes. For more information about how to use the SLEEP and WAKE modes and how to transition between these modes, see Section 5.

5 Functionality

The MMA8653FC is a low-power, digital output 3-axis linear accelerometer with a I^2C interface with embedded logic used to detect events and notify an external microprocessor over interrupt lines.

- 8-bit or 10-bit data
- Four different oversampling options that allow for the optimum resolution vs. current consumption trade-off to be made for a given application
- Low-power and auto-WAKE/SLEEP modes for reducing current consumption
- Freefall detection (one channel)
- Single default angle for portrait landscape detection algorithm, for addressing screen orientation
- Two independent interrupt output pins that are programmable among four interrupt sources (Data Ready, Freefall, Orientation, Auto-WAKE)

All functionality is available in ±2 g, ±4 g or ±8 g dynamic measurement ranges. There are many configuration settings for enabling all of the different functions. Separate application notes are available to help configure the device for each embedded functionality.

5.1 Device calibration

The device is factory calibrated for sensitivity and Zero-g offset for each axis. The trim values are stored in Non-Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the circuitry. In normal use, further calibration in the end application is not necessary. However, the MMA8653FC allows you to adjust the offset for each axis after power-up, by changing the default offset values. The user offset adjustments are stored in three volatile 8-bit registers (OFF_X, OFF_Y, OFF_Z).

5.2 8-bit or 10-bit data

The measured acceleration data is stored in the following registers as 2's complement 10-bit numbers:

- OUT_X_MSB, OUT_X_LSB
- OUT_Y_MSB, OUT_Y_LSB
- OUT_Z_MSB, OUT_Z_LSB

The most significant eight bits of each axis are stored in OUT_X (Y, Z)_MSB, so applications needing only 8-bit results can use these three registers (and ignore the OUT_X/Y/Z_LSB registers). To use only 8-bit results, the F_READ bit in CTRL_REG1 must be set. When the F_READ bit is cleared, the fast read mode is disabled.

- **When the full-scale is set to ±2 g**, the measurement range is –2 g to +1.996 g, and each count corresponds to (1/256) g (3.8 mg) at 10-bit resolution.
- **When the full-scale is set to ±4 g**, the measurement range is –4 g to +3.992 g, and each count corresponds to (1/128) g
- (7.8 mg) at 10-bit resolution.
- **When the full-scale is set to ±8 g**, the measurement range is –8 g to +7.984 g, and each count corresponds to (1/64) g (15.6 mg) at 10-bit resolution.
- **If only the 8-bit results are used**, then the resolution is reduced by a factor of 16.

For more information about the data manipulation between data formats and modes, see application note AN4083, *Data Manipulation and Basic Settings for Xtrinsic MMA865xFC Accelerometers*. There is a device driver available that can be used with the Sensor Toolbox demo board (LFSTBEB865xFC) with this application note.

Table 8. Accelerometer 10-bit output data

10-bit Data	Range ±2 g (3.9 mg/LSB)	Range ±4 g (7.8 mg/LSB)	Range ±8 g (15.6 mg/LSB)
01 1111 1111	1.996 g	+3.992 g	+7.984 g
01 1111 1110	1.992 g	+3.984 g	+7.968 g
…	…	…	…
00 0000 0001	0.003 g	+0.007 g	+0.015 g
00 0000 0000	0.000 g	0.000 g	0.000 g
11 1111 1111	–0.003 g	–0.007 g	–0.015 g
…	…	…	…
10 0000 0001	–1.961 g	–3.992 g	–7.984 g

Table 8. Accelerometer 10-bit output data (continued)

10-bit Data	Range ±2 g (3.9 mg/LSB)	Range ±4 g (7.8 mg/LSB)	Range ±8 g (15.6 mg/LSB)
10 0000 0000	–2.000 g	–4.000 g	–8.000 g
8-bit Data	Range ±2 g (15.6 mg)	Range ±4 g (31.25 mg)	Range ±8 g (62.5 mg)
0111 1111	1.984 g	+3.968 g	+7.937 g
0111 1110	1.968 g	+3.937 g	+7.875 g
…	…	…	…
0000 0001	+0.015 g	+0.031 g	+0.062 g
0000 0000	0.000 g	0.000 g	0.000 g
1111 1111	–0.015 g	–0.031 g	–0.062 g
…	…	…	…
1000 0001	–1.984 g	–3.968 g	–7.937 g
1000 0000	–2.000 g	–4.000 g	–8.000 g

Table 9. Accelerometer 8-bit output data

8-bit Data	Range ±2 g (15.6 mg/LSB)	Range ±4 g (31.25 mg/LSB)	Range ±8 g (62.5 mg/LSB)
0111 1111	1.9844 g	+3.9688 g	+7.9375 g
0111 1110	1.9688 g	+3.9375 g	+7.8750 g
…	…	…	…
0000 0001	+0.0156 g	+0.0313 g	+0.0625 g
0000 0000	0.000 g	0.0000 g	0.0000 g
1111 1111	–0.0156 g	–0.0313 g	–0.0625 g
…	…	…	…
1000 0001	–1.9844 g	–3.9688 g	–7.9375 g
1000 0000	–2.0000 g	–4.0000 g	–8.0000 g

5.3 Low power modes vs. high resolution modes

The MMA8653FC can be optimized for lower power modes or for higher resolution of the output data. One of the oversampling schemes of the data can be activated when MODS = 10 in Register 0x2B, which will improve the resolution of the output data only. The highest resolution is achieved at 1.56 Hz.

There is a trade-off between low power and high resolution. Low power can be achieved when the oversampling rate is reduced. When MODS = 11, the lowest power is achieved. The lowest power is achieved when the sample rate is set to 1.56 Hz.

5.4 Auto-WAKE/SLEEP mode

The MMA8653FC can be configured to transition between sample rates (with their respective current consumption) based on four of the interrupt functions of the device. The advantage of using the Auto-WAKE/SLEEP is that the system can automatically transition to a higher sample rate (higher current consumption) when needed, but spends the majority of the time in the SLEEP mode (lower current) when the device does not require higher sampling rates.

- **Auto-WAKE** refers to the device being triggered by one of the interrupt functions to transition to a higher sample rate. This may also interrupt the processor to transition from a SLEEP mode to a higher power mode.
- **SLEEP mode** occurs after the accelerometer has not detected an interrupt for longer than the user-definable timeout period. The device will transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode, to save on current during this period of inactivity.

The Interrupts that can WAKE the device from SLEEP are Orientation detection and Freefall detection. The interrupts that can keep the device from falling asleep are the same interrupts that can wake the device.

5.5 Freefall detection

MMA8653FC has an interrupt architecture for detecting a Freefall.

- Freefall can be enabled.
- Freefall is detected when the acceleration magnitude *is less than* the configured threshold.

The freefall configuration does not use a high-pass filter.

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is *below a user-specified threshold for a user-definable amount of time*. Usable threshold levels are typically between ±100 mg and ±500 mg.

5.6 Orientation detection

The MMA8653FC incorporates an advanced orientation detection algorithm with the ability to detect all six orientations shown in Figure 6. The algorithm uses a single default trip point setting. The transition from portrait to landscape is fixed at 45° midpoint angle and ±15° hysteresis angle. This allows for smooth transitions from portrait to landscape at approximately 30° and landscape to portrait at approximately 60° (Figure 7).

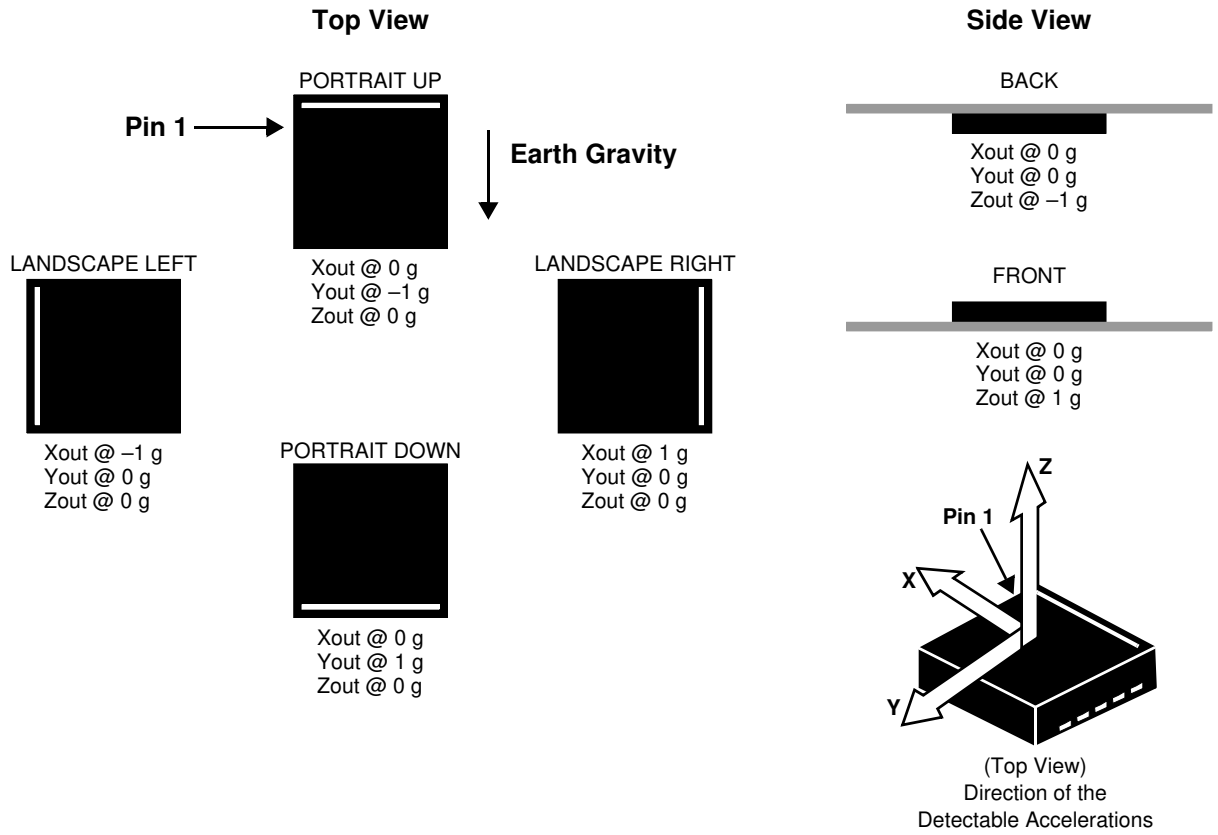


Figure 6. Sensitive axes orientation

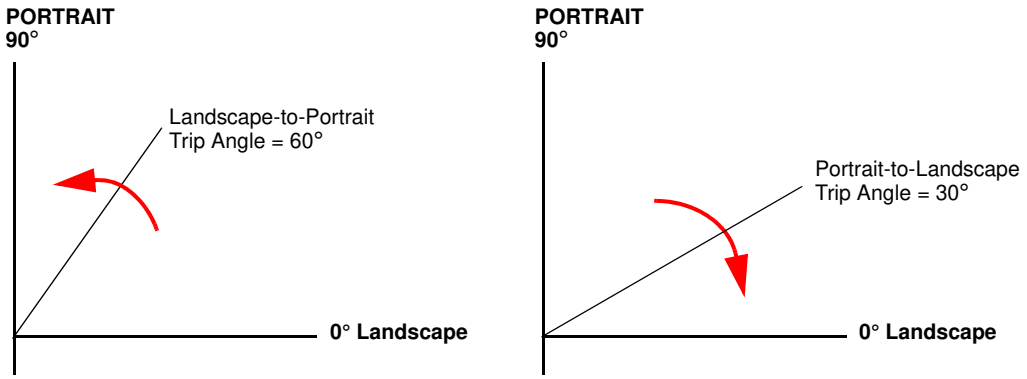


Figure 7. Landscape-to-Portrait transition trip angles

Based on the known functionality of linear accelerometers, when a device is oriented at a certain angle from flat and the device is rotating at slow angular speeds about the Z-axis, it is not possible to detect changes in acceleration. The angle at which the device no longer detects the orientation change is referred to as the “Z-lockout angle” (Figure 8).

The MMA8653FC orientation detection algorithm is configured to operate when the device is oriented at an angle of 29° or greater from flat (Zout = –1 g or Zout = 1 g), with an accuracy of ±2°.

.

When lifting the device upright from the flat position, orientation detection will be active for orientation angles greater than 29° from flat. This is the only setting available.

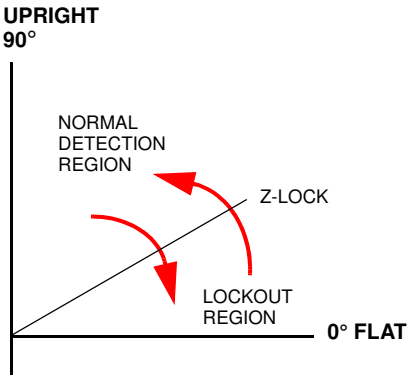


Figure 8. Z-Tilt angle lockout transition

5.7 Interrupt register configurations

There are four configurable interrupts in the MMA8653FC: Data Ready, Motion/Freefall, Orientation, and Auto-SLEEP events.

These four interrupt sources can be routed to one of two interrupt pins.

The interrupt source must be enabled and configured.

If the event flag is asserted because the event condition is detected, then the corresponding interrupt pin (INT1 or INT2) will assert.

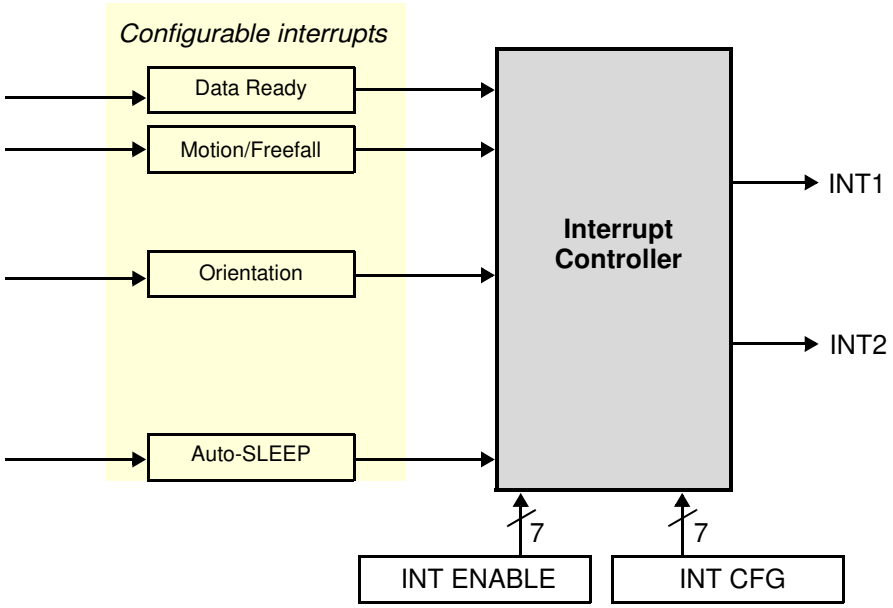


Figure 9. System interrupt generation

- The MMA8653FC features an interrupt signal that indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.
- The MMA8653FC may also be configured to generate *other interrupt signals* accordingly, to the programmable embedded functions of the device for Motion, Freefall, and Orientation.

5.8 Serial I²C interface

Acceleration data may be accessed through an I²C interface, thus making the device particularly suitable for direct interfacing to a microcontroller. The acceleration data and configuration registers embedded inside the MMA8653FC are accessed through the I²C serial interface (Table 10).

- To enable the I²C interface, VDDIO line must be tied high (to the interface supply voltage). If VDD is not present and VDDIO is present, then the MMA8653FC is in OFF mode—and communications on the I²C interface are ignored.
- The I²C interface may be used for communications between other I²C devices; the MMA8653FC does not affect the I²C bus.

Table 10. Serial Interface pins

Pin Name	Pin Description	Notes
SCL	I²C Serial Clock	**There are two signals associated with the I²C bus; the Serial Clock Line (SCL) and the Serial Data line (SDA).** • SDA is a bidirectional line used for sending and receiving the data to/from the interface. • External pullup resistors connected to VDDIO are expected for SDA and SCL. When the bus is free, both SCL and SDA lines are high.
SDA	I²C Serial Data	

The I²C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I²C standards (Table 11).

I²C operation:

1. The transaction on the bus is started through a start condition (START) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After START has been transmitted by the Master, the bus is considered busy.
2. The next byte of data transmitted after START contains the slave address in the first seven bits. The eighth bit tells whether the Master is *receiving data from the slave* or is *transmitting data to the slave*.
3. After a start condition and when an address is sent, each device in the system compares the first seven bits with its address. If the device's address matches the sent address, then the device considers itself addressed by the Master.

4. The 9th clock pulse following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low, so that it remains stable low during the high period of the acknowledge clock period.
5. A Master may also issue a repeated START during a data transfer. The MMA8653FC expects repeated STARTs to be used to randomly read from specific registers.
6. A low-to-high transition on the SDA line *while the SCL line is high* is defined as a stop condition (STOP). A data transfer is always terminated by a STOP.

The MMA8653FC's standard slave address is 0011101 or 0x01D. The slave addresses are factory programmed; alternate addresses are available upon request.

Table 11. I^2C Device address sequence

Command	[6:0] Device address	[6:0] Device address	R/W	8-bit final value
Read	0011101	0x1D	1	0x3B
Write	0011101	0x1D	0	0x3A

5.8.1 Single-byte read

1. The transmission of an 8-bit command begins on the falling edge of SCL. After the eight clock cycles are used to send the command, note that *the data returned* is sent with the MSB first after the data is received. Figure 10 shows the timing diagram for the accelerometer 8-bit I^2C read operation.
2. The Master (or MCU) transmits a start condition (ST) to the MMA8653FC [slave address (0x1D), with the R/W bit set to “0” for a write], and the MMA8653FC sends an acknowledgement.
3. Next the Master (or MCU) transmits the address of the register to read, and the MMA8653FC sends an acknowledgement.
4. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8653FC (0x1D), with the R/W bit set to “1” for a read from the previously selected register.
5. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

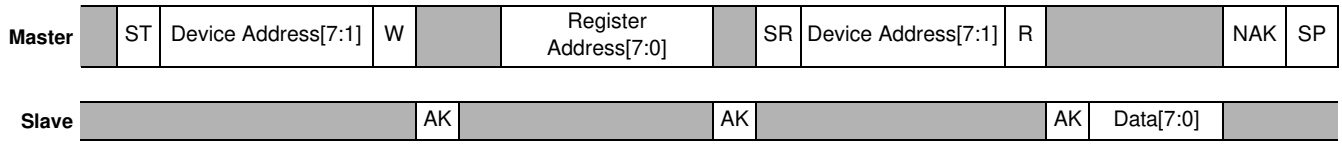


Figure 10. Single-Byte Read timing (I^2C)

NOTE

For the following subsections, use the following legend.

Legend

ST: Start Condition	SP: Stop Condition	NAK: No Acknowledge	W: Write = 0
SR: Repeated Start Condition	AK: Acknowledge	R: Read = 1	

5.8.2 Multiple byte read

(See Table 11 for next auto-increment address.)

1. When performing a multi-byte read or “burst read”, the MMA8653FC automatically increments the received register address commands after a read command is received.
2. After following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each MMA8653FC acknowledgment (AK) is received,
3. Until a no acknowledge (NAK) occurs from the Master,
4. Followed by a stop condition (SP), which signals the end of transmission.

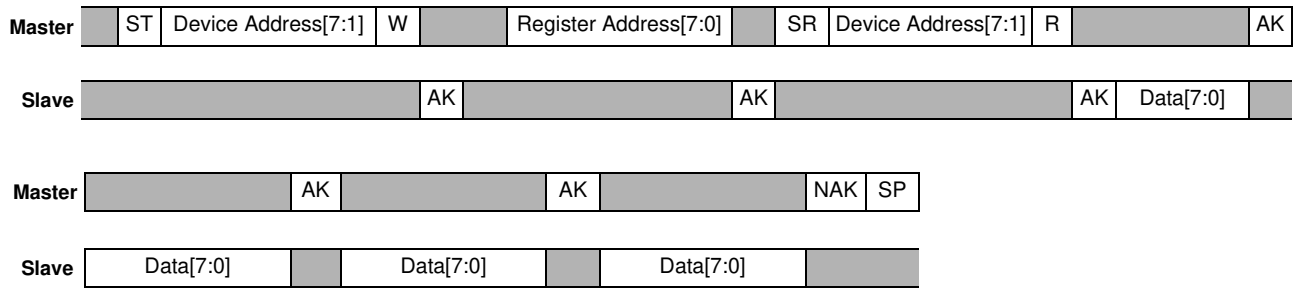


Figure 11. Multiple Byte Read timing (I^2C)

5.8.3 Single byte write

1. To start a write command, the Master transmits a start condition (ST) to the MMA8653FC, slave address ($1D) with the R/W bit set to “0” for a write,
2. The MMA8653FC sends an acknowledgement.
3. Next the Master (MCU) transmits the address of the register to write to, and the MMA8653FC sends an acknowledgement.
4. Then the Master (or MCU) transmits the 8-bit data to write to the designated register, and the MMA8653FC sends an acknowledgement that it has received the data. Because this transmission is complete, the Master transmits a stop condition (SP) to the data transfer. The data sent to the MMA8653FC is now stored in the appropriate register.

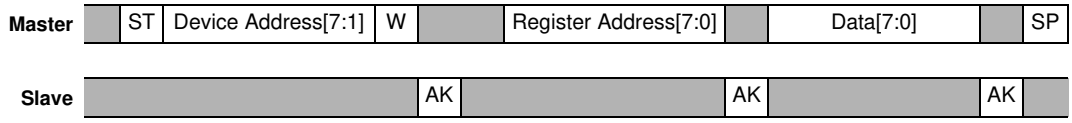


Figure 12. Single Byte Write timing (I^2C)

5.8.4 Multiple byte write

(See Table 11 for next auto-increment address.)

1. After a write command is received, the MMA8653FC *automatically increments* the received register address commands.
2. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each MMA8653FC acknowledgment (ACK) is received.

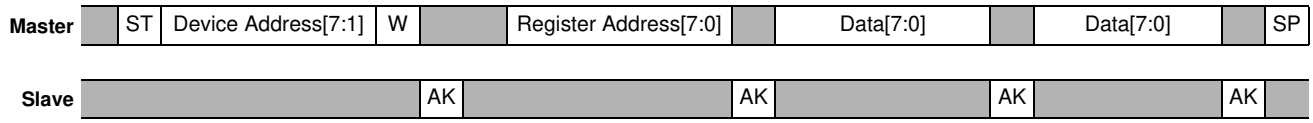


Figure 13. Multiple Byte Write timing (I^2C)

6 Register Descriptions

6.1 Register address map

Table 12. MMA8653FC register address map

Field	Type	Register Address	Auto-Increment Address		Default	Hex Value	Comment
			F_READ = 0	F_READ = 1			
STATUS[1],[2]	R	0x00	0x01		00000000	0x00	Real time status
OUT_X_MSB[1]	R	0x01	0x02	0x03	Output	—	[7:0] are 8 MSBs of 10-bit sample.
OUT_X_LSB[1]	R	0x02	0x03	0x00	Output	—	[7:6] are 2 LSBs of 10-bit real-time sample
OUT_Y_MSB[1]	R	0x03	0x04	0x05	Output	—	[7:0] are 8 MSBs of 10-bit real-time sample
OUT_Y_LSB[1]	R	0x04	0x05	0x00	Output	—	[7:6] are 2 LSBs of 10-bit real-time sample
OUT_Z_MSB[1]	R	0x05	0x06	0x00	Output	—	[7:0] are 8 MSBs of 10-bit real-time sample
OUT_Z_LSB[1]	R	0x06	0x00		Output	—	[7:6] are 2 LSBs of 10-bit real-time sample
Reserved	R	0x07–0x0A	—		00000000	0x00	Reserved. Read return 0x00.
SYSMOD	R	0x0B	0x0C		00000000	0x00	Current System Mode
INT_SOURCE[1],[2]	R	0x0C	0x0D		00000000	0x00	Interrupt status
WHO_AM_I[3]	R	0x0D	0x0E		01001010	0x5A	Device ID (0x5A)
XYZ_DATA_CFG[3],[4]	R/W	0x0E	0x0F		00000000	0x00	Dynamic Range Settings
Reserved	R	0x0F	—		00000000	0x00	Reserved. Read return 0x00.
PL_STATUS[1],[2]	R	0x10	0x11		00000000	0x00	Landscape/Portrait orientation status
PL_CFG[3],[4]	R/W	0x11	0x12		10000000	0x80	Landscape/Portrait configuration.
PL_COUNT[3],[4]	R/W	0x12	0x13		00000000	0x00	Landscape/Portrait debounce counter
PL_BF_ZCOMP[3]	R	0x13	0x14		01000100	0x44	Back/Front, Z-Lock Trip threshold
PL_THS_REG[3]	R	0x14	0x15		10000100	0x84	Portrait to Landscape Trip angle
FF_MT_CFG[3],[4]	R/W	0x15	0x16		00000000	0x00	Freefall/Motion functional block configuration
FF_MT_SRC[1],[2]	R	0x16	0x17		00000000	0x00	Freefall/Motion event source register
FF_MT_THS[3],[4]	R/W	0x17	0x18		00000000	0x00	Freefall/Motion threshold register
FF_MT_COUNT[3],[4]	R/W	0x18	0x19		00000000	0x00	Freefall/Motion debounce counter
Reserved	R	0x19–0x28	—		00000000	0x00	Reserved. Read return 0x00.
ASLP_COUNT[3],[4]	R/W	0x29	0x2A		00000000	0x00	Counter setting for Auto-SLEEP/WAKE
CTRL_REG1[3],[4]	R/W	0x2A	0x2B		00000000	0x00	Data Rates, ACTIVE Mode.
CTRL_REG2[3],[4]	R/W	0x2B	0x2C		00000000	0x00	Sleep Enable, OS Modes, RST, ST
CTRL_REG3[3],[4]	R/W	0x2C	0x2D		00000000	0x00	Wake from Sleep, IPOL, PP_OD
CTRL_REG4[3],[4]	R/W	0x2D	0x2E		00000000	0x00	Interrupt enable register
CTRL_REG5[3],[4]	R/W	0x2E	0x2F		00000000	0x00	Interrupt pin (INT1/INT2) map
OFF_X[3],[4]	R/W	0x2F	0x30		00000000	0x00	X-axis offset adjust
OFF_Y[3],[4]	R/W	0x30	0x31		00000000	0x00	Y-axis offset adjust
OFF_Z[3],[4]	R/W	0x31	0x0D		00000000	0x00	Z-axis offset adjust

1. The register data is only valid in ACTIVE mode.
2. Register contents are reset when transition from STANDBY to ACTIVE mode occurs.
3. Register contents are preserved when transition from ACTIVE to STANDBY mode occurs.
4. Modification of this register's content can only occur when device is in STANDBY mode, except CTRL_REG1 ACTIVE bit and CTRL_REG2 RST bit.

6.2 Register bit map

Table 13. MMA8653FC register bit map

Reg	Field	Definition	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	STATUS	Data Status	R	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
01	OUT_X_MSB	10-bit X Data	R	XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2
02	OUT_X_LSB	10-bit X Data	R	XD1	XD0	0	0	0	0	0	0
03	OUT_Y_MSB	10-bit Y Data	R	YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2
04	OUT_Y_LSB	10-bit Y Data	R	YD1	YD0	0	0	0	0	0	0
05	OUT_Z_MSB	10-bit Z Data	R	ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2
06	OUT_Z_LSB	10-bit Z Data	R	ZD1	ZD0	0	0	0	0	0	0
07–0A	Reserved	—	R	0	0	0	0	0	0	0	0
0B	SYSMOD	System Mode	R	0	0	0	0	0	0	SYSMOD1	SYSMOD0
0C	INT_SOURCE	Interrupt Status	R	SRC_ASLP	0	0	SRC_LNDPRT	0	SRC_FF_MT	0	SRC_DRDY
0D	WHO_AM_I	ID Register	R	0	1	0	1	1	0	1	0
0E	XYZ_DATA_CFG	Data Config	R/W	0	0	0	0	0	0	FS1	FS0
0F	Reserved	—	R	—	—	—	—	—	—	—	—
10	PL_STATUS	Portrait Landscape Status	R	NEWLP	LO	0	0	0	LAPO[1]	LAPO[0]	BAFRO
11	PL_CFG	Portrait Landscape Configuration	R/W	DBCNTM	PL_EN	0	0	0	0	0	0
12	PL_COUNT	Portrait Landscape Debounce	R/W	DBNCE[7]	DBNCE[6]	DBNCE[5]	DBNCE[4]	DBNCE[3]	DBNCE[2]	DBNCE[1]	DBNCE[0]
13	PL_BF_ZCOMP	Portrait Landscape Back/Front Z Comp	R	0	1	0	0	0	1	0	0
14	PL_THS_REG	Portrait Landscape Threshold	R	1	0	0	0	0	1	0	0
15	FF_MT_CFG	Freefall/Motion Config	R/W	ELE	OAE	ZEFE	YEFE	XEFE	0	0	0
16	FF_MT_SRC	Freefall/Motion Status	R	EA	0	ZHE	ZHP	YHE	YHP	XHE	XHP
17	FF_MT_THS	Freefall/Motion Threshold	R/W	DBCNTM	THS6	THS5	THS4	THS3	THS2	THS1	THS0
18	FF_MT_COUNT	Freefall/Motion Debounce	R/W	D7	D6	D5	D4	D3	D2	D1	D0
19–28	Reserved	—	R	—	—	—	—	—	—	—	—
29	ASLP_Count	Counter setting for Auto-SLEEP/WAKE	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2A	CTRL_REG1	Control Reg1	R/W	ASLP_RATE1	ASLP_RATE0	DR2	DR1	DR0	0	F_READ	ACTIVE
2B	CTRL_REG2	Control Reg2	R/W	ST	RST	—	SMODS1	SMODS0	SLPE	MODS1	MODS0
2C	CTRL_REG3	Control Reg3	R/W	—	—	WAKE_LNDPRT	—	WAKE_FF_MT	0	IPOL	PP_OD
2D	CTRL_REG4	Control Reg4	R/W	INT_EN_ASLP	—	—	INT_EN_LNDPRT	—	INT_EN_FF_MT	0	INT_EN_DRDY
2E	CTRL_REG5	Control Reg5	R/W	INT_CFG_ASLP	—	—	INT_CFG_LNDPRT	—	INT_CFG_FF_MT	0	INT_CFG_DRDY
2F	OFF_X	X 8-bit offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30	OFF_Y	Y 8-bit offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31	OFF_Z	Z 8-bit offset	R/W	D7	D6	D5	D4	D3	D2	D1	D0

Note: Bits showing "—" can read as either 0 or 1, and these bits have no definition.

6.3 Data registers

The following are the data registers for the MMA8653FC device. For more information about data manipulation in the MMA8653FC, see application note AN4083, *Data Manipulation and Basic Settings for Xtrinsic MMA865xFC Accelerometers.*

- When accessing the 8-bit data, the F_READ bit (register 0x2A) is set, which modifies the auto-incrementing to skip over the LSB data.
- When the F_READ bit is cleared, the 12-bit data is read, accessing all 6 bytes sequentially (X_MSB, X_LSB, Y_MSB, Y_LSB, Z_MSB, Z_LSB).

6.3.1 0x00: STATUS Data Status register

Data Status register 0x00 reflects the real-time status information of the X, Y and Z sample data; it contains the X, Y, and Z data overwrite and data ready flag.

These registers contain the X-axis, Y-axis, and Z-axis 12-bit output sample data (expressed as 2's complement numbers).

Table 14. 0x00 STATUS: Data Status register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Table 15. STATUS register bits

Bit(s)	Field	Description	Notes
7	ZYXOW	**X, Y, Z-axis data overwrite** • Set whenever a new acceleration data is produced *before completing the retrieval of the previous set*. This event occurs when the content of at least one acceleration data register (i.e., OUT_X, OUT_Y, OUT_Z) has been overwritten. • Cleared when the high bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the channels are read. 0 No data overwrite has occurred (default) 1 Previous X, Y, or Z data was overwritten by new X, Y, or Z data before it (the previous X, Y, or Z data) was read	
6	ZOW	**Z-axis data overwrite**	***For # = Z, Y, or X:*** • Set whenever a new acceleration sample *related to the #-axis* is generated *before the retrieval of the previous sample*. When this occurs, the previous sample is overwritten. • Cleared whenever the OUT_#_MSB register is read. 0 No data overwrite has occurred (default) 1 Previous Z-axis data was overwritten by new #-axis data before it (the previous #-axis data) was read
5	YOW	**Y-axis data overwrite**	
4	XOW	**X-axis data overwrite**	
3	ZYXDR	**X, Y, Z-axis new data ready** • Set when a new sample for any of the enabled channels is available. • Cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the channels are read. 0 No new set of data ready (default) 1 A new set of data is ready	
2	ZDR	**Z-axis new data available**	For # = Z, Y, or X • Set whenever a new acceleration sample *related to the #-axis* is generated. • Cleared whenever the OUT_#_MSB register is read. 0 No new #-axis data ready (default) 1 New #-axis data is ready
1	YDR	**Y-axis new data available**	
0	XDR	**X-axis new data available**	

Table 16. 0x01 OUT_X_MSB: X_MSB register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2

Table 17. 0x02 OUT_X_LSB: X_LSB register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD1	XD0	0	0	0	0	0	0

Table 18. 0x03 OUT_Y_MSB: Y_MSB register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2

Table 19. 0x04 OUT_Y_LSB: Y_LSB register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD1	YD0	0	0	0	0	0	0

Table 20. 0x05 OUT_Z_MSB: Z_MSB register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD9	ZD8	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2

Table 21. 0x06 OUT_Z_LSB: Z_LSB register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD1	ZD0	0	0	0	0	0	0

- OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x01 – 0x06, to reduce reading the status followed by 10-bit axis data to 7 bytes. If the F_READ bit is set (0x2A bit 1), then auto-increment will skip over LSB registers (to access the MSB data only). This will shorten the data acquisition from seven bytes to four bytes.
- The LSB registers can only be read immediately following the read access of the corresponding MSB register.
  - A random read access to the LSB registers is not possible.
  - *Reading the MSB register and then the LSB register in sequence* ensures that both bytes (LSB and MSB) belong to the same data sample, even if a new data sample arrives between reading the MSB and the LSB byte.

6.4 System status and ID registers

6.4.1 0x0B: SYSMOD System Mode register

The System mode register indicates the current device operating mode. Applications using the Auto-SLEEP/WAKE mechanism should use the SYSMOD register to synchronize the application with the device operating mode transitions.

Table 22. 0x0B SYSMOD: System Mode register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SYSMOD1	SYSMOD0

Table 23. SYSMOD register

Bit(s)	Field	Description
7–2	0	**Reserved**
1–0	SYSMOD[1:0]	**System Mode** 00 STANDBY mode (default) 01 WAKE mode 10 SLEEP mode

6.4.2 0x0C: INT_SOURCE System Interrupt Status register

In the interrupt source register, the status of the various embedded features can be determined.

- The bits that are set (logic ‘1’) indicate which function has asserted an interrupt.
- The bits that are cleared (logic ‘0’) indicate which function has not asserted (or has deasserted) an interrupt.

INT_SOURCE register bits are set by a low-to-high transition, and are cleared by reading the appropriate interrupt source register. For example, the SRC_DRDY bit is cleared when the ZYXDR bit (STATUS register) is cleared, but the SRC_DRDY bit is not cleared by simply reading the STATUS register (0x00), but is cleared by reading all the X, Y, and Z MSB data.

Table 24. 0x0C INT_SOURCE: System Interrupt Status register (Read Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRC_ASLP	0	0	SRC_LNDPRT	0	SRC_FF_MT	0	SRC_DRDY

Table 25. INT_SOURCE register

Bit(s)	Field	Description
7	SRC_ASLP	**Auto-SLEEP/WAKE interrupt status** bit • **WAKE-to-SLEEP** transition occurs when no interrupt occurs for a time period that exceeds the user-specified limit (ASLP_COUNT). This causes the system to transition to a user-specified low ODR setting. • **SLEEP-to-WAKE** transition occurs when the user-specified interrupt event has woken the system; thus causing the system to transition to a user-specified high ODR setting. • Reading the SYSMOD register clears the SRC_ASLP bit. 1 An interrupt event *that can cause a WAKE-to-SLEEP or SLEEP-to-WAKE system mode transition* has occurred. 0 No WAKE-to-SLEEP or SLEEP-to-WAKE system mode transition interrupt event has occurred. (default)
6	0	
5	0	
4	SRC_LNDPRT	**Landscape/Portrait Orientation interrupt status** bit • SRC_LNDPRT bit is asserted whenever the NEWLP bit (PL_STATUS register) is asserted and the interrupt has been enabled. • SRC_LNDPRT bit is cleared by reading the PL_STATUS register. 1 An interrupt was generated due to a change in the device orientation status. 0 No change in orientation status was detected. (default)
3	0	
2	SRC_FF_MT	**Freefall/Motion interrupt status** bit • SRC_FF_MT bit is asserted whenever the EA bit (FF_MT_SRC register) is asserted and the FF_MT interrupt has been enabled. • SRC_FF_MT bit is cleared by reading the FF_MT_SRC register. 1 The Freefall/Motion function interrupt is active. 0 No Freefall or Motion event was detected. (default)
1	0	
0	SRC_DRDY	**Data Ready Interrupt bit status** bit • SRC_DRDY bit is asserted when the ZYXOW and/or ZYXDR bit is set and the interrupt has been enabled. • SRC_DRDY bit is cleared by reading the X, Y, and Z data. 1 The X, Y, Z data ready interrupt is active (indicating the presence of new data and/or data overrun). 0 The X, Y, Z interrupt is not active. (default)

6.4.3 0x0D: WHO_AM_I Device ID register

The device identification register identifies the part. The default value is 0x5A (for MMA8653FC).
This value is programmed by Freescale before the part leaves the factory. For custom alternate values, contact Freescale.

Table 26. 0x0D: WHO_AM_I Device ID register (Read-Only) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	1	0	1	0

6.5 Data configuration registers

6.5.1 0x0E: XYZ_DATA_CFG register

The XYZ_DATA_CFG register sets the dynamic range.

Table 27. 0x0E: XYZ_DATA_CFG register (Read/Write) *Back to Register Address Map*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	FS1	FS0

Table 28. XYZ Data Configuration register

Bit(s)	Field	Description	
7–2	0		
1–0	FS[1:0]	**Output buffer data format using full scale** 00 ±2 g (default)	The default full scale value range is ±2 g.

Table 29. Full-Scale Range

FS1	FS0	Full-Scale Range
0	0	±2 g
0	1	±4 g
1	0	±8 g
1	1	Reserved