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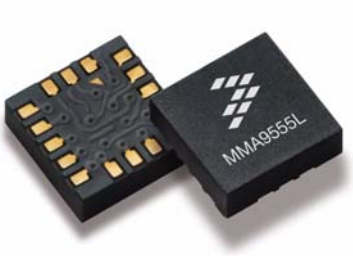
MMA9555L Intelligent Motion-Sensing Pedometer

MMA9555L

The MMA9555L intelligent motion-sensing pedometer is an extension of the MMA955xL intelligent sensor platform. This device incorporates a 3-axis MEMS accelerometer, signal conditioning, data conversion, and a 32-bit microcontroller. This intelligent motion-sensing sensor provides sophisticated pedometer functionality, activity level and six directional orientation monitoring.

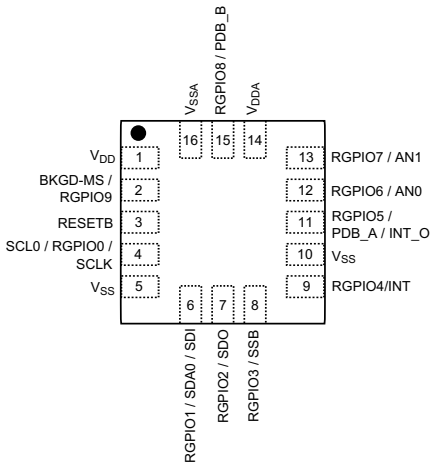
The integrated functionality of sensor initialization, calibration, data compensation, and computation functions off-loads CPU bandwidth from the system application processor. Therefore, total system power consumption is significantly reduced, because the application processor stays powered down until absolutely needed. In addition, the device can be configured for an autosleep/autowake capability.

MMA9555L is available in a plastic LGA package; the device is guaranteed to operate over the extended temperature range of –40 °C to +85 °C.



16-pin LGA
3 mm x 3 mm x 1 mm
Case 2094-01

Top view



Pin Connections

Features

- High resolution 3-axis accelerometer with 16-bit ADC (0.061 m*g*/LSB @ 2 *g*)
- Selectable *g* range (±2/4/8 *g*) and output data rates (488 Hz–3.8 Hz)
- One slave SPI or I^2C interface operating at up to 2 Mbps for communication with the host processor
- 1.8 V supply voltage low power consumption
  - 2 µA typical current at stop mode
  - 117 µA for pedometer running at active and 92 µA at suspend
  - 87 µA when six-direction detection mode
- Complete built-in firmware for smart sensing intelligence
  - Real time and preemptive application task scheduling
  - Command interpreter support command/response and streaming mode
  - Low-power pedometer with rich output information
    - Step counting
    - Speed, distance, calorie count estimation
    - Activity level (rest, walking, jogging, running)
  - Six-direction detection output
  - Extensive set of power-management features and low-power mode
  - GPIO2–GPIO8 can be used for expanded configurable GPIO functions
- Minimal external component requirements

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Typical Applications

This low-power, intelligent sensor is optimized for use in portable and mobile consumer products such as:

- Pedometers, wearable devices, smart watches, wristband
- Sleep monitoring
- Smart earphone
- Health monitoring

Ordering information

Part number	Firmware	Temperature range	Package description	Shipping
MMA9555LR1	Pedometer + Six Directions of Orientation + GPIO Input/Output	–40 °C to +85 °C	LGA-16	Tape and reel

Related Documentation

The MMA9555L device features and operations are described in reference manuals, release notes, and application notes. To find the most-current versions of these documents:

1. Go to the NXP homepage at: nxp.com.
2. In the Keyword search box at the top of the page, enter the device number MMA9555L.

In the Refine Your Results pane on the left, click on the Documentation link.

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1 Intelligent Sensing Platform Offering

NXP has a broad offering of MMA955xL devices.

The MMA9550L, MMA9551L, MMA9553L, and MMA9555L devices can function immediately as shipped. They have an internal command interpreter and applications scheduler. These devices can interact directly with the users' host system.

The MMA9550L, MMA9551L, MMA9553L and MMA9559L devices are programmable with additional user application software. These devices have a variety of user flash and RAM memory space available. The MMA9555L is provided with complete factory build application specific software, no additional user software programming in the device is needed.

NOTE

The information and specifications provided in this data sheet are specific to the MMA9555L. Information for the other devices can be found in the MMA955xL collateral and datasheet.

Table 1. NXP Intelligent Sensing Product Comparison

Feature - Device	MMA9550L	MMA9551L	MMA9553L	MMA9555L	MMA9559L
Key elements	Motion sensing	Gesture sensing	Pedometer	Pedometer + six-direction orientation + GPIO Input/Output	High flexibility
ADC resolution (bits)	10,12,14,16 bits	10,12,14,16 bits	10,12,14,16 bits	10,12,14,16 bits	10,12,14,16 bits
g measurement ranges	2 *g*, 4 *g*, 8 *g*	2 *g*, 4 *g*, 8 *g*	2 *g*, 4 *g*, 8 *g*	2 *g*, 4 *g*, 8 *g*	2 *g*, 4 *g*, 8 *g*
Real-time and preemptive scheduling	Yes	Yes	Yes	Yes	No
Event management	No	No	No	No	Yes
Slave Port Command Interpreter					
• Normal mode	Yes	Yes	Yes	Yes	No
• Legacy mode	Yes	Yes	Yes	Yes	No
• Streaming mode	Yes	Yes	Yes	Yes	No
Front-end processing					
• 100 Hz BW anti-aliasing	Yes	Yes	Yes	Yes	No
• 50 Hz BW anti-aliasing	Yes	Yes	Yes	Yes	No
• *g*-mode-dependent resolution	Yes	Yes	Yes	Yes	Yes
• Absolute value	Yes	Yes	Yes	Yes	No
• Low-pass filter	Yes	Yes	Yes	Yes	No
• High-pass filter	Yes	Yes	Yes	Yes	No
• Data-ready interrupt	Yes	Yes	Yes	Yes	Yes
Gesture applications					
• High *g*/Low *g*	No	Yes	No	No	No
• Tilt	No	Yes	No	No	No

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Table 1. NXP Intelligent Sensing Product Comparison (Continued)

Feature - Device	MMA9550L	MMA9551L	MMA9553L	MMA9555L	MMA9559L
• Portrait/Landscape	No	Yes	No	No	No
• Programmable orientation	No	Yes	No	No	No
• Tap/Double-tap	No	Yes	No	No	No
• Freefall	No	Yes	No	No	No
• Motion	No	Yes	No	No	No
Data-storage modules					
• Data FIFO	Yes	Yes	Yes	Yes	No
• Event queue	Yes	Yes	Yes	Yes	No
• Inter-process FIFO	No	No	No	No	Yes
Power-control module					
• Run and Stop on idle	Yes	Yes	Yes	Yes	Yes
• Run and No stop	Yes	Yes	Yes	Yes	Yes
• Stop NC	Yes	Yes	Yes	Yes	Yes
• Auto-Wake / Auto-Sleep / Doze	Yes	Yes	Yes	Yes	No
Data-management daemons	Yes	Yes	Yes	Yes	Yes
Pedometer applications					
• Step count	No	No	Yes	Yes	No
• Distance	No	No	Yes	Yes	No
• Adaptive distance	No	No	Yes	Yes	No
• Activity monitor	No	No	Yes	Yes	No
Six Directional Orientation	No	No	No	Yes	No
GPIO management	No	No	No	Yes	No

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2 General Description

2.1 Functional Overview

The MMA9555L is an intelligent motion sensing pedometer, it consists of a 3-axis, MEMS accelerometer and a mixed-signal ASIC with an integrated, 32-bit CPU. The mixed-signal ASIC can be utilized to measure and condition the outputs of the MEMS accelerometer, internal temperature sensor, or a differential analog signal from an external device.

The calibrated, measured sensor outputs can be read via the slave I^2C or SPI port and utilized internally within the MMA9555L to provide advanced intelligent motion detection outputs like pedometer step count, activity level and six directional orientation detections which can be accessed via the slave I^2C or SPI port.

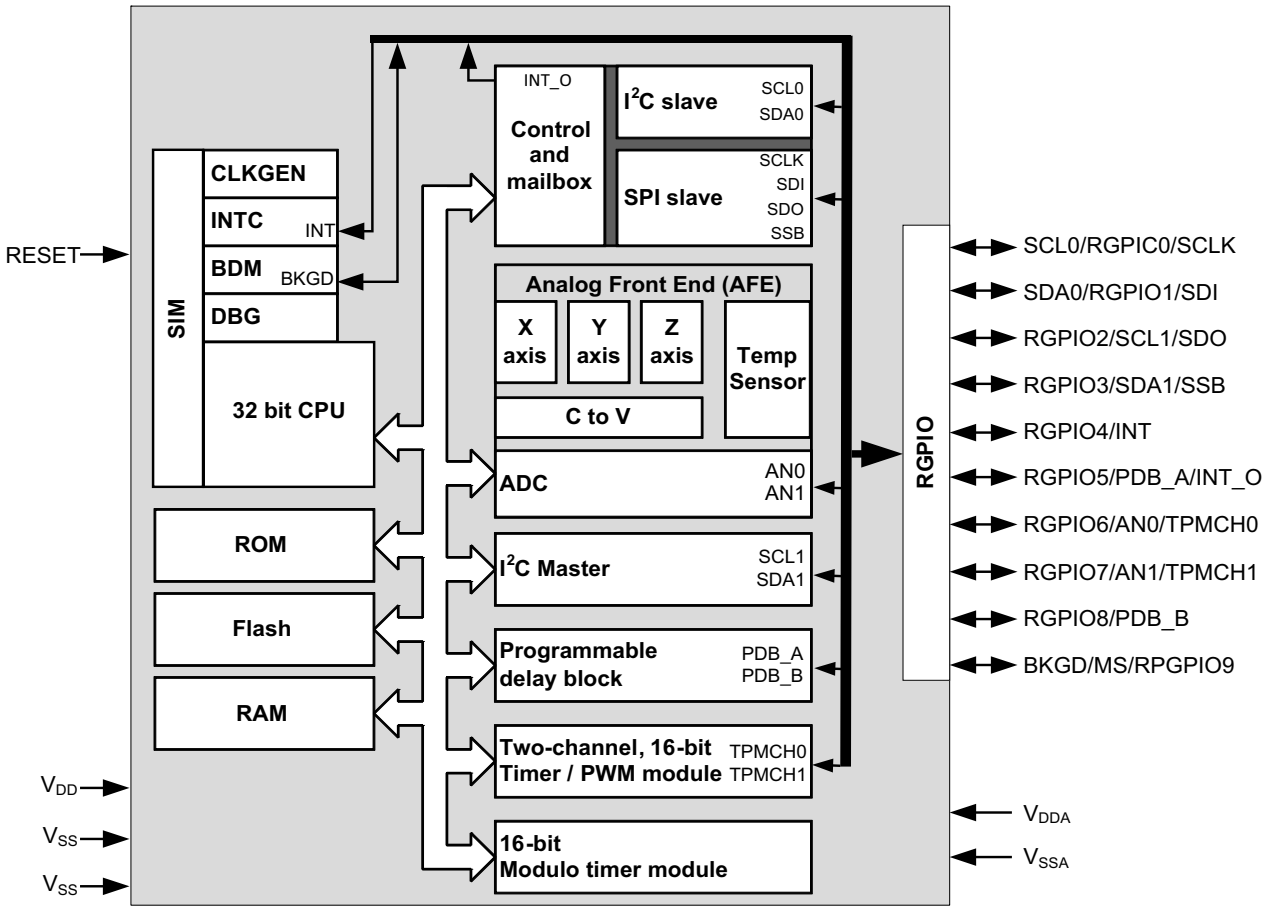

Figure 1. MMA9555L block diagram

A block-level view is shown in Figure 1 with building blocks of devices and built-in applications summarized at a high level. The analog/mixed-mode subsystem associated with a digital engine is composed of:

- The analog subsystem is composed of:
  - A 3-axis transducer that is an entirely passive block including the MEMS structures.
  - An Analog Front End (AFE) with the following:
    - A capacitance-to-voltage converter
    - An analog-to-digital converter
    - A temperature sensor
- The digital subsystem is composed of:
  - A 32-bit CPU
  - Memory: RAM, ROM, and flash
  - Rapid GPIO (RGPIO) port-control logic

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- I^2C or SPI slave interface
- System Integration Module (SIM)
- Clock-Generation Module

The slave interfaces (either SPI or I^2C) operate independently of the CPU subsystem. They can be accessed at any time, including while the device is in low-power, deep-sleep mode.

2.2 Pinout

The package pinout definition for this device is designed as a superset of functions on NXP's other MMA955xL offerings. All pins on the device are utilized and many are multiplexed.

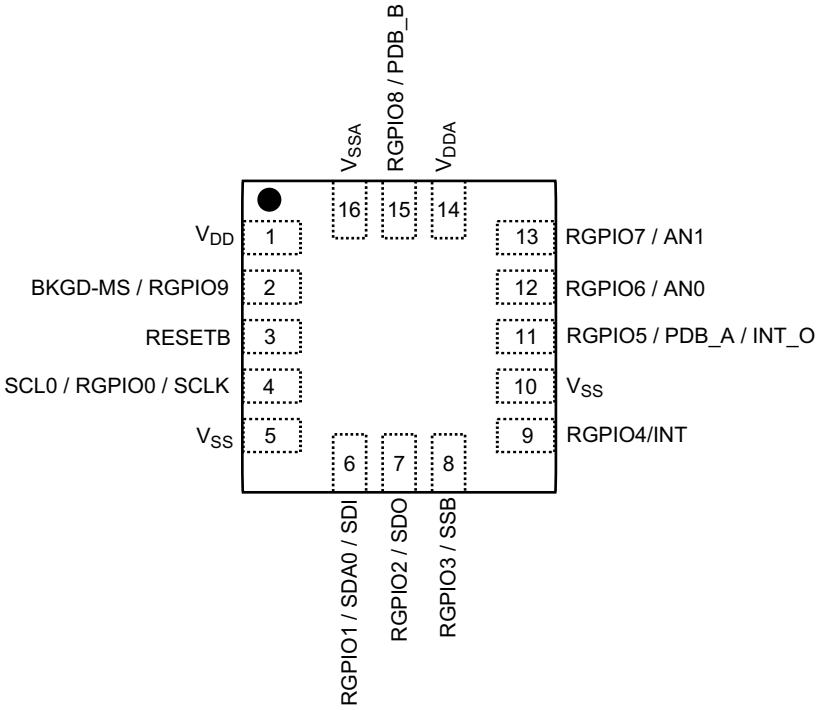

Figure 2. Device pinout (top view)

2.2.1 Pin Functions

The following table summarizes functional options for each pin on this device.

Table 2. Pin functions

Pin #	Pin Name	Description
1	V_{DD}	Digital power supply
2	BKGD / MS / RGPIO9	Background-debug / Mode select / RGPIO9
3	RESETB	Active-low reset. RESETB is an open-drain, bidirectional pin. By default, the output function is not on. Must be pulled to V_{DD} via resistor at startup. After startup, Reset may be asserted low to reset the device.
4	SCL0 / RGPIO0 / SCLK	Serial clock for slave I^2C / RGPIO0 / Serial clock for slave SPI
5	V_{SS}	Digital ground
6	SDA0 / RGPIO1 / SDI	Serial data for slave I^2C / RGPIO1 / SPI serial data input
7	RGPIO2 / SDO	RGPIO2 / SPI serial data output
8	RGPIO3 / SBB	RGPIO3 / SPI slave select. RGPIO3 / SSB = Low at startup selects SPI. High at startup selects I^2C.

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Table 2. Pin functions (Continued)

Pin #	Pin Name	Description
9	RGPIO4/INT	RGPIO4 / Interrupt input
10	RESERVED	Must be connected to V_{SS} ground externally
11	RGPIO5 / INT_O	RGPIO5 or INT_O slave-port interrupt output. INT_O can only output interrupts from the COCO bit. **For setting sensor data output interrupts, use RGPIO6–RGPIO9.**
12	RGPIO6 / AN0	RGPIO6 / ADC Input 0
13	RGPIO7 / AN1	RGPIO7 / ADC Input 1
14	V_{DDA}	Analog power
15	RGPIO8	RGPIO8
16	V_{SSA}	Analog ground

2.3 Pin Function Descriptions

This section provides a brief description of the various pin functions available on the MMA9555L pedometer sensor. Ten of the device pins are multiplexed with Rapid GPIO (RGPIO) functions.

V_{DD} and V_{SS}: Digital power and ground. V_{DD} is nominally 1.8 V.

V_{DDA} and V_{SSA}: Analog power and ground. V_{DDA} is nominally 1.8 V. To optimize performance, the V_{DDA} line can be filtered to remove any digital noise that might be present on the 1.8 V supply. (See Figure 3 and Figure 4.)

RESETB: The RESETB pin is an open-drain, bidirectional pin with an internal, weak, pullup resistor. At start-up, it is configured as an input pin, but also can be programmed to become bidirectional. By default, the output function is not on. Using this feature, the MMA9555L device can reset external devices for any purpose other than power-on reset. Reset must be pulled high at power up to boot to Application code space. If low, it will boot to ROM code. After startup, Reset may be asserted to reset the device. The total external capacitance to ground has to be limited when using RESETB-pin, output-drive capability. For more details, see the “System Integration Module” chapter of the MMA955xL *Intelligent, Motion-Sensing Platform Hardware Reference Manual* (MMA955xLHWRM), listed in “Related Documentation” on page 2.

Slave I^2C port: SDA0 and SCL0: These are the slave-I^2C data and clock signals, respectively. The MMA9555L device can be controlled via the serial port or via the slave SPI interface.

Analog-to-Digital Conversion: AN0, AN1: The on-chip ADC can be used to perform a differential, analog-to-digital conversion based on the voltage present across pins AN0(–) and AN1(+). Conversions for these pins are at the same Output Data Rate (ODR) as the MEMS transducer signals. Input levels are limited to 1.8 V differential.

Rapid General Purpose I/O: RGPIO[9:0]: The Intelligent Pedometer has a feature called Rapid GPIO (RGPIO). This is a 16-bit, input/output port with single-cycle write, set, clear, and toggle functions available to the CPU. The MMA9555L device brings out the lower 10 bits of that port as pins of the device. At reset, all of the RGPIO pins are configured as input pins, although pin muxing does reassign some pins to non-RGPIO function blocks. Pullups are disabled.

RGPIO[9:6] can be set as interrupt pins for most interrupt sources. INT_O can only output interrupts from the COCO bit. For setting sensor data output interrupts, use RGPIO6–RGPIO9.

RGPIO3 / SBB = Low at startup selects SPI. High at startup selects I^2C.

RGPIO[5] or INT_O can only output interrupts from the COCO bit. For setting sensor data output interrupts, use RGPIO6–RGPIO9.

RGPIO[9] is connected to BKGD/MS.

RGPIO[1:0] SDA0 and SCL0 are connected at reset.

Interrupts: INT: This input pin can be used to wake the CPU from a deep-sleep mode. It can be programmed to trigger on either rising or falling edge, or high or low level. This pin operates as a Level-7 (high-priority) interrupt.

Debug/Mode Control: BKGD/MS: At start-up, this pin operates as mode select. If this pin is pulled high during start up, the CPU will boot normally and run code. If this pin is pulled low during start-up, the CPU will boot into active Background-Debug Mode (BDM). In BDM, this pin operates as a bidirectional, single-wire, background-debug port. It can be used by development tools for downloading code into on-chip RAM and flash and to debug that code. There is an internal pullup resistor on this pin, therefore, It may be left floating.

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Slave SPI Interface: SCLK, SDI, SDO and SBB: These pins control the slave SPI clock, data in, data out, and slave-select signals, respectively. The MMA9555L platform can be controlled via this serial port or via the slave-I^2C interface. SBB has a special function at startup that selects the Slave interface mode. Low at startup selects SPI and high selects I^2C.

INT_O: The slave-port output interrupt pin can be used to flag the host when a response to a command is available to read on the slave port. INT_O can only output interrupts from the COCO bit. For sensor data output interrupts, use RGPI06–RGPIO9.

2.4 System Connections

2.4.1 Power Sequencing

An internal circuit powered by V_{DDA} provides the device with a power-on-reset signal. In order for this signal to be properly recognized, it is important that V_{DD} is powered up before or simultaneously with V_{DDA}. The voltage potential between V_{DD} and V_{DDA} must not be allowed to exceed the value specified in Table 6 on page 14.

2.4.2 Layout Recommendations

- Provide a low-impedance path from the board power supply to each power pin (V_{DD} and V_{DDA}) on the device and from the board ground to each ground pin (V_{SS} and V_{SSA}).
- Place 0.01 to 0.1 µF capacitors as close as possible to the package supply pins to meet the minimum bypass requirement. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs. V_{DDA}/V_{SSA} ceramic and tantalum capacitors tend to provide better tolerances.
- Capacitor leads and associated printed-circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins must be as short as possible.
- Bypass the power and ground with a capacitor of approximately 1 µF and a number of 0.1-µF ceramic capacitors.
- Minimize PCB trace lengths for high-frequency signals. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{DDA} and V_{SSA} pins.
- Use separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA}. Connect the separate analog and digital power and ground planes as close as possible to power supply outputs. If both analog circuit and digital circuits are powered by the same power supply, it is advisable to connect a small inductor or ferrite bead in series with both the V_{DDA} and V_{SSA} traces.
- Physically separate the analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. It is also desirable to place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Provide an interface to the BKGD/MS pin if in-circuit debug capability is desired.
- Ensure that resistors R_{P1} and R_{P2}, in the following figure, match the requirements stated in the I^2C standard. For the shown configuration, the value of 4.7 kΩ would be appropriate.

2.4.3 MMA9555L Pedometer Sensor as an Intelligent Slave

I^2C pullup resistors, and a few bypass capacitors are all that are required to attach this device to a host platform. The basic configurations are shown in the following two figures. In addition, the RGPIO pins can be programmed to generate interrupts to a host platform in response to the occurrence of real-time application events. In this case, the pins should be routed to the external interrupt pins of the CPU.

NOTE

Immediately after a device reset, the state of pin number 8 (RGPIO3 / SDA1 / SSB functions) is used to select the slave port interface mode. This implies important rules in the way the host controller or, more generally, the complete system should be handling this pin.

First of all, whenever a reset occurs on the MMA9555L, the RGPIO3 pin level shall be consistent with the interface mode of operation. This is particularly important if this pin is driven from external devices. If the RGPIO3 level does not match the current mode of operation, an alternate mode is selected and communication with the host is lost.

If I^2C mode is used, a good practice is to tie RGPIO3 to a pull-up resistor so that it defaults to high level. When using I^2C mode for the slave interface, the RGPIO3 pin plays two roles: RGPIO3 and mode selection. When the MMA9555L is powered on and the mode selection is I^2C, the RGPIO3 pin is released as a GPIO pin. The default setting of RGPIO3 is as an output pin and

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output low. In order to reduce the leakage current on the pull-up resistor, a large resistor value can be used or RGPIO3 can be set as an input pin.

When using SPI mode for the slave interface, the situation is more complex as the same pin plays two roles: SSB and mode selection. Moreover, after a SPI read or write operation, the SSB line returns to high level. Consequently, if the host is sending a command to the MMA9555L that induces a subsequent reset, immediately after the write transaction, the host shall force the SSB line to low level so that SPI mode is still selected after reset. The duration for the SSB line to be kept low typically depends on the latency between the write transaction and the execution of the reset command. Such latency can be significant for the MMA9555L pedometer firmware as the Command Interpreter and Scheduler Application are running at 30 Hz which gives a 33 ms typical latency.

The rule obviously applies also when a hardware reset is issued by the host through MMA9555L pin number 3 (RESETB active low). Again the host has to drive the SSB line low prior to release of the hardware reset line to high level, which triggers immediate MMA9555L reset and boot sequence. Keeping the SSB line low for a 1 ms duration (after RESETB is released) is enough for the MMA9555L slave device to re-boot into SPI mode.

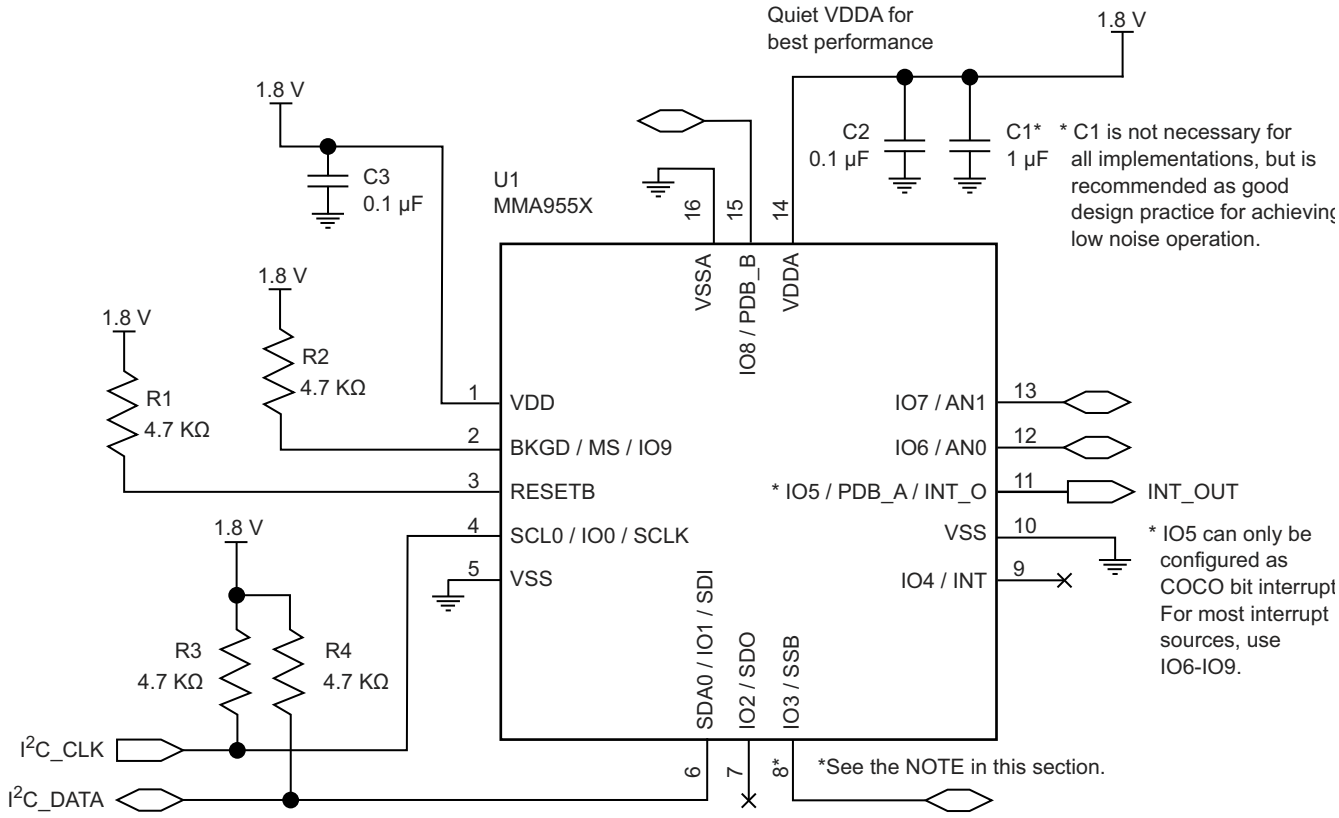

Figure 3. MMA9555L Pedometer Sensor as an I^2C slave

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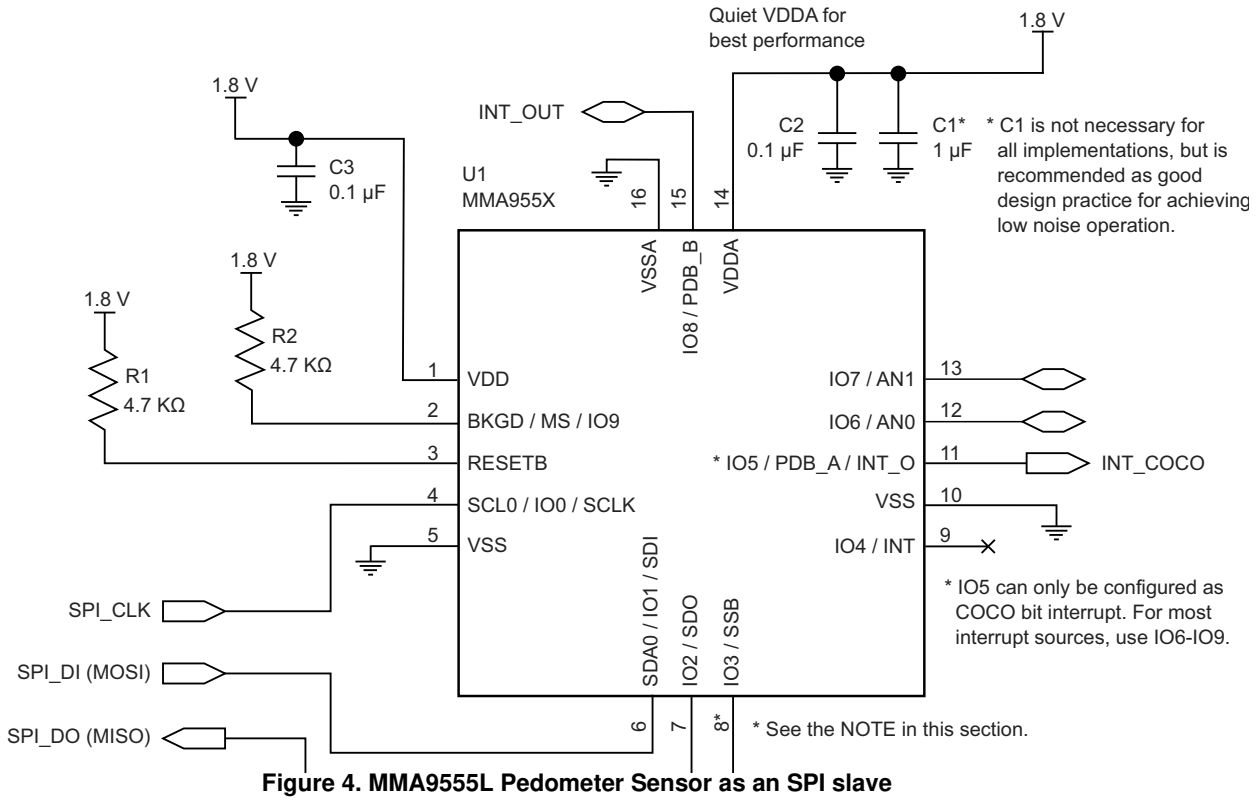

Figure 4. MMA9555L Pedometer Sensor as an SPI slave

2.4.4 Sensing Direction and Output Response

Figure 5 shows the device's default sensing direction when measuring gravity in a static manner from the six standard orientation modes: portrait up/down, landscape left/right and back/front.

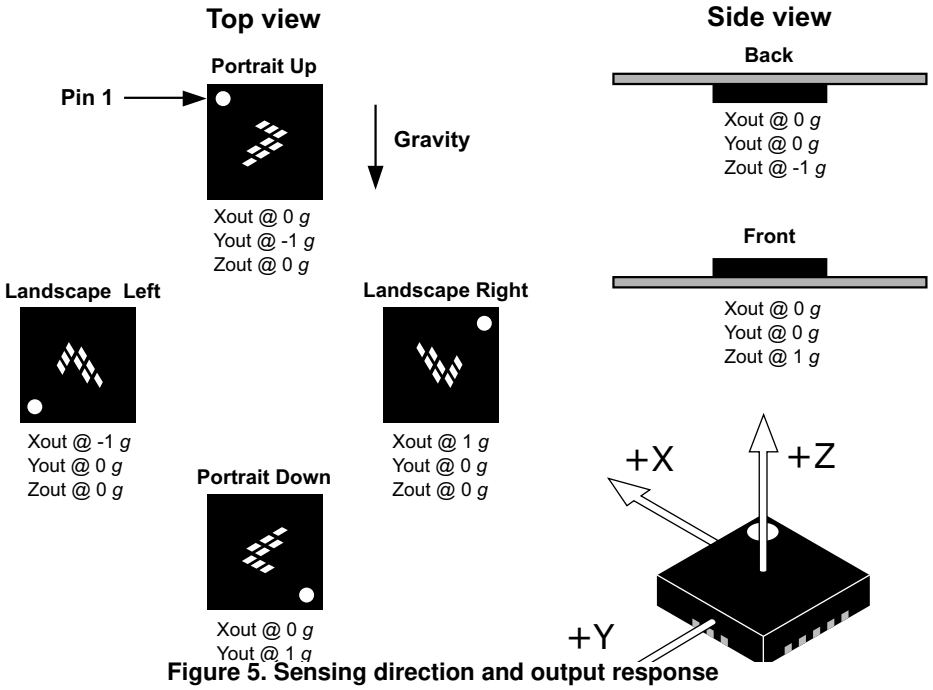

Figure 5. Sensing direction and output response

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3 Mechanical and Electrical Specifications

This section contains electrical specification tables and reference timing diagrams for the MMA9555L device, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

3.1 Definitions

Cross-axis sensitivity	The proportionality constant that relates a variation of accelerometer output to cross acceleration. This sensitivity varies with the direction of cross acceleration and is primarily due to misalignment.
Full range	The algebraic difference between the upper and lower values of the input range. Refer to the input/output characteristics.
Hardware compensated	Sensor modules on this device include hardware-correction factors for gain and offset errors that are calibrated during factory test using a least-squares fit of the raw sensor data.
Linearity error	The deviation of the sensor output from a least-squares linear fit of the input/output data.
Nonlinearity	The systematic deviation from the straight line that defines the nominal input/output relationship.
Pin group	The clustering of device pins into a number of logical pin groupings to simplify and standardize electrical data sheet parameters. Pin groups are defined in Section 3.2, “Pin Groups”.
Software compensated	NXP’s advanced nonlinear calibration functions that—with the first-order hardware gain and offset calibration features—improve sensor performance.
Warm-up time	The time from the initial application of power for a sensor to reach its specified performance under the documented operating conditions.

3.2 Pin Groups

The following pin groups are used throughout the remainder of this section.

Group 1 RESETB

Group 2 RESERVED

Group 3 RGPIO[9:0]

3.3 Absolute Maximum Ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 3. Absolute maximum ratings

Rating	Symbol	Minimum	Maximum	Unit
Digital supply voltage	V_{DD}	–0.3	2.0	V
Analog supply voltage	V_{DDA}	–0.3	2.0	V
Voltage difference, V_{DD} to V_{DDA}	$V_{DD} – V_{DDA}$	–0.1	0.1	V
Voltage difference, V_{SS} to V_{SSA}	$V_{SS} – V_{SSA}$	–0.1	0.1	V
Input voltage	V_{In}	–0.3	V_{DD} + 0.3	V
Input/Output pin-clamp current	I_C	–20	20	mA
Output voltage range (Open-Drain Mode)	V_{OUTOD}	–0.3	V_{DD} + 0.3	V
Storage temperature	T_{stg}	–40	125	°C
Mechanical shock	SH	—	5k	g

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3.4 Operating Conditions

Table 4. Nominal operating conditions

Rating	Symbol	Min	Typ	Max	Unit
Digital supply voltage	V_{DD}	1.71	1.8	1.89	V
Analog supply voltage	V_{DDA}	1.71	1.8	1.89	V
Voltage difference, V_{DD} to V_{DDA}	$V_{DD} – V_{DDA}$	–0.1	—	0.1	V
Voltage difference, V_{SS} to V_{SSA}	$V_{SS} – V_{SSA}$	–0.1	—	0.1	V
Input voltage high	V_{IH}	0.7 * V_{DD}	—	V_{DD}+0.1	V
Input voltage low	V_{IL}	V_{SS} – 0.3	—	0.3*V_{DD}	V
Operating temperature	T_A	–40	25	85	°C

3.5 Electrostatic Discharge (ESD) and Latch-up Protection Characteristics

Table 5. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human Body Model (HBM)	V_{HBM}	±2000	V
Machine Model (MM)	V_{MM}	±200	V
Charge Device Model (CDM)	V_{CDM}	±500	V
Latch-up current at 85 °C	I_{LAT}	±100	mA

3.6 General DC Characteristics

Table 6. DC characteristics[1]

Characteristic	Symbol	Condition(s)[2]	Min	Typ	Max	Unit
Output voltage high • Low-drive strength • High-drive strength	V_{OH}	Pin Groups 1 and 3 I_{LOAD} = –2 mA I_{LOAD} = –3 mA	V_{DD} – 0.5	—	—	V
Output voltage low • Low-drive strength • High-drive strength	V_{OL}	Pin Groups 1 and 3 I_{LOAD} = 2 mA I_{LOAD} = 3 mA	—	—	0.5	V
Output-low current Max total I_{OL} for all ports	I_{OLT}	—	—	—	24	mA
Output-high current Max total I_{OH} for all ports	I_{OHT}	—	—	—	24	mA
Input-leakage current	$\|I_{IN}\|$	Pin Group 2 V_{in} = V_{DD} or V_{SS}	—	0.1	1	µA
Hi-Z (off-state) leakage current	$\|I_{OZ}\|$	Pin Group 3 input resistors disabled V_{in} = V_{DD} or V_{SS}	—	0.1	1	µA
Pullup resistor	R_{PU}	when enabled	17.5	—	52.5	kΩ
Power-on-reset voltage	V_{POR}	—	—	1.50	—	V
Power-on-reset hysteresis	$V_{POR–hys}$	—	—	100	—	mV
Input-pin capacitance	C_{IN}	—	—	7	—	pF
Output-pin capacitance	C_{OUT}	—	—	7	—	pF

1. All conditions at nominal supply: V_{DD} = V_{DDA} = 1.8 V.
2. Pin groups are defined in "Pin Groups" on page 13.

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3.7 Supply Current Characteristics

Table 7. Supply current characteristics[1]

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Supply current in $STOP_{NC}$ mode	$I_{DD–SNC}$	Internal clocks disabled	—	2	—	µA
Supply current in $STOP_{SC}$ mode	$I_{DD–SSC}$	Internal clock in slow-speed mode	—	15	—	µA
Supply current in RUN mode[2]	$I_{DD–R}$	Internal clock in fast mode	—	3.1	—	mA

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8$ V.
2. Total current with the analog section active, 16 bits ADC resolution selected, MAC unit used and all peripheral clocks enabled.

3.8 Accelerometer Transducer Mechanical Characteristics

Table 8. Accelerometer characteristics

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Full range	A_{FR}	2 *g*	±1.8	±2	±2.2	g
		4 *g*	±3.6	±4	±4.4	
		8 *g*	±7.2	±8	±8.8	
Sensitivity/resolution	A_{SENS}	2 *g*	—	0.061	—	m*g*/LSB
		4 *g*	—	0.122	—	
		8 *g*	—	0.244	—	
Zero-*g* level offset accuracy (Pre-board mount)	OFF_{PBM}	2 *g*	–100	—	+100	m*g*
		4 *g*				
		8 *g*				
Nonlinearity Best fit straight line	A_{NL}	2 *g*	—	±0.25	—	% A_{FR}
		4 *g*	—	±0.5	—	
		8 *g*	—	±1	—	
Sensitivity change vs.temperature	TC_{SA}	2 *g*	—	±0.17	—	%/°C
Zero-*g* level change vs. temperature[1]	TC_{Off}	—	—	±1.9	—	m*g*/°C
Zero-*g* Level offset accuracy (Post-board mount)	OFF_{BM}	2 *g*	–100	—	+100	m*g*
		4 *g*				
		8 *g*				
Output data bandwidth	BW	—	—	ODR/2	—	Hz
Output noise	Noise	2 *g*, ODR = 488 Hz	—	100	—	µ*g*/sqrt(Hz)
		8 *g*, ODR = 488 Hz	—	120	—	µ*g*/sqrt(Hz)
Cross-axis sensitivity	—	—	–5	—	5	%

1. Relative to 25 °C.

3.9 ADC Characteristics

Table 9. ADC characteristics[1]

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Input voltage	V_{AI}	Voltage at AN0 or AN1	0.2	—	1.1	V
Differential input voltage	V_{ADI}	AN1 – AN0	–0.9	—	0.9	V
Full-scale range	V_{FS}	—	—	1.8	—	V
Programmable resolution	R_{ES}	—	10	14	16	Bits

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Table 9. ADC characteristics[1] (Continued)

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Conversion time @ 14-bits resolution (Three-sample frame)	t_c	—	—	207	—	µs
Integral nonlinearity	INL	Full scale	—	±15	—	LSB
Differential nonlinearity	DNL	—	—	±2	—	LSB
Input leakage	I_{IA}	—	—	—	±2	µA

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8$ V and $R_{ES} = 14$, unless otherwise noted.

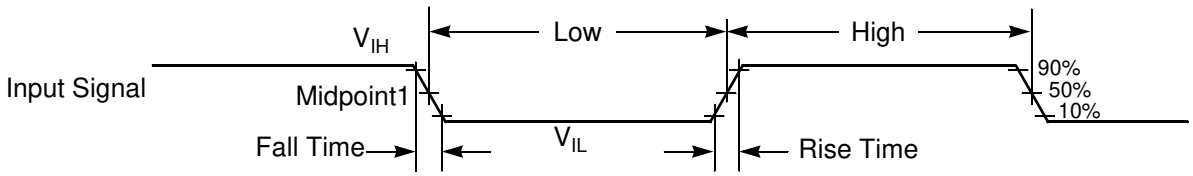
3.10 ADC Sample Rates

The MMA9555L internal ADC supports the following sample output rates, while the pedometer application uses 30.52 fps as default:

- 488.28 frames per second (fps)
- 244.14 fps
- 122.07 fps
- 61.04 fps
- 30.52 fps
- 15.26 fps
- 7.63 fps
- 3.81 fps

3.11 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 4 on page 14. Unless otherwise specified, propagation delays are measured from the 50-percent to 50-percent point. Rise and fall times are measured between the 10-percent and 90-percent points, as shown in the following figure.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 6. Input signal measurement references

The subsequent figure shows the definitions of the following signal states:

- Active state, when a bus or signal is driven and enters a low-impedance state
- Three-stated, when a bus or signal is placed in a high-impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

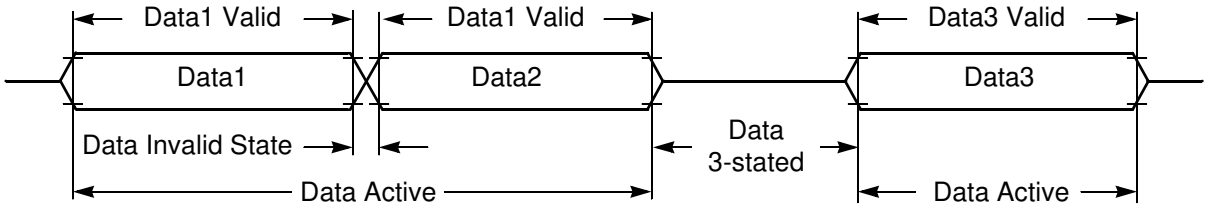


Figure 7. Signal states

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3.12 General Timing Control

Table 10. General timing characteristics[1]

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
V_{DD} rise time	T_{rvdd}	10% to 90%	—	—	1	ms
POR release delay[2]	T_{POR}	Power-up	0.35		1.5	ms
Warm-up time	T_{WU}	From $STOP_{NC}$	—	7	—	sample periods
Frequency of operation	F_{OPH}	Full Speed Clock	—	8	—	MHz
	F_{OPL}	Slow Clock	—	62.5	—	KHz
System clock period	t_{CYCH}	Full Speed Clock	—	125	—	ns
	t_{CYCL}	Slow Clock	—	16	—	µs
Full/Slow clock ratio	—	—	—	128	—	
Oscillator frequency absolute accuracy @ 25 °C	—	Full Speed Clock	–5	—	+5	%
Oscillator frequency variation over temperature (–40 °C to 85 °C vs. ambient)	—	Slow Clock	–6	—	+6	%
Minimum RESET assertion duration	t_{RA}	—	4T[3]	—	—	—

1. All conditions at nominal supply: $V_{DD} = V_{DDA} = 1.8$ V
2. This is the time measured from $V_{DD} = V_{POR}$ until the internal reset signal is released.
3. In the formulas, T = 1 system clock cycle. In full speed mode, T is nominally 125 ns. In slow speed mode, T is nominally 16 µs.

3.13 I2C Timing

This device includes a slave I^2C module that can be used to control the sensor and can be active 100 percent of the time.

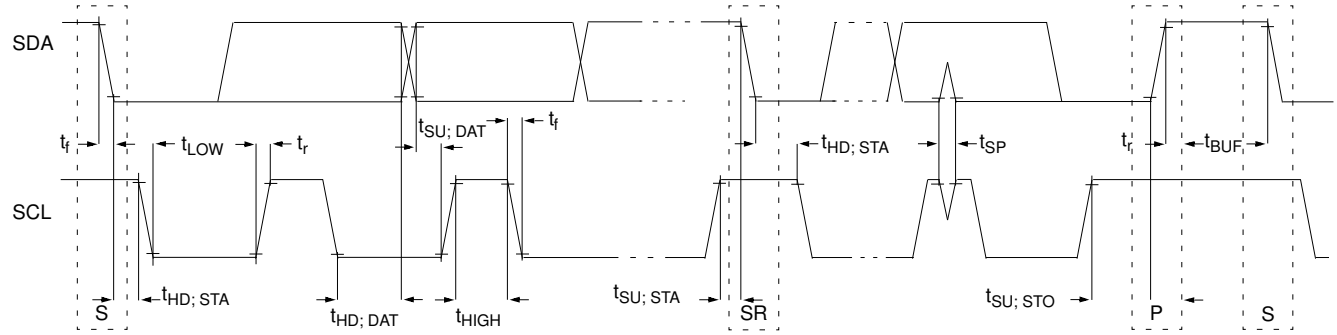

Figure 8. I^2C standard and fast-mode timing

3.13.1 Slave I2C

Table 11. I^2C Speed Ranges

Mode	Max Baud Rate (f_{SCL})	Min Bit Time	Min SCL Low (t_{LOW})	Min SCL High (t_{HIGH})	Min Data setup Time ($t_{SU;\,DAT}$)	Min/Max Data Hold Time ($t_{HD;\,DAT}$)
Standard	100 kHz	10 µs	4.7 µs	4 µs	250 ns	0 µs/3.45 µs[1]
Fast	400 kHz	2.5 µs	1.3 µs	0.6 µs	100 ns	0 µs/0.9 µs[1]
Fast +	1 MHz	1 µs	500 ns	260 ns	50 ns	0 µs/0.45 µs[1]
High-speed supported	2.0 MHz	0.5 µs	200 ns	200 ns	10 ns[2]	0 ns/70 ns (100 pf)[1]

1. The maximum $t_{HD;\,DAT}$ must be at least a transmission time less than $t_{VD;DAT}$ or $t_{VD;ACK}$. For details, see the I2C standard.
2. Timing met with IFE = 0, DS = 1, and SE = 1. Refer to the chapter titled *Port Controls* in the *MMA955xL Intelligent, Motion-Sensing Platform Hardware Reference Manual* (MMA955xLHWRM), listed in "Related Documentation" on page 2.

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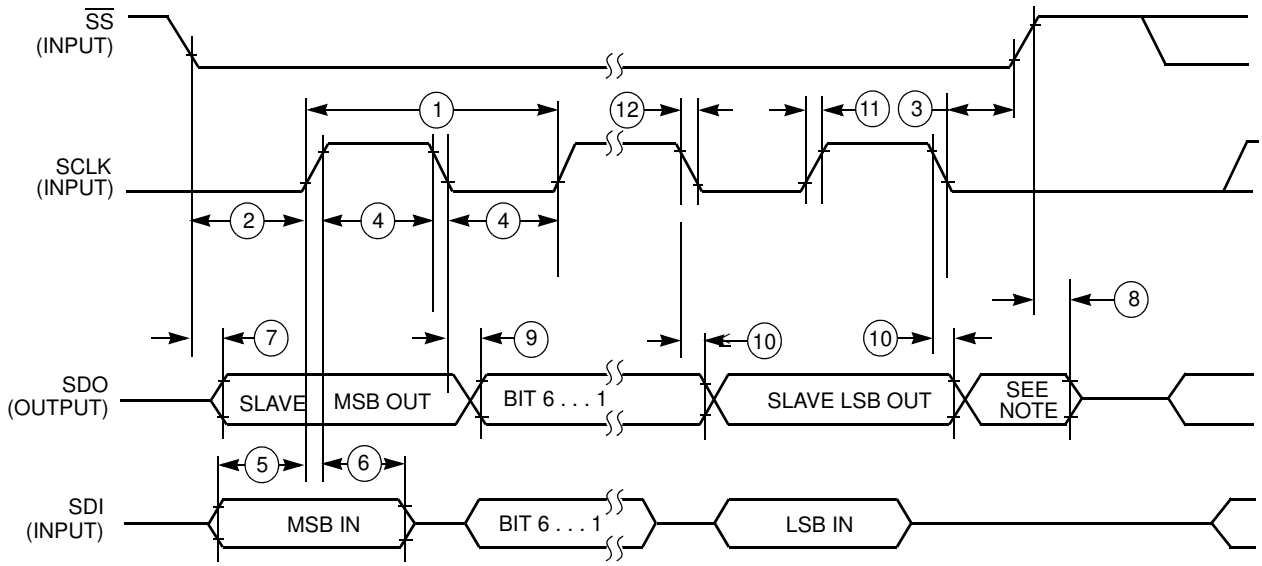
3.14 Slave SPI Timing

Table 12. Slave SPI timing

Time Period (1)	Function	Symbol	Min	Max	Unit
—	Operating frequency	f_{op}	0	$F_{OPH}/4$	Hz
1	SCLK period	t_{SCLK}	4	—	t_{CYCH}
2	Enable lead time	t_{Lead}	0.5	—	t_{CYCH}
3	Enable lag time	t_{Lag}	0.5	—	t_{CYCH}
4	Clock (SCLK) high or low time	t_{WSCLK}	200	—	ns
5	Data-setup time (inputs)	t_{SU}	15	—	ns
6	Data-hold time (inputs)	t_{HI}	25	—	ns
7	Access time	t_a	—	25	ns
8	SDO-disable time	t_{dis}	—	25	ns
9	Data valid (after SCLK edge)	t_v	—	25	ns
10	Data-hold time (outputs)	t_{HO}	0	—	ns
11	Rise time Input Output	 t_{RI} t_{RO}	 — —	 25 25	 ns ns
12	Fall time Input Output	 t_{FI} t_{FO}	 — —	 25 25	 ns ns

1. Time period from Figure 9.



NOTE:
1. Not defined but normally MSB of character just received.

Figure 9. SPI slave timing

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4 Communication Interface

4.1 Overview of Communication Interface

All access to the MMA9555L is made via the slave, serial Communication Interface that is part of the hardware and firmware infrastructure of the platform. The communication occurs in Command/Response (Normal) or Quick Read (Legacy) mode.

Commands are sent from the host and through the slave communications port (either SPI or I^2C). The Communication Interface interprets the command and sends the data to the correct application. The application executes the command and returns with data, if requested with the command response. It also responds with error codes when appropriate.

The Communications Interface works with the Mailbox application to implement the command and response. The mailboxes' functionality is configured with two applications: the MBOX Configuration application (APP_ID = 0x18) and the MBOX application (APP_ID = 0x04).

4.2 Mailbox Interface

Commands are received through a set of 32 mailboxes that are 32 registers arranged consecutively to provide addressable memory regions. Each mailbox can hold one byte of data.

After a command has completed, the Communication Interface writes the results to the mailboxes and the results (response out) are retrieved by the host via the SPI or the I^2C slave interface.

The following figure shows the structure of the data packet when writing one byte into a specific mailbox.

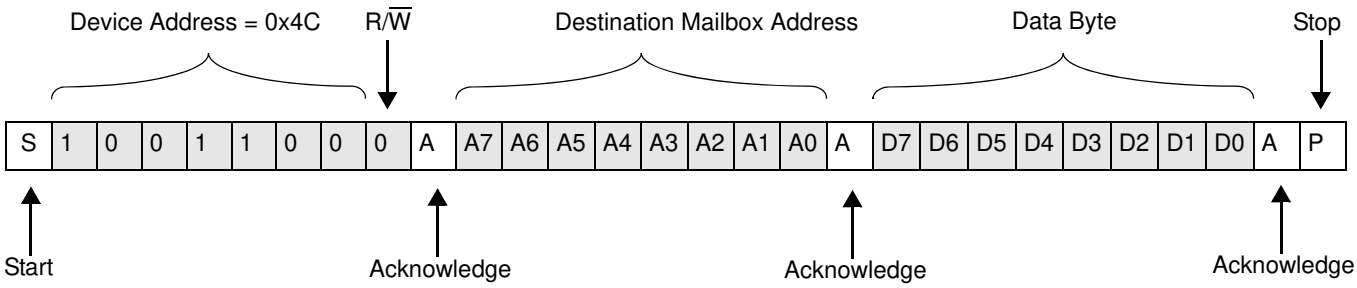

Figure 10. I^2C interface writing one byte of information to a mailbox

If the transaction contains more than one data byte, the internal-destination mailbox address is automatically incremented so that the incoming byte is placed in the next mailbox. For mailbox addresses greater than 31 bytes or for transactions where the mailbox address auto-increments past mailbox 31, the destination address wraps back to the start of the mailbox addresses.

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4.2.1 Mailbox Timing

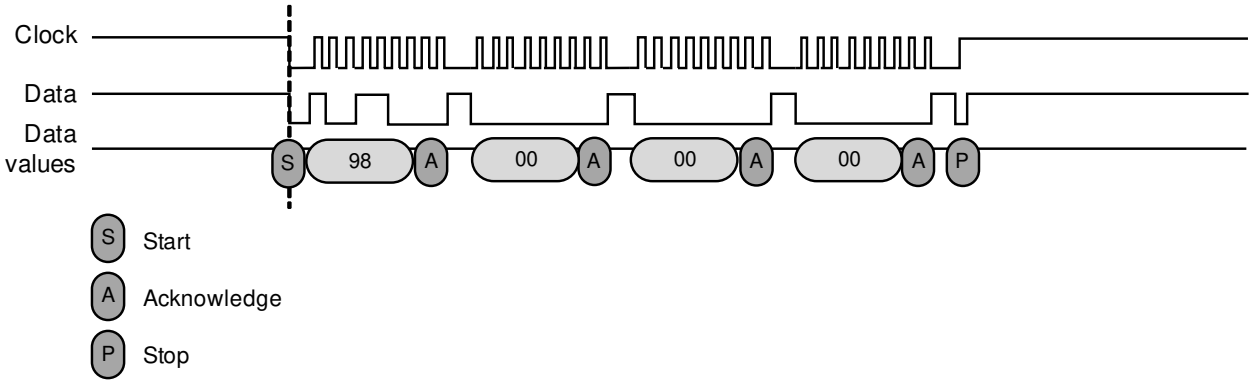
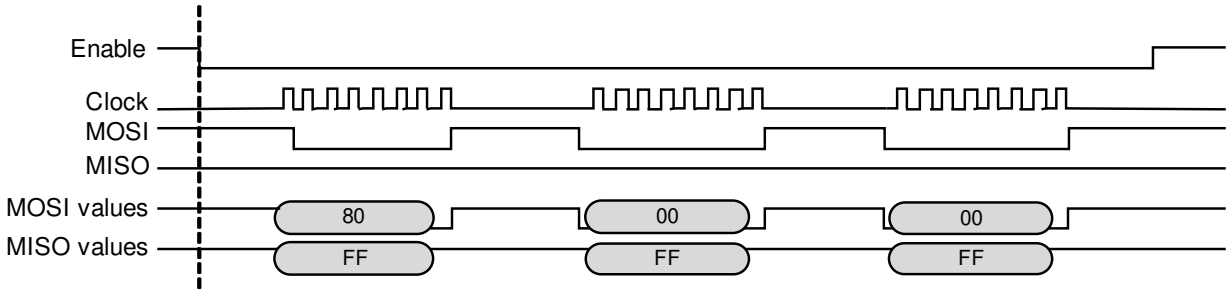


Figure 11. I²C timing diagram



MISO: SPI Master In, Slave Out
MOSI: SPI Master Out, Slave In
SPI: Serial, Peripheral Interface

Figure 12. SPI timing diagram

4.3 Mailbox Usage

Commands to the MMA9555L consist of a write followed by one or more reads. It may take some time to complete the command and a flag can be checked to determine if the command has completed. That flag is the Command Complete (COCO) bit, the seventh bit of the read data in the second mailbox. (See Table 16 on page 23.)

On a read operation, the COCO bit indicates if the command has been processed. The host processor can determine the status of the command's processing by repeatedly reading or polling the second mailbox until the COCO bit is set. Alternatively, the

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MMA9555L can be configured to assert an interrupt signal at the completion of a command. If configured, the INT_O interrupt will be set immediately after the COCO bit has been set.

For more information, see “Configuring mailbox operational mode” on page 96.

4.3.1 Mailbox Command Format for a Write

Commands written to the MMA9555L are sent in the format shown in the following table. Mailboxes are filled with data, depending on the target application. All commands start with the APP_ID, the command, the destination offset, and the number of data bytes to write.

All commands must be written in a single, I^2C/SPI transaction starting at Mailbox 0, but the response can be read from any subset of the mailbox registers.

For a write-request command, the first four mailboxes must be written with enough bytes to hold the requested number of bytes. The format of the data bytes is specific to the targeted application. (Applications are described in Table 15.)

Table 13. Mailbox commands formats

Offset	7	6	5	4	3	2	1	0
0x00	Application ID (APP_ID)							
0x01	0	Command			Byte offset (upper 4 bits)			
0x02	Byte offset (lower 8 bits)							
0x03	Requested number of bytes to read/write							
0x04	Write data 0							
0x05	Write data 1							
0x06	Write data 2							
….	Write data n							

The following table gives the details of the different parts of the data packet for a Write command.

Table 14. Mailbox command format details

Block	Description
Application ID	Application targeted for the issued command, see Table 15.
Command	Command to be performed: • 0: Read application fixed bytes (version information) • 1: Read application configuration bytes • 2: Write application configuration bytes • 3: Read application status or output
Byte offset	Sets the offset of the first byte to be accessed, counting from the start of the register space. This enables a subset of the registers to be accessed by setting the start location to something other than zero.
Requested number of bytes	Number of bytes requested to be read or written.
Write data	The data being written.

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4.3.2 Application IDs, names, and descriptions

The following table gives the names and IDs of the NXP applications associated with MMA9555L.

Table 15. Application descriptions

Application ID	Application Name	Description
0x00	Version	Returns a 12-byte pack with the device identifier number and the version numbers of the ROM, firmware, and hardware. (For more details, see Chapter 5, “Version Application”.)
0x01	Scheduler	Configures the system, applications, and the MMA9555L infrastructure to run at specific sample rates. Additionally, the identifier reads the number of times each task has been executed.
0x02	Reserved	
0x03	GPIO-AppMap	Configures the GPIO application to map a specific application output bit to specific GPIO pins. (For more details, see Chapter 7, “GPIO-AppMap Application”) The GPIO pins are limited to GPIO6 through 9.
0x04	Mailbox	Configures an internal mailbox table to map which output bytes from specific application identifiers will be accessible in the Normal mode and the Legacy mode’s Quick-Read registers mailboxes. The application identifier can perform a table reset to reinstall the default values when the MMA9555L resets.
0x05	Reserved	
0x06	Analog Front End	Configures different parameters of the AFE and reads XYZ data from the accelerometer. For further details, see Chapter 9, “Analog Front End Application”.
0x0C–0x0D	Reserved	
0x0F	Data FIFO	Configures parameters of the Data-FIFO application and reads the output bytes from its output structure and the contents of the FIFO buffer.
0x10	Event queue	Configures parameters of the Event-queue application and reads the output bytes from its output structure and the contents of the Event-queue buffer.
0x11	Status register	Provides access to the MMA9555L system-status information.
0x12	Wake/Sleep	Configures the power-control modes of the accelerometer. The application has three modes of operation: Run, Doze, and Sleep.
0x13–0x14	Reserved	
0x15	Pedometer	Application that can detect the step count.
0x16	Reserved	
0x17	Reset/suspend/clear	Controls the Reset/Suspend/Clear functions of the MMA9555L.
0x18	Mailbox mode config	Configures different operation modes of the mailbox and provides the status value of the mailbox when Stream mode is running.
0x19	GPIO Input/Output	Controls GPIO2–GPIO8 as input or output pins.
0x1B–0x1F	Reserved	
0x20–0xFF	Reserved	Indicates an invalid application index.

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4.3.3 Mailbox command format for a read

Though all commands must be written in a single I^2C/SPI transaction starting at Mailbox 0, the response can be read from any subset of the mailbox registers. When the MMA9555L is configured to stream data (as in FIFO mode), the read commands must be constructed as multiples of 32 bytes in order to trigger the internal transfer of the next set of data to the mailboxes.

A read-request command requires a write to the first four mailboxes.

The format of the information returned from the MMA9555L is shown in Table 16. Similar to the command format, the response format follows the specific application's format.

Mailboxes are filled with data depending on the target application.

All responses start with the responding APP_ID, the COCO the ERROR STATUS, the actual data count, and the requested data count.

The format of the remaining data bytes is specific to the responding application.

Table 16. Mailbox response formats

Mailbox	7	6	5	4	3	2	1	0
0x00	Application ID (APP_ID)							
0x01	COCO	Error code						
0x02	Actual number of bytes read/written							
0x03	Requested number of bytes to read/write							
0x04	Read data 0							
0x05	Read data 1							
0x06	Read data 2							
….	Read data n							

Table 17 describes the details of the different parts and fields of a response message.

Table 17. Mailbox response format details

Block	Description
Application ID (APP_ID)	The ID of the application that is responding. (See Table 16 on page 23.)
COCO	Command complete. This bit must be set to 0b when a command is written and is set to 1b by the MMA9555L platform, when the command has been processed. The other registers do not contain valid results until this bit is set.
Error code	The seven bytes that store the error code of the command. A zero indicates there was no error. (For more information, see Table 18.)
Actual number of bytes	Actual number of bytes read or written. This block reports back the actual number of bytes that were read or written. It is normally the same as the requested number of bytes, but it will be reduced if the requested number of bytes plus the Byte Offset exceeds the number of bytes in the requested block's data structure.
Requested number of bytes	Number of bytes requested to be read or written.
Read data	The data that was read.

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Table 18 describes the status or error-code results returned in Mailbox 0x01.

Table 18. Error-Status codes returned in Mailbox 0x01

Error Code	Name	Description
0x00	MCI _ERROR_NONE	Command completed with no errors.
0x04	MCI _ERROR_PARAM	Incorrect input parameter. Error may be due to an incorrect application ID, an incomplete command, or an incorrect offset.
0x19	MCI _INVALID_COUNT	Returned when the command COUNT is greater than the output structure size.
0x1C	MCI_ERROR_COMMAND	Returned any time that the command interpreter does not recognize a command code.
0x21	MCI_ERROR_INVALID_LENGTH	Returned when the host sends a number of bytes with a wrong payload. MMA9555L checks any mismatches between the amount of bytes received and the actual payload sent by the host.
0x22	MCI_ERROR_FIFO_BUSY	FIFO is busy performing a push operation and it is not possible to execute any other function.
0x23	MCI_ERROR_FIFO_ALLOCATED	Returned when the host tries to reconfigure the FIFO module. The FIFO application configuration can only be written once. In order to reconfigure the FIFO, the whole device must be reset. This is because the FIFO application requests RAM and RAM can only be allocated once.
0x24	MCI_ERROR_FIFO_OVERSIZE	Returned when the host wants to set a FIFO buffer size out of the memory boundaries within the MMA9555L device.

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5 Version Application

The MMA9555L device's system-version information is stored in a 12-byte packet and contains system-identity information including device-hardware ID; the versions of the ROM bootloader, primary firmware, and hardware; and the system-build information.

Table 19 describes the system-version packet and its corresponding mailbox alignment.

Application ID	0x00
Default speed	Always available.
Configuration registers	None.
Status registers	None.

Table 19. Version command description bytes

Mailbox number	Description	Byte
4	Device identifier	31:24
5	Device identifier	24:16
6	Device identifier	15:8
7	Device identifier	7:0
8	ROM major version number	7:0
9	ROM minor version number	7:0
10	Firmware major version number	7:0
11	Firmware minor version number	7:0
12	Hardware major version number	7:0
13	Hardware minor version number	7:0
14	Build major version number	7:0
15	Build minor version number	7:0

Table 20 describes the Build Major and Build Minor version-number fields.

Table 20. Version application, Build major and minor bytes

Byte	Address	Description	Bit fields
3	0x1FD	Build major version number	• 7–3 Build's day of the month Range, 1 to 31 • 2–0 Year of build, from 2010 Range, 0 to 7.
4	0x1FC	Build minor version number	• 7 — Release – 1 Engineering version – 0 Production release • 6–4 Build number • 3–0 Month of build Range, 1 to 12

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