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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# 14 channel configurable power management integrated circuit

The SMARTMOS PF0100Z AEC Q100 grade 2 automotive power management integrated circuit (PMIC) provides a highly programmable/ configurable architecture, with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF0100Z can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications. With on-chip one time programmable (OTP) memory, the PF0100Z is available in pre-programmed standard versions, or non-programmed to support custom programming. The PF0100Z is especially suited to the i.MX 6 family of devices and is supported by full system level reference designs, and pre-programmed versions of the device.

## Features:

- Four to six buck converters, depending on configuration
  - Single/dual phase/ parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (one time programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- I<sup>2</sup>C control
- Individually programmable on, off, and standby modes

## PF0100Z Automotive

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### POWER MANAGEMENT

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**ES SUFFIX (WF-TYPE)**  
**98ASA00589D**  
**56 QFN 8X8**

## Applications:

- GPS
- Auto infotainment
- Heads up display (HUD)
- Rear displays
- Digital instrumentation cluster (DIC)

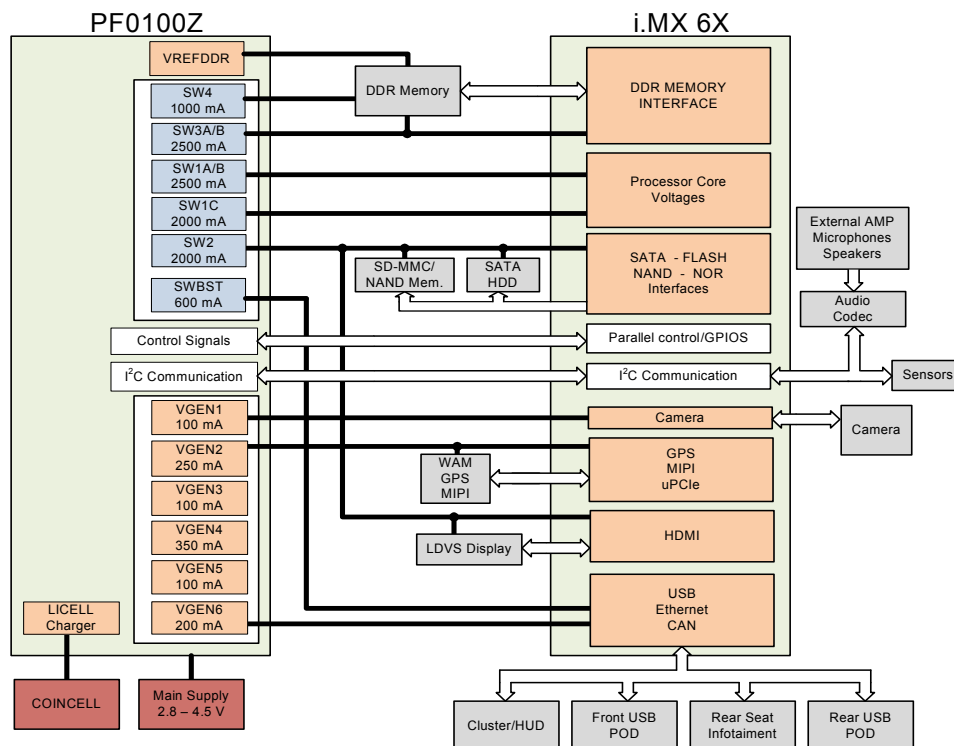


Figure 1. Simplified application diagram

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

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# 1 Orderable parts

The PF0100Z is available with both pre-programmed and non-programmed OTP memory configurations. The non-programmed device uses “NP” as the programming code. The pre-programmed devices are identified using the program codes from [Table 1](#), which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in [Table 9](#).

**Table 1. Orderable part variations**

Part Number	Temperature (T <sub>A</sub> )	Package	Programming	Reference designs	Notes
MMPF0100NPAZES	-40 °C to 105 °C	56 QFN ES, 8x8 mm 0.5 mm pitch WF-Type (wetable flank)	NP	MCIMX6QAICPU1 MCIMX6SAICPU1 MCIMX6DLAICPU1	(1), (2), (3)
MMPF0100F0AZES			F0	MCIMX6Q-SDP MCIMX6Q-SDB MCIMX6DL-SDP	(1), (2)
MMPF0100F6AZES			F6	-	
MMPF0100F8AZES			F8	-	
MMPF0100F9AZES			F9	MCIMX6QPlusAICPU3	(1), (2), (3)
MMPF0100FAAZES			FA	-	

**Notes**

1. For tape and reel add an R2 suffix to the part number.
2. These reference designs use the default startup configuration (VDDOTP = VCOREDIG), which is available on any OTP programmed part.
3. SW2 can support an output current rating of 2.5 A in NP, F9 and FA versions when SW2ILIM=0

## 1.1 PF0100Z version differences

PF0100AZ is an improved version of the PF0100Z power management IC. [Table 2](#) summarizes the difference between the two versions and should be referred to when migrating from the PF0100Z to the PF0100AZ.

**Table 2. Differences between PF0100Z and PF0100AZ**

Description	PF0100Z	PF0100AZ
Version identification	Reading SILICON REV register at address 0x03 will return 0x11. DEVICEID register at address 0x00 will read 0x10 in PF0100Z and PF0100AZ	Reading SILICON REV register at address 0x03 will return 0x21. DEVICEID register at address 0x00 will read 0x10 in PF0100Z and PF0100AZ
VSNVS current limit	VSNVS current limit increased in the PF0100AZ. see <a href="#">VSNVS LDO/switch</a>	
OTP_FUSE_PORx register setting during OTP programming	In the PF0100Z, FUSE_POR1, FUSE_POR2, and FUSE_POR3 bits are XOR'ed into the FUSE_POR_XOR bit. The FUSE_POR_XOR bit has to be 1 for fuses to be loaded during startup. This can be achieved by setting any one or all of the FUSE_PORx bits during OTP programming.	In the PF0100AZ, the XOR function is removed. It is required to set FUSE_POR1, FUSE_POR2, and FUSE_POR3 bits during OTP programming.
Erratum ER19	Erratum ER19 applicable to PF0100Z. Applications expecting to operate in the conditions mentioned in ER19 need to implement an external workaround to overcome the problem. Refer to the product errata for details	Errata ER19 fixed in PF0100AZ. External workaround not required
Erratum ER20	Erratum ER20 applicable to PF0100Z	Errata ER20 fixed in PF0100AZ
Erratum ER22	Erratum ER22 applicable to PF0100Z	Errata ER22 fixed in PF0100AZ. Workaround not required
Ambient operating temperature	-40 °C to 85 °C	-40 °C to 105 °C

## 2 Internal block diagram

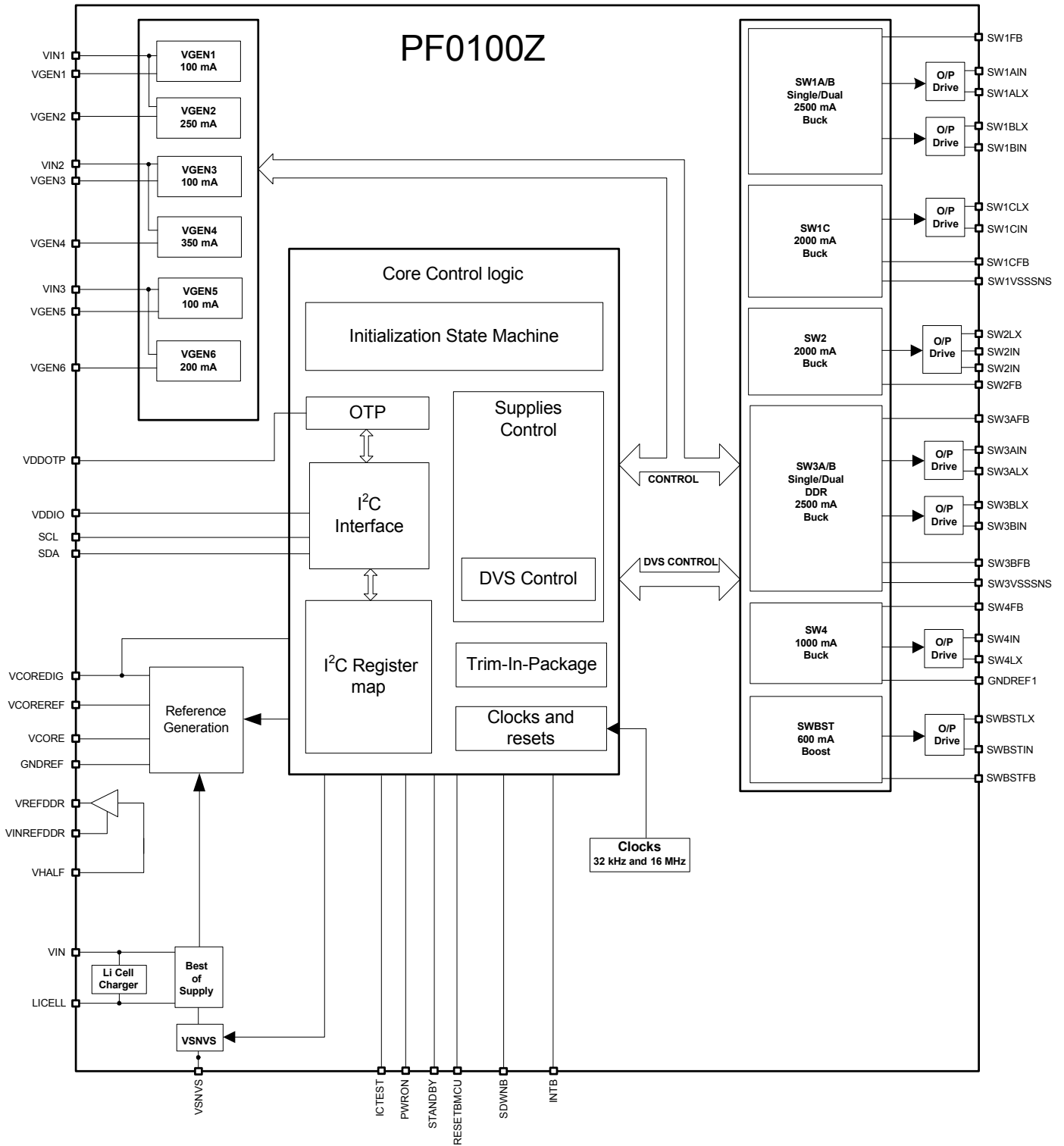


Figure 2. Simplified internal block diagram

### 3 Pin connections

#### 3.1 Pinout diagram

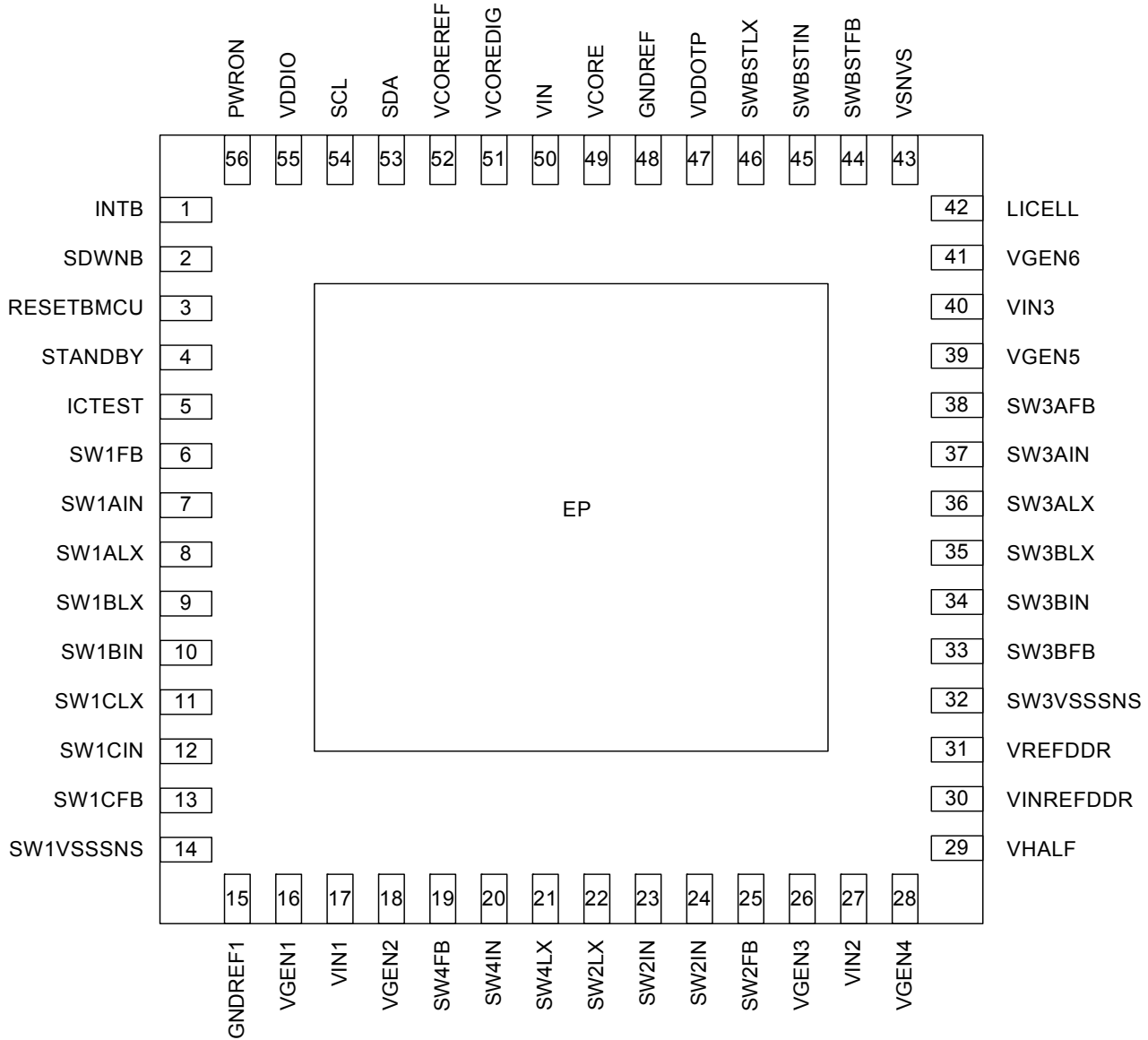


Figure 3. Pinout diagram

## 3.2 Pin definitions

Table 3. PF0100Z pin definitions

Pin number	Pin name	Pin function	Max rating	Type	Definition
1	INTB	O	3.6 V	Digital	Open drain interrupt signal to processor
2	SDWNB	O	3.6 V	Digital	Open drain signal to indicate an imminent system shutdown
3	RESETMCU	O	3.6 V	Digital	Open drain reset output to processor. Alternatively can be used as a power good output.
4	STANDBY	I	3.6 V	Digital	Standby input signal from processor
5	ICTEST	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.
6	SW1FB <sup>(5)</sup>	I	3.6 V	Analog	Output voltage feedback for SW1A/B. Route this trace separately from the high current path and terminate at the output capacitance.
7	SW1AIN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW1A regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
8	SW1ALX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 1A switch node connection
9	SW1BLX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 1B switch node connection
10	SW1BIN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW1B regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
11	SW1CLX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 1C switch node connection
12	SW1CIN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW1C regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
13	SW1CFB <sup>(5)</sup>	I	3.6V	Analog	Output voltage feedback for SW1C. Route this trace separately from the high current path and terminate at the output capacitance.
14	SW1VSSNS	GND	-	GND	Ground reference for regulators SW1ABC. It is connected externally to GNDREF through a board ground plane.
15	GNDREF1	GND	-	GND	Ground reference for regulators SW2 and SW4. It is connected externally to GNDREF, via board ground plane.
16	VGEN1	O	2.5 V	Analog	VGEN1 regulator output, Bypass with a 2.2 $\mu$ F ceramic output capacitor.
17	VIN1	I	3.6 V	Analog	VGEN1, 2 input supply. Bypass with a 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.
18	VGEN2	O	2.5 V	Analog	VGEN2 regulator output, Bypass with a 4.7 $\mu$ F ceramic output capacitor.
19	SW4FB <sup>(5)</sup>	I	3.6 V	Analog	Output voltage feedback for SW4. Route this trace separately from the high current path and terminate at the output capacitance.
20	SW4IN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW4 regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
21	SW4LX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 4 switch node connection
22	SW2LX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 2 switch node connection
23	SW2IN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW2 regulator. Connect pin 23 together with pin 24 and bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to these pins as possible.
24	SW2IN <sup>(5)</sup>	I	4.8 V	Analog	
25	SW2FB <sup>(5)</sup>	I	3.6 V	Analog	Output voltage feedback for SW2. Route this trace separately from the high current path and terminate at the output capacitance.
26	VGEN3	O	3.6 V	Analog	VGEN3 regulator output. Bypass with a 2.2 $\mu$ F ceramic output capacitor.
27	VIN2	I	3.6 V	Analog	VGEN3,4 input. Bypass with a 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.
28	VGEN4	O	3.6 V	Analog	VGEN4 regulator output, Bypass with a 4.7 $\mu$ F ceramic output capacitor.
29	VHALF	I	3.6 V	Analog	Half supply reference for VREFDDR



Table 3. PF0100Z pin definitions (continued)

Pin number	Pin name	Pin function	Max rating	Type	Definition
30	VINREFDDR	I	3.6 V	Analog	VREFDDR regulator input. Bypass with at least 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.
31	VREFDDR	O	3.6 V	Analog	VREFDDR regulator output
32	SW3VSSNS	GND	-	GND	Ground reference for the SW3 regulator. Connect to GNDREF externally via the board ground plane.
33	SW3BFB <sup>(5)</sup>	I	3.6 V	Analog	Output voltage feedback for SW3B. Route this trace separately from the high current path and terminate at the output capacitance.
34	SW3BIN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW3B regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
35	SW3BLX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 3B switch node connection
36	SW3ALX <sup>(5)</sup>	O	4.8 V	Analog	Regulator 3A switch node connection
37	SW3AIN <sup>(5)</sup>	I	4.8 V	Analog	Input to SW3A regulator. Bypass with at least a 4.7 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
38	SW3AFB <sup>(5)</sup>	I	3.6 V	Analog	Output voltage feedback for SW3A. Route this trace separately from the high current path and terminate at the output capacitance.
39	VGEN5	O	3.6 V	Analog	VGEN5 regulator output. Bypass with a 2.2 $\mu$ F ceramic output capacitor.
40	VIN3	I	4.8 V	Analog	VGEN5, six input. Bypass with a 1.0 $\mu$ F decoupling capacitor as close to the pin as possible.
41	VGEN6	O	3.6 V	Analog	VGEN6 regulator output. By pass with a 2.2 $\mu$ F ceramic output capacitor.
42	LICELL	I/O	3.6 V	Analog	Coin cell supply input/output
43	VSNVS	O	3.6 V	Analog	LDO or coin cell output to processor
44	SWBSTFB <sup>(5)</sup>	I	5.5 V	Analog	Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes.
45	SWBSTIN <sup>(5)</sup>	I	4.8 V	Analog	Input to SWBST regulator. Bypass with at least a 2.2 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F decoupling capacitor as close to the pin as possible.
46	SWBSTLX <sup>(5)</sup>	O	7.5 V	Analog	SWBST switch node connection
47	VDDOTP	I	10 V <sup>(4)</sup>	Digital & Analog	Supply to program OTP fuses
48	GNDREF	GND	-	GND	Ground reference for the main band gap regulator.
49	VCORE	O	3.6 V	Analog	Analog core supply
50	VIN	I	4.8 V	Analog	Main chip supply
51	VCOREDIG	O	1.5 V	Analog	Digital core supply
52	VCOREREF	O	1.5 V	Analog	Main band gap reference
53	SDA	I/O	3.6 V	Digital	I <sup>2</sup> C data line (open drain)
54	SCL	I	3.6 V	Digital	I <sup>2</sup> C clock
55	VDDIO	I	3.6 V	Analog	Supply for I <sup>2</sup> C bus
56	PWRON	I	3.6 V	Digital	Power on/off from processor
-	EP	GND	-	GND	Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation.

## Notes

- 10 V Maximum voltage rating during OTP fuse programming. 7.5 V Maximum DC voltage rated otherwise.
- Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and pin SWxIN should be connected to VIN with a 0.1  $\mu$ F bypass capacitor.

## 4 General product characteristics

### 4.1 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
<b>Electrical ratings</b>				
$V_{IN}$	Main input supply voltage	-0.3 to 4.8	V	
$V_{DDOTP}$	OTP programming input supply voltage	-0.3 to 10	V	
$V_{LCELL}$	Coin cell voltage	-0.3 to 3.6	V	
$V_{ESD}$	ESD ratings Human body model VSNVS pin All other pins Charge device model	$\pm 1800$ $\pm 2000$ $\pm 500$	V	(6)

**Notes**

- ESD testing is performed in accordance with the human body model (HBM) ( $C_{ZAP} = 100 \text{ pF}$ ,  $R_{ZAP} = 1500 \text{ }\Omega$ ), and the charge device model (CDM), robotic ( $C_{ZAP} = 4.0 \text{ pF}$ ).

## 4.2 Thermal characteristics

**Table 5. Thermal ratings**

Symbol	Description (rating)	Min.	Max.	Unit	Notes
<b>Thermal ratings</b>					
$T_A$	Ambient operating temperature range PF0100Z PF0100AZ	-40 -40	85 105	°C	
$T_J$	Operating junction temperature range	-40	125	°C	(7)
$T_{ST}$	Storage temperature range	-65	150	°C	
$T_{PPRT}$	Peak package reflow temperature	–	Note 9	°C	(8)(9)

**QFN56 thermal resistance and package dissipation ratings**

$R_{\theta JA}$	Junction to ambient Natural convection Four layer board (2s2p) Eight layer board (2s6p)	– –	28 15	°C/W	(10)(11)(12)
$R_{\theta JMA}$	Junction to ambient (at 200 ft/min) Four layer board (2s2p)	–	22	°C/W	(10)(12)
$R_{\theta JB}$	Junction to board	–	10	°C/W	(13)
$R_{\theta JCBOTTOM}$	Junction to case bottom	–	1.2	°C/W	(14)
$\Psi_{JT}$	Junction to package top Natural convection	–	2.0	°C/W	(15)

**Notes**

- Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See [Table 6](#) for thermal protection features.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
- NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to [www.nxp.com](http://www.nxp.com), search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When the Greek letter ( $\Psi$ ) is not available, the thermal characterization parameter is written as Psi-JT.

### 4.2.1 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in [Table 5](#). To optimize the thermal management and to avoid overheating, the PF0100Z provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I are generated when the respective thresholds specified in [Table 6](#) are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF0100Z. This thermal protection acts above the thermal protection threshold listed in [Table 6](#). To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured so this protection is not tripped under normal conditions.

**Table 6. Thermal protection thresholds**

Parameter	Min.	Typ.	Max.	Units	Notes
Thermal 110 °C threshold (THERM110)	100	110	120	°C	
Thermal 120 °C threshold (THERM120)	110	120	130	°C	
Thermal 125 °C threshold (THERM125)	115	125	135	°C	
Thermal 130 °C threshold (THERM130)	120	130	140	°C	
Thermal warning hysteresis	2.0	–	4.0	°C	
Thermal protection threshold	130	140	150	°C	

## 4.3 Electrical characteristics

### 4.3.1 General Specifications

**Table 7. General PMIC Static Characteristics**

PF0100Z  $T_A = -40\text{ °C}$  to  $85\text{ °C}$ , PF0100AZ  $T_A = -40\text{ °C}$  to  $105\text{ °C}$ ,  $V_{IN} = 2.8\text{ V}$  to  $4.5\text{ V}$ ,  $V_{DDIO} = 1.7\text{ V}$  to  $3.6\text{ V}$ , typical external component values and full load current range, unless otherwise noted.

Pin name	Parameter	Load condition	Min.	Max.	Unit
PWRON	$V_{IL}$	–	0.0	$0.2 * V_{SNVS}$	V
	$V_{IH}$	–	$0.8 * V_{SNVS}$	3.6	V
RESETBMCU	$V_{OL}$	-2.0 mA	0.0	0.4	V
	$V_{OH}$	Open drain	$0.7 * V_{IN}$	$V_{IN}$	V
SCL	$V_{IL}$	–	0.0	$0.2 * V_{DDIO}$	V
	$V_{IH}$	–	$0.8 * V_{DDIO}$	3.6	V
SDA	$V_{IL}$	–	0.0	$0.2 * V_{DDIO}$	V
	$V_{IH}$	–	$0.8 * V_{DDIO}$	3.6	V
	$V_{OL}$	-2.0 mA	0.0	0.4	V
	$V_{OH}$	Open drain	$0.7 * V_{DDIO}$	$V_{DDIO}$	V
INTB	$V_{OL}$	-2.0 mA	0.0	0.4	V
	$V_{OH}$	Open drain	$0.7 * V_{IN}$	$V_{IN}$	V
SDWNB	$V_{OL}$	-2.0 mA	0.0	0.4	V
	$V_{OH}$	Open drain	$0.7 * V_{IN}$	$V_{IN}$	V
STANDBY	$V_{IL}$	–	0.0	$0.2 * V_{SNVS}$	V
	$V_{IH}$	–	$0.8 * V_{SNVS}$	3.6	V
VDDOTP	$V_{IL}$	–	0.0	0.3	V
	$V_{IH}$	–	1.1	1.7	V

## 4.3.2 Current consumption

The current consumption of the individual blocks is described in detail throughout this specification. For convenience, a summary table follows for standard use cases.

**Table 8. Current consumption summary**

PF0100Z  $T_A = -40\text{ °C}$  to  $85\text{ °C}$ , PF0100AZ  $T_A = -40\text{ °C}$  to  $105\text{ °C}$ ,  $V_{IN} = 3.6\text{ V}$ ,  $V_{DDIO} = 1.7\text{ V}$  to  $3.6\text{ V}$ ,  $LICELL = 1.8\text{ V}$  to  $3.3\text{ V}$ ,  $V_{SNVS} = 3.0\text{ V}$ , typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ ,  $V_{DDIO} = 3.3\text{ V}$ ,  $LICELL = 3.0\text{ V}$ ,  $V_{SNVS} = 3.0\text{ V}$  and  $25\text{ °C}$ , unless otherwise noted.

Mode	PF0100Z conditions	System conditions	Typ.	Max.	Unit	Notes
Coin Cell	VSNVS from LICELL All other blocks off $V_{IN} = 0.0\text{ V}$ $V_{SNVSVOLT}[2:0] = 110$	No load on VSNVS	4.0	7.0	$\mu\text{A}$	(16),(18), (21)
Off MMPF0100Z	VSNVS from VIN or LICELL Wake-up from PWRON active 32 k RC on All other blocks off $V_{IN} \geq UVDET$	No load on VSNVS, PMIC able to wake-up	16	21	$\mu\text{A}$	(17),(18)
Off MMPF0100AZ	VSNVS from VIN or LICELL Wake-up from PWRON active 32 k RC on All other blocks off $V_{IN} \geq UVDET$	No load on VSNVS, PMIC able to wake-up	17	25	$\mu\text{A}$	(17),(18)
Sleep	VSNVS from VIN Wake-up from PWRON active Trimmed reference active SW3A/B PFM Trimmed 16 MHz RC off 32 k RC on VREFDDR disabled $T_A = -40\text{ °C}$ to $85\text{ °C}$ $T_A = -40\text{ °C}$ to $105\text{ °C}$ (PF0100AZ Only)	No load on VSNVS. DDR memories in self refresh	122 122	220 250	$\mu\text{A}$	(18)
Standby MMPF0100Z	VSNVS from either VIN or LICELL SW1A/B combined in PFM SW1C in PFM SW2 in PFM SW3A/B combined in PFM SW4 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VGEN1-6 enabled VREFDDR enabled	No load on VSNVS. Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)	297 297	450 (19) 1000 (20)	$\mu\text{A}$	(18)



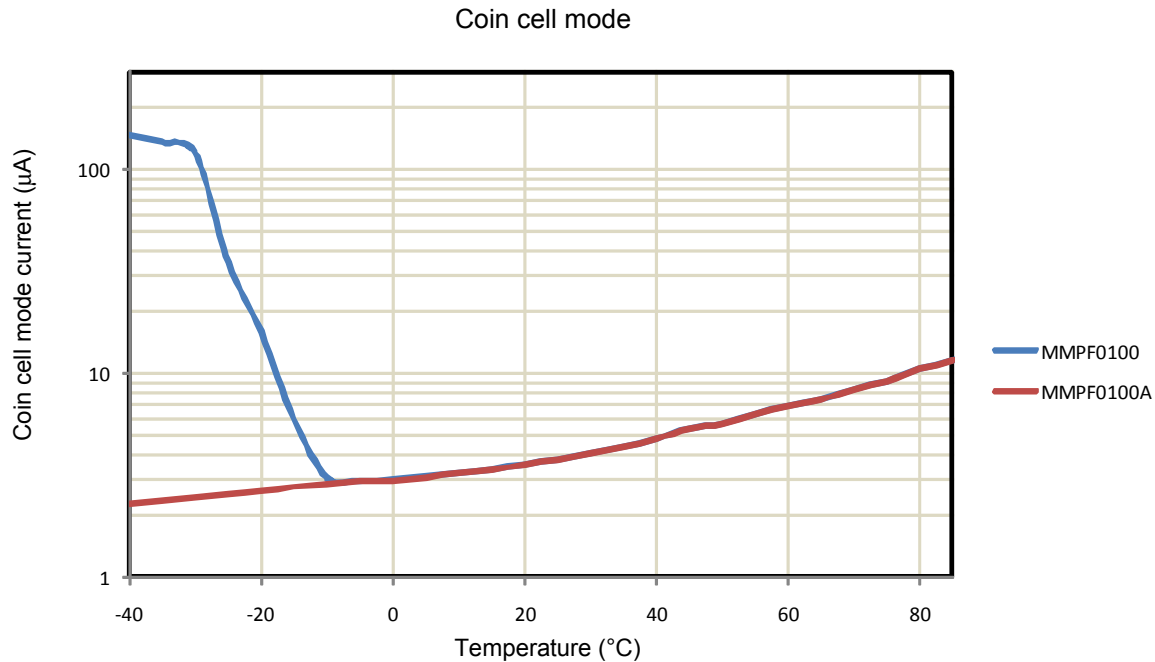
**Table 8. Current consumption summary (continued)**

PF0100Z  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ , PF0100AZ  $T_A = -40\text{ }^\circ\text{C}$  to  $105\text{ }^\circ\text{C}$ ,  $V_{IN} = 3.6\text{ V}$ ,  $V_{DDIO} = 1.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{LICELL} = 1.8\text{ V}$  to  $3.3\text{ V}$ ,  $V_{SNVS} = 3.0\text{ V}$ , typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ ,  $V_{DDIO} = 3.3\text{ V}$ ,  $V_{LICELL} = 3.0\text{ V}$ ,  $V_{SNVS} = 3.0\text{ V}$  and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

Standby MMPF0100AZ	VSNVS from either VIN or LICELL SW1A/B combined in PFM SW1C in PFM SW2 in PFM SW3A/B combined in PFM SW4 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VGEN1-6 enabled VREFDDR enabled $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ $T_A = -40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$	No load on VSNVS. Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)			$\mu\text{A}$	(18)
			297	450		
			297	550		

Notes

16. Refer to [Figure 4](#) for coin cell mode characteristics over temperature.
17. When  $V_{IN}$  is below the UVDET threshold, in the range of  $1.8\text{ V} \leq V_{IN} < 2.65\text{ V}$ , the quiescent current increases by  $50\text{ }\mu\text{A}$ , typically.
18. For PFM operation, headroom should be  $300\text{ mV}$  or greater.
19. From  $0\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$
20. From  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$
21. Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due an internal path from RESETBMCU to VIN. The additional current is  $<30\text{ }\mu\text{A}$  with a pull up resistor of  $100\text{ k}\Omega$ . The i.MX 6x processors have an internal pull up from the POR\_B pin to the VDD\_SNVS\_IN pin. For i.MX 6x applications, if additional current in the coin cell mode is not desired, use an external switch to disconnect the RESETBMCU path when VIN is removed. For non-i.MX 6 applications, pull-up RESETBMCU to a rail that is off in the coin cell mode.



**Figure 4. Current overtemperature waveforms**

## 5 General description

The PF0100Z is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX 6 series of application processors.

### 5.1 Features

This section summarizes the PF0100Z features.

- Input voltage range to PMIC: 2.8 V - 4.5 V
- Buck regulators
  - Four to six channel configurable
    - SW1A/B/C, 4.5 A (single); 0.3 V to 1.875 V
    - SW1A/B, 2.5 A (single/dual); SW1C 2.0 A (independent); 0.3 V to 1.875 V
    - SW2, 2.0 A; 0.4 V to 3.3 V (2.5 A; 1.2 V to 3.3 V <sup>(22)</sup>)
    - SW3A/B, 2.5 A (single/dual); 0.4 V to 3.3 V
    - SW3A, 1.25 A (independent); SW3B, 1.25 A (independent); 0.4 V to 3.3 V
    - SW4, 1.0 A; 0.4 V to 3.3 V
    - SW4, VTT mode provide DDR termination at 50% of SW3A
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS
  - Programmable output voltage
  - Programmable current limit
  - Programmable soft start
  - Programmable PWM switching frequency
  - Programmable OCP with fault interrupt
- Boost regulator
  - SWBST, 5.0 V to 5.15 V, 0.6 A, OTG support
  - Modes: PFM and Auto
  - OCP fault interrupt
- LDOs
  - Six user programable LDO
    - VGEN1, 0.80 V to 1.55 V, 100 mA
    - VGEN2, 0.80 V to 1.55 V, 250 mA
    - VGEN3, 1.8 V to 3.3 V, 100 mA
    - VGEN4, 1.8 V to 3.3 V, 350 mA
    - VGEN5, 1.8 V to 3.3 V, 100 mA
    - VGEN6, 1.8 V to 3.3 V, 200 mA
  - Soft start
  - LDO/switch supply
    - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 400  $\mu$ A
- DDR memory reference voltage
  - VREFDDR, 0.6 V to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP (one time programmable) memory for device configuration
  - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I<sup>2</sup>C interface
- User programmable standby, sleep, and off modes

#### Notes

22. SW2 capable of 2.5 A in NP/F9/FA versions

## 5.2 Functional block diagram

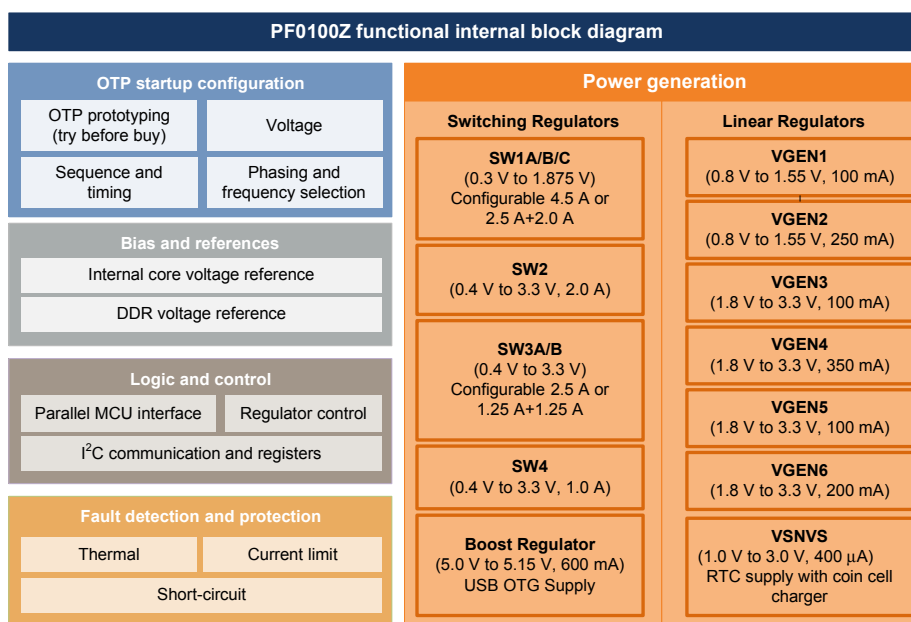


Figure 5. Functional block diagram

## 5.3 Functional description

### 5.3.1 Power generation

The PF0100Z PMIC features four buck regulators (up to six independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination, and a DDR voltage reference to supply voltages for the application processor and peripheral devices.

The number of independent buck regulator outputs can be configured from four to six, thereby providing flexibility to operate with higher current capability, or to operate as independent outputs for applications requiring more voltage rails with lower current demands. Further, SW1 and SW3 regulators can be configured as single/dual phase and/or independent converters. One of the buck regulators, SW4, can also operate as a tracking regulator when used for memory termination. The buck regulators provide the supply to processor cores and to other low voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry.

Depending on the system power path configuration, the six general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operating with or without VTT termination. The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; VSNVS may be powered from  $V_{IN}$ , or from a coin cell.

### 5.3.2 Control logic

The PF0100Z PMIC is fully programmable via the I<sup>2</sup>C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Start-up sequence of the device is selected upon the initial OTP configuration explained in the [Start-up](#) section, or by configuring the “try before buy” feature to test different power up sequences before choosing the final OTP configuration.

The PF0100Z PMIC has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures supply of critical internal logic and other circuits from the coin cell during brief interruptions from the main battery. A charger for the coin cell is included as well.

## 5.3.2.1 Interface signals

### 5.3.2.1.1 PWRON

PWRON is an input signal to the IC generating a turn-on event. It can be configured to detect a level, or an edge using the PWRON\_CFG bit. Refer to section [6.4.2.1 Turn on events, page 30](#) for more details.

### 5.3.2.1.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted, the part enters standby mode and when de-asserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. Refer to the section [6.4.1.3 Standby mode, page 28](#) for more details.

Note: When operating the PMIC at  $V_{IN} \leq 2.85$  V and VSNVS is programmed for a 3.0 V output, a coin cell must be present to provide VSNVS, or the PMIC does not reliably enter and exit the STANDBY mode.

### 5.3.2.1.3 RESETBMCU

RESETBMCU is an open-drain, active low output configurable for two modes of operation. In its default mode, it is de-asserted 2.0 ms to 4.0 ms after the last regulator in the start-up sequence is enabled; refer to [Figure 6](#) as an example. In this mode, the signal can be used to bring the processor out of reset, or as an indicator all supplies have been enabled; it is only asserted for a turn-off event.

When configured for its fault mode, RESETBMCU is de-asserted after the start-up sequence is completed only if no faults occurred during start-up. At anytime, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted, LOW. The PF0100Z is turned off if the fault persists for more than 100 ms typically. The PWRON signal restarts the part, though if the fault persists, the sequence described previously is repeated. To enter the fault mode, set bit OTP\_PG\_EN of register OTP\_PWRGD EN to "1". This register, 0xE8, is located on [Table 136. Extended page 1, page 106](#) of the register map. To test the fault mode, the bit may be set during TBB prototyping, or the mode may be permanently chosen by programming OTP fuses.

### 5.3.2.1.4 SDWNB

SDWNB is an open drain, active low output notifying the processor of an imminent PMIC shut down. It is asserted low for one 32 kHz clock cycle before powering down and then de-asserted in the OFF state.

### 5.3.2.1.5 INTB

INTB is an open-drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a "1" to the fault interrupt bit.

## 6 Functional block requirements and behaviors

### 6.1 Start-up

The PF0100Z can be configured to start-up from either the internal OTP configuration, or with a hard-coded configuration built in to the device. The internal hard-coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kΩ resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP devices, selecting the OTP configuration causes the PF0100Z not to start-up. However, the PF0100Z can be controlled through the I<sup>2</sup>C port for prototyping and programming. Once programmed, the NP device starts up with the customer programmed configuration.

#### 6.1.1 Device start-up configuration

[Table 9](#) shows the default configuration, which can be accessed on all devices as described previously, as well as the pre-programmed OTP configurations.

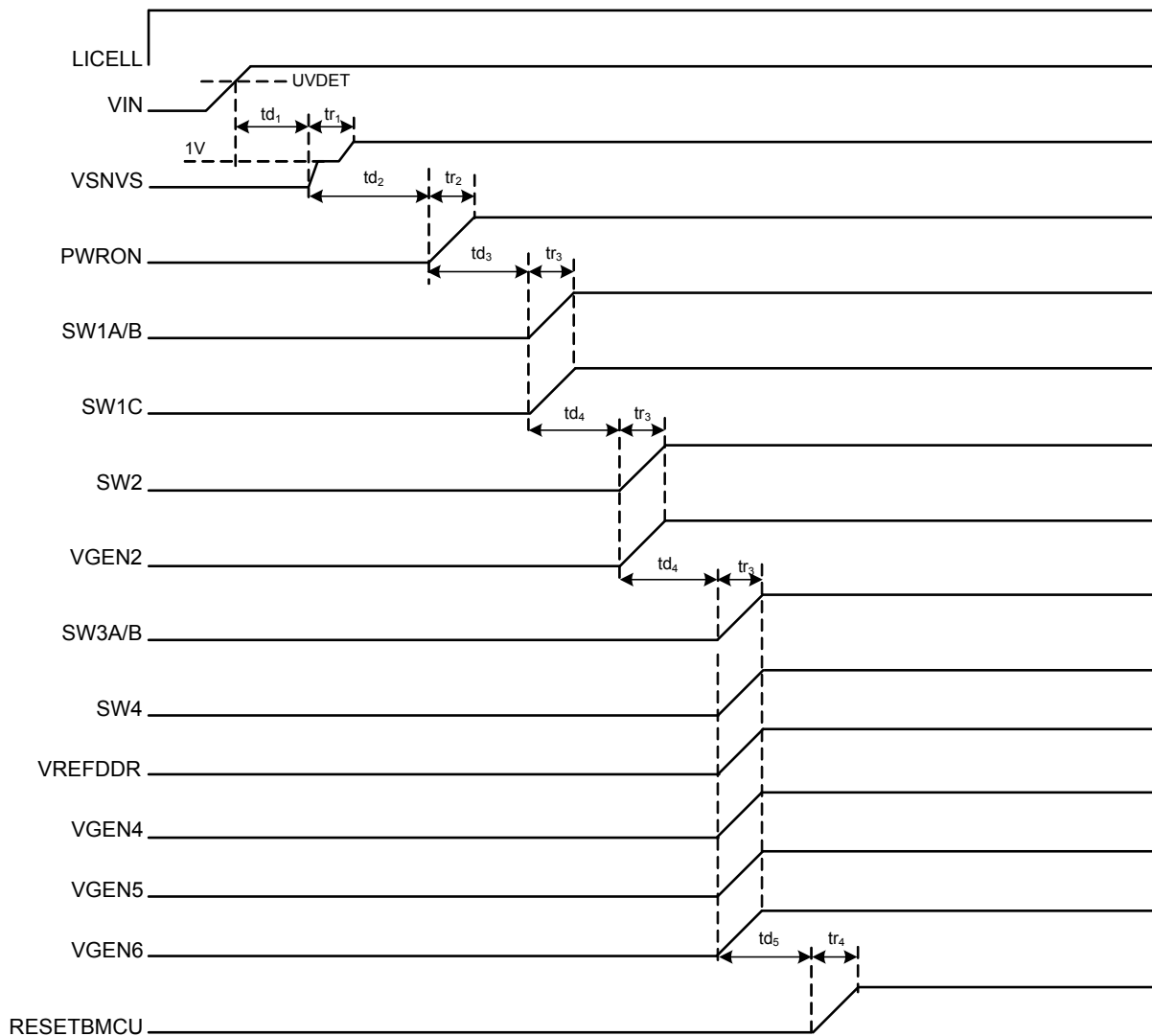
**Table 9. Start-up configuration**

Registers	Default configuration	Pre-programmed OTP configuration				
	All devices	F0	F6	F8	F9	FA
Default I <sup>2</sup> C Address	0x08	0x08	0x08	0x08	0x08	0x08
VSNVS_VOLT	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
SW1AB_VOLT	1.375 V	1.375 V	1.375 V	1.425 V	1.375 V	1.375 V
SW1AB_SEQ	1	1	2	1	5	5
SW1C_VOLT	1.375 V	1.375 V	1.375 V	1.425 V	1.375 V	1.375 V
SW1C_SEQ	1	2	2	2	5	5
SW2_VOLT	3.0 V	3.3 V	3.3 V	3.0 V	1.375 V	1.375 V
SW2_SEQ	2	5	4	5	5	5
SW3A_VOLT	1.5 V	1.5 V	1.35 V	1.5 V	1.350 V	1.5 V
SW3A_SEQ	3	3	3	3	6	6
SW3B_VOLT	1.5 V	1.5 V	1.35 V	1.5 V	1.350 V	1.5 V
SW3B_SEQ	3	3	3	3	6	6
SW4_VOLT	1.8 V	3.15 V	1.8 V	3.15 V	1.825 V	1.825 V
SW4_SEQ	3	6	4	-	7	7
SWBST_VOLT	-	5.0 V	5.0 V	-	5.0 V	5.0 V
SWBST_SEQ	-	13	Off	-	10	10
VREFDDR_SEQ	3	3	3	3	6	6
VGEN1_VOLT	-	1.5 V	1.2 V	1.5 V	1.2 V	1.2 V
VGEN1_SEQ	-	9	5	-	-	-
VGEN2_VOLT	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V
VGEN2_SEQ	2	10	Off	-	8	8
VGEN3_VOLT	-	2.5 V	2.8 V	2.5 V	1.8 V	1.8 V
VGEN3_SEQ	-	11	5	-	8	8
VGEN4_VOLT	1.8 V	1.8 V	1.8 V	1.8 V	3.0 V	3.0 V
VGEN4_SEQ	3	7	4	-	4	4



**Table 9. Start-up configuration (continued)**

Registers	Default configuration	Pre-programmed OTP configuration				
	All devices	F0	F6	F8	F9	FA
VGEN5_VOLT	2.5 V	2.8 V	3.3 V	2.8 V	2.5 V	2.5 V
VGEN5_SEQ	3	12	5	-	8	8
VGEN6_VOLT	2.8 V	3.3 V	3.0 V	2.8 V	2.8 V	2.8 V
VGEN6_SEQ	3	8	1	6	7	7
PU CONFIG, SEQ_CLK_SPEED	1.0 ms	2.0 ms	0.5 ms	2.0 ms	0.5 ms	0.5 ms
PU CONFIG, SWDVS_CLK	6.25 mV/ $\mu$ s	1.5625 mV/ $\mu$ s	6.25 mV/ $\mu$ s	25 mV/16 $\mu$ s	6.25 mV/ $\mu$ s	6.25 mV/ $\mu$ s
PU CONFIG, PWRON	Level sensitive					
SW1AB CONFIG	SW1AB Single Phase, SW1C Independent Mode, 2.0 MHz				SW1ABC Single Phase, 2.0 MHz	
SW1C CONFIG	2.0 MHz					
SW2 CONFIG	2.0 MHz					
SW3A CONFIG	SW3AB Single Phase, 2.0 MHz					
SW3B CONFIG	2.0 MHz					
SW4 CONFIG	No VTT, 2.0 MHz					
PG EN	RESETBMCU in Default Mode					



\*VSNVS starts from 1.0 V if LICELL is valid before VIN.

Figure 6. Default start-up sequence

Table 10. Default start-up sequence timing

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
$t_{D1}$	Turn-on delay of VSNVS	–	5.0	–	ms	(23)
$t_{R1}$	Rise time of VSNVS	–	3.0	–	ms	
$t_{D2}$	User determined delay	–	1.0	–	ms	
$t_{R2}$	Rise time of PWRON	–	(24)	–	ms	
$t_{D3}$	Turn-on delay of first regulator					
	SEQ_CLK_SPEED[1:0] = 00	–	2.0	–	ms	(25)
	SEQ_CLK_SPEED[1:0] = 01	–	2.5	–		
	SEQ_CLK_SPEED[1:0] = 10	–	4.0	–		
SEQ_CLK_SPEED[1:0] = 11	–	7.0	–			
$t_{R3}$	Rise time of regulators	–	0.2	–	ms	(26)

**Table 10. Default start-up sequence timing (continued)**

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
$t_{D4}$	Delay between regulators					
	SEQ_CLK_SPEED[1:0] = 00	–	0.5	–	ms	
	SEQ_CLK_SPEED[1:0] = 01	–	1.0	–		
	SEQ_CLK_SPEED[1:0] = 10	–	2.0	–		
	SEQ_CLK_SPEED[1:0] = 11	–	4.0	–		
$t_{R4}$	Rise time of RESETBMCU	–	0.2	–	ms	
$t_{D5}$	Turn-on delay of RESETBMCU	–	2.0	–	ms	

**Notes**

23. Assumes LICELL voltage is valid before  $V_{IN}$  is applied. If LICELL is not valid before  $V_{IN}$  is applied then VSNVS turn-on delay may extend to a maximum of 24 ms.
24. Depends on the external signal driving PWRON.
25. Default configuration.
26. Rise time is a function of slew rate of regulators and nominal voltage selected.

## 6.1.2 One time programmability (OTP)

OTP allows the programming of start-up configurations for a variety of applications. Before permanently programming the IC by programming fuses, a configuration may be prototyped by using the “try before buy” (TBB) feature. Further, an error correction code (ECC) algorithm is available to correct a single bit error and to detect multiple bit errors when fuses are programmed.

The following parameters which can be configured by OTP are listed.

- General: I<sup>2</sup>C slave address, PWRON pin configuration, start-up sequence and timing
- Buck regulators: Output voltage, dual/single phase or independent mode configuration, switching frequency, and soft start ramp rate
- Boost regulator and LDOs: Output voltage

**NOTE:** When prototyping or programming fuses, the user must ensure register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the start-up sequence.

### 6.1.2.1 Start-up sequence and timing

Each regulator has 5-bits allocated to program its start-up time slot from a turn on event; therefore, each can be placed from position one to thirty-one in the start-up sequence. The all zeros code indicates a regulator is not part of the start-up sequence and remains off. See [Table 11](#). The delay between each position is equal; however, four delay options are available. See [Table 12](#). The start-up sequence terminates at the last programmed regulator.

**Table 11. Start-up sequence**

SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0]	Sequence
00000	Off
00001	SEQ_CLK_SPEED[1:0] * 1
00010	SEQ_CLK_SPEED[1:0] * 2
*	*
*	*
*	*
*	*
11111	SEQ_CLK_SPEED[1:0] * 31

**Table 12. Start-up Sequence Clock Speed**

SEQ_CLK_SPEED[1:0]	Time (μs)
00	500
01	1000
10	2000
11	4000

### 6.1.2.2 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON\_CFG = 0), or as an edge sensitive input (PWRON\_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into sleep mode. As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters sleep mode.

**Table 13. PWRON configuration**

PWRON_CFG	Mode
0	PWRON pin HIGH = ON PWRON pin LOW = OFF or sleep mode
1	PWRON pin pulled LOW momentarily = ON PWRON pin LOW for 4.0 seconds = OFF or sleep mode

### 6.1.2.3 I<sup>2</sup>C address configuration

The I<sup>2</sup>C device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the I<sup>2</sup>C address to avoid bus conflicts. Address bit, I2C\_SLV\_ADDR[3] in OTP\_I2C\_ADDR register is hard coded to “1” while the lower three LSBs of the I<sup>2</sup>C address (I2C\_SLV\_ADDR[2:0]) are programmable as shown in [Table 14](#).

**Table 14. I<sup>2</sup>C address configuration**

I2C_SLV_ADDR[3] hard coded	I2C_SLV_ADDR[2:0]	I <sup>2</sup> C device address (Hex)
1	000	0x08
1	001	0x09
1	010	0x0A
1	011	0x0B
1	100	0x0C
1	101	0x0D
1	110	0x0E
1	111	0x0F

### 6.1.2.4 Soft start ramp rate

The start-up ramp rate or soft start ramp rate can be chosen from the same options as shown in [6.4.4.2.1 Dynamic voltage scaling, page 34](#).

### 6.1.3 OTP prototyping

Before permanently programming fuses, it is possible to test the desired configuration by using the “try before buy” feature. With this feature, the configuration is loaded from the OTP registers. These registers merely serve as temporary storage for the values to be written to the fuses, for the values read from the fuses, or for the values read from the default configuration. To avoid confusion, these registers are referred to as the TBBOTP registers. The portion of the register map concerning OTP is shown in [Table 136](#) and [Table 137](#).

The contents of the TBBOTP registers are initialized to zero when a valid VIN is first applied. The values then loaded into the TBBOTP registers depend on the setting of the VDDOTP pin and on the value of the TBB\_POR and FUSE\_POR bits. Refer to [Table 15](#).

- If VDDOTP = VCOREDIG (1.5 V), the values are loaded from the default configuration.
- If VDDOTP = 0.0 V, TBB\_POR = 0 and FUSE\_POR = 1, the values are loaded from the fuses. In the MMPF0100Z, FUSE\_POR1, FUSE\_POR2, and FUSE\_POR3 are XOR'ed into the FUSE\_POR\_XOR bit. The FUSE\_POR\_XOR must be 1 for fuses to be loaded. This is achieved by setting any one or all of the FUSE\_PORx bits. The XOR function is removed in the MMPF0100AZ. It is required to set all of the FUSE\_PORx bits to be able to load the fuses.
- If VDDOTP = 0.0 V, TBB\_POR = 0 and FUSE\_POR = 0, the TBBOTP registers remain initialized at zero.

The initial value of TBB\_POR is always “0”; only when VDDOTP = 0.0 V and TBB\_POR is set to “1” are the values from the TBBOTP registers maintained and not loaded from a different source.

The contents of the TBBOTP registers are modified by I<sup>2</sup>C. To communicate with I<sup>2</sup>C, VIN must be valid and VDDIO, to which SDA and SCL are pulled up, must be powered by a 1.7 V to 3.6 V supply. V<sub>IN</sub>, or the coin cell voltage must be valid to maintain the contents of the registers. To power on with the contents of the TBBOTP registers, the following conditions must exist; VIN is valid, VDDOTP = 0.0 V, TBB\_POR = 1, and there is a valid turn-on event. Refer to the application note [AN4536](#) for an example of prototyping.

### 6.1.4 Reading OTP fuses

As described in the previous section, the contents of the fuses are loaded to the TBBOTP registers when the following conditions are met; VIN is valid, VDDOTP = 0.0 V, TBB\_POR = 0 and FUSE\_POR = 1. If ECC were enabled at the time the fuses were programmed, the error corrected values can be loaded into the TBBOTP registers if desired. Once the fuses are loaded and a turn-on event occurs, the PMIC powers on with the configuration programmed in the fuses. For more details on reading the OTP fuses, see application note [AN4536](#).

### 6.1.5 Programming OTP fuses

The programmable parameters are shown in the TBBOTP registers in the [Table 136. Extended page 1, page 106](#) of the register map. The PF0100AZ offers ECC, the control registers for which functions are located in [Table 137. Extended page 2, page 110](#) of the register map. There are ten banks of twenty-six fuses each which can be programmed. For more details on programming the OTP fuses, see application note [AN4536](#).

**Table 15. Source of start-up sequence**

VDDOTP(V)	TBB_POR	FUSE_POR	Start-up sequence
0	0	0	None
0	0	1	OTP fuses
0	1	x	TBBOTP registers
1.5	x	x	Factory defined



## 6.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within -8.0%/+8.0%. The 32 kHz untrimmed clock is only used in the following conditions:

- $V_{IN} < UVDET$
- All regulators are in sleep mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up,  $V_{IN} > UVDET$
- $PWRON\_CFG = 1$ , for power button debounce timing

In addition, when the 16 MHz is active in the on mode, the debounce times in [Table 26](#) are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock.

**Table 16. 16 MHz clock specifications**

PF0100Z  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ , PF0100AZ  $T_A = -40\text{ }^\circ\text{C}$  to  $105\text{ }^\circ\text{C}$ ,  $V_{IN} = 2.8\text{ V}$  to  $4.5\text{ V}$ , LICELL =  $1.8\text{ V}$  to  $3.3\text{ V}$  and typical external component values. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ , LICELL =  $3.0\text{ V}$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
$V_{IN16MHz}$	Operating voltage From VIN	2.8	–	4.5	V	
$f_{16MHz}$	16 MHz clock frequency	14.7	16	17.2	MHz	
$f_{2MHz}$	2.0 MHz clock frequency	1.84	–	2.15	MHz	(27)

Notes

27. The 2.0 MHz clock is derived from the 16 MHz clock.

### 6.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as  $\pm 3\%$  of the nominal frequency. Contact your NXP representative for detailed information on this feature.

## 6.3 Bias and references block description

### 6.3.1 Internal core voltage references

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. The bandgap and the rest of the core circuitry are supplied from VCORE. The performance of the regulators is directly dependent on the performance of the bandgap. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell. [Table 17](#) shows the main characteristics of the core circuitry.

**Table 17. Core voltages electrical specifications<sup>(29)</sup>**

PF0100Z  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ , PF0100AZ  $T_A = -40\text{ }^\circ\text{C}$  to  $105\text{ }^\circ\text{C}$ ,  $V_{IN} = 2.8\text{ V}$  to  $4.5\text{ V}$ , LICELL =  $1.8\text{ V}$  to  $3.3\text{ V}$ , and typical external component values. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ , LICELL =  $3.0\text{ V}$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
<b>VCOREDIG (digital core supply)</b>						
$V_{COREDIG}$	Output voltage On mode <sup>(28)</sup> Coin cell mode and off	– –	1.5 1.3	– –	V	
<b>VCORE (analog core supply)</b>						
$V_{CORE}$	Output voltage On mode and charging <sup>(28)</sup> Off and Coin cell mode	– –	2.775 0.0	– –	V	

**Table 17. Core voltages electrical specifications<sup>(29)</sup> (continued)**

PF0100Z  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ , PF0100AZ  $T_A = -40\text{ }^\circ\text{C}$  to  $105\text{ }^\circ\text{C}$ ,  $V_{IN} = 2.8\text{ V}$  to  $4.5\text{ V}$ , LICELL =  $1.8\text{ V}$  to  $3.3\text{ V}$ , and typical external component values. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ , LICELL =  $3.0\text{ V}$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
<b>VCOREREF (bandgap / regulator reference)</b>						
$V_{COREREF}$	Output voltage <sup>(28)</sup>	–	1.2	–	V	
$V_{COREREFACC}$	Absolute accuracy	–	0.5	–	%	
$V_{COREREFTEMP}$	Temperature drift	–	0.25	–	%	

- Notes
- 28.  $3.0\text{ V} < V_{IN} < 4.5\text{ V}$ , no external loading on VCOREDIG, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.
  - 29. For information only

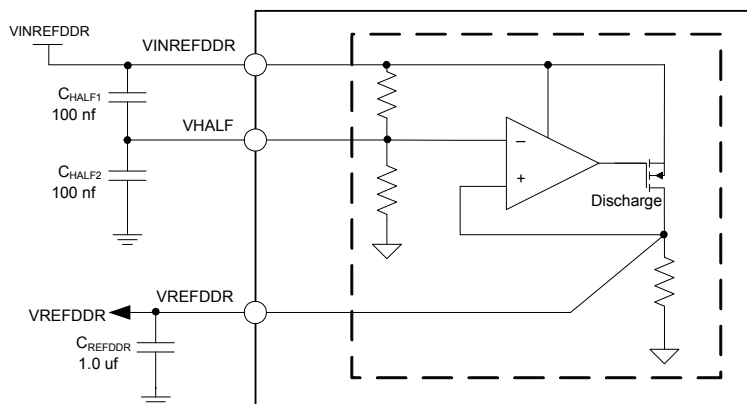
### 6.3.1.1 External components

**Table 18. External components for core voltages**

Regulator	Capacitor value ( $\mu\text{F}$ )
VCOREDIG	1.0
VCORE	1.0
VCOREREF	0.22

### 6.3.2 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. Its typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider uses a voltage follower to drive the load.



**Figure 7. VREFDDR block diagram**

#### 6.3.2.1 VREFDDR control register

The VREFDDR voltage reference is controlled by a single bit in VREFDDCTRL register in [Table 19](#).

Table 19. Register VREFDDCTRL - ADDR 0x6A

Name	Bit #	R/W	Default	Description
UNUSED	3:0	–	0x00	unused
VREFDDREN	4	R/W	0x00	Enable or disables VREFDDR output voltage 0 = VREFDDR disabled 1 = VREFDDR enabled
UNUSED	7:5	–	0x00	unused

### 6.3.2.1.1 External components

Table 20. VREFDDR external components <sup>(30)</sup>

Capacitor	Capacitance ( $\mu\text{F}$ )
VINREFDDR <sup>(31)</sup> to VHALF	0.1
VHALF to GND	0.1
VREFDDR	1.0

## Notes

30. Use X5R or X7R capacitors.

31. VINREFDDR to GND, 1.0  $\mu\text{F}$  minimum capacitance is provided by buck regulator output.

### 6.3.2.1.2 VREFDDR specifications

Table 21. VREFDDR electrical characteristics

PF0100Z  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ , PF0100AZ  $T_A = -40\text{ }^\circ\text{C}$  to  $105\text{ }^\circ\text{C}$ ,  $V_{IN} = 3.6\text{ V}$ ,  $I_{REFDDR} = 0.0\text{ mA}$ ,  $V_{INREFDDR} = 1.5\text{ V}$  and typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 3.6\text{ V}$ ,  $I_{REFDDR} = 0.0\text{ mA}$ ,  $V_{INREFDDR} = 1.5\text{ V}$ , and  $25\text{ }^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
<b>VREFDDR</b>						
$V_{INREFDDR}$	Operating input voltage range	1.2	–	1.8	V	
$I_{REFDDR}$	Operating load current range	0.0	–	10	mA	
$I_{REFDDRLIM}$	Current limit $I_{REFDDR}$ when $V_{REFDDR}$ is forced to $V_{INREFDDR}/4$	10.5	15	25	mA	
$I_{REFDDRQ}$	Quiescent current	–	8.0	–	$\mu\text{A}$	<sup>(32)</sup>

## Active Mode – DC

$V_{REFDDR}$	Output voltage $1.2\text{ V} < V_{INREFDDR} < 1.8\text{ V}$ $0.0\text{ mA} < I_{REFDDR} < 10\text{ mA}$	–	$V_{INREFDDR}/2$	–	V	
$V_{REFDDRTOL}$	Output voltage tolerance $1.2\text{ V} < V_{INREFDDR} < 1.8\text{ V}$ $0.6\text{ mA} \leq I_{REFDDR} \leq 10\text{ mA}$ $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ $T_A = -40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$ (PF0100AZ only)	–1.0 –1.2	– –	1.0 1.2	%	
$V_{REFDDRLOR}$	Load regulation $1.0\text{ mA} < I_{REFDDR} < 10\text{ mA}$ $1.2\text{ V} < V_{INREFDDR} < 1.8\text{ V}$	–	0.40	–	mV/mA	