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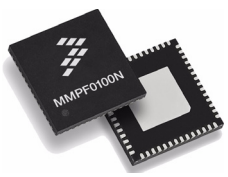
Document Number: MMPF0100
Rev. 17.0, 1/2017

14 channel configurable power management integrated circuit

PF0100

POWER MANAGEMENT

EP SUFFIX (E-TYPE)
98ASA00405D
56 QFN 8X8



ES SUFFIX (WF-TYPE)
98ASA00589D
56 QFN 8X8

The PF0100 SMARTMOS power management integrated circuit (PMIC) provides a highly programmable/ configurable architecture, with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF0100 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications. With on-chip one time programmable (OTP) memory, the PF0100 is available in pre-programmed standard versions, or non-programmed to support custom programming. The PF0100 is defined to power an entire embedded MCU platform solution such as i.MX 6 based eReader, IPTV, medical monitoring, and home/factory automation.

Features:

- Four to six buck converters, depending on configuration
  - Single/Dual phase/ parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (one time programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- I^2C control
- Individually programmable ON, OFF, and standby modes

Applications:

- Tablets
- IPTV
- eReaders
- Set top boxes
- Industrial control
- Medical monitoring
- Home automation/ alarm/ energy management

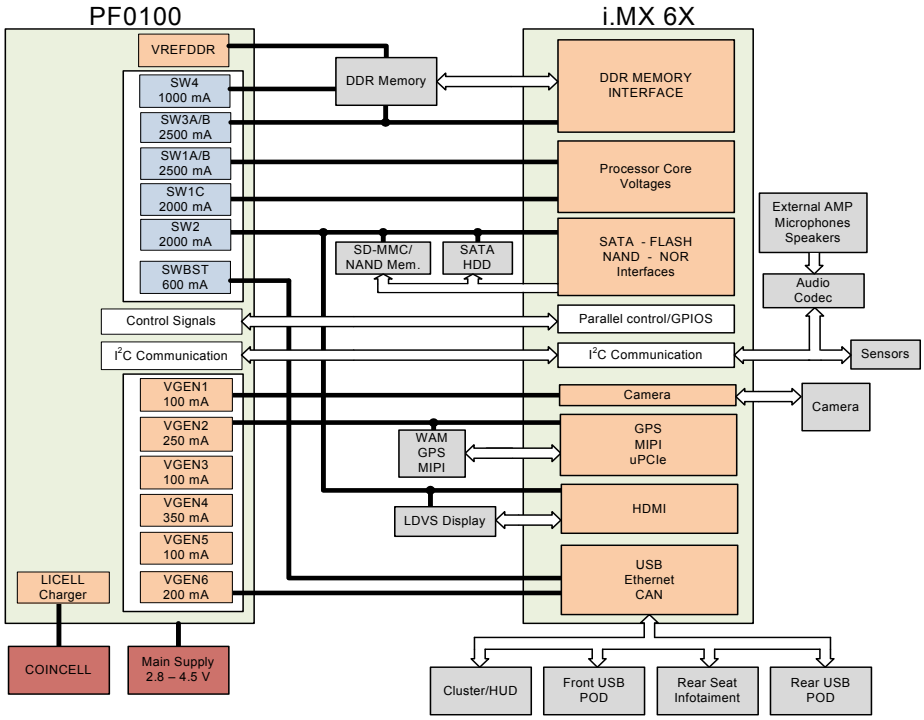


Figure 1. Simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

The PF0100 is available with both pre-programmed and non-programmed OTP memory configurations. The non-programmed device uses “NP” as the programming code. The pre-programmed devices are identified using the program codes from Table 1, which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in Table 10.

Table 1. Orderable Part Variations

Part Number	Temperature (T_A)	Package	Programming	Reference Designs	Notes
MMPF0100NPAEP	-40 °C to 85 °C (for use in consumer applications)	56 QFN 8x8 mm - 0.5 mm pitch E-Type QFN (full lead)	NP	N/A	(1), (2)
MMPF0100F0AEP			F0	MCIMX6Q-SDP MCIMX6Q-SDB MCIMX6DL-SDP	
MMPF0100F1AEP			F1	MCIMX6SLEVK	(1), (2), (3)
MMPF0100F2AEP			F2	N/A	
MMPF0100F3AEP			F3	N/A	(1), (2)
MMPF0100F4AEP			F4	N/A	
MMPF0100F6AEP			F6	MCIMX6SX-SDB	
MMPF0100FCAEP			FC	N/A	(1), (2)
MMPF0100FDAEP			FD	MCIMX6SLLEVK	
MMPF0100NPANES	-40 °C to 105 °C (for use in extended industrial applications)	56 QFN 8x8 mm - 0.5 mm pitch WF-Type QFN (wettable flank)	NP	N/A	(1), (2), (4)
MMPF0100F0ANES			F0	MCIMX6Q-SDP MCIMX6Q-SDB MCIMX6DL-SDP	(1), (2)
MMPF0100F3ANES			F3	N/A	
MMPF0100F4ANES			F4	N/A	
MMPF0100F6ANES			F6	MCIMX6SX-SDB	
MMPF0100F9ANES			F9	N/A	(1), (2), (4)
MMPF0100FAANES			FA	N/A	
MMPF0100FBANES			FB	N/A	
MMPF0100FCANES			FC	N/A	(1), (2)

Notes

1. For tape and reel, add an R2 suffix to the part number.
2. For programming details see Table 10. The available OTP options are not restricted to the listed reference designs. They can be used in any application where the listed voltage and sequence details are acceptable.
3. For designs using the i.MX 6SoloLite, it is recommended to use the F3 OTP option instead of the F1 OTP option and F4 OTP option instead of the F2 OTP option.
4. SW2 can support an output current rating of 2.5 A in NP, F9, and FA Industrial versions only (ANES suffix) when SW2ILIM=0

1.1 PF0100 version differences

PF0100A is an improved version of the PF0100 power management IC. Table 2 summarizes the difference between the two versions and should be referred to when migrating from the PF0100 to the PF0100A. Note that programming options are the same for both versions of the device.

Table 2. Differences between PF0100 and PF0100A

Description	PF0100	PF0100A
Version identification	Reading SILICON REV register at address 0x03 returns 0x11. DEVICEID register at address 0x00 reads 0x10 in PF0100 and PF0100A	Reading SILICON REV register at address 0x03 returns 0x21. DEVICEID register at address 0x00 reads 0x10 in PF0100 and PF0100A
VSNVS current limit	VSNVS current limit increased in the PF0100A	
OTP_FUSE_PORx register setting during OTP programming	In the PF0100, FUSE_POR1, FUSE_POR2, and FUSE_POR3 bits are XOR'ed into the FUSE_POR_XOR bit. The FUSE_POR_XOR bit has to be 1 for fuses to be loaded during startup. This can be achieved by setting any one or all of the FUSE_PORx bits during OTP programming.	In the PF0100A, the XOR function is removed. It is required to set FUSE_POR1, FUSE_POR2, and FUSE_POR3 bits during OTP programming.
Erratum ER19	Erratum ER19 applicable to PF0100. Applications expecting to operate in the conditions mentioned in ER19 need to implement an external workaround to overcome the problem. Refer to the product errata for details	Errata ER19 fixed in PF0100A. External workaround not required
Erratum ER20	Erratum ER20 applicable to PF0100	Errata ER20 fixed in PF0100A
Erratum ER22	Erratum ER22 applicable to PF0100	Errata ER22 fixed in PF0100A. Workaround not required

In addition to the version differences, Table 3 shows the differences on the test temperature rating for each version of PF0100 covered on this datasheet.

Table 3. Ambient temperature range

Device	Qualification tier	Ambient temperature range (T_{MIN} to T_{MAX})
MMPF0100	Consumer and Industrial	T_A = -40 °C to 85 °C
MMPF0100A	Consumer	T_A = -40 °C to 85 °C
MMPF0100AN	Extended Industrial	T_A = -40 °C to 105 °C

2 Internal block diagram

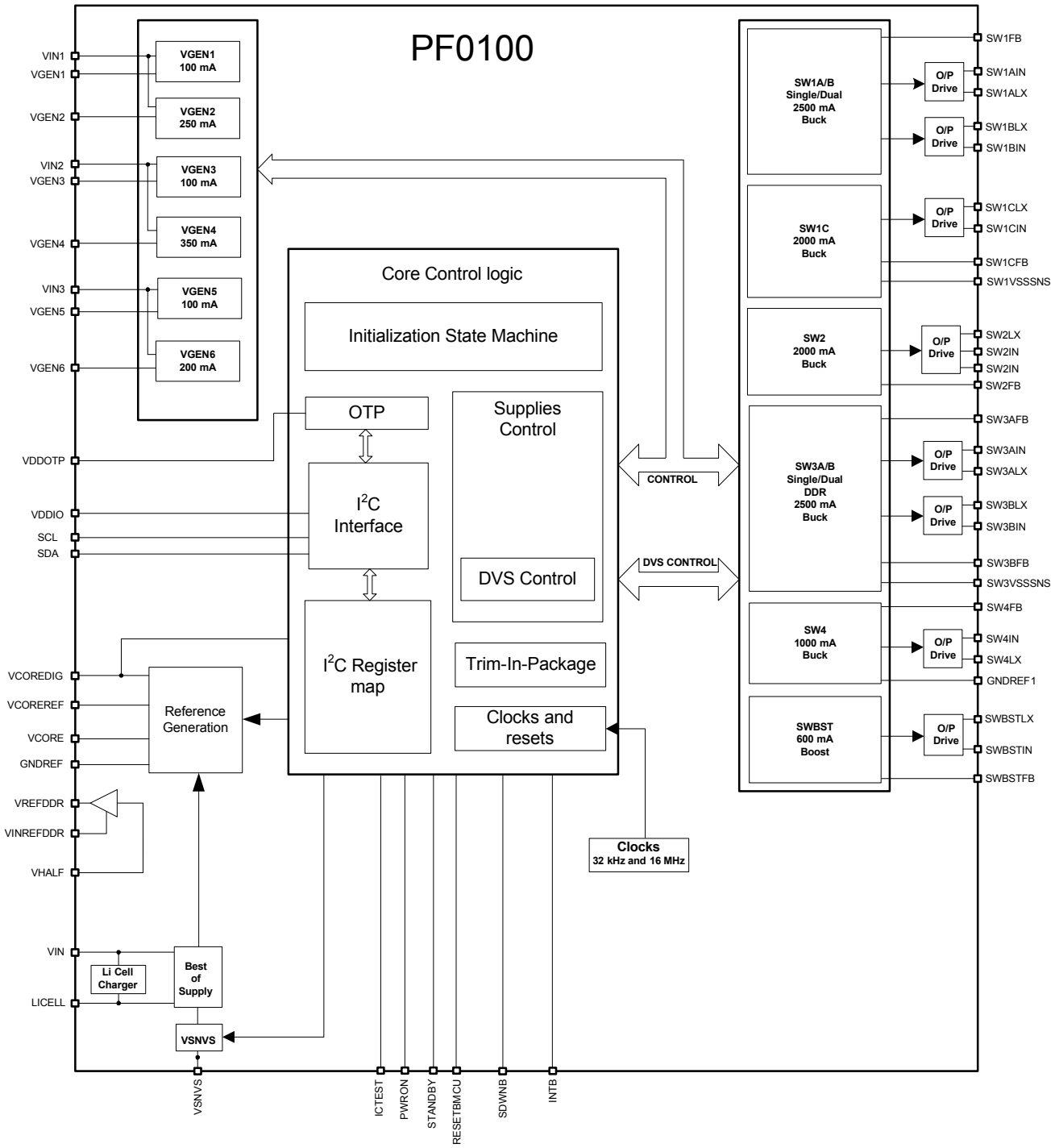


Figure 2. Simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

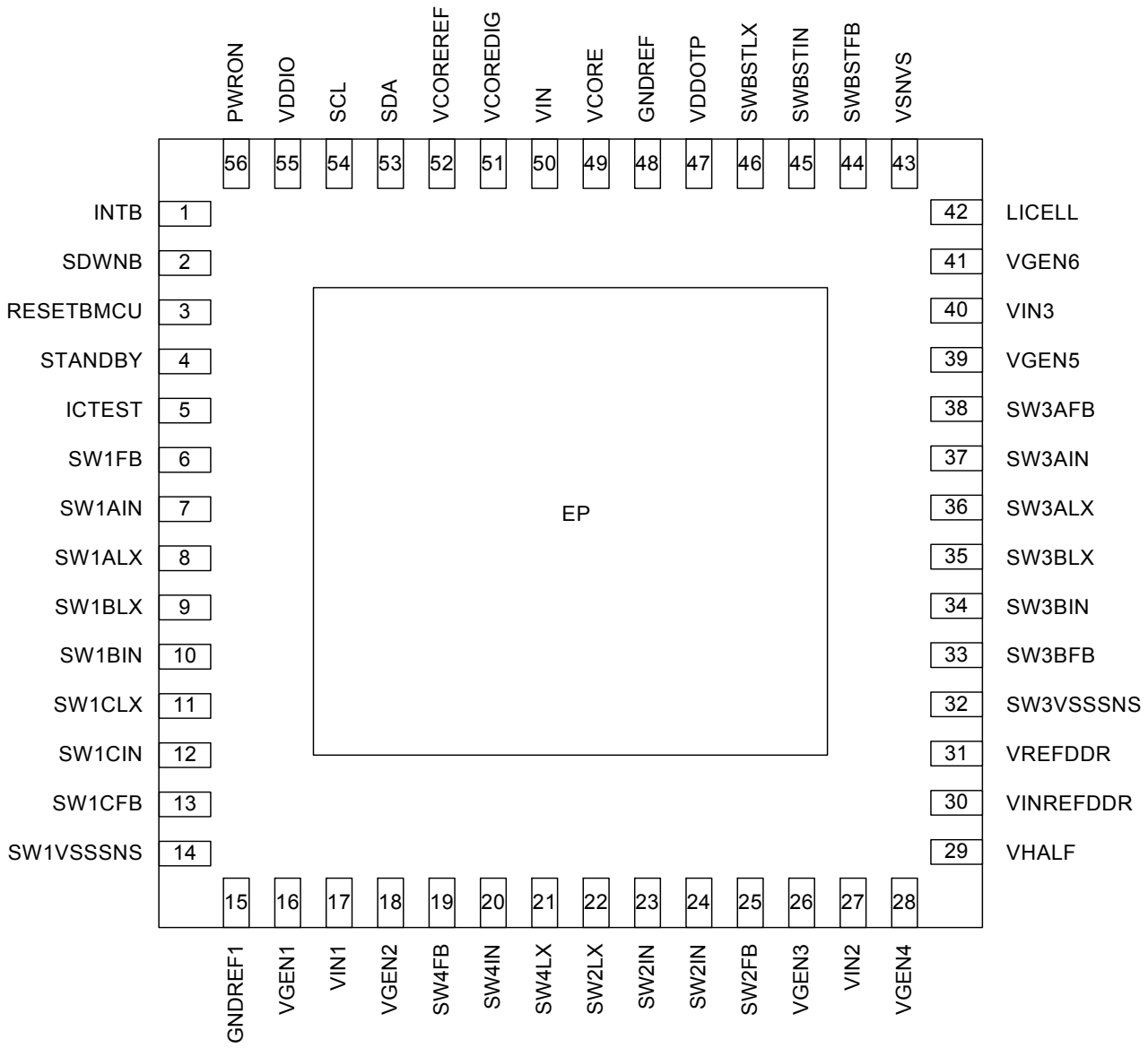


Figure 3. Pinout diagram

PF0100

3.2 Pin definitions

Table 4. PF0100 pin definitions

Pin number	Pin name	Pin function	Max rating	Type	Definition
1	INTB	O	3.6 V	Digital	Open drain interrupt signal to processor
2	SDWNB	O	3.6 V	Digital	Open drain signal to indicate an imminent system shutdown
3	RESETBMCU	O	3.6 V	Digital	Open drain reset output to processor. Alternatively can be used as a power good output.
4	STANDBY	I	3.6 V	Digital	Standby input signal from processor
5	ICTEST	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.
6	SW1FB (6)	I	3.6 V	Analog	Output voltage feedback for SW1A/B. Route this trace separately from the high current path and terminate at the output capacitance.
7	SW1AIN (6)	I	4.8 V	Analog	Input to SW1A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
8	SW1ALX (6)	O	4.8 V	Analog	Regulator 1A switch node connection
9	SW1BLX (6)	O	4.8 V	Analog	Regulator 1B switch node connection
10	SW1BIN (6)	I	4.8 V	Analog	Input to SW1B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
11	SW1CLX (6)	O	4.8 V	Analog	Regulator 1C switch node connection
12	SW1CIN (6)	I	4.8 V	Analog	Input to SW1C regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
13	SW1CFB (6)	I	3.6V	Analog	Output voltage feedback for SW1C. Route this trace separately from the high current path and terminate at the output capacitance.
14	SW1VSSSNS	GND	-	GND	Ground reference for regulators SW1ABC. It is connected externally to GNDREF through a board ground plane.
15	GNDREF1	GND	-	GND	Ground reference for regulators SW2 and SW4. It is connected externally to GNDREF, via board ground plane.
16	VGEN1	O	2.5 V	Analog	VGEN1 regulator output, Bypass with a 2.2 µF ceramic output capacitor.
17	VIN1	I	3.6 V	Analog	VGEN1, 2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
18	VGEN2	O	2.5 V	Analog	VGEN2 regulator output, Bypass with a 4.7 µF ceramic output capacitor.
19	SW4FB (6)	I	3.6 V	Analog	Output voltage feedback for SW4. Route this trace separately from the high current path and terminate at the output capacitance.
20	SW4IN (6)	I	4.8 V	Analog	Input to SW4 regulator. Bypass with at least a 4.7µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
21	SW4LX (6)	O	4.8 V	Analog	Regulator 4 switch node connection
22	SW2LX (6)	O	4.8 V	Analog	Regulator 2 switch node connection
23	SW2IN (6)	I	4.8 V	Analog	Input to SW2 regulator. Connect pin 23 together with pin 24 and bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to these pins as possible.
24	SW2IN (6)	I	4.8 V	Analog	
25	SW2FB (6)	I	3.6 V	Analog	Output voltage feedback for SW2. Route this trace separately from the high current path and terminate at the output capacitance.
26	VGEN3	O	3.6 V	Analog	VGEN3 regulator output. Bypass with a 2.2 µF ceramic output capacitor.
27	VIN2	I	3.6 V	Analog	VGEN3,4 input. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
28	VGEN4	O	3.6 V	Analog	VGEN4 regulator output, Bypass with a 4.7 µF ceramic output capacitor.

Table 4. PF0100 pin definitions (continued)

Pin number	Pin name	Pin function	Max rating	Type	Definition
29	VHALF	I	3.6 V	Analog	Half supply reference for VREFDDR
30	VINREFDDR	I	3.6 V	Analog	VREFDDR regulator input. Bypass with at least 1.0 µF decoupling capacitor as close to the pin as possible.
31	VREFDDR	O	3.6 V	Analog	VREFDDR regulator output
32	SW3VSSSNS	GND	-	GND	Ground reference for the SW3 regulator. Connect to GNDREF externally via the board ground plane.
33	SW3BFB (6)	I	3.6 V	Analog	Output voltage feedback for SW3B. Route this trace separately from the high current path and terminate at the output capacitance.
34	SW3BIN (6)	I	4.8 V	Analog	Input to SW3B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
35	SW3BLX (6)	O	4.8 V	Analog	Regulator 3B switch node connection
36	SW3ALX (6)	O	4.8 V	Analog	Regulator 3A switch node connection
37	SW3AIN (6)	I	4.8 V	Analog	Input to SW3A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
38	SW3AFB (6)	I	3.6 V	Analog	Output voltage feedback for SW3A. Route this trace separately from the high current path and terminate at the output capacitance.
39	VGEN5	O	3.6 V	Analog	VGEN5 regulator output. Bypass with a 2.2 µF ceramic output capacitor.
40	VIN3	I	4.8 V	Analog	VGEN5, 6 input. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
41	VGEN6	O	3.6 V	Analog	VGEN6 regulator output. By pass with a 2.2 µF ceramic output capacitor.
42	LICELL	I/O	3.6 V	Analog	Coin cell supply input/output
43	VSNVS	O	3.6 V	Analog	LDO or coin cell output to processor
44	SWBSTFB (6)	I	5.5 V	Analog	Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes.
45	SWBSTIN (6)	I	4.8 V	Analog	Input to SWBST regulator. Bypass with at least a 2.2 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
46	SWBSTLX (6)	O	7.5 V	Analog	SWBST switch node connection
47	VDDOTP	I	10 V(5)	Digital and Analog	Supply to program OTP fuses
48	GNDREF	GND	-	GND	Ground reference for the main band gap regulator.
49	VCORE	O	3.6 V	Analog	Analog Core supply
50	VIN	I	4.8 V	Analog	Main chip supply
51	VCOREDIG	O	1.5 V	Analog	Digital Core supply
52	VCOREREF	O	1.5 V	Analog	Main band gap reference
53	SDA	I/O	3.6 V	Digital	I^2C data line (Open drain)
54	SCL	I	3.6 V	Digital	I^2C clock
55	VDDIO	I	3.6 V	Analog	Supply for I^2C bus. Bypass with 0.1 µF ceramic capacitor
56	PWRON	I	3.6 V	Digital	Power On/off from processor
-	EP	GND	-	GND	Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation.

Notes

5. 10 V Maximum voltage rating during OTP fuse programming. 7.5 V Maximum DC voltage rated otherwise.
6. Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

4 General product characteristics

4.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
V_{IN}	Main input supply voltage	-0.3 to 4.8	V	
V_{DDOTP}	OTP programming input supply voltage	-0.3 to 10	V	
V_{LICELL}	Coin cell voltage	-0.3 to 3.6	V	
V_{ESD}	ESD ratings Human body model Charge device model	 ±2000 ±500	V	(7)

Notes

7. ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM), robotic (C_{ZAP} = 4.0 pF).

4.2 Thermal characteristics

Table 6. Thermal ratings

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal ratings					
T_A	Ambient operating temperature range • PF0100 • PF0100A • PF0100AN	 -40 -40 -40	 85 85 105	°C	
T_J	Operating junction temperature range	-40	125	°C	(8)
T_{ST}	Storage temperature range	-65	150	°C	
T_{PPRT}	Peak package reflow temperature	–	Note 10	°C	(9)(10)
QFN56 thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction to ambient • Natural convection • Four layer board (2s2p) • Eight layer board (2s6p)	 – –	 28 15	°C/W	(11)(12)(13)
$R_{\theta JMA}$	Junction to ambient (@200 ft/min) • Four layer board (2s2p)	 –	 22	°C/W	(11)(13)
$R_{\theta JB}$	Junction to board	–	10	°C/W	(14)
$R_{\Theta JCBOTTOM}$	Junction to case bottom	–	1.2	°C/W	(15)
ΨJT	Junction to package top • Natural convection	–	2.0	°C/W	(16)

Notes

8. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Table 7 for thermal protection features.
9. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
10. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
11. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
12. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
13. Per JEDEC JESD51-6 with the board horizontal.
14. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
15. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
16. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letter (Ψ) are not available, the thermal characterization parameter is written as Psi-JT.

4.2.1 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 6. To optimize the thermal management and to avoid overheating, the PF0100 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I are generated when the respective thresholds specified in Table 7 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the PF0100. This thermal protection acts above the thermal protection threshold listed in Table 7. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured so protection is not tripped under normal conditions.

Table 7. Thermal protection thresholds

Parameter	Min.	Typ.	Max.	Units
Thermal 110 °C Threshold (THERM110)	100	110	120	°C
Thermal 120 °C Threshold (THERM120)	110	120	130	°C
Thermal 125 °C Threshold (THERM125)	115	125	135	°C
Thermal 130 °C Threshold (THERM130)	120	130	140	°C
Thermal Warning Hysteresis	2.0	–	4.0	°C
Thermal Protection Threshold	130	140	150	°C

4.3 Electrical characteristics

4.3.1 General specifications

Table 8. General PMIC static characteristics.

T_{MIN} to T_{MAX} (See Table 3), VIN = 2.8 to 4.5 V, VDDIO = 1.7 to 3.6 V, typical external component values and full load current range, unless otherwise noted.

Pin name	Parameter	Load condition	Min.	Max.	Unit
PWRON	V_{IL}	–	0.0	0.2 * VSNVS	V
	V_{IH}	–	0.8 * VSNVS	3.6	V
RESETBMCU	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7* VIN	VIN	V
SCL	V_{IL}	–	0.0	0.2 * VDDIO	V
	V_{IH}	–	0.8 * VDDIO	3.6	V
SDA	V_{IL}	–	0.0	0.2 * VDDIO	V
	V_{IH}	–	0.8 * VDDIO	3.6	V
	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7*VDDIO	VDDIO	V
INTB	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7* VIN	VIN	V
SDWNB	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7* VIN	VIN	V
STANDBY	V_{IL}	–	0.0	0.2 * VSNVS	V
	V_{IH}	–	0.8 * VSNVS	3.6	V
VDDOTP	V_{IL}	–	0.0	0.3	V
	V_{IH}	–	1.1	1.7	V

4.3.2 Current consumption

Table 9. Current consumption summary

T_{MIN} to T_{MAX} (See Table 3), VIN = 3.6 V, VDDIO = 1.7 V to 3.6 V, LICELL = 1.8 V to 3.3 V, VSNVS = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, VDDIO = 3.3 V, LICELL = 3.0 V, VSNVS = 3.0 V and 25 °C, unless otherwise noted.

Mode	PF0100 conditions	System conditions	Typical	MAX	Unit	Notes
Coin Cell	VSNVS from LICELL All other blocks off VIN = 0.0 V VSNVSVOLT[2:0] = 110	No load on VSNVS	4.0	7.0	µA	(17),(19), (23)
Off MMPF0100	VSNVS from VIN or LICELL Wake-up from PWRON active 32 k RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	16	21	µA	(18),(19)
Off MMPF0100A	VSNVS from VIN or LICELL Wake-up from PWRON active 32 k RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	17	25	µA	(18),(19)
Sleep	VSNVS from VIN Wake-up from PWRON active Trimmed reference active SW3A/B PFM Trimmed 16 MHz RC off 32 k RC on VREFDDR disabled	No load on VSNVS. DDR memories in self refresh	122 122	220(22) 250(21)	µA	(19)
Standby MMPF0100	VSNVS from either VIN or LICELL SW1A/B combined in PFM SW1C in PFM SW2 in PFM SW3A/B combined in PFM SW4 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VGEN1-6 enabled VREFDDR enabled	No load on VSNVS. Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)	297 297	450 (20) 1000 (22)	µA	(19)
Standby MMPF0100A	VSNVS from either VIN or LICELL SW1A/B combined in PFM SW1C in PFM SW2 in PFM SW3A/B combined in PFM SW4 in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VGEN1-6 enabled VREFDDR enabled	No load on VSNVS. Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)	297 297	450 (22) 550(21)	µA	(19)

Notes

17. Refer to Figure 4 for coin cell mode characteristics over temperature.
18. When VIN is below the UVDET threshold, in the range of 1.8 V ≤ V_{IN} < 2.65 V, the quiescent current increases by 50 µA, typically.
19. For PFM operation, headroom should be 300 mV or greater.
20. From 0 °C to 85 °C
21. From -40 °C to 105 °C, applicable only to extended industrial parts.
22. From -40 °C to 85 °C, applicable to consumer, industrial and extended industrial part numbers.
23. Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due an internal path from RESETBMCU to V_{IN}. The additional current is < 30 µA with a pull up resistor of 100 kΩ. The i.MX 6x processors have an internal pull up from the POR_B pin to the VDD_SNVS_IN pin. For i.MX 6x applications, if additional current in the coin cell mode is not desired, use an external switch to disconnect the RESETBMCU path when V_{IN} is removed. For non-i.MX 6 applications, pull-up RESETBMCU to a rail off in the coin cell mode.

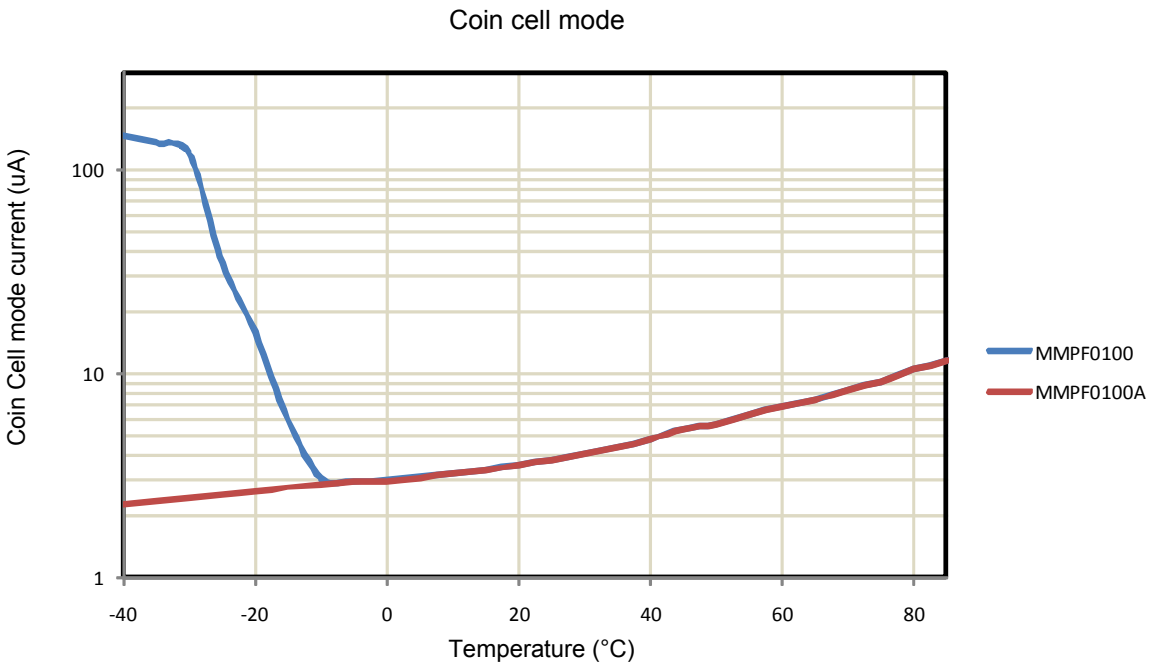


Figure 4. Coin cell mode current vs temperature

5 General description

The PF0100 is the power management integrated circuit (PMIC) designed primarily for use with NXP's i.MX 6 series of application processors.

5.1 Features

This section summarizes the PF0100 features.

- Input voltage range to PMIC: 2.8 V - 4.5 V
- Buck regulators
  - Four to six channel configurable
    - SW1A/B/C, 4.5 A (single); 0.3 V to 1.875 V
    - SW1A/B, 2.5 A (single/dual); SW1C 2.0 A (independent); 0.3 V to 1.875 V
    - SW2, 2.0 A; 0.4 V to 3.3 V (2.5 A; 1.2 V to 3.3 V [24])
    - SW3A/B, 2.5 A (single/dual); 0.4 V to 3.3 V
    - SW3A, 1.25 A (independent); SW3B, 1.25 A (independent); 0.4 V to 3.3 V
    - SW4, 1.0 A; 0.4 V to 3.3 V
    - SW4, VTT mode provide DDR termination at 50% of SW3A
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS
  - Programmable output voltage
  - Programmable current limit
  - Programmable soft start
  - Programmable PWM switching frequency
  - Programmable OCP with fault interrupt
- Boost regulator
  - SWBST, 5.0 V to 5.15 V, 0.6 A, OTG support
  - Modes: PFM and auto
  - OCP fault interrupt
- LDOs
  - Six user programable LDO
    - VGEN1, 0.80 V to 1.55 V, 100 mA
    - VGEN2, 0.80 V to 1.55 V, 250 mA
    - VGEN3, 1.8 V to 3.3 V, 100 mA
    - VGEN4, 1.8 V to 3.3 V, 350 mA
    - VGEN5, 1.8 V to 3.3 V, 100 mA
    - VGEN6, 1.8 V to 3.3 V, 200 mA
  - Soft start
  - LDO/switch supply
    - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 400 μA
- DDR memory reference voltage
  - VREFDDR, 0.6 V to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP(one time programmable) memory for device configuration
  - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I^2C interface
- User programmable standby, sleep, and off modes

Notes

24. SW2 capable of 2.5 A in NP, F9, and FA Industrial versions only (ANES suffix)

5.2 Functional block diagram

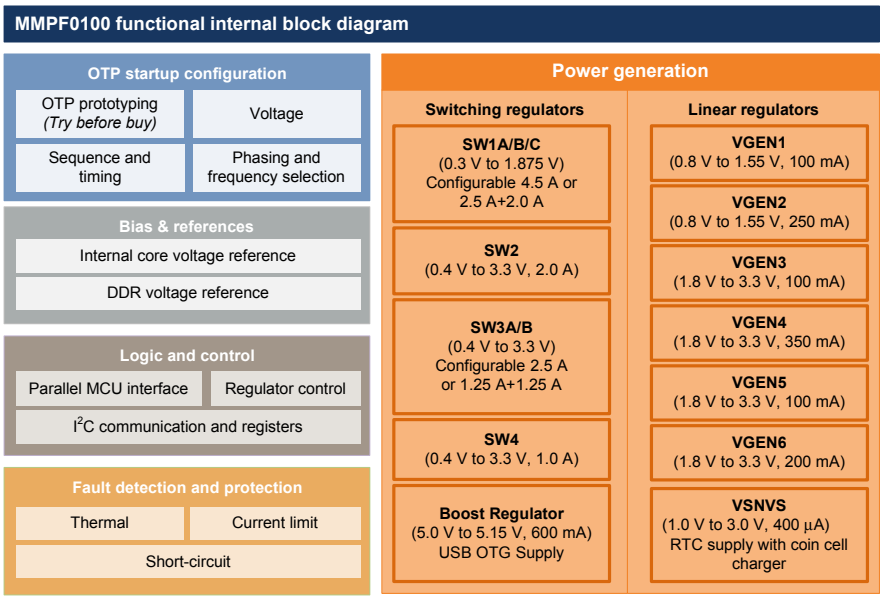


Figure 5. Functional block diagram

5.3 Functional description

5.3.1 Power generation

The PF0100 PMIC features four buck regulators (up to six independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltages for the application processor and peripheral devices.

The number of independent buck regulator outputs can be configured from four to six, thereby providing flexibility to operate with higher current capability, or to operate as independent outputs for applications requiring more voltage rails with lower current demands. Further, SW1 and SW3 regulators can be configured as single/dual phase and/or independent converters. One of the buck regulators, SW4, can also operate as a tracking regulator when used for memory termination. The buck regulators provide the supply to processor cores and to other low voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry.

Depending on the system power path configuration, the six general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operating with or without VTT termination. The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; VSNVS may be powered from VIN, or from a coin cell.

5.3.2 Control logic

The PF0100 PMIC is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Start-up sequence of the device is selected upon the initial OTP configuration explained in the Start-up section, or by configuring the “Try Before Buy” feature to test different power up sequences before choosing the final OTP configuration.

The PF0100 PMIC has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures supply of critical internal logic and other circuits from the coin cell in case of brief interruptions from the main battery. A charger for the coin cell is included as well.

5.3.2.1 Interface signals

5.3.2.1.1 PWRON

PWRON is an input signal to the IC generating a turn-on event. It can be configured to detect a level, or an edge using the PWRON_CFG bit. Refer to section 6.4.2.1 Turn on events, page 31 for more details.

5.3.2.1.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. Refer to the section 6.4.1.3 Standby mode, page 29 for more details.

Note: When operating the PMIC at VIN ≤ 2.85 V and VSNVS is programmed for a 3.0 V output, a coin cell must be present to provide VSNVS, or the PMIC does not reliably enter and exit the STANDBY mode.

5.3.2.1.3 RESETBMCU

RESETBMCU is an open drain, active low output configurable for two modes of operation. In its default mode, it is de-asserted 2.0 ms to 4.0 ms after the last regulator in the start-up sequence is enabled; refer to Figure 6 as an example. In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn-off event.

When configured for its fault mode, RESETBMCU is de-asserted after the start-up sequence is completed only if no faults occurred during start-up. At anytime, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted, LOW. The PF0100 is turned off if the fault persists for more than 100 ms typically. The PWRON signal restarts the part, though if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP_PG_EN of register OTP PWRGD EN to “1”. This register, 0xE8, is located on Table 137 of the register map. To test the fault mode, the bit may be set during TBB prototyping, or the mode may be permanently chosen by programming OTP fuses.

5.3.2.1.4 SDWNB

SDWNB is an open drain, active low output notifying the processor of an imminent PMIC shut down. It is asserted low for one 32 kHz clock cycle before powering down and is then de-asserted in the OFF state.

5.3.2.1.5 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

6 Functional block requirements and behaviors

6.1 Start-up

The PF0100 can be configured to start-up from either the internal OTP configuration, or with a hard-coded configuration built in to the device. The internal hard-coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kΩ resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP devices, selecting the OTP configuration causes the PF0100 to not start-up. However, the PF0100 can be controlled through the I^2C port for prototyping and programming. Once programmed, the NP device starts up with the customer programmed configuration.

6.1.1 Device start-up configuration

Table 10 shows the default configuration, which can be accessed on all devices as described previously, as well as the pre-programmed OTP configurations.

Table 10. Start-up configuration

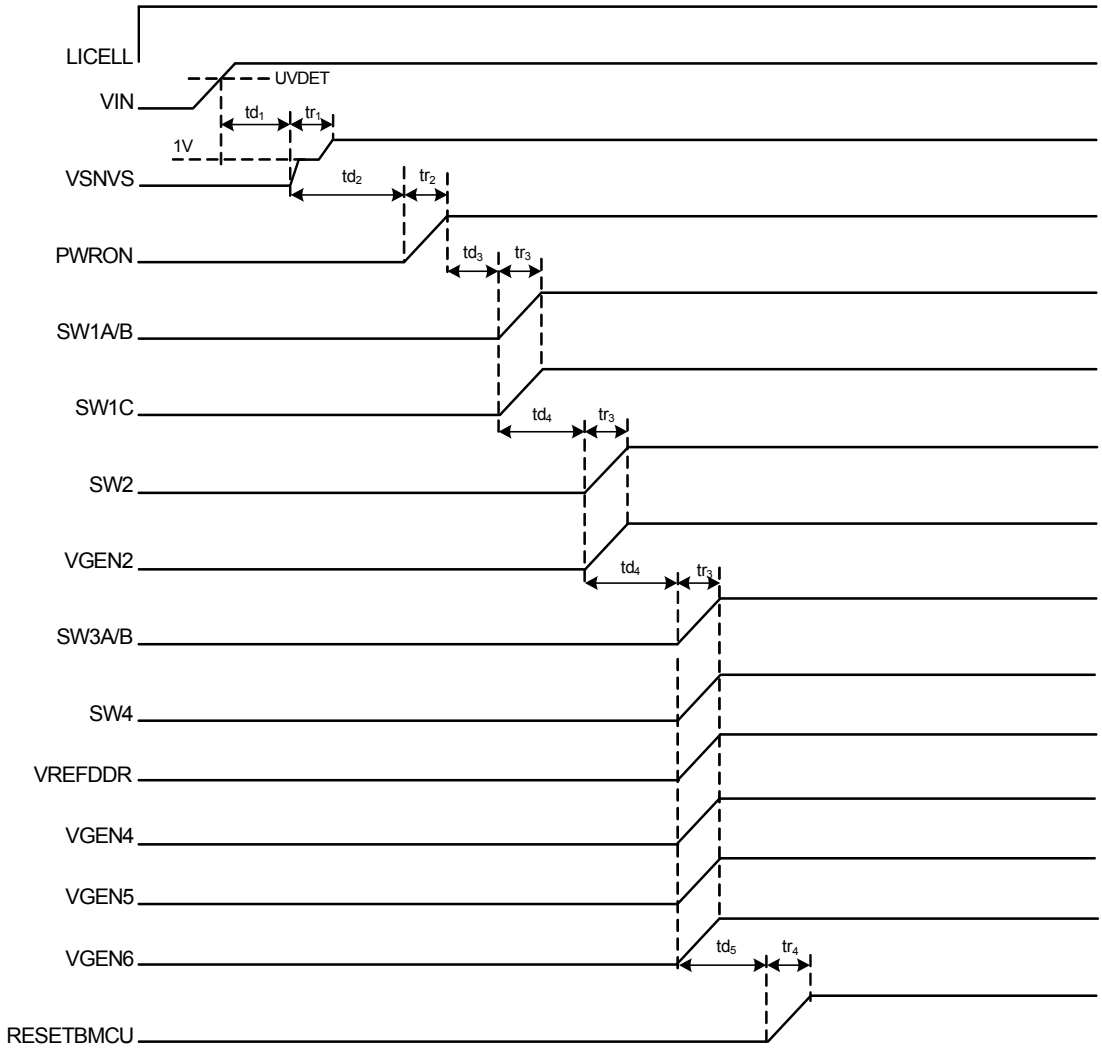
Registers	Default configuration	Pre-programmed OTP configuration										
	All devices	F0	F1[25]	F2[25]	F3	F4	F6	F9	FA	FB	FC	FD
Default I^2C Address	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08
VSNVS_VOLT	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
SW1AB_VOLT	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.2 V
SW1AB_SEQ	1	1	1	1	2	2	2	5	5	2	2	2
SW1C_VOLT	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V	1.2 V
SW1C_SEQ	1	2	1	1	2	2	2	5	5	2	2	2
SW2_VOLT	3.0 V	3.3 V	3.15 V	3.15 V	3.15 V	3.15 V	3.3 V	1.375 V	1.375 V	3.3 V	3.3 V	3.15 V
SW2_SEQ	2	5	2	2	1	1	4	5	5	6	5	1
SW3A_VOLT	1.5 V	1.5 V	1.2 V	1.5 V	1.2 V	1.5 V	1.35 V	1.350 V	1.5 V	1.2 V	1.35 V	1.2 V
SW3A_SEQ	3	3	4	4	4	4	3	6	6	4	3	4
SW3B_VOLT	1.5 V	1.5 V	1.2 V	1.5 V	1.2 V	1.5 V	1.35 V	1.350 V	1.5 V	1.2 V	1.35 V	1.2 V
SW3B_SEQ	3	3	4	4	4	4	3	6	6	4	3	4
SW4_VOLT	1.8 V	3.15 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.825 V	1.825 V	1.8 V	3.15 V	1.8 V
SW4_SEQ	3	6	3	3	3	3	4	7	7	3	6	3
SWBST_VOLT	-	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V
SWBST_SEQ	-	13	6	6	6	6	Off	10	10	Off	13	6
VREFDDR_SEQ	3	3	4	4	4	4	3	6	6	4	3	4
VGEN1_VOLT	-	1.5 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.5 V	1.5 V	1.2 V
VGEN1_SEQ	-	9	4	4	4	4	5	-	-	3	9	-
VGEN2_VOLT	1.5 V	1.5 V	-	-	-	-	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V
VGEN2_SEQ	2	10	-	-	-	-	Off	8	8	Off	10	7
VGEN3_VOLT	-	2.5 V	-	-	-	-	2.8 V	1.8 V	1.8 V	2.5 V	2.5 V	1.8 V
VGEN3_SEQ	-	11	-	-	-	-	5	8	8	Off	11	7
VGEN4_VOLT	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	3.0 V	3.0 V	1.8 V	1.8V	1.8 V
VGEN4_SEQ	3	7	3	3	3	3	4	4	4	7	7	3
VGEN5_VOLT	2.5 V	2.8 V	2.5 V	2.5 V	2.5 V	2.5 V	3.3 V	2.5 V	2.5 V	2.8 V	2.8 V	2.5 V

Table 10. Start-up configuration (continued)

Registers	Default configuration	Pre-programmed OTP configuration										
	All devices	F0	F1[25]	F2[25]	F3	F4	F6	F9	FA	FB	FC	FD
VGEN5_SEQ	3	12	5	5	5	5	5	8	8	1	1	5
VGEN6_VOLT	2.8 V	3.3 V	-	-	-	-	3.0 V	2.8 V	2.8 V	3.3 V	3.3 V	2.8 V
VGEN6_SEQ	3	8	-	-	-	-	1	7	7	8	8	7
PU CONFIG, SEQ_CLK_SPEED	1.0 ms	2.0 ms	1.0 ms	1.0 ms	1.0 ms	1.0 ms	0.5 ms	0.5 ms	0.5 ms	2.0 ms	2.0 ms	1.0 ms
PU CONFIG, SWDVS_CLK	6.25 mV/µs	1.5625 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs	6.25 mV/µs	6.25 mV/µs	1.5625 mV/µs	1.5625 mV/µs	12.5 mV/µs
PU CONFIG, PWRON	Level sensitive											
SW1AB CONFIG	SW1AB Single Phase, SW1C Independent Mode, 2.0 MHz							SW1ABC Single Phase, 2.0 MHz		SW1AB Single Phase, SW1C Independent mode, 2.0 MHz		
SW1C CONFIG	2.0 MHz											
SW2 CONFIG	2.0 MHz											
SW3A CONFIG	SW3AB Single Phase, 2.0 MHz											
SW3B CONFIG	2.0 MHz											
SW4 CONFIG	No VTT, 2.0 MHz											
PG EN	RESETBMCU in default mode											

Notes

25. For designs using the i.MX 6SoloLite, it is recommended to use the F3 OTP option instead of the F1 OTP option and F4 OTP option instead of the F2 OTP option.



*VSNVS starts from 1.0 V if LICELL is valid before VIN.

Figure 6. Default start-up sequence

Table 11. Default start-up sequence timing

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{D1}	Turn-on delay of VSNVS	–	5.0	–	ms	(26)
t_{R1}	Rise time of VSNVS	–	3.0	–	ms	
t_{D2}	User determined delay	–	1.0	–	ms	
t_{R2}	Rise time of PWRON	–	(27)	–	ms	
t_{D3}	Turn-on delay of first regulator					
	• SEQ_CLK_SPEED[1:0] = 00	–	2.0	–	ms	
	• SEQ_CLK_SPEED[1:0] = 01	–	2.5	–		(28)
	• SEQ_CLK_SPEED[1:0] = 10	–	4.0	–		
	• SEQ_CLK_SPEED[1:0] = 11	–	7.0	–		
t_{R3}	Rise time of regulators	–	0.2	–	ms	(29)

Table 11. Default start-up sequence timing (continued)

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{D4}	Delay between regulators					
	• SEQ_CLK_SPEED[1:0] = 00	–	0.5	–	ms	
	• SEQ_CLK_SPEED[1:0] = 01	–	1.0	–		
	• SEQ_CLK_SPEED[1:0] = 10	–	2.0	–		
	• SEQ_CLK_SPEED[1:0] = 11	–	4.0	–		
t_{R4}	Rise time of RESETBMCU	–	0.2	–	ms	
t_{D5}	Turn-on delay of RESETBMCU	–	2.0	–	ms	

Notes
26. Assumes LICELL voltage is valid before VIN is applied. If LICELL is not valid before VIN is applied then VSNVS turn-on delay may extend to a maximum of 24 ms.
27. Depends on the external signal driving PWRON.
28. Default configuration.
29. Rise time is a function of slew rate of regulators and nominal voltage selected.

6.1.2 One time programmability (OTP)

OTP allows the programming of start-up configurations for a variety of applications. Before permanently programming the IC by programming fuses, a configuration may be prototyped by using the “Try Before Buy” (TBB) feature. Further, an error correction code(ECC) algorithm is available to correct a single bit error and to detect multiple bit errors when fuses are programmed.

The parameters which can be configured by OTP are listed below.

- General: I^2C slave address, PWRON pin configuration, start-up sequence and timing
- Buck regulators: Output voltage, dual/single phase or independent mode configuration, switching frequency, and soft start ramp rate
- Boost regulator and LDOs: Output voltage

NOTE: When prototyping or programming fuses, the user must ensure register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the start-up sequence.

6.1.2.1 Start-up sequence and timing

Each regulator has 5-bit allocated to program its start-up time slot from a turn on event; therefore, each can be placed from position one to thirty-one in the start-up sequence. The all zeros code indicates a regulator is not part of the start-up sequence and remains off. See Table 12. The delay between each position is equal; however, four delay options are available. See Table 13. The start-up sequence terminates at the last programmed regulator.

Table 12. Start-up sequence

SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0]	Sequence
00000	Off
00001	SEQ_CLK_SPEED[1:0] * 1
00010	SEQ_CLK_SPEED[1:0] * 2
*	*
*	*
*	*
*	*
11111	SEQ_CLK_SPEED[1:0] * 31

Table 13. Start-up sequence clock speed

SEQ_CLK_SPEED[1:0]	Time (µs)
00	500
01	1000
10	2000
11	4000

6.1.2.2 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON_CFG = 0), or as an edge sensitive input (PWRON_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into sleep mode. As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters sleep mode.

Table 14. PWRON configuration

PWRON_CFG	Mode
0	PWRON pin HIGH = ON PWRON pin LOW = OFF or Sleep mode
1	PWRON pin pulled LOW momentarily = ON PWRON pin LOW for 4.0 seconds = OFF or Sleep mode

6.1.2.3 I^2C address configuration

The I^2C device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the I^2C address to avoid bus conflicts. Address bit, I2C_SLV_ADDR[3] in OTP_I2C_ADDR register is hard coded to “1” while the lower three LSBs of the I^2C address (I2C_SLV_ADDR[2:0]) are programmable as shown in Table 15.

Table 15. I^2C address configuration

I2C_SLV_ADDR[3] hard coded	I2C_SLV_ADDR[2:0]	I^2C device address (Hex)
1	000	0x08
1	001	0x09
1	010	0x0A
1	011	0x0B

Table 15. I^2C address configuration (continued)

I2C_SLV_ADDR[3] hard coded	I2C_SLV_ADDR[2:0]	I^2C device address (Hex)
1	100	0x0C
1	101	0x0D
1	110	0x0E
1	111	0x0F

6.1.2.4 Soft start ramp rate

The start-up ramp rate or soft start ramp rate can be chosen from the same options as shown in 6.4.4.2.1 Dynamic voltage scaling, page 35.

6.1.3 OTP prototyping

Before permanently programming fuses, it is possible to test the desired configuration by using the “Try Before Buy” feature. With this feature, the configuration is loaded from the OTP registers. These registers merely serve as temporary storage for the values to be written to the fuses, for the values read from the fuses, or for the values read from the default configuration. To avoid confusion, these registers are referred to as the TBBOTP registers. The portion of the register map concerned with OTP is shown in Table 137 and Table 138.

The contents of the TBBOTP registers are initialized to zero when a valid V_{IN} is first applied. The values loaded into the TBBOTP registers depend on the setting of the VDDOTP pin and on the value of the TBB_POR and FUSE_POR_XOR bits. Refer to Table 16.

- If VDDOTP = VCOREDIG (1.5 V), the values are loaded from the default configuration.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 1, the values are loaded from the fuses. In the MMPF0100, FUSE_POR1, FUSE_POR2, and FUSE_POR3 are XOR’ed into the FUSE_POR_XOR bit. The FUSE_POR_XOR has to be 1 for fuses to be loaded. This can be achieved by setting any one or all of the FUSE_PORx bits. In the MMPF0100A, the XOR function is removed. It is required to set all of the FUSE_PORx bits to be able to load the fuses.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 0, the TBBOTP registers remain initialized at zero.

The initial value of TBB_POR is always “0”; only when VDDOTP = 0.0 V and TBB_POR is set to “1” are the values from the TBBOTP registers maintained and not loaded from a different source.

The contents of the TBBOTP registers are modified by I^2C. To communicate with I^2C, VIN must be valid and VDDIO, to which SDA and SCL are pulled up, must be powered by a 1.7 V to 3.6 V supply. VIN, or the coin cell voltage must be valid to maintain the contents of the registers. To power on with the contents of the TBBOTP registers, the following conditions must exist; VIN is valid, VDDOTP = 0.0 V, TBB_POR = 1 and there is a valid turn-on event. Refer to the application note AN4536 for an example of prototyping.

6.1.4 Reading OTP fuses

As described in the previous section, the contents of the fuses are loaded to the TBBOTP registers when the following conditions are met; VIN is valid, VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 1. If ECC were enabled at the time the fuses were programmed, the error corrected values can be loaded into the TBBOTP registers if desired. Once the fuses are loaded and a turn-on event occurs, the PMIC powers on with the configuration programmed in the fuses. For more details on reading the OTP fuses, see application note AN4536.

6.1.5 Programming OTP fuses

The parameters which can be programmed are shown in the TBBOTP registers in Table 137. Extended page 1, page 111 of the register map. The PF0100 offers ECC, the control registers for which functions are located in Extended Page 2 of the register map. There are ten banks of twenty-six fuses each which can be programmed. Programming the fuses requires an 8.25 V, 100 mA supply powering the VDDOTP pin, bypassed with 10 to 20 μF of capacitance. For more details on programming the OTP fuses, see application note AN4536.

Table 16. Source of start-up sequence

VDDOTP(V)	TBB_POR	FUSE_POR_XOR	Start-up sequence
0	0	0	None
0	0	1	OTP fuses
0	1	x	TBBOTP registers
1.5	x	x	Factory defined

6.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within -8.0/+8.0%. The 32 kHz untrimmed clock is only used in the following conditions:

- VIN < UVDET
- All regulators are in sleep mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, VIN > UVDET
- PWRON_CFG = 1, for power button debounce timing

In addition, when the 16 MHz is active in the ON mode, the debounce times in Table 27 are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock.

Table 17. 16 MHz clock specifications

T_{MIN} to T_{MAX} (See Table 3), V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
$V_{IN16MHz}$	Operating voltage from VIN	2.8	–	4.5	V	
f_{16MHZ}	16 MHz clock frequency	14.7	16	17.2	MHz	
f_{2MHZ}	2.0 MHz clock frequency	1.84	–	2.15	MHz	(30)

Notes

30. 2.0 MHz clock is derived from the 16 MHz clock.

6.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency. Contact your NXP representative for detailed information on this feature.

6.3 Bias and references block description

6.3.1 Internal core voltage references

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. The bandgap and the rest of the core circuitry are supplied from VCORE. The performance of the regulators is directly dependent on the performance of the bandgap. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell. Table 18 shows the main characteristics of the core circuitry.

Table 18. Core voltages electrical specifications[32]

T_{MIN} to T_{MAX} (See Table 3), V_{IN} = 2.8 V to 4.5 V, LICELL = 1.8 V to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
VCOREDIG (digital core supply)						
$V_{COREDIG}$	Output voltage • ON mode • Coin cell mode and OFF	 – –	 1.5 1.3	 – –	V	(31) —
VCORE (analog core supply)						
V_{CORE}	Output voltage • ON mode and charging • OFF and coin cell mode	 – –	 2.775 0.0	 – –	V	(31) —
VCOREREF (bandgap / regulator reference)						
$V_{COREREF}$	Output voltage	–	1.2	–	V	(31)
$V_{COREREFACC}$	Absolute accuracy	–	0.5	–	%	
$V_{COREREFTACC}$	Temperature drift	–	0.25	–	%	

Notes

31. 3.0 V < V_{IN} < 4.5 V, no external loading on VCOREDIG, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.
32. For information only.

6.3.1.1 External components

Table 19. External components for core voltages

Regulator	Capacitor value (µF)
VCOREDIG	1.0
VCORE	1.0
VCOREREF	0.22

6.3.2 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. Its typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

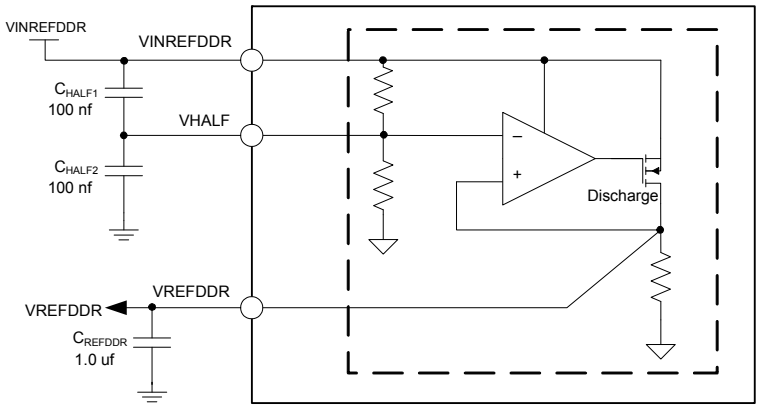


Figure 7. VREFDDR block diagram