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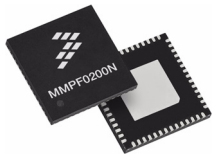
12 channel configurable power management integrated circuit

PF0200

POWER MANAGEMENT

The PF0200 Power Management Integrated Circuit (PMIC) provides a highly programmable/ configurable architecture, with fully integrated power devices and minimal external components. With up to four buck converters, one boost regulator, six linear regulators, RTC supply, and coin-cell charger, the PF0200 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications. With on-chip One Time Programmable (OTP) memory, the PF0200 is available in pre-programmed standard versions, or non-programmed to support custom programming. The PF0200 is especially suited to the i.MX 6SoloLite, i.MX 6Solo and i.MX 6DualLite versions of the i.MX 6 family of devices and is supported by full system level reference designs, and pre-programmed versions of the device. This device is powered by SMARTMOS technology.

EP SUFFIX (E-TYPE)
56 QFN 8X8
98ASA00405D



ES SUFFIX (WF-TYPE)
56 QFN 8X8
98ASA00589D

Features:

- Three to four buck converters, depending on configuration
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (One Time Programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- I^2C control
- Individually programmable ON, OFF, and Standby modes

Applications

- Tablets
- IPTV
- Industrial Control
- Medical monitoring
- Home automation/ alarm/ energy management

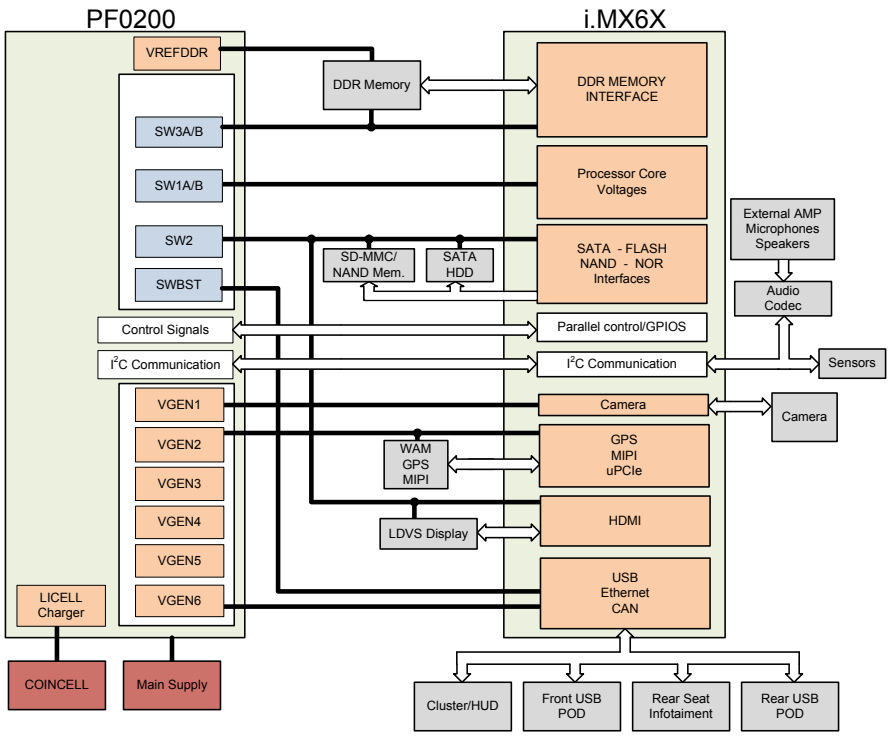


Figure 1. Simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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1 Orderable parts

The PF0200 is available with both pre-programmed and non-programmed OTP memory configurations. The non-programmed device uses “NP” as the programming code. The pre-programmed devices are identified using the program codes from Table 1, which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in Table 8. Contact your NXP representative for more details.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Programming	Reference designs	Qualification tier	Notes
MMPF0200NPAEP	-40 to 85 °C	56 QFN 8x8 mm - 0.5 mm pitch E-Type QFN (full lead)	NP	N/A	Consumer	(2)(1)
MMPF0200F0AEP			F0	N/A		(2)(1)
MMPF0200F3AEP			F3	N/A		(2)(1)
MMPF0200F4AEP			F4	N/A		(2)(1)
MMPF0200F6AEP			F6	i.MX6SX-SDB		(2)(1)
MMPF0200F0ANES	-40 to 105 °C	56 QFN 8x8 mm - 0.5 mm pitch WF-Type QFN (wettable flank)	F0	N/A	Extended Industrial	(2)(1)
MMPF0200F3ANES			F3	N/A		(2)(1)
MMPF0200F4ANES			F4	N/A		(2)(1)

Notes
1. For Tape and Reel add an R2 suffix to the part number.
2. For programming details see Table 8.

2 Internal block diagram

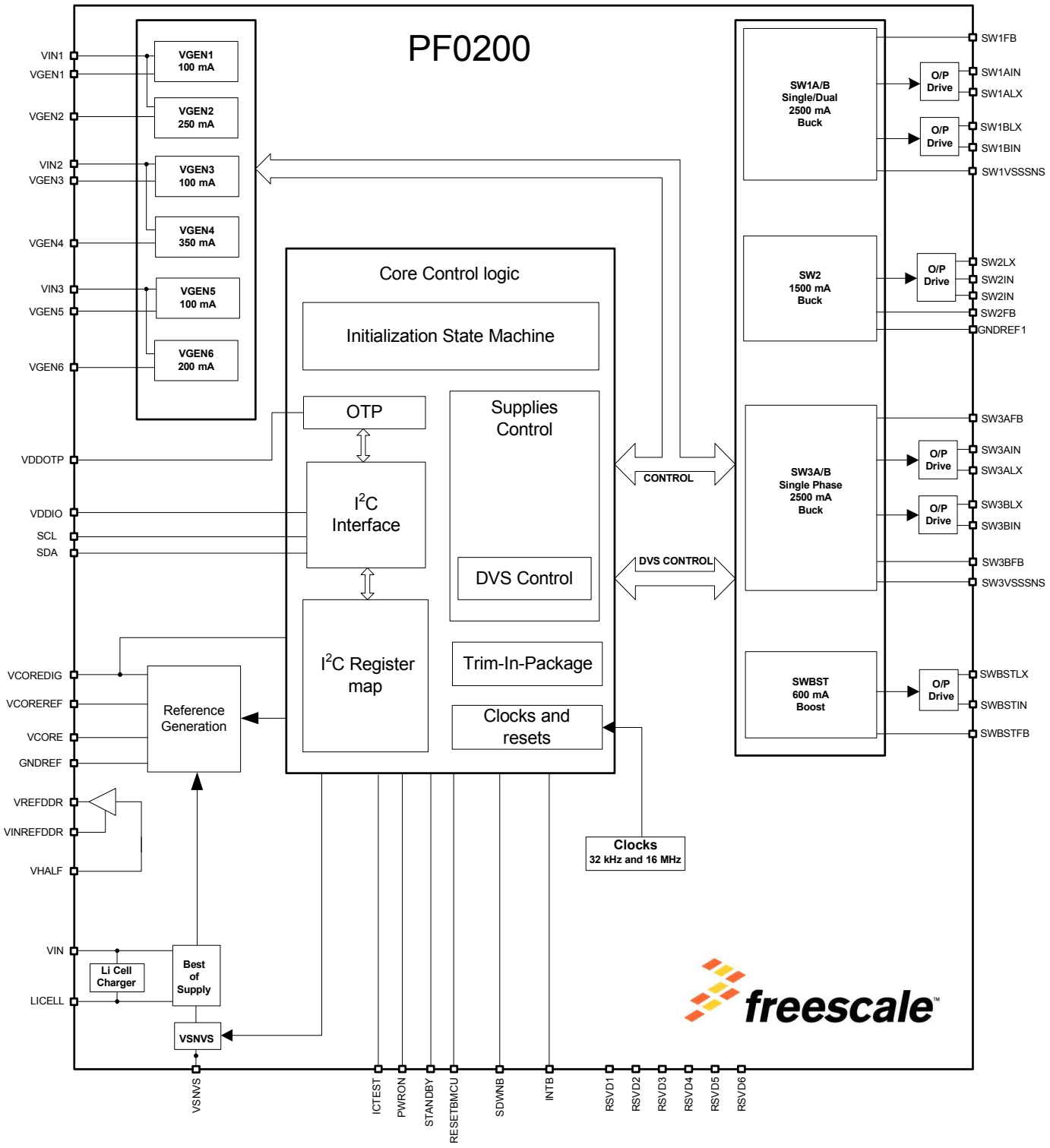


Figure 2. PF0200 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

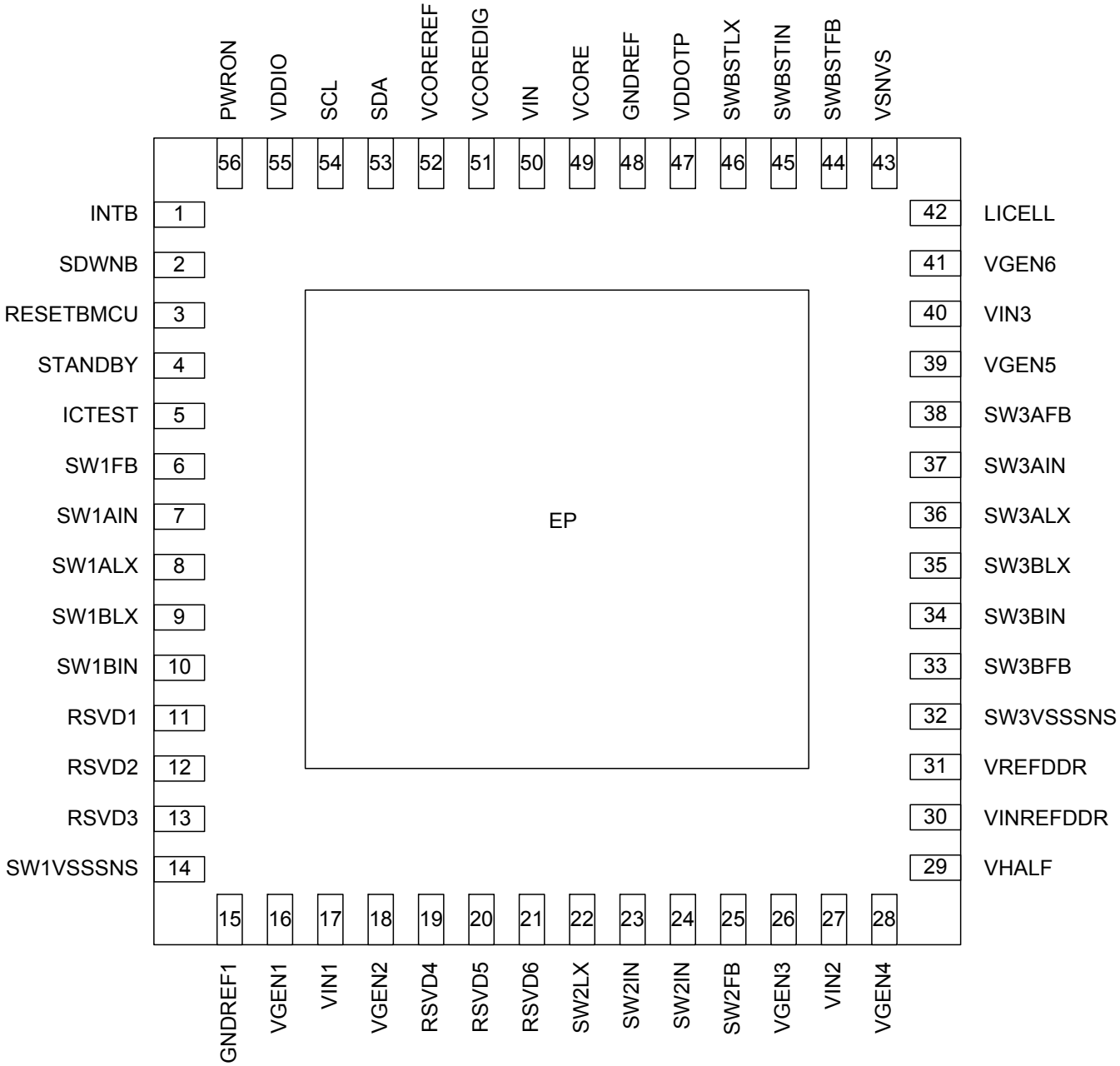


Figure 3. Pinout diagram

3.2 Pin definitions

Table 2. PF0200 pin definitions

Pin number	Pin name	Pin function	Max rating	Type	Definition
1	INTB	O	3.6 V	Digital	Open drain interrupt signal to processor
2	SDWNB	O	3.6 V	Digital	Open drain signal to indicate an imminent system shutdown
3	RESETBMCU	O	3.6 V	Digital	Open drain reset output to processor. Alternatively can be used as a Power Good output.
4	STANDBY	I	3.6 V	Digital	Standby input signal from processor
5	ICTEST	I	7.5 V	Digital/ Analog	Reserved pin. Connect to GND in application.
6	SW1FB (4)	I	3.6 V	Analog	Output voltage feedback for SW1A/B. Route this trace separately from the high-current path and terminate at the output capacitance.
7	SW1AIN (4)	I	4.8 V	Analog	Input to SW1A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
8	SW1ALX (4)	O	4.8 V	Analog	Regulator 1A switch node connection
9	SW1BLX (4)	O	4.8 V	Analog	Regulator 1B switch node connection
10	SW1BIN (4)	I	4.8 V	Analog	Input to SW1B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
11	RSVD1	-	-	Reserved	Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected.
12	RSVD2	-	-	Reserved	Reserved for pin to pin compatibility. Connect this pin to VIN.
13	RSVD3	-	-	Reserved	Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected.
14	SW1VSSSNS	GND	-	GND	Ground reference for regulator SW1AB. It is connected externally to GNDREF through a board ground plane.
15	GNDREF1	GND	-	GND	Ground reference for regulator SW2. It is connected externally to GNDREF, via board ground plane.
16	VGEN1	O	2.5 V	Analog	VGEN1 regulator output, Bypass with a 2.2 µF ceramic output capacitor.
17	VIN1	I	3.6 V	Analog	VGEN1, 2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
18	VGEN2	O	2.5 V	Analog	VGEN2 regulator output, Bypass with a 4.7 µF ceramic output capacitor.
19	RSVD4	-	-	Reserved	Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected.
20	RSVD5	-	-	Reserved	Reserved for pin to pin compatibility. Connect this pin to VIN
21	RSVD6	-	-	Reserved	Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected.
22	SW2LX (4)	O	4.8 V	Analog	Regulator 2 switch node connection
23	SW2IN (4)	I	4.8 V	Analog	Input to SW2 regulator. Connect pin 23 together with pin 24 and bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to these pins as possible.
24	SW2IN (4)	I	4.8 V	Analog	
25	SW2FB (4)	I	3.6 V	Analog	Output voltage feedback for SW2. Route this trace separately from the high-current path and terminate at the output capacitance.
26	VGEN3	O	3.6 V	Analog	VGEN3 regulator output. Bypass with a 2.2 µF ceramic output capacitor.
27	VIN2	I	3.6 V	Analog	VGEN3,4 input. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.

Table 2. PF0200 pin definitions (continued)

Pin number	Pin name	Pin function	Max rating	Type	Definition
28	VGEN4	O	3.6 V	Analog	VGEN4 regulator output, Bypass with a 4.7 µF ceramic output capacitor.
29	VHALF	I	3.6 V	Analog	Half supply reference for VREFDDR
30	VINREFDDR	I	3.6 V	Analog	VREFDDR regulator input. Bypass with at least 1.0 µF decoupling capacitor as close to the pin as possible.
31	VREFDDR	O	3.6 V	Analog	VREFDDR regulator output
32	SW3VSSSNS	GND	-	GND	Ground reference for the SW3 regulator. Connect to GNDREF externally via the board ground plane.
33	SW3BFB (4)	I	3.6 V	Analog	Output voltage feedback for SW3B. Route this trace separately from the high-current path and terminate at the output capacitance.
34	SW3BIN (4)	I	4.8 V	Analog	Input to SW3B regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
35	SW3BLX (4)	O	4.8 V	Analog	Regulator 3B switch node connection
36	SW3ALX (4)	O	4.8 V	Analog	Regulator 3A switch node connection
37	SW3AIN (4)	I	4.8 V	Analog	Input to SW3A regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
38	SW3AFB (4)	I	3.6 V	Analog	Output voltage feedback for SW3A. Route this trace separately from the high-current path and terminate at the output capacitance.
39	VGEN5	O	3.6 V	Analog	VGEN5 regulator output. Bypass with a 2.2 µF ceramic output capacitor.
40	VIN3	I	4.8 V	Analog	VGEN5, 6 input. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible.
41	VGEN6	O	3.6 V	Analog	VGEN6 regulator output. By pass with a 2.2 µF ceramic output capacitor.
42	LICELL	I/O	3.6 V	Analog	Coin cell supply input/output
43	VSNVS	O	3.6 V	Analog	LDO or coin cell output to processor
44	SWBSTFB (4)	I	5.5 V	Analog	Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes.
45	SWBSTIN (4)	I	4.8 V	Analog	Input to SWBST regulator. Bypass with at least a 2.2 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible.
46	SWBSTLX (4)	O	7.5 V	Analog	SWBST switch node connection
47	VDDOTP	I	10 V (3)	Digital & Analog	Supply to program OTP fuses
48	GNDREF	GND	-	GND	Ground reference for the main band gap regulator.
49	VCORE	O	3.6 V	Analog	Analog Core supply
50	VIN	I	4.8 V	Analog	Main chip supply
51	VCOREDIG	O	1.5 V	Analog	Digital Core supply
52	VCOREREF	O	1.5 V	Analog	Main band gap reference
53	SDA	I/O	3.6 V	Digital	I^2C data line (Open drain)
54	SCL	I	3.6 V	Digital	I^2C clock
55	VDDIO	I	3.6 V	Analog	Supply for I^2C bus. Bypass with 0.1 µF decoupling capacitor as close to the pin as possible.
56	PWRON	I	3.6 V	Digital	Power On/off from processor

Table 2. PF0200 pin definitions (continued)

Pin number	Pin name	Pin function	Max rating	Type	Definition
-	EP	GND	-	GND	Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation.

Notes

3. 10 V Maximum voltage rating during OTP fuse programming. 7.5 V Maximum DC voltage rated otherwise.
4. Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

4 General product characteristics

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Symbol	Description	Value	Unit	Notes
Electrical ratings				
V_{IN}	Main input supply voltage	-0.3 to 4.8	V	
V_{DDOTP}	OTP programming input supply voltage	-0.3 to 10	V	
V_{LICELL}	Coin cell voltage	-0.3 to 3.6	V	
V_{ESD}	ESD Ratings Human Body Model Charge Device Model	 ±2000 ±500	V	(5)

Notes

5. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).

4.2 Thermal characteristics

Table 4. Thermal ratings

Symbol	Description (rating)	Min.	Max.	Unit	
Thermal ratings					
T_A	Ambient Operating Temperature Range PF0200A PF0200AN	 -40 -40	 85 105	°C	
T_J	Operating Junction Temperature Range	-40	125	°C	(6)
T_{ST}	Storage Temperature Range	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature	–	Note 8	°C	(7)(8)
QFN56 Thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction to Ambient Natural Convection Four layer board (2s2p) Eight layer board (2s6p)	 – –	 28 15	°C/W	(9)(10)(11)
$R_{\theta JMA}$	Junction to Ambient (@200 ft/min) Four layer board (2s2p)	 –	 22	°C/W	(9)(11)
$R_{\theta JB}$	Junction to Board	–	10	°C/W	(12)
$R_{\Theta JCBOTTOM}$	Junction to Case Bottom	–	1.2	°C/W	(13)
ΨJT	Junction to Package Top Natural Convection	–	2.0	°C/W	(14)

Notes

6. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Table 5 for thermal protection features.
7. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
8. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.
9. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
10. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
11. Per JEDEC JESD51-6 with the board horizontal.
12. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
13. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
14. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.2.1 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the PF0200 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I will be generated when the respective thresholds specified in Table 5 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry will shut down the PF0200. This thermal protection will act above the thermal protection threshold listed in Table 5. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

Table 5. Thermal protection thresholds

Parameter	Min.	Typ.	Max.	Units	Notes
Thermal 110 °C Threshold (THERM110)	100	110	120	°C	
Thermal 120 °C Threshold (THERM120)	110	120	130	°C	
Thermal 125 °C Threshold (THERM125)	115	125	135	°C	
Thermal 130 °C Threshold (THERM130)	120	130	140	°C	
Thermal Warning Hysteresis	2.0	–	4.0	°C	
Thermal Protection Threshold	130	140	150	°C	

4.3 Electrical characteristics

4.3.1 General specifications

Table 6. General PMIC static characteristics

Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, VIN = 2.8 to 4.5 V, VDDIO = 1.7 to 3.6 V, typical external component values and full load current range, unless otherwise noted.

Pin name	Parameter	Load condition	Min.	Max.	Unit
PWRON	V_{IL}	–	0.0	0.2 * V_{SNVS}	V
	V_{IH}	–	0.8 * V_{SNVS}	3.6	V
RESETBMCU	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7* V_{IN}	VIN	V
SCL	V_{IL}	–	0.0	0.2 * V_{DDIO}	V
	V_{IH}	–	0.8 * V_{DDIO}	3.6	V
SDA	V_{IL}	–	0.0	0.2 * V_{DDIO}	V
	V_{IH}	–	0.8 * V_{DDIO}	3.6	V
	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7*V_{DDIO}	V_{DDIO}	V
INTB	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7* V_{IN}	V_{IN}	V
SDWNB	V_{OL}	-2.0 mA	0.0	0.4	V
	V_{OH}	Open Drain	0.7* V_{IN}	V_{IN}	V
STANDBY	V_{IL}	–	0.0	0.2 * V_{SNVS}	V
	V_{IH}	–	0.8 * V_{SNVS}	3.6	V
VDDOTP	V_{IL}	–	0.0	0.3	V
	V_{IH}	–	1.1	1.7	V

4.3.2 Current consumption

Table 7. Current consumption summary

Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, VIN = 3.6 V, VDDIO = 1.7 to 3.6 V, LICELL = 1.8 to 3.3 V, VSNVS = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, VDDIO = 3.3 V, LICELL = 3.0 V, VSNVS = 3.0 V and 25 °C, unless otherwise noted.

Mode	PF0200 conditions	System Conditions	Typ.	Max.	Unit
Coin Cell (15),(16),(19)	VSNVS from LICELL All other blocks off VIN = 0.0 V VSNVSVOLT[2:0] = 110	No load on VSNVS	4.0	7.0	µA
Off (15)(17)	VSNVS from VIN or LICELL Wake-up from PWRON active 32 k RC on All other blocks off VIN ≥ UVDET	No load on VSNVS, PMIC able to wake-up	17	25	µA
Sleep (18)	VSNVS from VIN Wake-up from PWRON active Trimmed reference active SW3A/B PFM Trimmed 16 MHz RC off 32 k RC on VREFDDR disabled	No load on VSNVS. DDR memories in self refresh	122 122	220(20) 250(21)	µA
Standby (18)	VSNVS from either VIN or LICELL SW1A/B combined in PFM SW2 in PFM SW3A/B combined in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VGEN1-6 enabled VREFDDR enabled	No load on VSNVS. Processor enabled in low power mode. All rails powered on except boost (load = 0 mA)	270 270	430(20) 525(21)	µA

Notes

15. At 25 °C only.
16. Refer to Figure 4 for Coin Cell mode characteristics over temperature.
17. When VIN is below the UVDET threshold, in the range of 1.8 V ≤ VIN < 2.65 V, the quiescent current increases by 50 µA, typically.
18. For PFM operation, headroom should be 300 mV or greater.
19. Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due an internal path from RESETBMCU to VIN. The additional current is <30 µA with a pull up resistor of 100 kΩ. The i.MX 6 processors have an internal pull-up from the POR_B pin to the VDD_SNVS_IN pin. If additional current in the coin cell mode is not desired for i.MX6 applications, use an external switch to disconnect the RESETBMCU path when VIN is removed. Pull-up RESETBMCU to a rail that is off in the coin cell mode, for non-i.MX 6 applications.
20. From -40 to 85 °C, Applicable to Consumer and Extended Industrial part numbers
21. From -40 to 105 °C, Applicable only to Extended Industrial parts

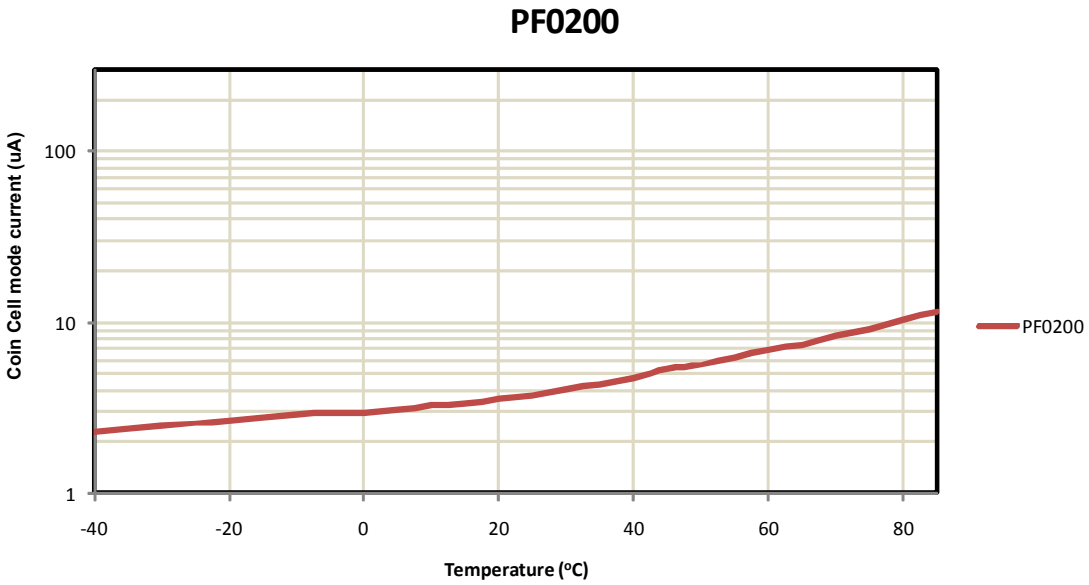


Figure 4. Coin cell mode current versus temperature

5 General description

The PF0200 is the Power Management Integrated Circuit (PMIC) designed primarily for use with NXP's i.MX 6 series of application processors.

5.1 Features

This section summarizes the PF0200 features.

- Input voltage range to PMIC: 2.8 - 4.5 V
- Buck regulators
  - Three to four channel configurable
    - SW1A/B, 2.5 A; 0.3 to 1.875 V
    - SW2, 1.5 A; 0.4 to 3.3 V
    - SW3A/B, 2.5 A (single phase); 0.4 to 3.3 V
    - SW3A, 1.25 A (independent); SW3B, 1.25 A (independent); 0.4 to 3.3 V
  - Dynamic voltage scaling
  - Modes: PWM, PFM, APS
  - Programmable output voltage
  - Programmable current limit
  - Programmable soft start
  - Programmable PWM switching frequency
  - Programmable OCP with fault interrupt
- Boost regulator
  - SWBST, 5.0 to 5.15 V, 0.6 A, OTG support
  - Modes: PFM and Auto
  - OCP fault interrupt
- LDOs
  - Six user programable LDO
    - VGEN1, 0.80 to 1.55 V, 100 mA
    - VGEN2, 0.80 to 1.55 V, 250 mA
    - VGEN3, 1.8 to 3.3 V, 100 mA
    - VGEN4, 1.8 to 3.3 V, 350 mA
    - VGEN5, 1.8 to 3.3 V, 100 mA
    - VGEN6, 1.8 to 3.3 V, 200 mA
  - Soft start
  - LDO/Switch supply
    - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 400 μA
- DDR memory reference voltage
  - VREFDDR, 0.6 to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP(One time programmable) memory for device configuration
  - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I^2C interface
- User programmable Standby, Sleep, and Off modes

5.2 Functional block diagram

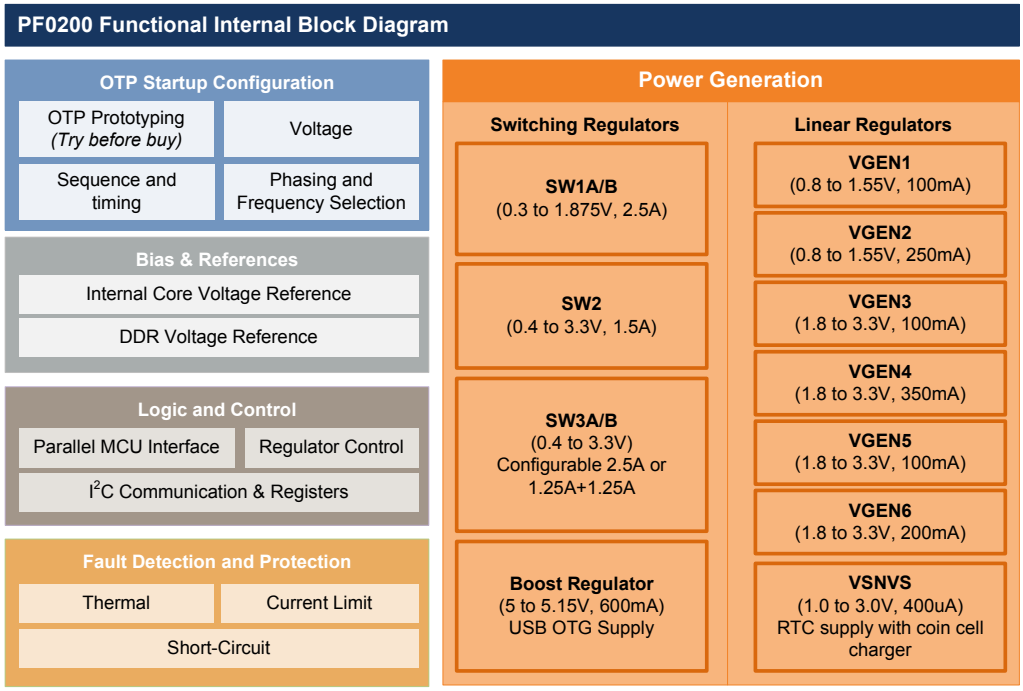


Figure 5. Functional block diagram

5.3 Functional description

5.3.1 Power generation

The PF0200 PMIC features three buck regulators (up to four independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltages for the application processor and peripheral devices.

The number of independent buck regulator outputs can be configured from three to four, thereby providing flexibility to operate with higher current capability, or to operate as independent outputs for applications requiring more voltage rails with lower current demands. The SW3 regulator can be configured as a single phase or with two independent outputs. The buck regulators provide the supply to processor cores and to other low-voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry.

Depending on the system power path configuration, the six general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operating with or without VTT termination. The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; VSNVS may be powered from VIN, or from a coin cell.

5.3.2 Control logic

The PF0200 PMIC is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Start-up sequence of the device is selected upon the initial OTP configuration explained in the Start-up section, or by configuring the “Try Before Buy” feature to test different power up sequences before choosing the final OTP configuration.

The PF0200 PMIC has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures supply of critical internal logic and other circuits from the coin cell in case of brief interruptions from the main battery. A charger for the coin cell is included as well.

5.3.2.1 Interface signals

PWRON

PWRON is an input signal to the IC that generates a turn-on event. It can be configured to detect a level, or an edge using the PWRON_CFG bit. Refer to section Turn on events for more details.

STANDBY

STANDBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. Refer to the section Standby mode for more details.

Note: When operating the PMIC at VIN ≤ 2.85 V and VSNVS is programmed for a 3.0 V output, a coin cell must be present to provide VSNVS, or the PMIC will not reliably enter and exit the STANDBY mode.

RESETBMCU

RESETBMCU is an open-drain, active low output configurable for two modes of operation. In its default mode, it is de-asserted 2.0 to 4.0 ms after the last regulator in the start-up sequence is enabled; refer to Figure 6 as an example. In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn-off event.

When configured for its fault mode, RESETBMCU is de-asserted after the start-up sequence is completed only if no faults occurred during start-up. At anytime, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted, LOW. The PF0200 is turned off if the fault persists for more than 100 ms typically. The PWRON signal restarts the part, though if the fault persists, the sequence described above will be repeated. To enter the fault mode, set bit OTP_PG_EN of register OTP PWRGD EN to “1”. This register, 0xE8, is located on Extended page 1 of the register map. To test the fault mode, the bit may be set during TBB prototyping, or the mode may be permanently chosen by programming OTP fuses.

SDWNB

SDWNB is an open-drain, active low output that notifies the processor of an imminent PMIC shutdown. It is asserted low for one 32 kHz clock cycle before powering down and is then de-asserted in the OFF state.

INTB

INTB is an open-drain, active low output. It is asserted when any fault occurs, provided that the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

6 Functional block requirements and behaviors

6.1 Start-up

The PF0200 can be configured to start-up from either the internal OTP configuration, or with a hard-coded configuration built into the device. The internal hard-coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kohm resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP devices, selecting the OTP configuration causes the PF0200 to not start-up. However, the PF0200 can be controlled through the I^2C port for prototyping and programming. Once programmed, the NP device will startup with the customer programmed configuration.

6.1.1 Device start-up configuration

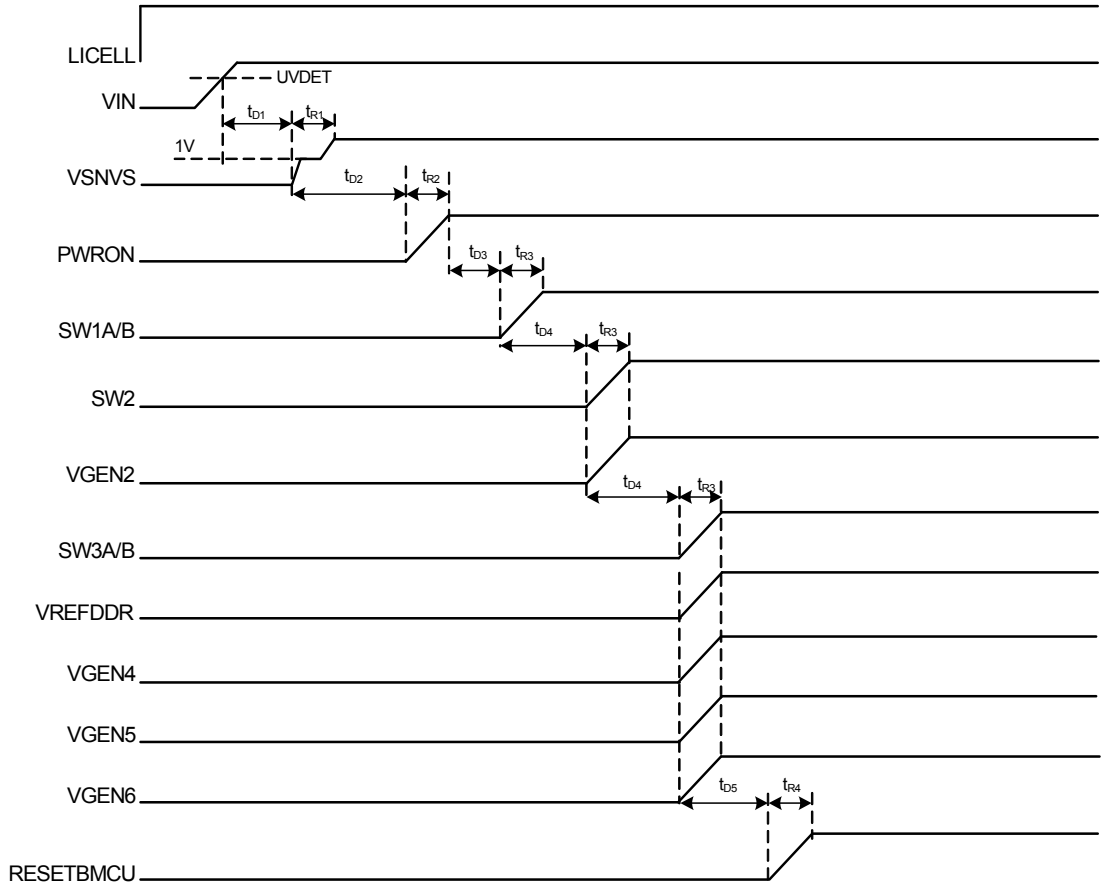
Table 8 shows the Default Configuration which can be accessed on all devices as described above, as well as the pre-programmed OTP configurations.

Table 8. Start-up configuration

Registers	Default configuration	Pre-programmed OTP configuration			
	All devices	F0	F3	F4	F6
Default I^2C Address	0x08	0x08	0x08	0x08	0x08
VSNVS_VOLT	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
SW1AB_VOLT	1.375 V	1.375 V	1.375 V	1.375 V	1.375 V
SW1AB_SEQ	1	1	2	2	2
SW2_VOLT	3.0 V	3.3 V	3.15 V	3.15 V	3.3 V
SW2_SEQ	2	5	1	1	4
SW3A_VOLT	1.5 V	1.5 V	1.2 V	1.5 V	1.35 V
SW3A_SEQ	3	3	4	4	3
SW3B_VOLT	1.5 V	1.5 V	1.2 V	1.5 V	1.35 V
SW3B_SEQ	3	3	4	4	3
SWBST_VOLT	-	5.0 V	5.0 V	5.0 V	5.0 V
SWBST_SEQ	-	13	6	6	-
VREFDDR_SEQ	3	3	4	4	3
VGEN1_VOLT	-	1.5 V	1.2 V	1.2 V	1.2 V
VGEN1_SEQ	-	9	4	4	5
VGEN2_VOLT	1.5 V	1.5 V	-	-	1.5 V
VGEN2_SEQ	2	10	-	-	-
VGEN3_VOLT	-	2.5 V	1.8 V	1.8 V	2.8 V
VGEN3_SEQ	-	11	3	3	5
VGEN4_VOLT	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
VGEN4_SEQ	3	7	3	3	4
VGEN5_VOLT	2.5 V	2.8 V	2.5 V	2.5 V	3.3 V
VGEN5_SEQ	3	12	5	5	5
VGEN6_VOLT	2.8 V	3.3 V	-	-	3.0 V
VGEN6_SEQ	3	8	-	-	1

Table 8. Start-up configuration (continued)

Registers	Default configuration	Pre-programmed OTP configuration			
	All devices	F0	F3	F4	F6
PU CONFIG, SEQ_CLK_SPEED	1.0 ms	2.0 ms	1.0 ms	1.0 ms	0.5 ms
PU CONFIG, SWDVS_CLK	6.25 mV/µs	1.5625 mV/µs	12.5 mV/µs	12.5 mV/µs	6.25 mV/µs
PU CONFIG, PWRON	Level sensitive				
SW1AB CONFIG	SW1AB Single Phase, 2.0 MHz				
SW2 CONFIG	2.0 MHz				
SW3A CONFIG	SW3AB Single Phase, 2.0 MHz				
SW3B CONFIG	2.0 MHz				
PG EN	RESETBMCU in Default Mode				



*VSNVS will start from 1.0 V if LICELL is valid before VIN.

Figure 6. Default start-up sequence

Table 9. Default start-up sequence timing

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{D1}	Turn-on delay of VSNVS	–	5.0	–	ms	(22)
t_{R1}	Rise time of VSNVS	–	3.0	–	ms	
t_{D2}	User determined delay	–	1.0	–	ms	
t_{R2}	Rise time of PWRON	–	(23)	–	ms	(23)
t_{D3}	Turn-on delay of first regulator					
	SEQ_CLK_SPEED[1:0] = 00	–	2.0	–	ms	
	SEQ_CLK_SPEED[1:0] = 01	–	2.5	–		(24)
	SEQ_CLK_SPEED[1:0] = 10	–	4.0	–		
	SEQ_CLK_SPEED[1:0] = 11	–	7.0	–		
t_{R3}	Rise time of regulators	–	0.2	–	ms	(25)
t_{D4}	Delay between regulators					
	SEQ_CLK_SPEED[1:0] = 00	–	0.5	–	ms	
	SEQ_CLK_SPEED[1:0] = 01	–	1.0	–		
	SEQ_CLK_SPEED[1:0] = 10	–	2.0	–		
	SEQ_CLK_SPEED[1:0] = 11	–	4.0	–		
t_{R4}	Rise time of RESETBMCU	–	0.2	–	ms	
t_{D5}	Turn-on delay of RESETBMCU	–	2.0	–	ms	

Notes

22. Assumes LICELL voltage is valid before VIN is applied. If LICELL is not valid before VIN is applied then VSNVS turn-on delay may extend to a maximum of 24 ms.
23. Depends on the external signal driving PWRON.
24. Default configuration.
25. Rise time is a function of slew rate of regulators and nominal voltage selected.

6.1.2 One time programmability (OTP)

OTP allows the programming of start-up configurations for a variety of applications. Before permanently programming the IC by programming fuses, a configuration may be prototyped by using the “Try Before Buy” (TBB) feature. An error correction code(ECC) algorithm is available to correct a single bit error and to detect multiple bit errors when fuses are programmed.

The parameters that can be configured by OTP are listed below.

- General: I^2C slave address, PWRON pin configuration, start-up sequence and timing
- Buck regulators: Output voltage, single phase or independent mode configuration, switching frequency, and soft start ramp rate
- Boost regulator and LDOs: Output voltage

NOTE: When prototyping or programming fuses, the user must ensure that register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it will be gated by the buck regulator in the start-up sequence.

6.1.2.1 Start-up sequence and timing

Each regulator has 5-bits allocated to program its start-up time slot from a turn on event; therefore, each can be placed from position one to thirty-one in the start-up sequence. The all zeros code indicates that a regulator is not part of the start-up sequence and will remain off. See Table 10. The delay between each position is equal; however, four delay options are available. See Table 11. The start-up sequence will terminate at the last programmed regulator.

Table 10. Start-up sequence

SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0]	Sequence
00000	Off
00001	SEQ_CLK_SPEED[1:0] * 1
00010	SEQ_CLK_SPEED[1:0] * 2
*	*
*	*
*	*
*	*
11111	SEQ_CLK_SPEED[1:0] * 31

Table 11. Start-up sequence clock speed

SEQ_CLK_SPEED[1:0]	Time (µs)
00	500
01	1000
10	2000
11	4000

6.1.2.2 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON_CFG = 0), or as an edge sensitive input (PWRON_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into Sleep mode. As an edge sensitive input, such as when connected to a mechanical switch, a falling edge will turn on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part will turn off or enter Sleep mode.

Table 12. PWRON configuration

PWRON_CFG	Mode
0	PWRON pin HIGH = ON PWRON pin LOW = OFF or Sleep mode
1	PWRON pin pulled LOW momentarily = ON PWRON pin LOW for 4.0 seconds = OFF or Sleep mode

6.1.2.3 I^2C address configuration

The I^2C device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the I^2C address to avoid bus conflicts. Address bit, I2C_SLV_ADDR[3] in OTP_I2C_ADDR register is hard coded to “1” while the lower three LSBs of the I^2C address (I2C_SLV_ADDR[2:0]) are programmable as shown in Table 13.

Table 13. I^2C address configuration

I2C_SLV_ADDR[3] hard coded	I2C_SLV_ADDR[2:0]	I^2C device address (Hex)
1	000	0x08
1	001	0x09
1	010	0x0A
1	011	0x0B

Table 13. I^2C address configuration (continued)

I2C_SLV_ADDR[3] hard coded	I2C_SLV_ADDR[2:0]	I^2C device address (Hex)
1	100	0x0C
1	101	0x0D
1	110	0x0E
1	111	0x0F

6.1.2.4 Soft start ramp rate

The start-up ramp rate or soft start ramp rate can be chosen from the same options as shown in Dynamic voltage scaling.

6.1.3 OTP prototyping

It is possible to test the desired configuration by using the “Try Before Buy” feature, before permanently programming fuses. The configuration is loaded from the OTP registers with this feature. These registers merely serve as temporary storage for the values to be written to the fuses, for the values read from the fuses, or for the values read from the default configuration. To avoid confusion, these registers will be referred to as the TBBOTP registers. The portion of the register map that concerns OTP is shown in Table 121 and Table 122.

The contents of the TBBOTP registers are initialized to zero when a valid VIN is first applied. The values that are then loaded into the TBBOTP registers depend on the setting of the VDDOTP pin and on the value of the TBB_POR and FUSE_POR_XOR bits. Refer to Table 14.

- If VDDOTP = VCOREDIG (1.5 V), the values are loaded from the default configuration.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 1, the values are loaded from the fuses. It is required to set all the FUSE_PORx bits to load the fuses.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 0, the TBBOTP registers remain initialized at zero.

The initial value of TBB_POR is always “0”; only when VDDOTP = 0.0 V and TBB_POR is set to “1” are the values from the TBBOTP registers maintained and not loaded from a different source.

The contents of the TBBOTP registers are modified by I^2C. To communicate with I^2C, VIN must be valid and VDDIO, to which SDA and SCL are pulled up, must be powered by a 1.7 to 3.6 V supply. V_{IN}, or the coin cell voltage must be valid to maintain the contents of the registers. To power on with the contents of the TBBOTP registers, the following conditions must exist; VIN is valid, VDDOTP = 0.0 V, TBB_POR = 1 and there is a valid turn-on event.

6.1.4 Reading OTP fuses

As described in the previous section, the contents of the fuses are loaded to the TBBOTP registers. When the following conditions are met; VIN is valid, VDDOTP = 0.0 V, TBB_POR = 0, and FUSE_POR_XOR = 1. If ECC is enabled at the time the fuses were programmed, the error corrected values can be loaded into the TBBOTP registers if desired. Once the fuses are loaded and a turn-on event occurs, the PMIC will power on with the configuration programmed in the fuses. Contact your NXP representative for more details on reading the OTP fuses.

6.1.5 Programming OTP fuses

The parameters that can be programmed are shown in the TBBOTP registers in the Extended page 1 of the register map. The PF0200 offers ECC, the control registers for which functions are located in Extended page 2 of the register map. There are ten banks of twenty-six fuses, each that can be programmed.

Table 14. Source of start-up sequence

VDDOTP(V)	TBB_POR	FUSE_POR_XOR	Start-up sequence
0	0	0	None
0	0	1	OTP fuses
0	1	x	TBBOTP registers
1.5	x	x	Factory defined

6.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within -8.0/+8.0%. The 32 kHz untrimmed clock is only used in the following conditions:

- VIN < UVDET
- All regulators are in SLEEP mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, VIN > UVDET
- PWRON_CFG = 1, for power button debounce timing

In addition, when the 16 MHz is active in the ON mode, the debounce times in Table 25 are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock.

Table 15. 16 MHz clock specifications

Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, V_{IN} = 2.8 to 4.5 V, LICELL = 1.8 to 3.3 V and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
$V_{IN16MHz}$	Operating Voltage From VIN	2.8	–	4.5	V	
f_{16MHZ}	16 MHz Clock Frequency	14.7	16	17.3	MHz	
f_{2MHZ}	2.0 MHz Clock Frequency	1.84	–	2.16	MHz	(26)

Notes

26. 2.0 MHz clock is derived from the 16 MHz clock.

6.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency.

6.3 Bias and references block description

6.3.1 Internal core voltage references

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. The bandgap and the rest of the core circuitry are supplied from VCORE. The performance of the regulators is directly dependent on the performance of the bandgap. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell. Table 16 shows the main characteristics of the core circuitry.

Table 16. Core voltages electrical specifications[28]

Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, V_{IN} = 2.8 to 4.5 V, LICELL = 1.8 to 3.3 V, and typical external component values. Typical values are characterized at V_{IN} = 3.6 V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

Symbol	Parameters	Min.	Typ.	Max.	Units	Notes
VCOREDIG (digital core supply)						
$V_{COREDIG}$	Output Voltage ON mode Coin cell mode and OFF	 – –	 1.5 1.3	 – –	V	(27)
VCORE (Analog core supply)						
V_{CORE}	Output Voltage ON mode and charging OFF and Coin cell mode	 – –	 2.775 0.0	 – –	V	(27)
VCOREREF (bandgap / regulator reference)						
$V_{COREREF}$	Output Voltage	–	1.2	–	V	(27)
$V_{COREREFACC}$	Absolute Accuracy	–	0.5	–	%	
$V_{COREREFTACC}$	Temperature Drift	–	0.25	–	%	

Notes

27. 3.0 V < V_{IN} < 4.5 V, no external loading on VCOREDIG, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.
28. For information only.

6.3.1.1 External components

Table 17. External components for core voltages

Regulator	Capacitor value (µF)
VCOREDIG	1.0
VCORE	1.0
VCOREREF	0.22

6.3.2 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. Its typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low-frequency pole. This divider then utilizes a voltage follower to drive the load.

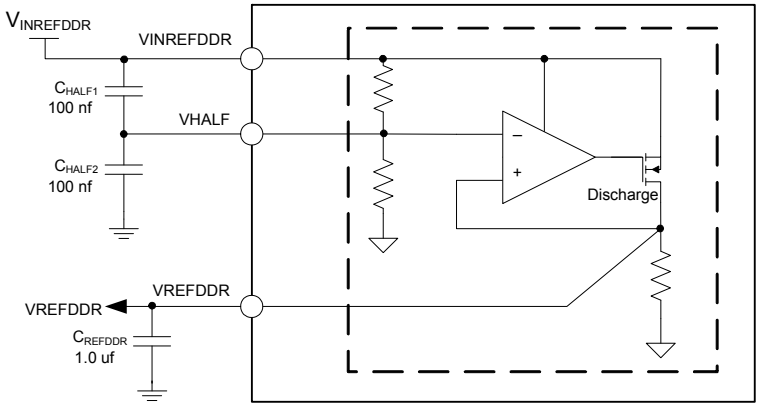


Figure 7. VREFDDR block diagram

6.3.2.1 VREFDDR control register

The VREFDDR voltage reference is controlled by a single bit in VREFDDCRTL register in Table 18.

Table 18. Register VREFDDCRTL - ADDR 0x6A

Name	Bit #	R/W	Default	Description
UNUSED	3:0	–	0x00	UNUSED
VREFDDREN	4	R/W	0x00	Enable or disables VREFDDR output voltage 0 = VREFDDR Disabled 1 = VREFDDR Enabled
UNUSED	7:5	–	0x00	UNUSED

External components

Table 19. VREFDDR external components[29]

Capacitor	Capacitance (µF)
VINREFDDR[30] to VHALF	0.1
VHALF to GND	0.1
VREFDDR	1.0

Notes
29. Use X5R or X7R capacitors.
30. VINREFDDR to GND, 1.0 µF minimum capacitance is provided by buck regulator output.

VREFDDR specifications

Table 20. VREFDDR electrical characteristics

Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VREFDDR						
$V_{INREFDDR}$	Operating Input Voltage Range	1.2	–	1.8	V	
I_{REFDDR}	Operating Load Current Range	0.0	–	10	mA	
$I_{REFDDRLIM}$	Current Limit I_{REFDDR} when V_{REFDDR} is forced to $V_{INREFDDR}$/4	10.5	15	25	mA	
$I_{REFDDRQ}$	Quiescent Current	–	8.0	–	µA	(31)
Active mode – DC						
V_{REFDDR}	Output Voltage 1.2 V < $V_{INREFDDR}$ < 1.8 V 0.0 mA < I_{REFDDR} < 10 mA	–	$V_{INREFDDR}$/2	–	V	
$V_{REFDDRTOL}$	Output Voltage Tolerance (TA = -40 to 85 °C) 1.2 V < $V_{INREFDDR}$ < 1.8 V 0.6 mA ≤ I_{REFDDR} ≤ 10 mA	–1.0	–	1.0	%	
$V_{REFDDRTOL}$	Output Voltage Tolerance (TA = -40 to 85 °C), applicable only to the extended Industrial version 1.2 V < $V_{INREFDDR}$ < 1.8 V 0.6 mA ≤ I_{REFDDR} ≤ 10 mA	–1.20	–	1.2	%	
$V_{REFDDRLOR}$	Load Regulation 1.0 mA < I_{REFDDR} < 10 mA 1.2 V < $V_{INREFDDR}$ < 1.8 V	–	0.40	–	mV/mA	

Table 20. VREFDDR electrical characteristics (continued)

Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V and typical external component values, unless otherwise noted. Typical values are characterized at V_{IN} = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.5 V, and 25 °C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Active mode – AC						
$t_{ONREFDDR}$	Turn-on Time Enable to 90% of end value $V_{INREFDDR}$ = 1.2 V, 1.8 V I_{REFDDR} = 0.0 mA	–	–	100	µs	
$t_{OFFREFDDR}$	Turn-off Time Disable to 10% of initial value $V_{INREFDDR}$ = 1.2 V, 1.8 V I_{REFDDR} = 0.0 mA	–	–	10	ms	
$V_{REFDDROSH}$	Start-up Overshoot $V_{INREFDDR}$ = 1.2 V, 1.8 V I_{REFDDR} = 0.0 mA	–	1.0	6.0	%	
$V_{REFDDRTLR}$	Transient Load Response $V_{INREFDDR}$ = 1.2 V, 1.8 V	–	5.0	–	mV	

Notes

31. When VREFDDR is off there is a quiescent current of 1.5 µA typical.

6.4 Power generation

6.4.1 Modes of operation

The operation of the PF0200 can be reduced to five states, or modes: ON, OFF, Sleep, Standby, and Coin Cell. Figure 8 shows the state diagram of the PF0200, along with the conditions to enter and exit from each state.