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□ MN101C77 Series

Type	MN101C77A	MN101C77C	MN101C77D	MN101C77F	MN101CF77G
Internal ROM type	Mask ROM				FLASH
ROM (byte)	32K	48K	64K	96K	128K
RAM (byte)	1.5K	3K	6K		
Package (Lead-free)	LQFP064-P-1414	LQFP064-P-1414, TQFP064-P-1010C	LQFP064-P-1414		LQFP064-P-1414, TQFP064-P-1010C
Minimum Instruction Execution Time	<p>[Standard] 0.1 μs (at 2.5 V to 3.6 V, 20 MHz)* 0.2 μs (at 2.1 V to 3.6 V, 10 MHz)* 0.5 μs (at 1.8 V to 3.6 V, 4 MHz)* 62.5 μs (at 1.8 V to 3.6 V, 32 kHz)*</p> <p>[Double speed] 0.119 μs (at 2.5 V to 3.6 V, 8.39 MHz)*</p> <p>*: The operation guarantee range for flash memory built-in type is 2.7 V to 3.6 V.</p>				

■ Interrupts

RESET. Watchdog. External 0 to 4. Timer 0. Timer 1. Timer 4 to 6. Timer 7 (2 systems). Time base. Serial 0 reception. Serial 0 transmission. Serial 1 reception. Serial 1 transmission. Serial 3. Serial 4. Automatic transfer finish. A/D conversion finish. Key interrupts (8 lines)

■ Timer Counter

8-bit timer × 5

Timer 0Square-wave/8-bit PWM output. Event count. Remote control carrier output. Pulse width measurement

Timer 1Square-wave output. Event count. Synchronous output event

Timer 4Square-wave/8-bit PWM output. Event count. Pulse width measurement. Serial 1 baud rate timer

Timer 5Square-wave/8-bit PWM output. Event count. Pulse width measurement. Serial 0 baud rate timer

Timer 68-bit freerun timer

Timer 0, 1 can be cascade-connected

16-bit timer × 1

Timer 7Square-wave/16-bit PWM output (cycle/duty continuous variable). Event count. Synchronous output event. Pulse width measurement. Input capture

Time base timer: One-minute count setting

Watchdog timer × 1

■ Serial interface

Synchronous type/UART (full-duplex) × 2: Serial 0, 1

Synchronous type/Single-master I²C × 1: Serial 3

I²C slave × 1: Serial 4

Serial 4.....I²C high-speed transfer mode. 7-bit/10-bit address setting. General call

■ DMA controller

Maximum transfer cycles: 255

Starting factor: External request. Various types of interrupt. Software

Transfer mode: 1-byte transfer. Word transfer. Burst transfer

■ I/O Pins

I/O 53 : Common use. Specified pull-up resistor available. Input/output selectable (bit unit)

■ A/D converter

10-bit × 7 channels (with S/H)

■ D/A converter

8-bit × 2 channels (Serves as AD pin, as well)

■ Special Ports

Buzzer output. Remote control carrier output. High-current drive port

■ ROM Correction

Correcting address designation: Up to 3 addresses possible

MN101C77A, MN101C77C, MN101C77D, MN101C77F, MN101CF77G □

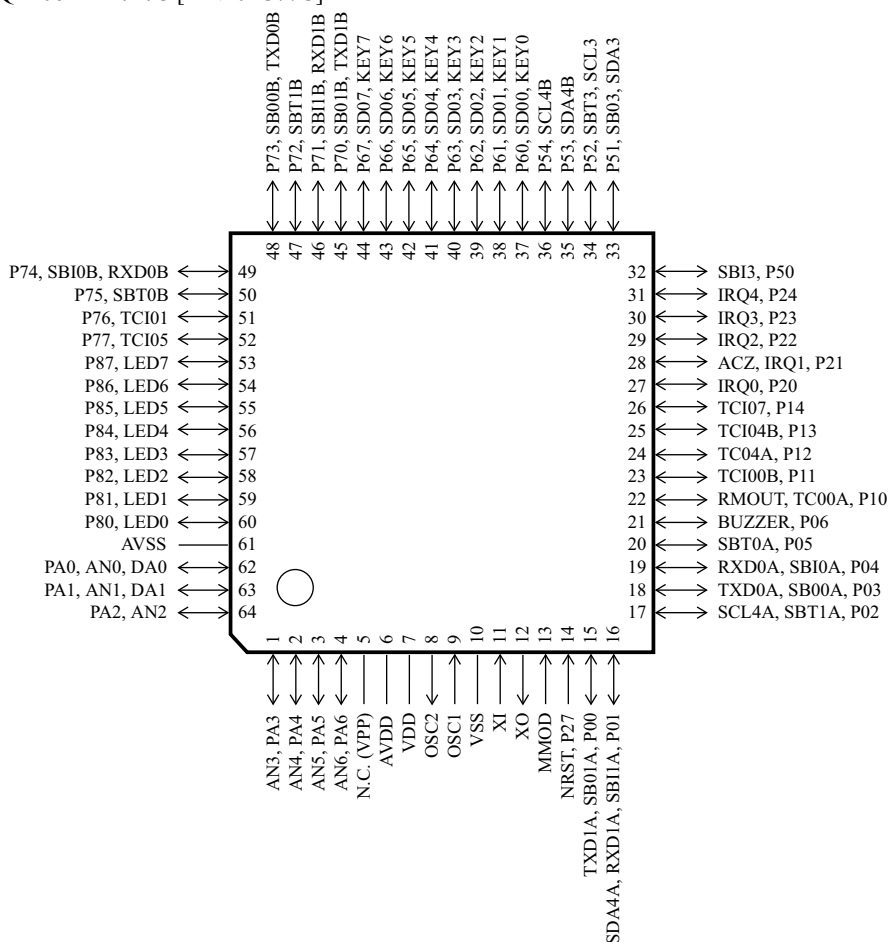
Electrical Characteristics (Supply current)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 20 MHz (fs = fosc/2). VDD = 3.3 V		6	12	mA
	IDD2	fosc = 8.39 MHz (fs = fosc/2). VDD = 3.3 V		3	6	mA
	IDD3	fx = 32.768 kHz (fs = fx/2). VDD = 3.3 V			40	μA
Supply current at HALT	IDD4	fx = 32.768 kHz. VDD = 3.3 V. Ta = 25 °C		5	10	μA
	IDD5	fx = 32.768 kHz. VDD = 3.3 V			40	μA
Supply current at STOP	IDD6	VDD = 3.3 V. Ta = 25 °C			2	μA
	IDD7	VDD = 3.3 V. Ta = 85 °C			30	μA

Ta = -40 °C to +85 °C. VDD = 1.8 V to 3.6 V. VSS = 0 V

Pin Assignment

LQFP064-P-1414, TQFP064-P-1010C [MN101C77C]



Note) Pin 5 serves as the VPP pin in the MN101CF77G, and cannot be used as a user pin.

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