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Evaluation board circuit diagram and implementation < MN63Y1210A >

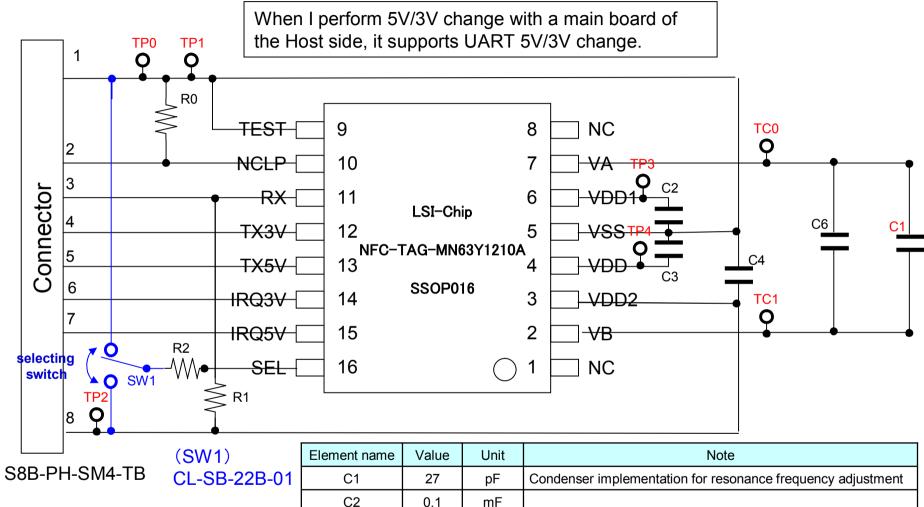
Ver 1.1

2013/10/21

Automotive & Industrial Systems Company Panasonic Corporation

2 Connection diagram of the evaluation board

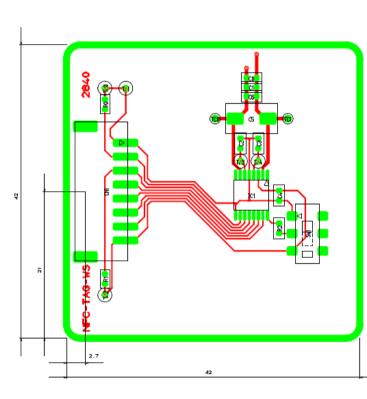
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1	C1	27	pF	Condenser implementation for resonance frequency adjustment
	C2	0.1	mF	
	C3	0.01	mF	
	C4	0.1	mF	
	C6	330	pF	Condenser implementation for resonance frequency adjustment
	R0、R1	100	kΩ	It is for reference board alone evaluations
	R2	0	Ω	

Pattern drawing and part list of Evaluation board 3

Parts list



Pattern drawing

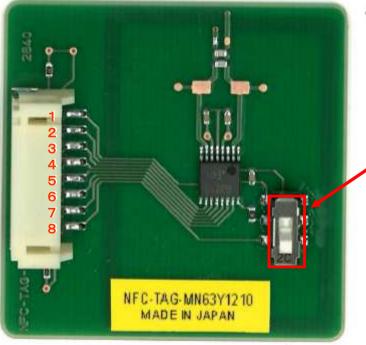
	No	Part Number	Manufacturer	Parameter	Tolerance	Rated V/ W	LxW [mm]
	IC1	NFC-TAG-MN63Y1210A	Panasonic	_	_	4.6V	6.4×5
	CN1	S8B-PH-SM4-TB	JST	_	_	100V	19.9x8.6
	TP0	Unconnected Pin	_	_	_	_	_
	TP1	Unconnected Pin	_	_	_	_	_
	TP2	Unconnected Pin	_	_	_	_	_
	TP3	Unconnected Pin	_	_	_	_	_
	TP4	Unconnected Pin	_	_	_	_	_
	R0	RK73B1JTTD104J	KOA	100kΩ	±5%	0.1W	1.6x0.8
	R1	RK73B1JTTD104J	KOA	100kΩ	±5%	0.1W	1.6x0.8
R	UART	RK73Z1JTTD	KOA	0∼50mΩ	_	0.1W	1.6x0.8
2	CLK synchronous	Unconnected Pin	_	_	_	_	-
R	UART	Unconnected Pin	_	_	_	_	_
3	CLK synchronous	RK73Z1JTTD	КОА	0∼50mΩ	_	0.1W	1.6x0.8
	C0	_	_	_	_	_	_
	C1	_	_	_	_	_	—
	C2	GRM188R71E104KA01D	Murata	0.1 <i>μ</i> F	±10%	25V	1.6x0.8
	C3	GRM188R71H103KA01D	Murata	0.01 µ F	±10%	25V	1.6x0.8
	C4	GRM188R71E104KA01D	Murata	0.1 <i>µ</i> F	±10%	25V	1.6x0.8
	C6	GRM1885C1H331JA01D	Murata	330pF	±5%	50V	1.6x0.8

4 MN63Y1210A AnntenaBoard

The change with the expression, please reach with a switch in UART and the CLK same period.

After having changed it, please carry out an initialization of the smartphone side.

Pin Number	Terminal Name			
1	VSS			
2	NCLP			
3	RX			
4	TX3V			
5	TX5V			
6	IRQ3V			
7	IRQ5V			
8	VDD2			

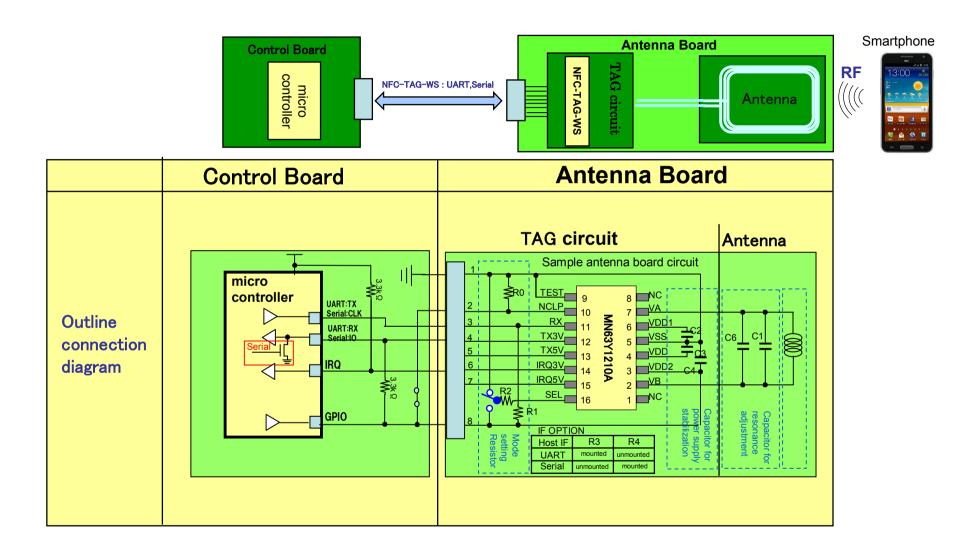


selector switch

Under : CLK synchronization type (Default)

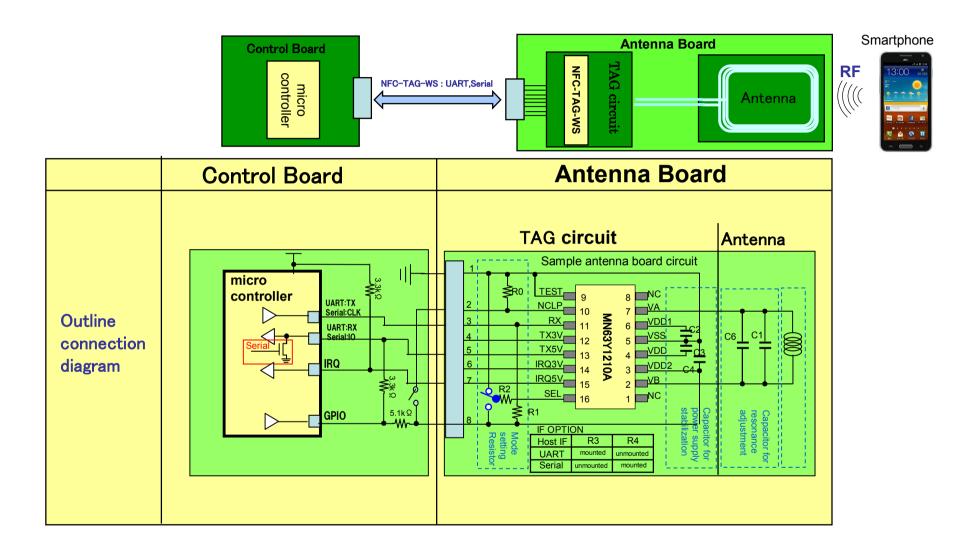
⁵ Connection example with MCU board for 3.3V

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Connection example with MCU board for 5V

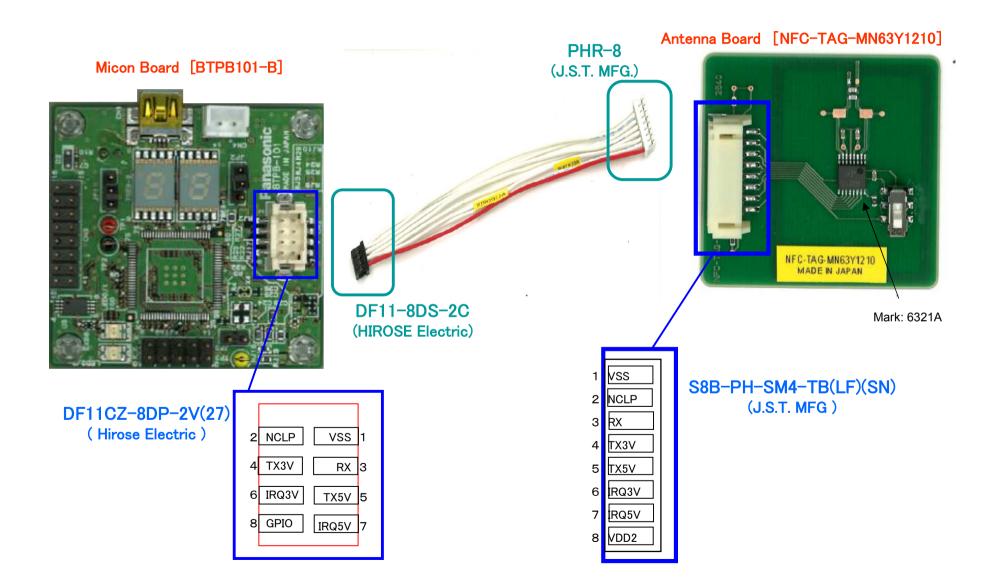
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7 Connector specifications

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