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Gate Driver Providing Galvanic isolation Series

Isolation voltage 2500Vrms 1ch Gate Driver Providing Galvanic Isolation

BM6101FV-C

●General Description

The BM6101FV-C is a gate driver with isolation voltage 2500Vrms, I/O delay time of 350ns, and minimum input pulse width of 180ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function, thermal protection function, and short current protection (SCP, DESAT) function.

●Features

- Providing Galvanic Isolation
- Active Miller Clamping
- Fault signal output function (Adjustable output holding time)
- Undervoltage lockout function
- Thermal protection function
- Short current protection function (Adjustable reset time)
- Soft turn-off function for short current protection (Adjustable turn-off time)
- Supporting Negative VEE
- UL1577 Recognized:File No. E356010
- AEC-Q100 Qualified(Note 1) (Note 1:Grade1)

●Key Specifications

- Isolation voltage: 2500Vrms(Max.)
- Maximum gate drive voltage: 24V(Max.)
- I/O delay time: 350ns(Max.)
- Minimum input pulse width: 180ns(Max.)

●Package

	W(Typ.) x D(Typ.) x H(Max.)
SSOP-B20W	6.50mm x 8.10mm x 2.01mm

●Applications

- Automotive isolated IGBT/MOSFET inverter gate drive
- Automotive DC-DC converter
- Industrial inverters system
- UPS system

●Typical Application Circuits

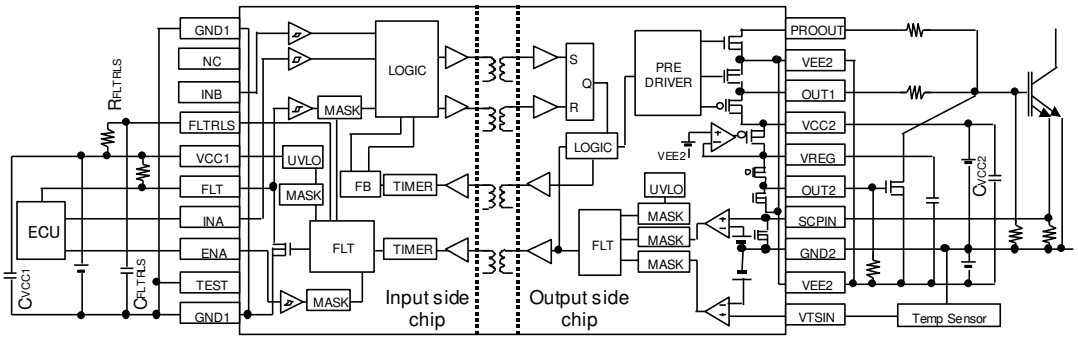


Figure 1. For using 4-pin IGBT (for using SCP function)

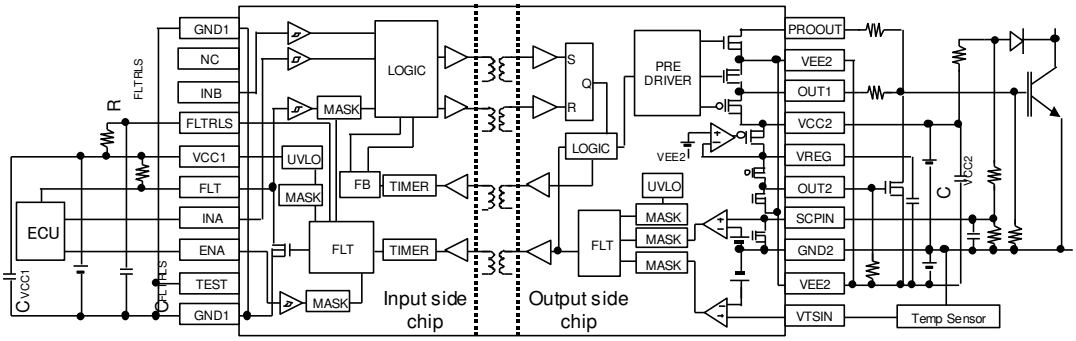


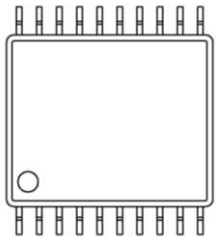
Figure 2. For using 3-pin IGBT (for using DESAT function)

●**Recommended range of external constants**

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
FLTRLS	C_{FLTRLS}	-	0.01	0.47	uF
	R_{FLTRLS}	50	200	1000	kΩ
VREG	C_{VREG}	1.0	3.3	10.0	uF
VCC1	C_{VCC1}	0.1	1.0	-	uF
VCC2	C_{VCC2}	0.33	-	-	uF

●**Pin Configuration**

SSOP-B20W
(TOP VIEW)



1pin

Figure 3. Pin configuration

●**Pin Description**

Pin No.	Pin Name	Function
1	VTSIN	Thermal detection pin
2	VEE2	Output-side negative power supply pin
3	GND2	Output-side ground pin
4	SCPIN	Short current detection pin
5	OUT2	MOS FET control pin for Miller Clamp
6	VREG	Power supply pin for driving MOS FET for Miller Clamp
7	VCC2	Output-side positive power supply pin
8	OUT1	Output pin
9	VEE2	Output-side negative power supply pin
10	PROOUT	Soft turn-off pin
11	GND1	Input-side ground pin
12	NC	No Connect
13	INB	Invert / non-invert selection pin
14	FLTRLS	Fault output holding time setting pin
15	VCC1	Input-side power supply pin
16	FLT	Fault output pin
17	INA	Control input pin
18	ENA	Input enabling signal input pin
19	TEST	Mode setting pin
20	GND1	Input-side ground pin

●Description of pins and cautions on layout of board

1) VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2) GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3) VCC2 (Output-side positive power supply pin)
The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to OUT1 pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VCC2 and the GND2 pins.

4) VEE2 (Output-side negative power supply pin)
The VEE2 pin is a power supply pin on the output side. To suppress voltage fluctuations due to OUT1 pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VEE2 and the GND2 pins. To use no negative power supply, connect the VEE2 pin to the GND2 pin.

5) GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

6) IN (Control input terminal)
The IN pin is a pin used to determine output logic.

ENA	INB	INA	OUT1
H	X	X	L
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L

7) FLT (Fault output pin)
The FLT pin is an open drain pin used to output a fault signal when a fault occurs (i.e., when the undervoltage lockout function (UVLO), short current protection function (SCP) or thermal protection function is activated).
This pin is I/O pin and if L voltage is externally input, the output is set to L status regardless of other input logic. Consequently, be sure to connect the pull-up resistor between VCC1 pin and the FLT pin even if this pin is not used.

Pin	FLT
While in normal operation	Hi-Z
When an Fault occurs (When UVLO, SCP or thermal protection is activated)	L

8) FLTRLS (Fault output holding time setting pin)
The FLTRLS pin is a pin used to make setting of time to hold a Fault signal. Connect a capacitor between the FLTRLS pin and the GND1 pin, and a resistor between it and the VCC1 pin.
The Fault signal is held until the FLTRLS pin voltage exceeds a voltage set with the V_{FLTRLS} parameter. To set holding time to 0 ms, do not connect the capacitor. Short-circuiting the FLTRLS pin to the VCC1 pin will cause a high current to flow in the FLTRLS pin and, in an open state, may cause the IC to malfunction. To avoid such trouble, be sure to connect a resistor between the FLTRLS and the VCC1 pins.

9) OUT1 (Output pin)
The OUT1 pin is a pin used to drive the gate of a power device.

10) OUT2 (MOS FET control pin for Miller Clamp)
The OUT2 pin is a pin for controlling the external MOS switch for preventing increase in gate voltage due to the miller current of the power device connected to OUT1 pin.

11) VREG (Power supply pin for driving MOS FET for Miller Clamp)
The VREG pin is a power supply pin for driving MOS FET for Miller Clamp. Be sure to connect a capacitor between VREG pin and VEE2 pin for preventing the oscillation and to reduce voltage fluctuations due to OUT2 pin output current.

12) PROOUT (Soft turn-off pin)
The PROOUT pin is a pin used to put the soft turn-off function of a power devise in operation when the SCP function is activated. This pin combines with the gate voltage monitoring pin for Miller Clamp.

13) SCPIN (Short current detection pin)
The SCPIN pin is a pin used to detect current for short current protection. When the SCPIN pin voltage exceeds a voltage set with the V_{SCDET} parameter, the SCP function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the SCPIN pin to the GND2 pin if the short current protection is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{SCPMSK} is set.

14) VTSIN (Thermal detection pin)

The VTSIN pin is a temperature sensor voltage input pin, which can be used for thermal protection of an output device. If VTSIN pin voltage becomes V_{TSDET} or less, OUT pin is set to L. In the open status, the IC may malfunction, so be sure to supply the VTSPIN more than V_{TSDET} if the thermal protection function is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{TSMSK} is set.

15) TEST(Mode setting pin)

The TEST pin is an operation mode setting pin. This pin is usually connected to GND1 pin. If the TEST pin is connected to the VCC1 pin, Input-side UVLO function is disabled.

●Description of functions and examples of constant setting

1) Miller Clamp function

When OUT1=L and PROOUT pin voltage < V_{OUT2ON}, H is output from OUT2 pin and the external MOS switch is turned ON. When OUT1=H, L is output from OUT2 pin and the external MOS switch is turned OFF. While the short-circuit protection function is activated, L is output from OUT2 pin and the external MOS switch is turned OFF.

Short current	SCPIN	IN	PROOUT	OUT2
Detected	Not less than V_{SCDET}	X	X	L
Not detected	X	L	Not less than V_{OUT2ON}	Hi-Z
	X	L	Not more than V_{OUT2ON}	H
	X	H	X	L

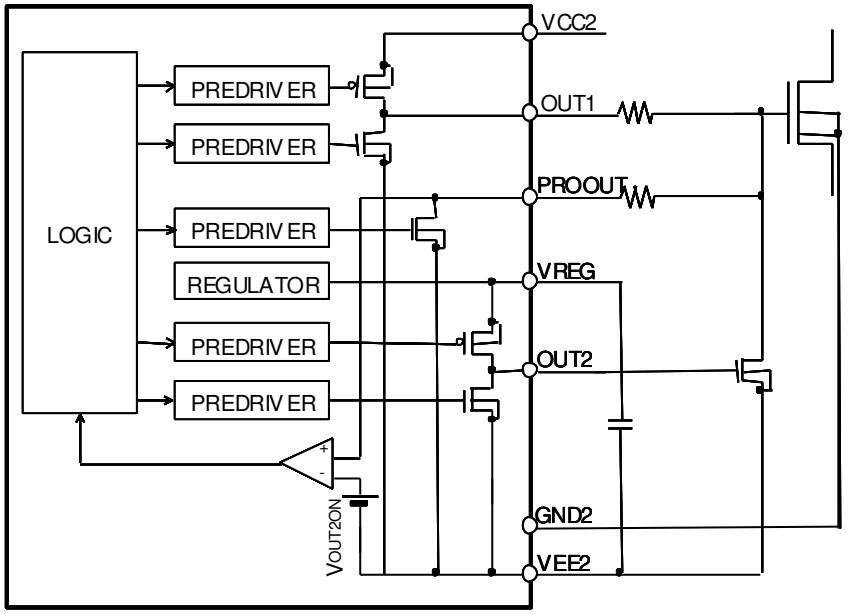


Figure 4. Block diagram of Miller Clamp function

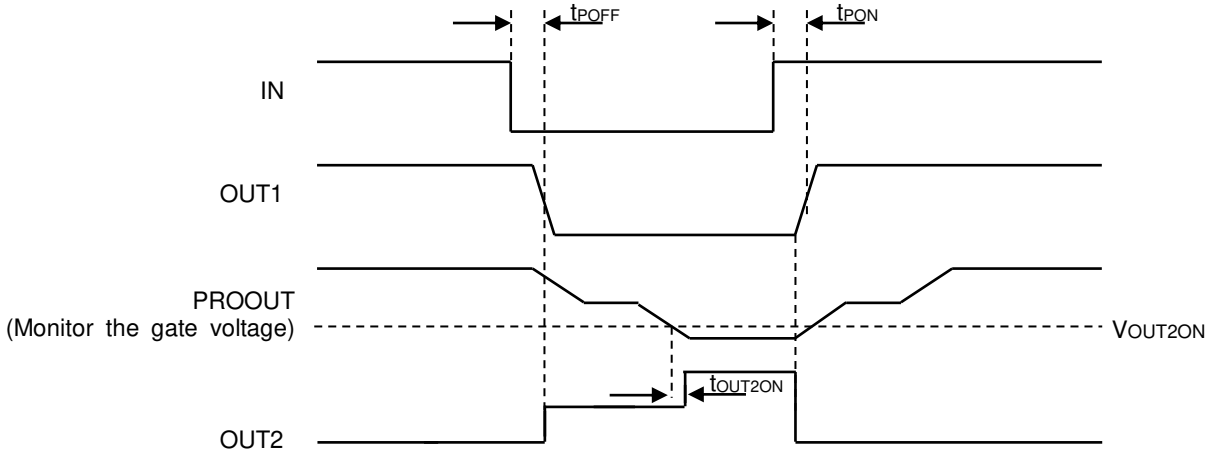


Figure 5. Timing chart of Miller Clamp function

2) Fault status output

This function is used to output a fault signal from the FLT pin when a fault occurs (i.e., when the undervoltage lockout function (UVLO), short current protection function (SCP) or thermal protection function is activated) and hold the Fault signal until the set Fault output holding time is completed. The Fault output holding time t_{FLTRLS} is given as the following equation with the settings of capacitor C_{FLTRLS} and resistor R_{FLTRLS} connected to the FLTRLS pin. For example, when C_{FLTRLS} is set to 0.01μF and R_{FLTRLS} is set to 200kΩ, the holding time will be set to 2 ms.

t_{FLTRLS} [ms]= C_{FLTRLS} [μF]•R_{FLTRLS} [kΩ]

To set the fault output holding time to “0” ms, only connect the resistor R_{FLTRLS}.

Status	FLT pin
Normal	Hi-Z
Fault occurs	L

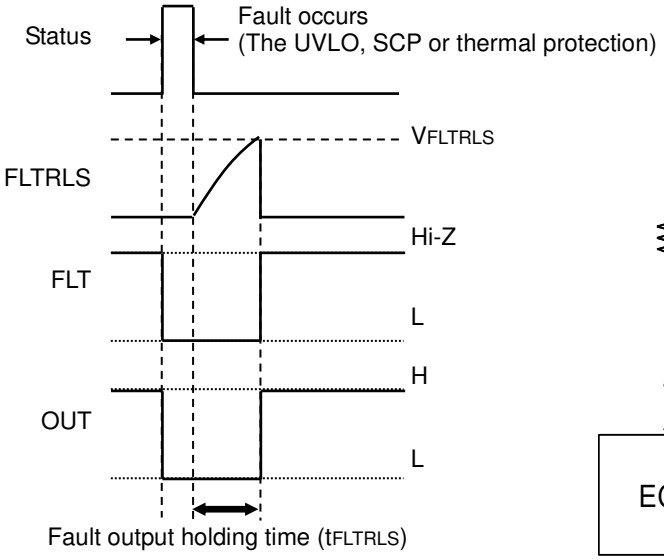


Figure 6. Fault Status Output Timing Chart

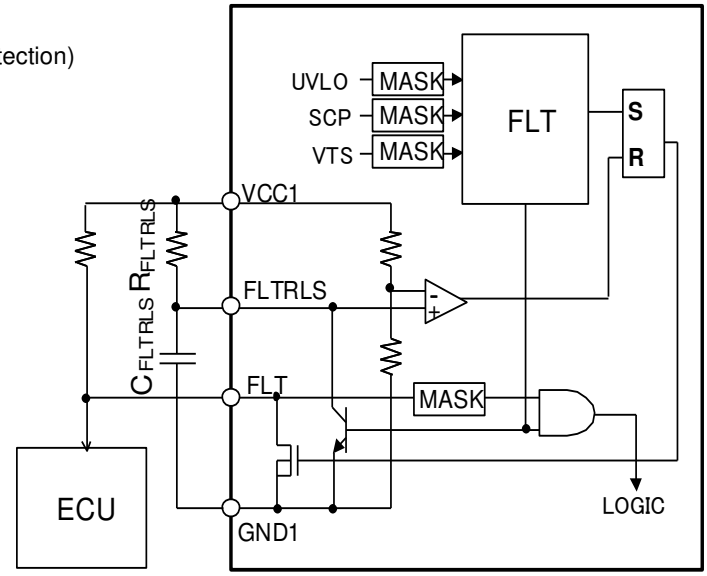


Figure 7. Fault Output Block Diagram

3) Undervoltage Lockout (UVLO) function

The BM6101FV-C incorporates the undervoltage lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage, the OUT pin and the FLT pin both will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. However, during the fault output holding time set in “2) Fault status output” section, the OUT pin and the FLT pin will hold the “L” signal. In addition, to prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on both low and high voltage sides.

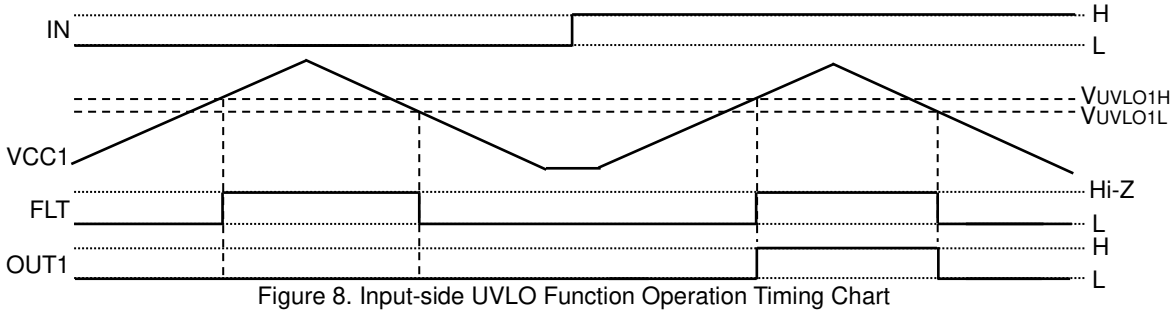


Figure 8. Input-side UVLO Function Operation Timing Chart

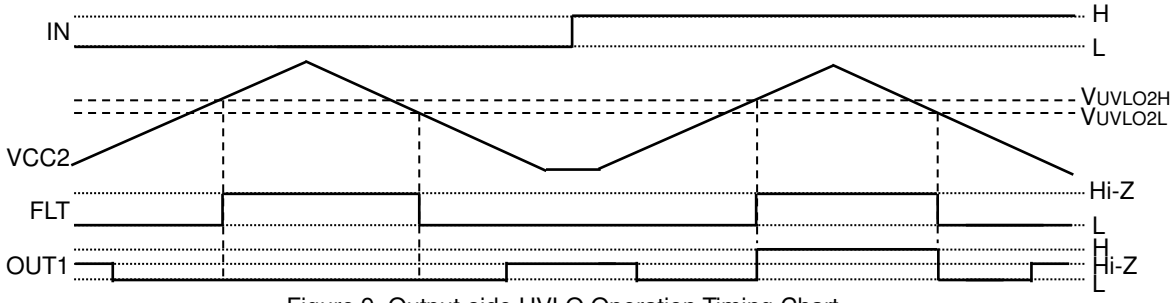


Figure 9. Output-side UVLO Operation Timing Chart

4) Short current protection function (SCP, DESAT)

When the SCPIN pin voltage exceeds a voltage set with the V_{SCDET} parameter, the SCP function will be activated. When the SCP function is activated, the OUT1 pin voltage will be set to the “Hi-Z” level first, and then the PROOUT pin voltage to the “L” level (soft turn-off).Next, after t_{STO} has passed after the short-circuit current falls below the threshold value, OUT pin becomes L and PROOUT pin becomes L. Finally, when the fault output holding time set in “2) fault status output” section on page 5 is completed, the SCP function will be released.

When OUT1=L or Hi-Z, internal MOSFET connected to SCPIN pin turns ON to discharge C_{BLANK}. When OUT1=H, internal MOSFET connected to SCPIN turns OFF.

$V_{COLLECTOR}/V_{DRAIN}$ which Desaturation Protection starts operation (V_{DESAT}) and the blanking time (t_{BLANK}) can be calculated by the formula below;

$$V_{DESAT}[V] = V_{SCDET} \bullet \frac{R3+R2}{R3} - V_{F_D}$$

$$V_{CC2_{MIN}}[V] > V_{SCDET} \bullet \frac{R3+R2+R1}{R3}$$

$$t_{BLANKoutemal}[s] = -\frac{R2+R1}{R3+R2+R1} \bullet R3 \bullet (C_{BLANK} + 27 \bullet 10^{-12}) \bullet \ln(1 - \frac{R3+R2+R1}{R3} \bullet \frac{V_{SCDET}}{V_{CC2}}) + 0.65 \bullet 10^{-6}$$

V_{DESAT}	Reference Value		
	R1	R2	R3
4.0V	15 kΩ	39 kΩ	6.8 kΩ
4.5V	15 kΩ	43 kΩ	6.8 kΩ
5.0V	15 kΩ	36 kΩ	5.1 kΩ
5.5V	15 kΩ	39 kΩ	5.1 kΩ
6.0V	15 kΩ	43 kΩ	5.1 kΩ
6.5V	15 kΩ	62 kΩ	6.8 kΩ
7.0V	15 kΩ	68 kΩ	6.8 kΩ
7.5V	15 kΩ	82 kΩ	7.5 kΩ
8.0V	15 kΩ	91 kΩ	8.2 kΩ
8.5V	15 kΩ	82 kΩ	6.8 kΩ
9.0V	15 kΩ	130 kΩ	10 kΩ
9.5V	15 kΩ	91 kΩ	6.8 kΩ
10.0V	15 kΩ	130 kΩ	9.1 kΩ

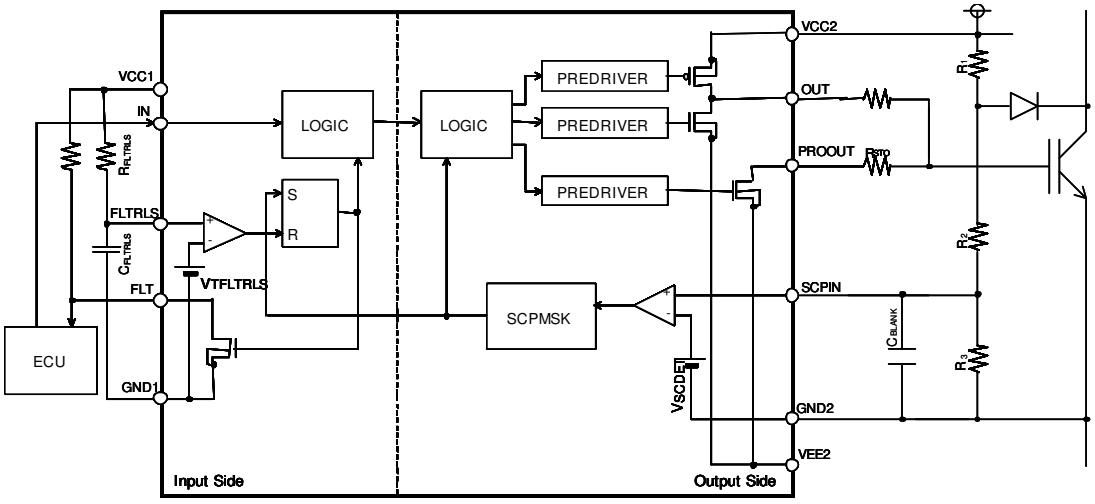
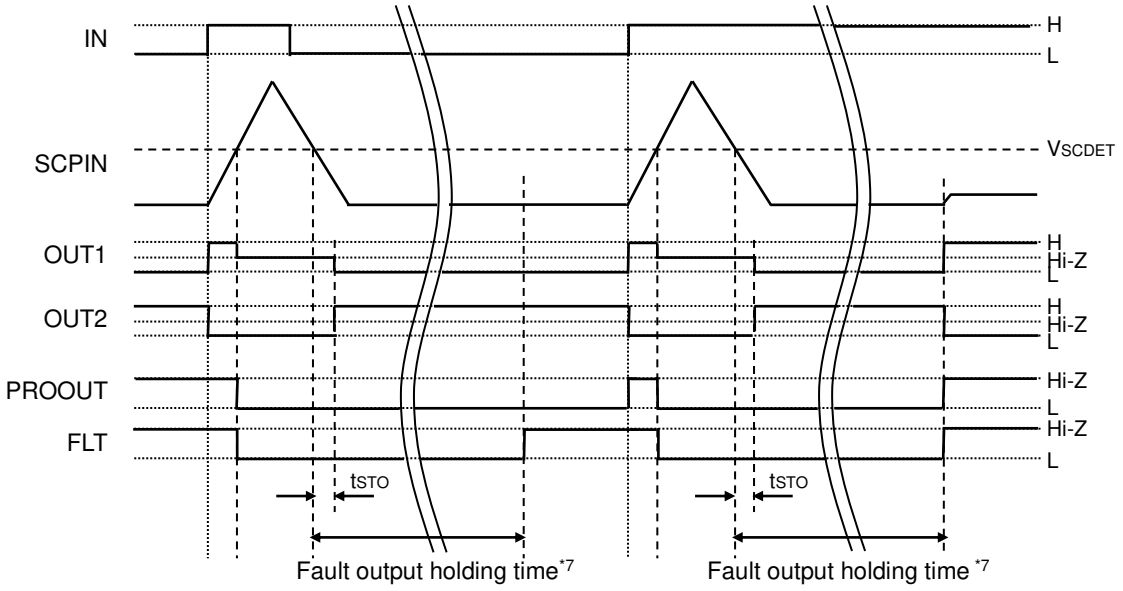
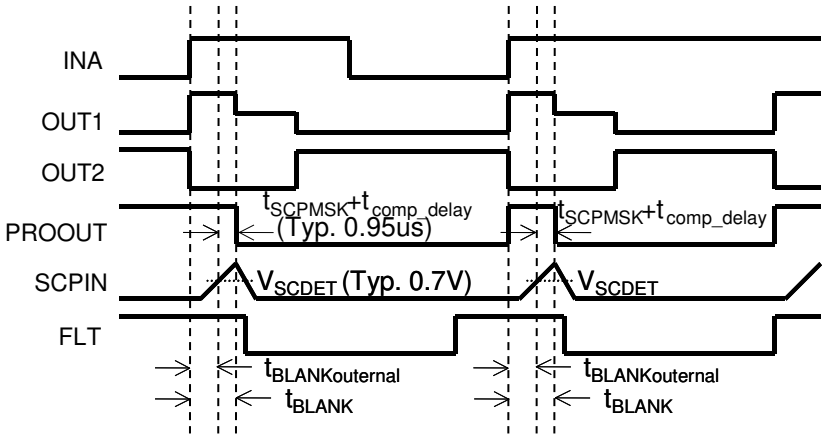


Figure 10. Block Diagram for DESAT



*7: "2) Fault status output" section on page 5

Figure 11. SCP Operation Timing Chart



t_{comp_delay} : Detection delay time of internal comparator

Figure 12. DESAT sequence

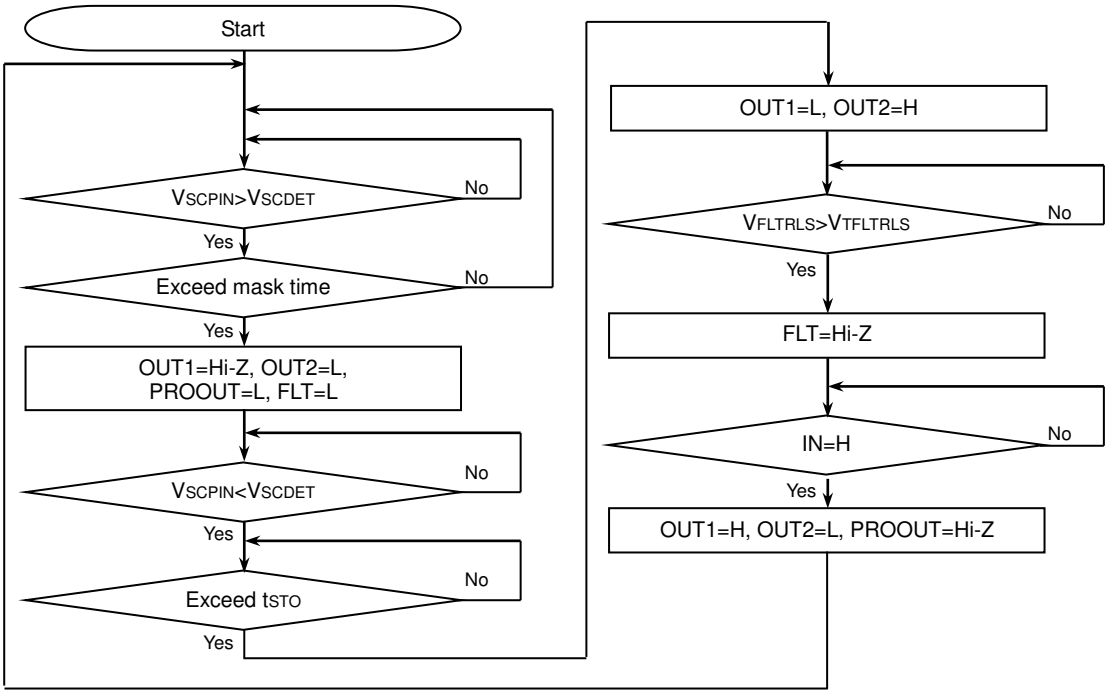


Figure 13. SCP Operation Status Transition Diagram

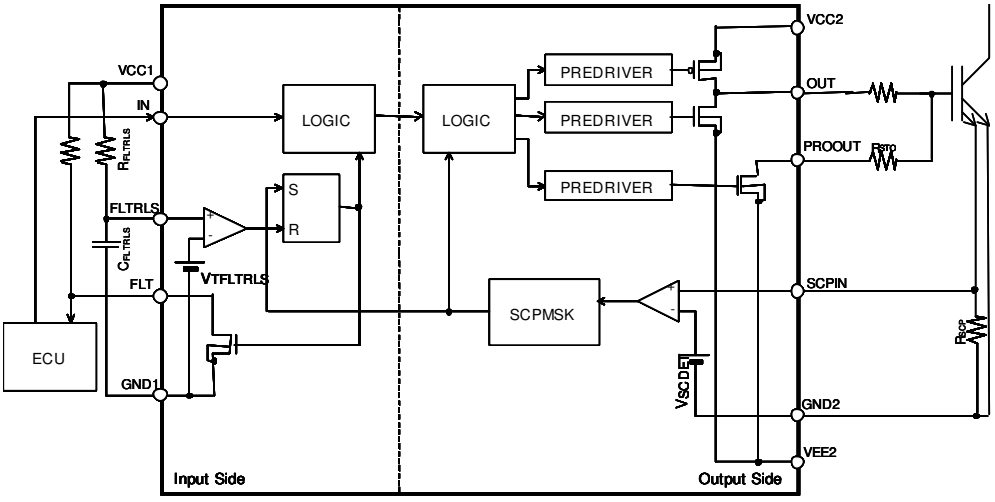


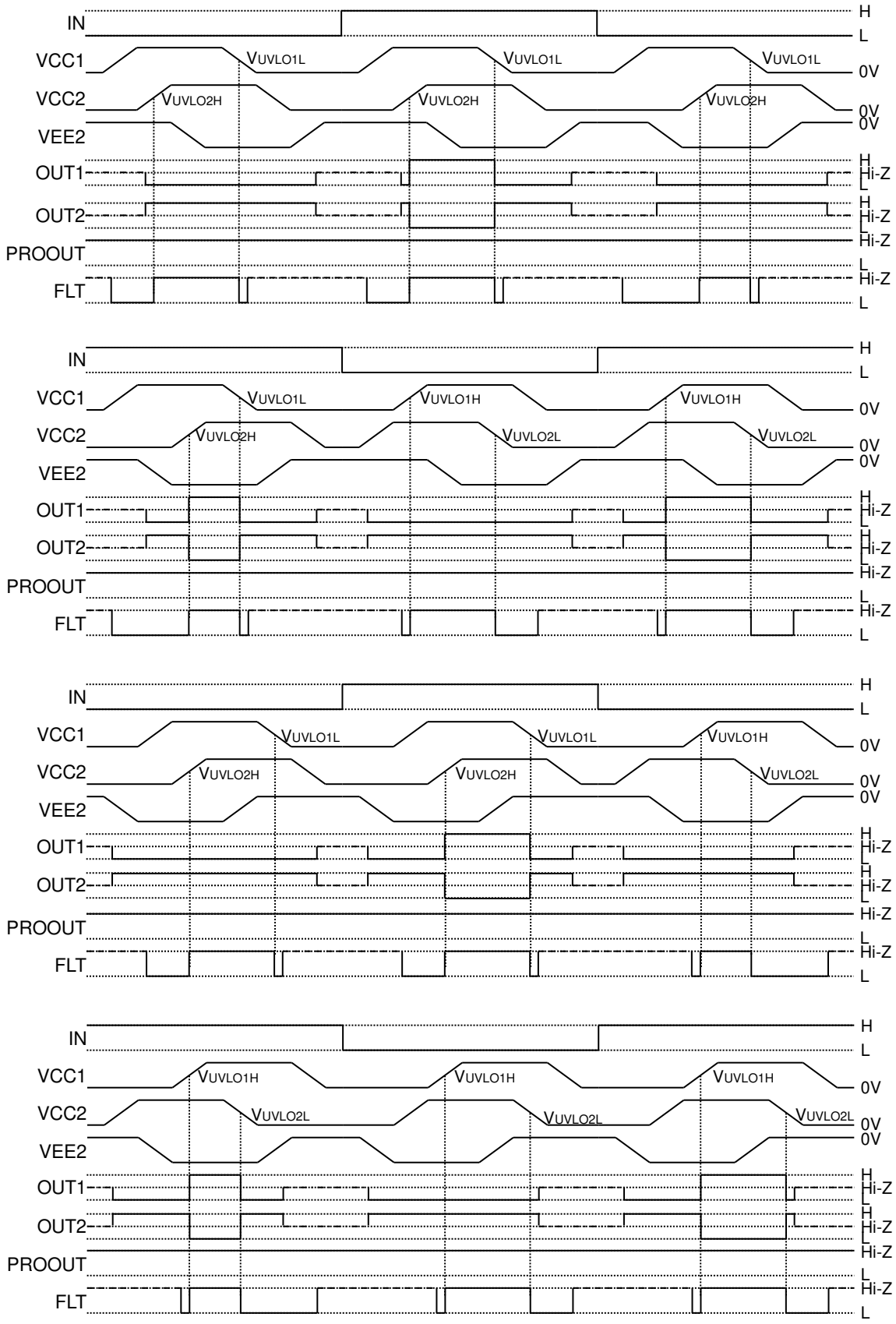
Figure 14. Block Diagram for SCP

5）I/O condition table

No.	Status	Input									Output			
		VCC1	VCC2	VTSIN	SCPIN	FLT	ENA	INB	INA	PROOUT	OUT1	OUT2	PROOUT	FLT
1	SCP	X	X	X	H	X	X	X	X	X	Hi-Z	L	L	L
2	VCC1UVLO	UVLO	X	X	L	X	X	X	X	H	L	Hi-Z	Hi-Z	L
3		UVLO	X	X	L	X	X	X	X	L	L	H	Hi-Z	L
4	VCC2UVLO	X	UVLO	X	L	X	X	X	X	H	L	Hi-Z	Hi-Z	L
5		X	UVLO	X	L	X	X	X	X	L	L	H	Hi-Z	L
6	Thermal protection	○	○	L	L	X	X	X	X	H	L	Hi-Z	Hi-Z	L
7		○	○	L	L	X	X	X	X	L	L	H	Hi-Z	L
8	FLT external input	○	○	H	L	L	X	X	X	H	L	Hi-Z	Hi-Z	Hi-Z
9		○	○	H	L	L	X	X	X	L	L	H	Hi-Z	Hi-Z
10	Disable	○	○	H	L	H	H	X	X	H	L	Hi-Z	Hi-Z	Hi-Z
11		○	○	H	L	H	H	X	X	L	L	H	Hi-Z	Hi-Z
12	Non-invert operation L input	○	○	H	L	H	L	L	L	H	L	Hi-Z	Hi-Z	Hi-Z
13		○	○	H	L	H	L	L	L	L	L	H	Hi-Z	Hi-Z
14	Non-invert operation H input	○	○	H	L	H	L	L	H	X	H	L	Hi-Z	Hi-Z
15	Invert operation L input	○	○	H	L	H	L	H	L	X	H	L	Hi-Z	Hi-Z
16	Invert operation H input	○	○	H	L	H	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z
17		○	○	H	L	H	L	H	H	L	L	H	Hi-Z	Hi-Z

○: VCC1 or VCC2 > UVLO, X:Don't care

6) Power supply startup / shutoff sequence



: Since the VCC2 to VEE2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

: Since the VCC1 pin voltage is low and the FLT output MOS does not turn ON, the output pins become Hi-Z conditions.

Figure 15. Power supply startup / shutoff sequence

●Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3 to +7.0*1	V
Output-side positive supply voltage	V_{CC2}	-0.3 to +30.0*2	V
Output-side negative supply voltage	V_{EE2}	-15.0 to +0.3*2	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	36.0	V
INA, INB, ENA pin input voltage	V_{IN}	-0.3 to +VCC1+0.3 or 7.0*1	V
FLT pin input voltage	V_{FLT}	-0.3 to +VCC1+0.3 or 7.0*1	V
FLTRLS pin input voltage	V_{FLTRLS}	-0.3 to +VCC1+0.3 or 7.0*1	V
VTSIN pin input voltage	V_{VTSIN}	-0.3 to +10.0*2	V
SCPIN pin input voltage	V_{SCPIN}	-0.3 to +10.0*2	V
VREG pin output current	I_{VREG}	10	mA
OUT1 pin output current (DC)	I_{OUT1}	0.4*3	A
OUT1 pin output current (Peak 1us)	$I_{OUT1PEAK}$	5.0	A
OUT2 pin output current (DC)	I_{OUT2}	0.1*3	A
OUT2 pin output current (Peak 1us)	$I_{OUT2PEAK}$	1	A
PROOUT pin output current	I_{PROOUT}	0.2*3	A
FLT output current	I_{FLT}	10	mA
Power dissipation	P_d	1.19*4	W
Operating temperature range	T_{opr}	-40 to +125	℃
Storage temperature range	T_{stg}	-55 to +150	℃
Junction temperature	T_{jmax}	+150	℃

*1 Relative to GND1.
*2 Relative to GND2.
*3 Should not exceed Pd and Tj=150°C.
*4 Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.

●Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
Input-side supply voltage	V_{CC1}*5	4.5	5.5	V
Output-side positive supply voltage	V_{CC2}*6	14	24	V
Output-side negative supply voltage	V_{EE2}*6	-12	0	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	14	32	V
VTSIN pin input voltage	V_{VTSIN}*6	0	5	V

***5 Relative to GND1.**
***6 Relative to GND2.**

●Insulation related characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

●Electrical Characteristics

（Unless otherwise specified Ta=-40℃ to 125℃, V_{CC1}=4.5V to 5.5V, V_{CC2}=14V to 24V, V_{EE2}=-12V to 0V）

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current 1	I_{CC1}	0.20	0.45	0.70	mA	OUT=L
Input side circuit current 2	I_{CC12}	0.20	0.45	0.70	mA	OUT=H
Input side circuit current 3	I_{CC13}	1.2	2.0	2.8	mA	INA=10kHz, Duty=50%
Input side circuit current 4	I_{CC14}	2.1	3.5	4.9	mA	INA=20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	1.9	3.2	4.5	mA	VCC2=14V, OUT=L
Output side circuit current 2	I_{CC22}	1.3	2.1	2.9	mA	VCC2=14V, OUT=H
Output side circuit current 3	I_{CC23}	2.1	3.5	4.9	mA	VCC2=18V, OUT=L
Output side circuit current 4	I_{CC24}	1.4	2.4	3.4	mA	VCC2=18V, OUT=H
Output side circuit current 5	I_{CC25}	2.4	4.0	5.6	mA	VCC2=24V, OUT=H
Output side circuit current 6	I_{CC26}	1.6	2.7	3.8	mA	VCC2=24V, OUT=L
Logic block						
Logic high level input voltage	V_{INH}	$0.7\times V_{CC1}$	-	V_{CC1}	V	INA, INB, ENA, FLT
Logic low level input voltage	V_{INL}	0	-	$0.3\times V_{CC1}$	V	INA, INB, ENA, FLT
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA, INB
Logic pull-up resistance	R_{INU}	25	50	100	kΩ	ENA
Logic input mask time	t_{INMSK}	80	130	180	ns	INA, INB
ENA, FLT mask time	t_{FLTMSK}	4	10	20	μs	ENA, FLT
Output						
OUT1 ON resistance (Source)	R_{ONH}	0.7	1.8	4.0	Ω	I_{OUT}=40mA
OUT1 ON resistance (Sink)	R_{ONL}	0.4	0.9	2.0	Ω	I_{OUT}=40mA
OUT1 maximum current	I_{OUTMAX}	3.0	4.5	-	A	VCC2=18V Design assurance
PROOUT ON resistance	R_{ONPRO}	0.4	0.9	2.0	Ω	I_{PROOUT}=40mA
Turn ON time	t_{PON}	180	265	350	ns	
Turn OFF time	t_{POFF}	180	265	350	ns	
Propagation distortion	t_{PDIST}	-60	0	60	ns	t_{POFF} - t_{PON}
Rise time	t_{RISE}	-	50	100	ns	10nF between OUT1-VEE2
Fall time	t_{FALL}	-	50	100	ns	10nF between OUT1-VEE2
OUT2 ON resistance (Source)	R_{ON2H}	2.0	4.5	9.0	Ω	I_{OUT2}=40mA
OUT2 ON resistance (Sink)	R_{ON2L}	1.5	3.5	7.0	Ω	I_{OUT2}=40mA
OUT2 ON threshold voltage	V_{OUT2ON}	1.8	2	2.2	V	Relative to VEE2
OUT2 output delay time	t_{OUT2ON}	-	15	50	ns	
VREG output voltage	V_{REG}	9	10	11	V	Relative to VEE2
Common Mode Transient Immunity	CM	100	-	-	kV/μs	Design assurance
Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	4.05	4.25	4.45	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.95	4.15	4.35	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	4	10	30	μs	
VCC2 UVLO OFF voltage	V_{UVLO2H}	11.5	12.5	13.5	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	10.5	11.5	12.5	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	4	10	30	μs	
SCPIN Input voltage	V_{SCPIN}	-	0.1	0.22	V	I_{SCPIN}=1mA
SCP detection voltage	V_{SCDET}	0.665	0.700	0.735	V	
SCP detection mask time	t_{SCPMSK}	0.55	0.8	1.05		
Soft turn OFF release time	t_{STO}	30		110	μs	
Thermal detection voltage	V_{TSDET}	1.60	1.70	1.80	V	
Thermal detection mask time	t_{TSMSK}	4	10	30	μs	
FLT output low voltage	V_{FLTL}	-	0.18	0.40	V	I_{FLT}=5mA
FLTRLS threshold	$V_{TFLTRLS}$	$0.64\times V_{CC1}$ -0.1	$0.64\times V_{CC1}$	$0.64\times V_{CC1}$ +0.1	V	

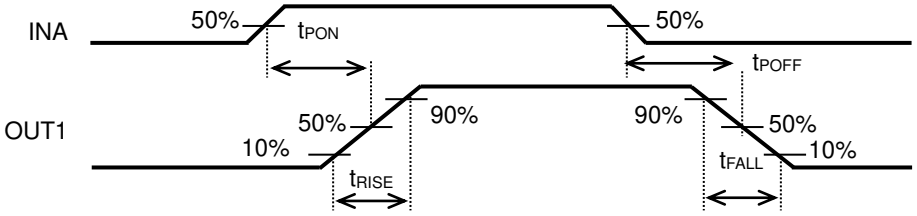


Figure 16. INA-OUT1 Timing Chart

●UL1577 Ratings Table

Following values are described in UL Report.

Parameter	Values	Units	Conditions
Side 1 (Input Side) Circuit Current	0.45	mA	VCC1=5.0V, OUT1=L
Side 2 (Output Side) Circuit Current	3.5	mA	VCC2=18V, VEE2=0V, OUT1=L
Side 1 (Input Side) Consumption Power	2.25	mW	VCC1=5.0V, OUT1=L
Side 2 (Output Side) Consumption Power	63	mW	VCC2=18V, VEE2=0V, OUT1=L
Isolation Voltage	2500	Vrms	
Maximum Operating (Ambient) Temperature	125	℃	
Maximum Junction Temperature	150	℃	
Maximum Strage Temperature	150	℃	
Maximum Data Transmission Rate	2.5	MHz	

●Typical Performance Curves

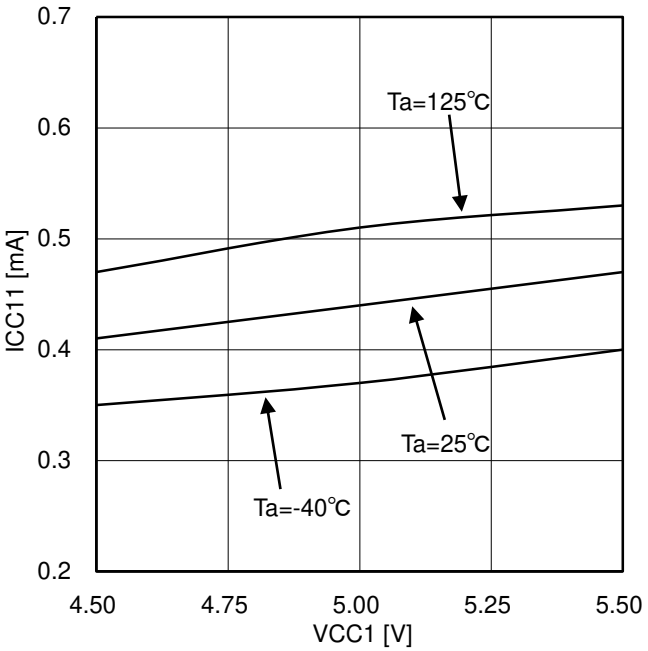


Figure 17. Input side circuit current (at OUT1=L)

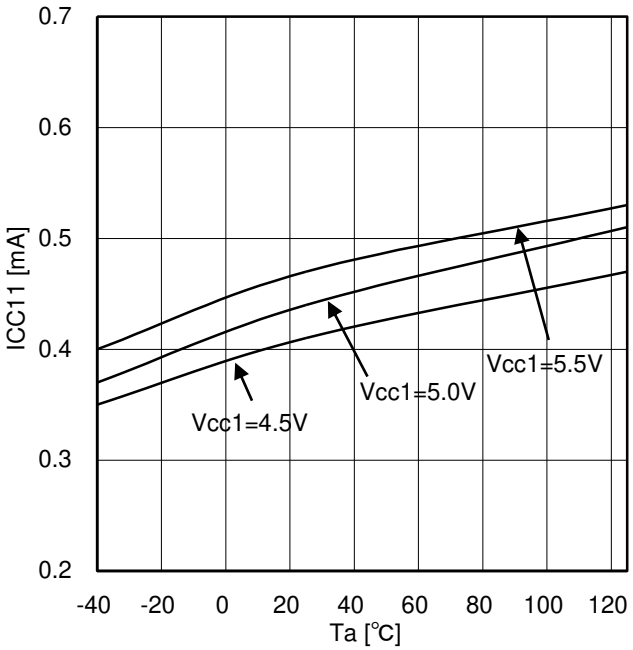


Figure 18. Input side circuit current (at OUT1=L)

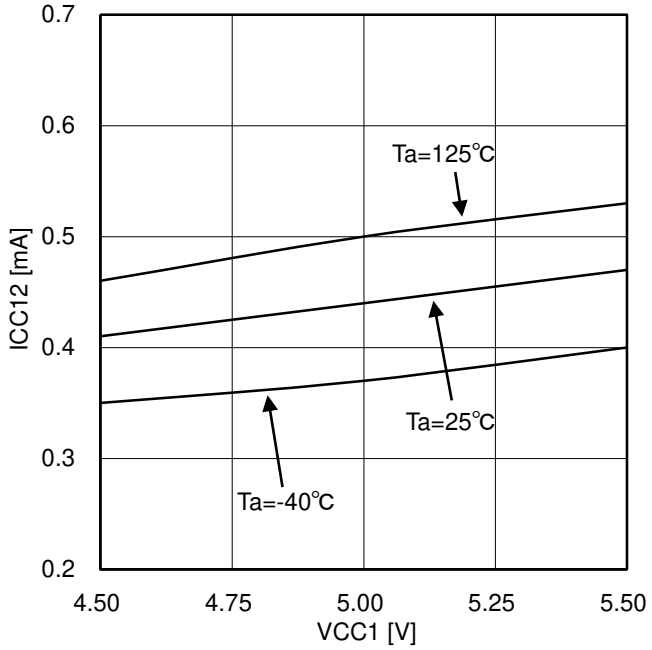


Figure 19. Input side circuit current (at OUT1=H)

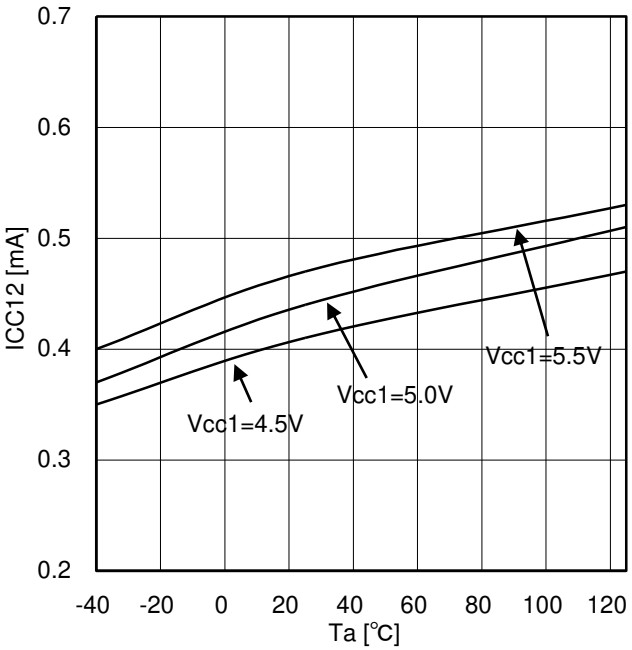


Figure 20. Input side circuit current (at OUT1=H)

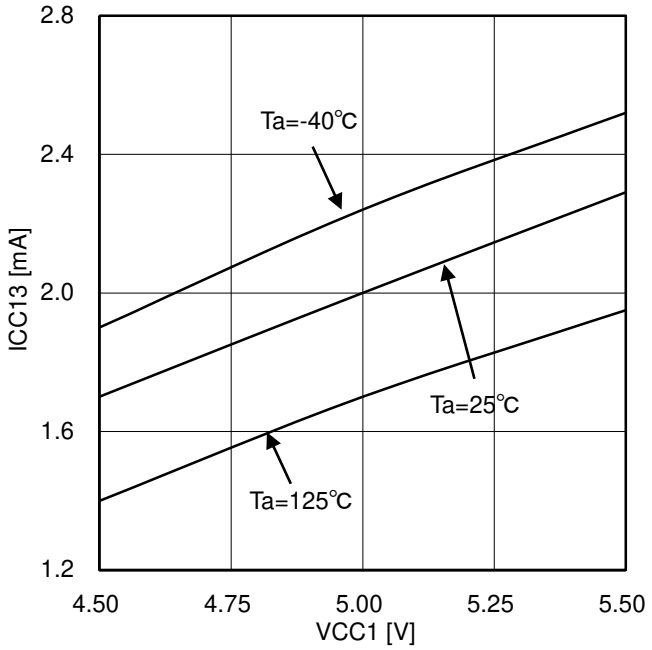


Figure 21. Input side circuit current
(at INA=10kHz and Duty=50%)

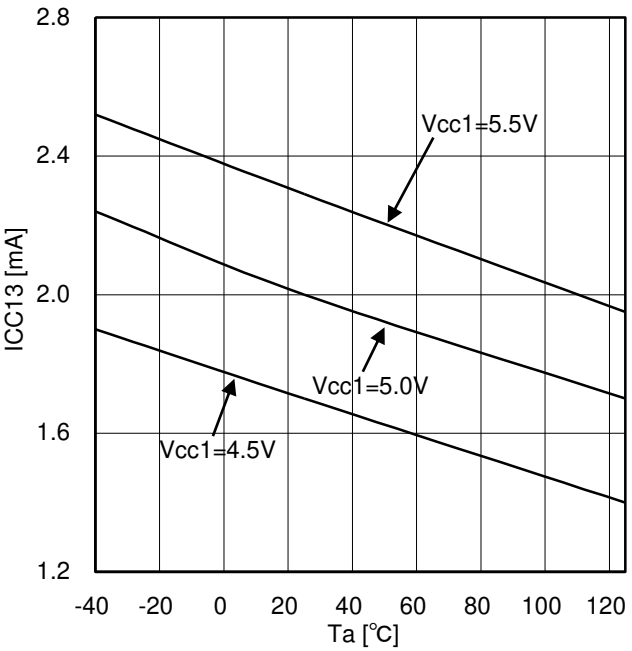


Figure 22. Input side circuit current
(at INA=10kHz and Duty=50%)

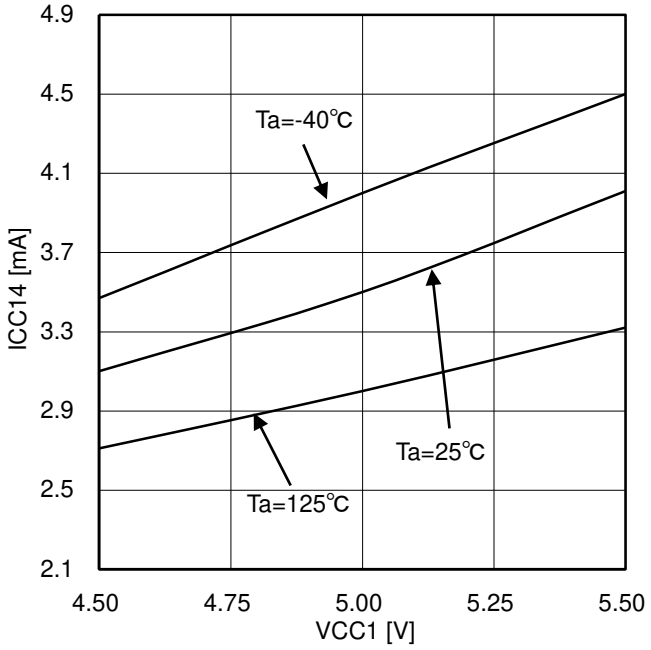


Figure 23. Input side circuit current (at INA=20kHz and Duty=50%)

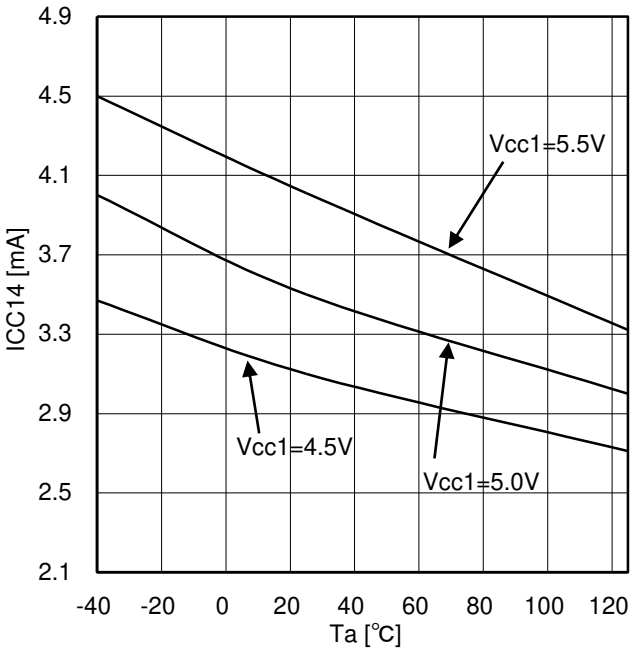


Figure 24. Input side circuit current (at INA=20kHz and Duty=50%)

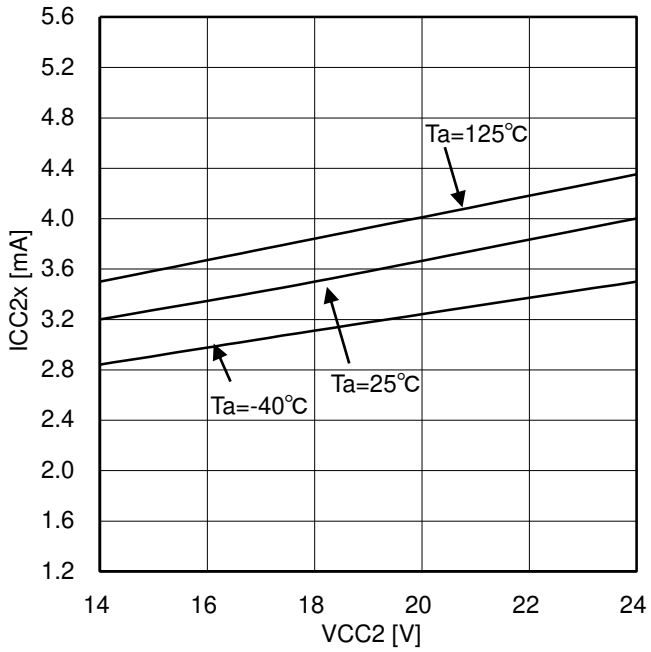


Figure 25. Output side circuit current (at OUT1=L)

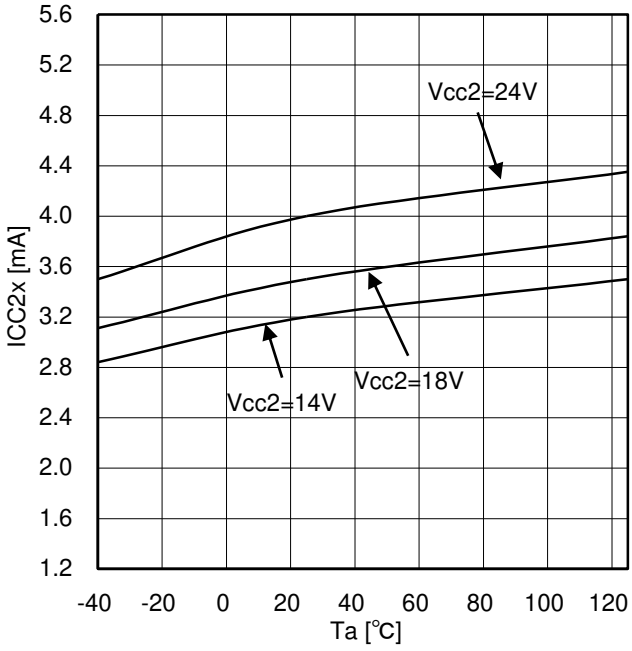


Figure 26. Output side circuit current (at OUT1=L)

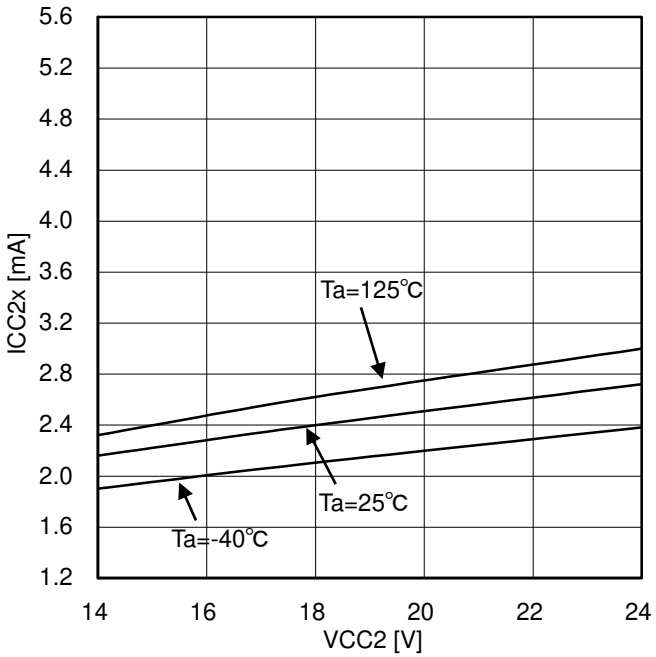


Figure 27. Output side circuit current (at OUT1=H)

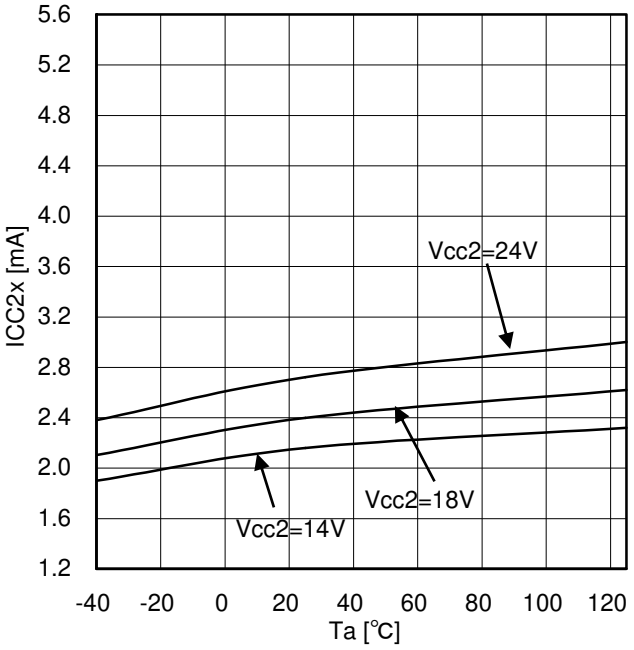


Figure 28. Output side circuit current (at OUT1=H)

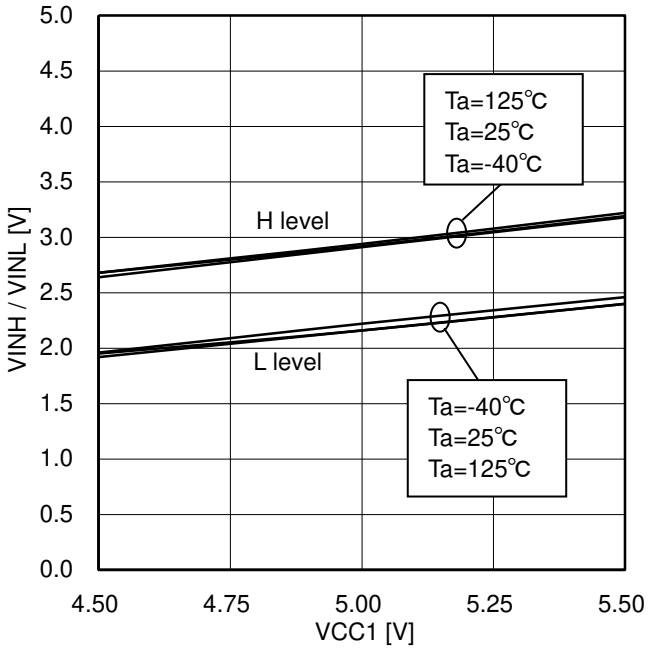


Figure 29. Logic (INA/INB/ENA) High/Low level input voltage

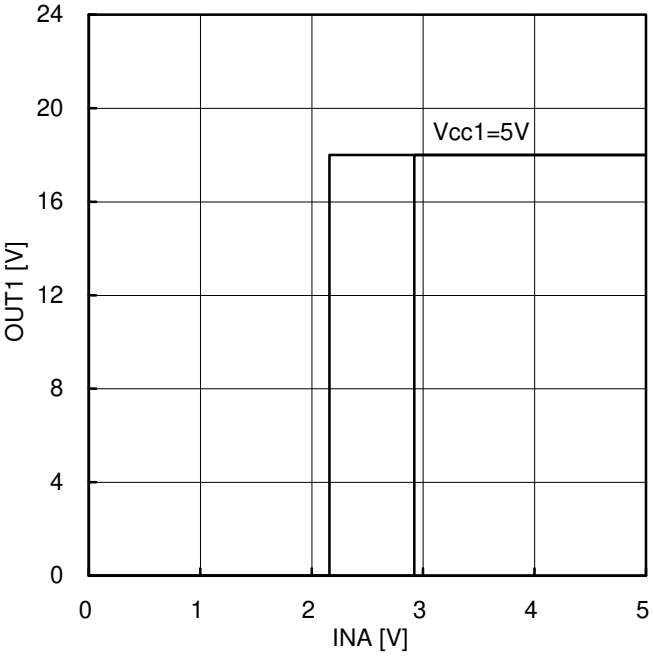


Figure 30. Logic (INA/INB/ENA) High/Low level input voltage at Ta=25℃

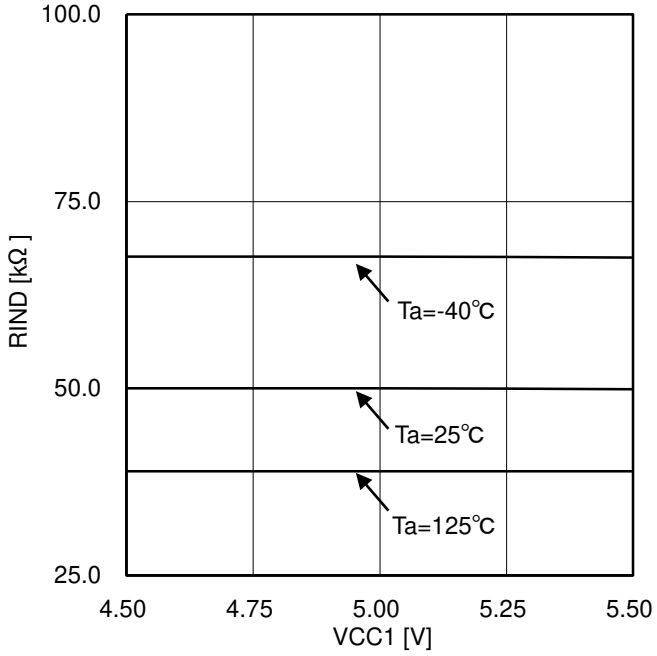


Figure 31. Logic pull-down resistance

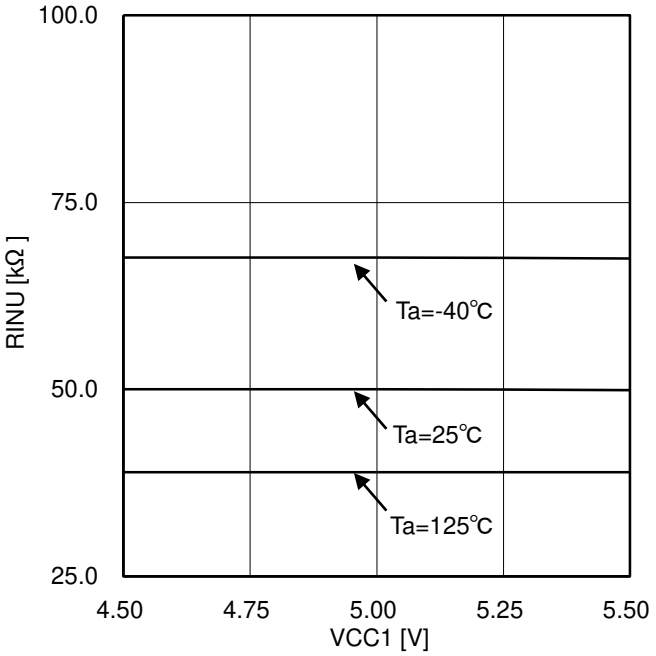


Figure 32. Logic pull-up resistance

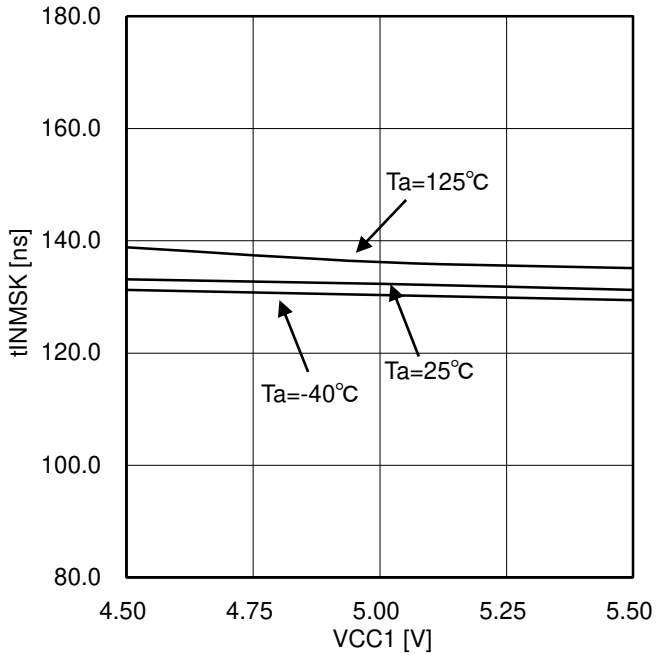


Figure 33. Logic (INA/INB) input mask time (High pulse)

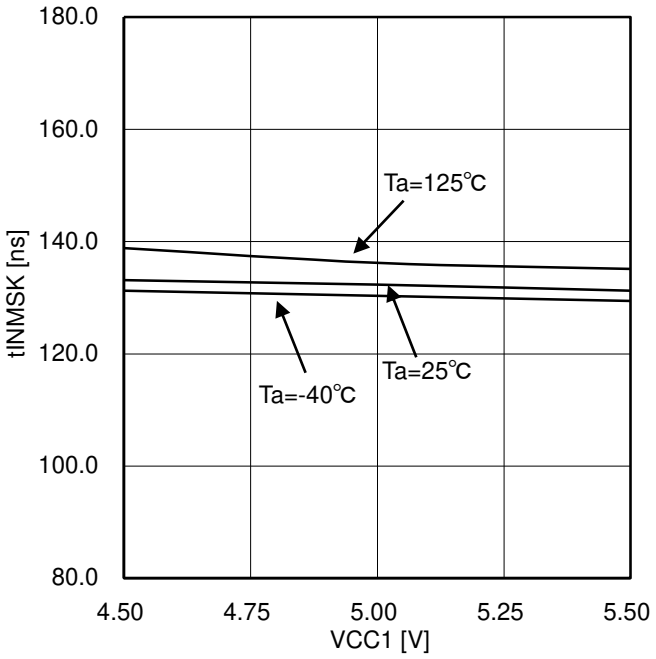


Figure 34. Logic (INA/INB) input mask time (Low pulse)

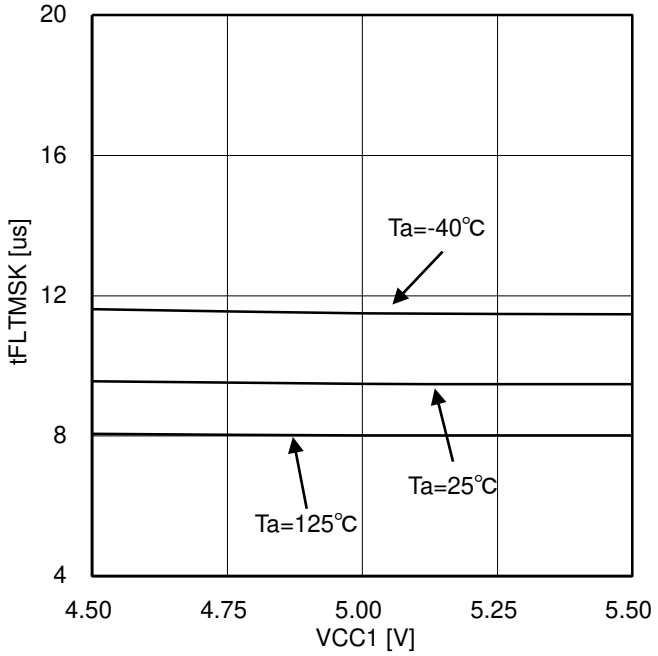


Figure 35. ENA input mask time

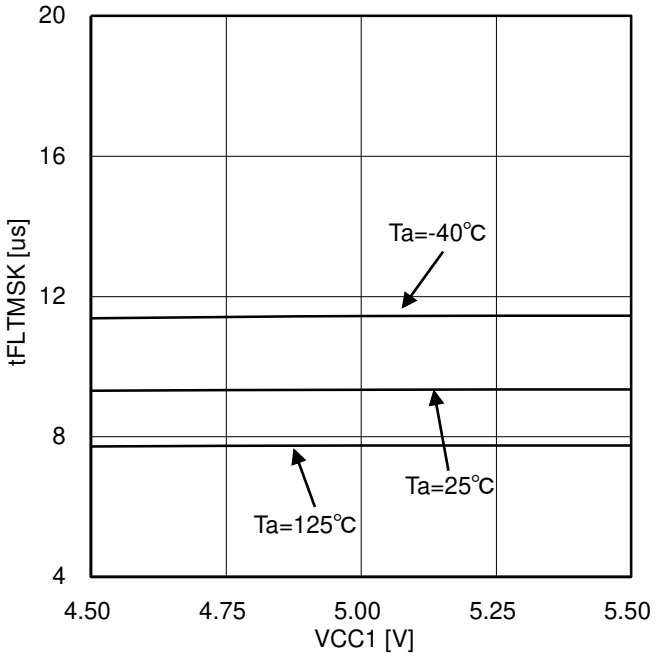


Figure 36. FLT input mask time

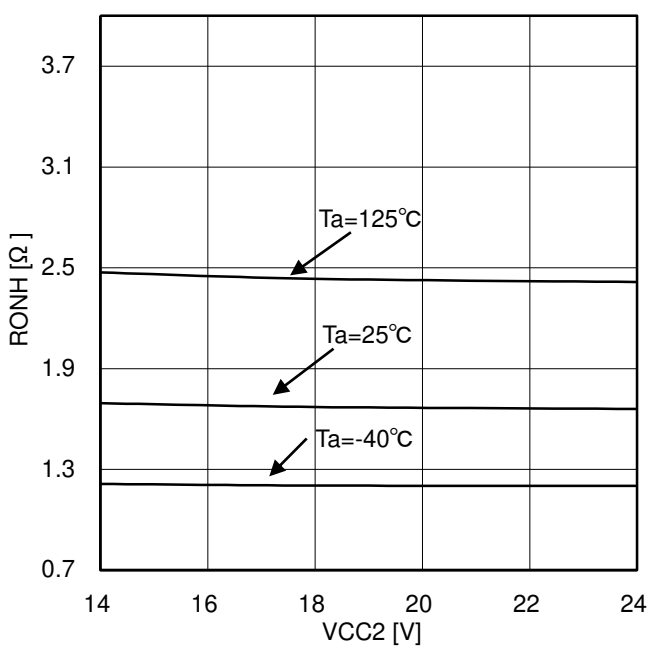


Figure 37. OUT1 ON resistance (Source)

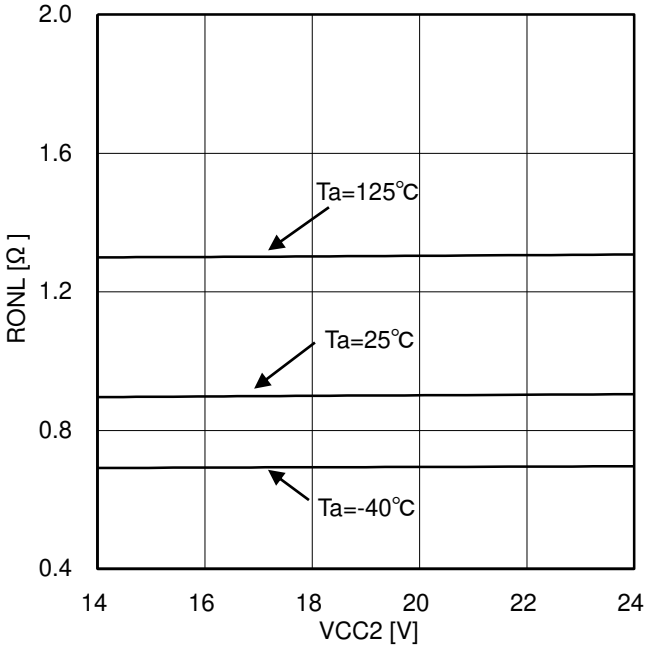


Figure 38. OUT1 ON resistance (Sink)

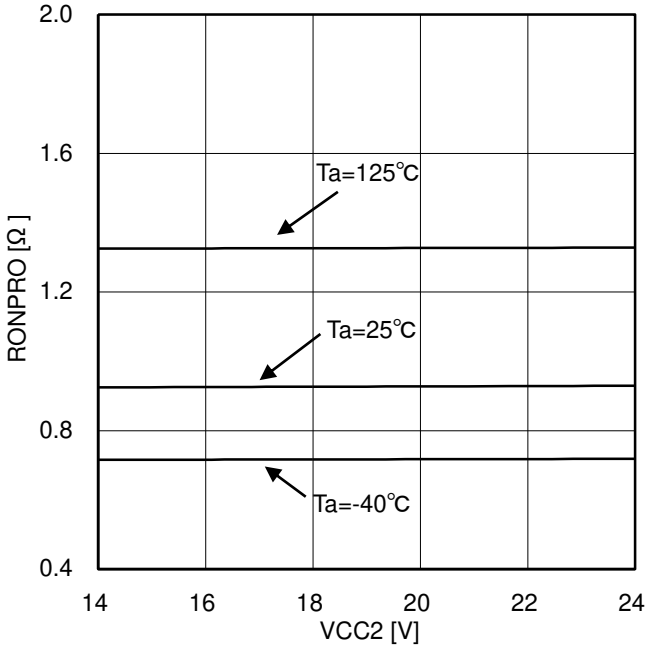


Figure 39. PROOUT ON resistance

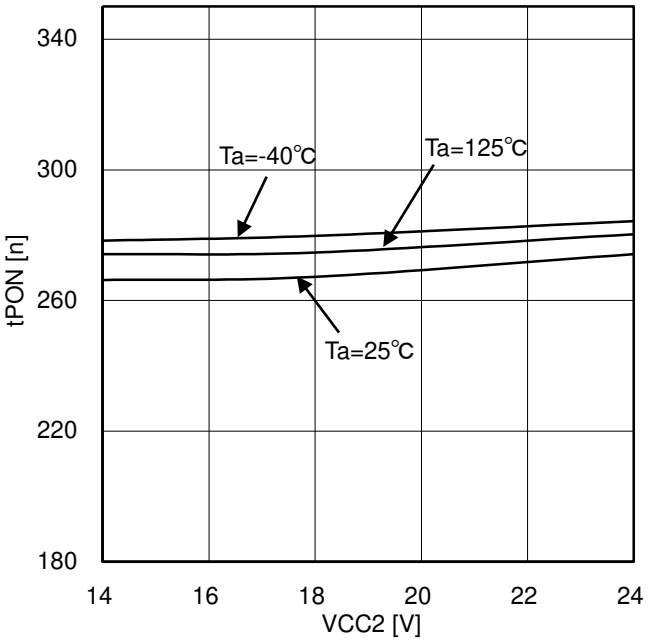


Figure 40. Turn ON time

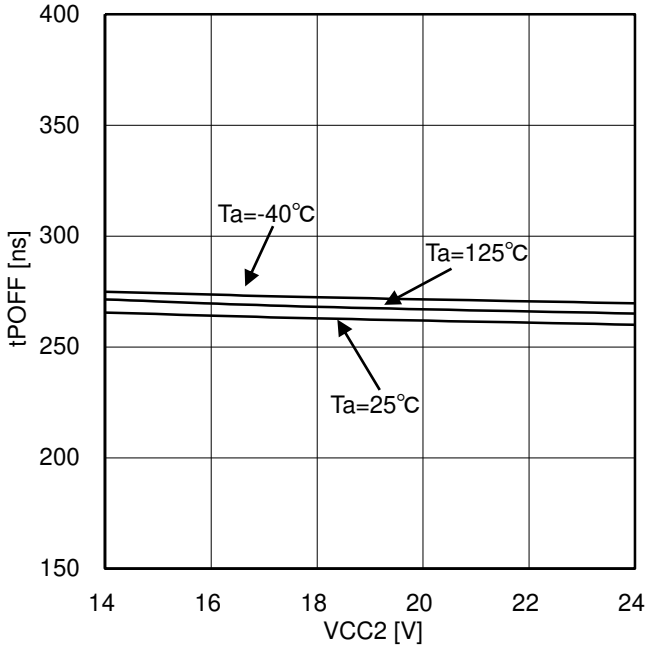


Figure 41. Turn OFF time

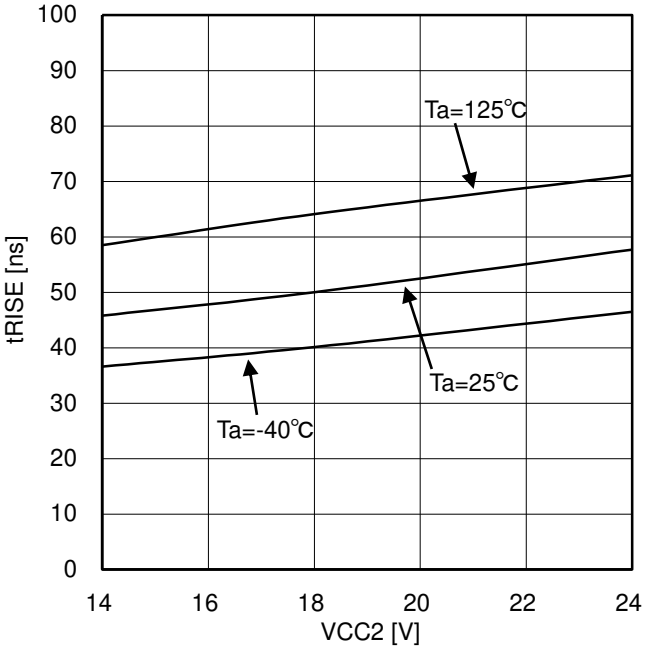


Figure 42. Rise time (10nF between OUT1-VEE2)

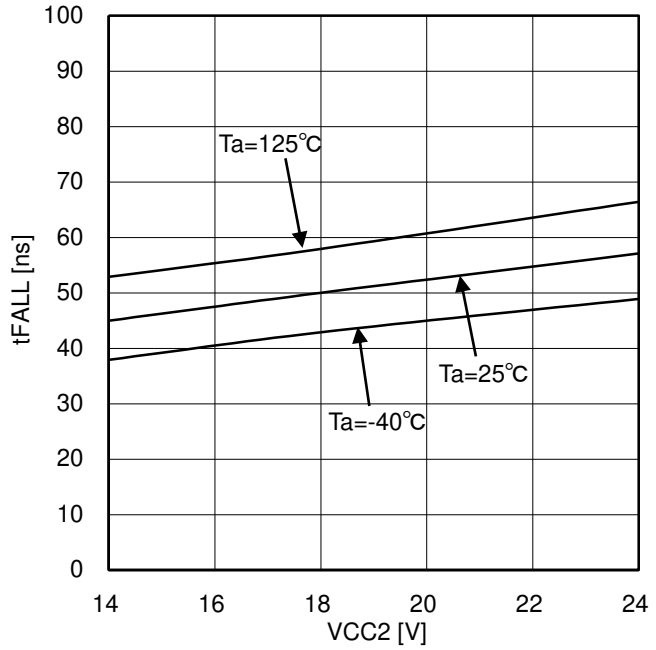


Figure 43. Fall time (10nF between OUT1-VEE2)

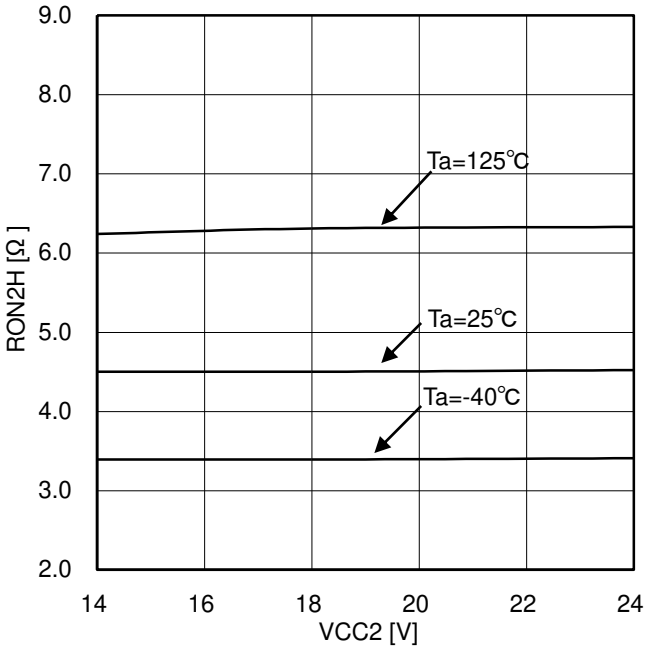


Figure 44. OUT2 ON resistance (Source)

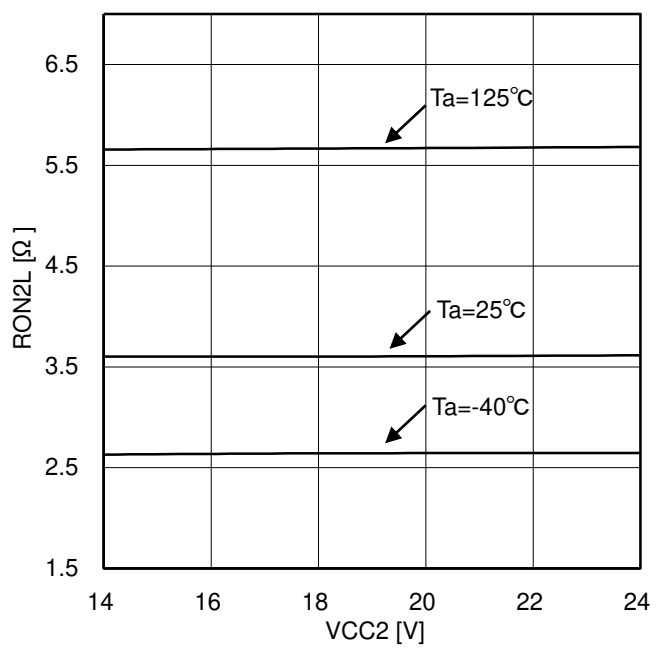


Figure 45. OUT2 ON resistance (Sink)

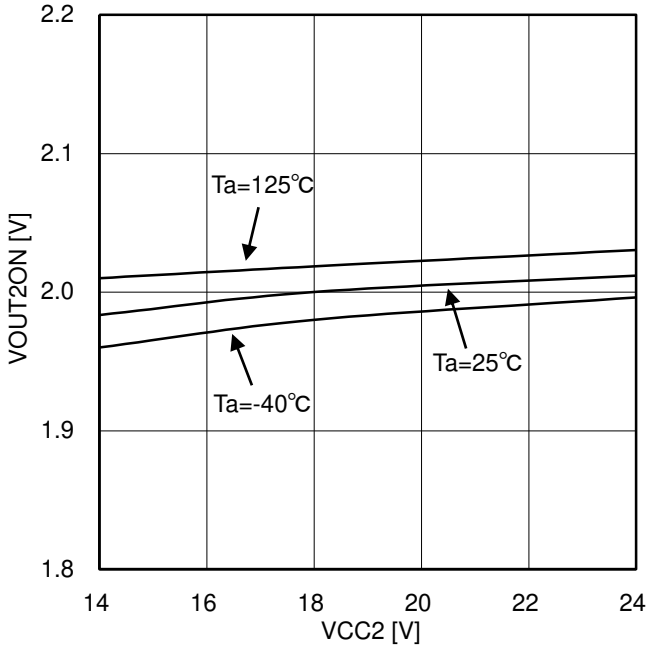


Figure 46. OUT2 ON threshold voltage

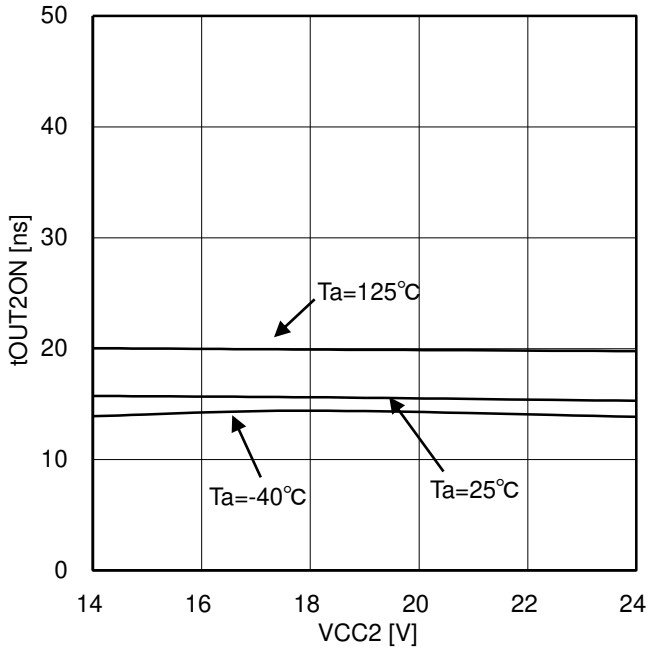


Figure 47. OUT2 output delay time

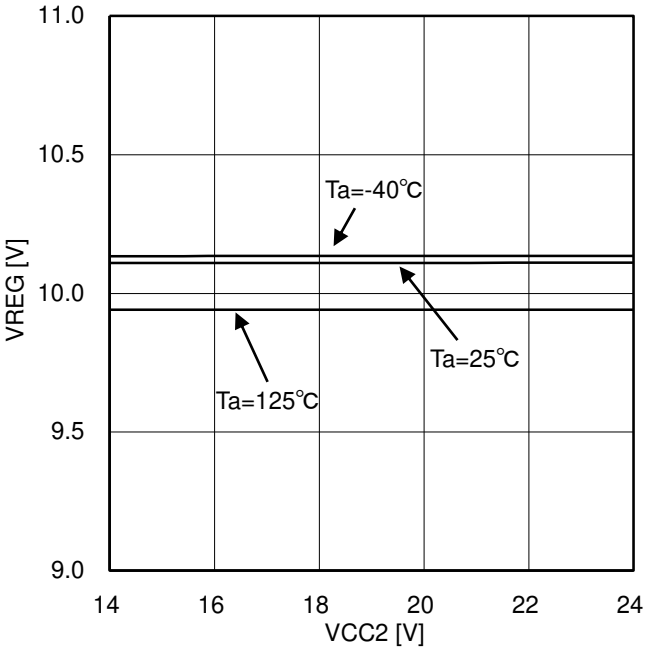


Figure 48. VREG output voltage

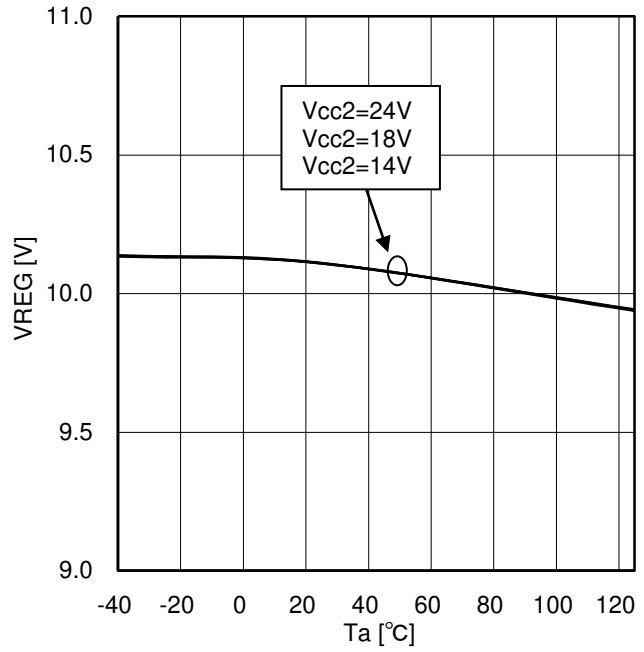


Figure 49. VREG output voltage

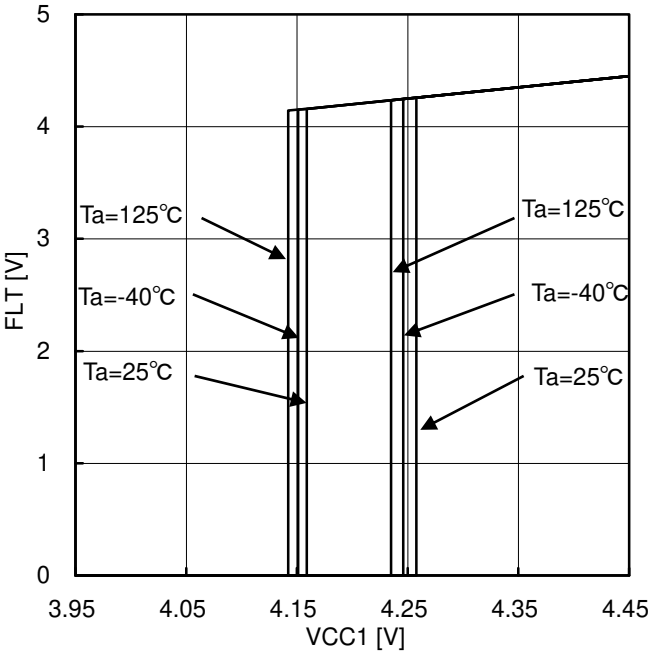


Figure 50. VCC1 UVLO ON/OFF voltage

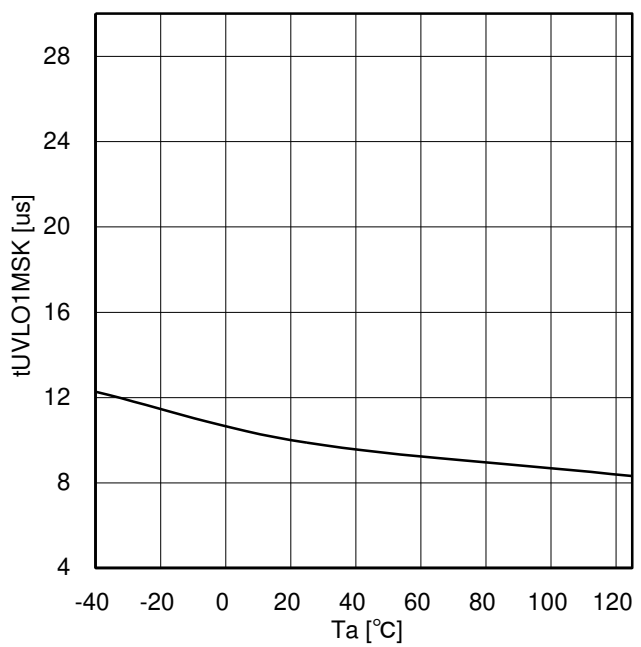


Figure 51. VCC1 UVLO mask time

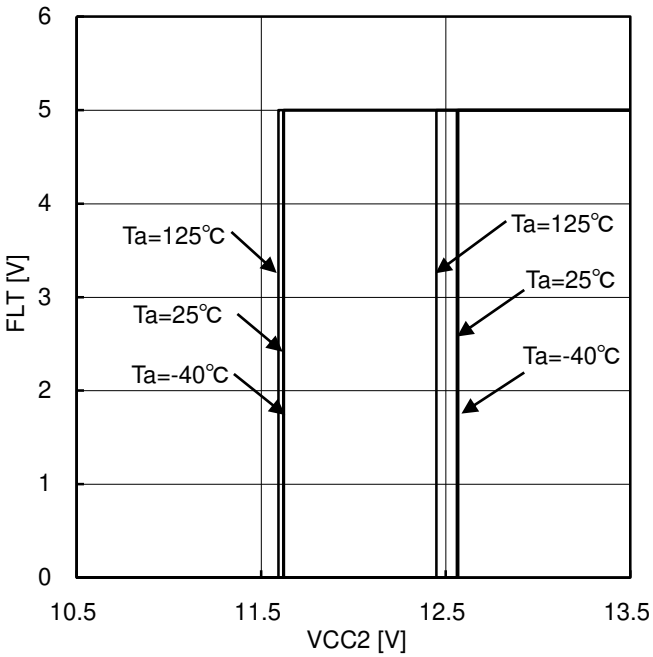


Figure 52. VCC2 UVLO ON/OFF voltage (at VCC1=5V)

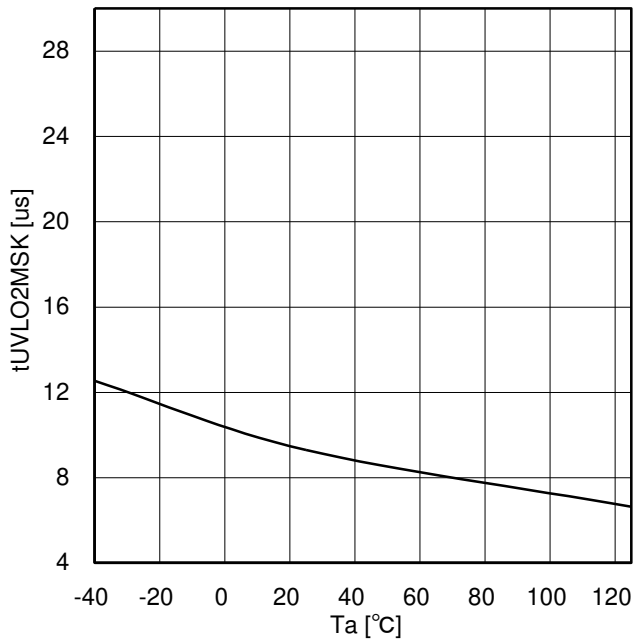


Figure 53. VCC2 UVLO mask time

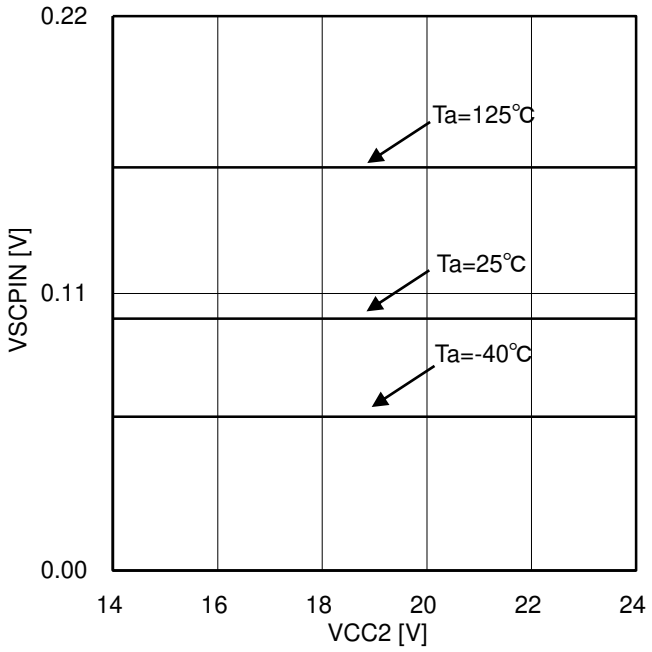


Figure 54. SCPIN input voltage (at ISCPIN=1mA)

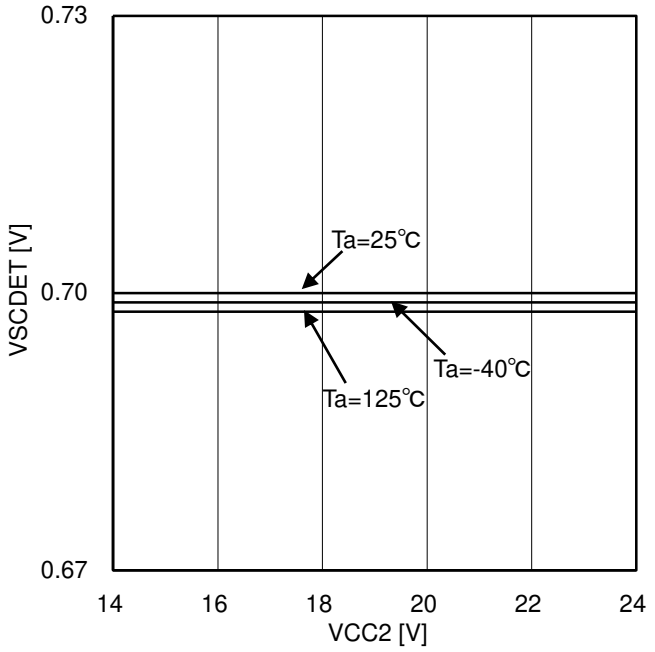


Figure 55. SCP detection voltage

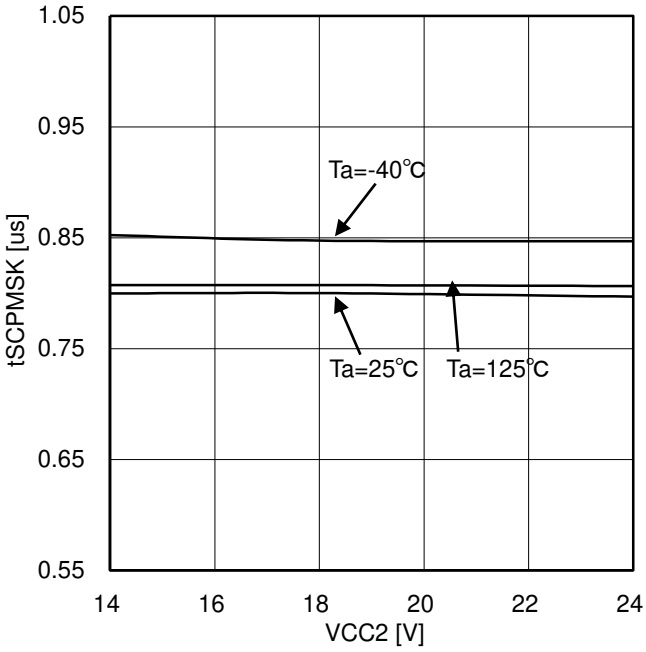


Figure 56. SCP detection mask time

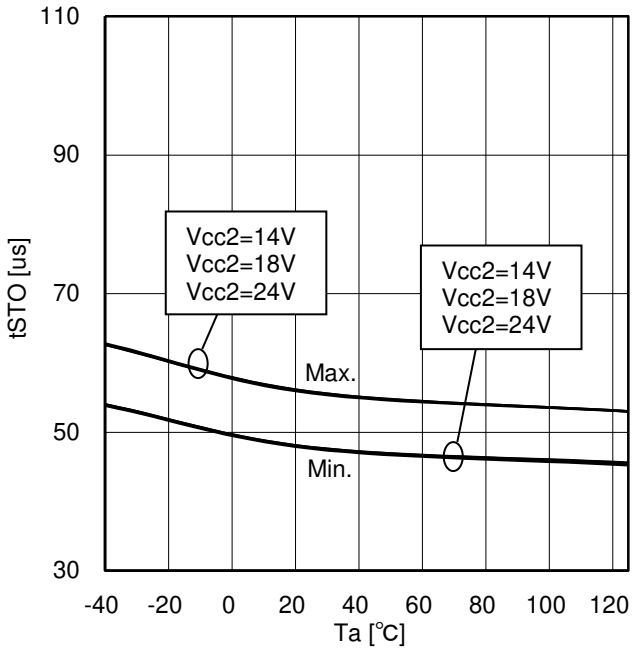


Figure 57. Soft turn OFF release time

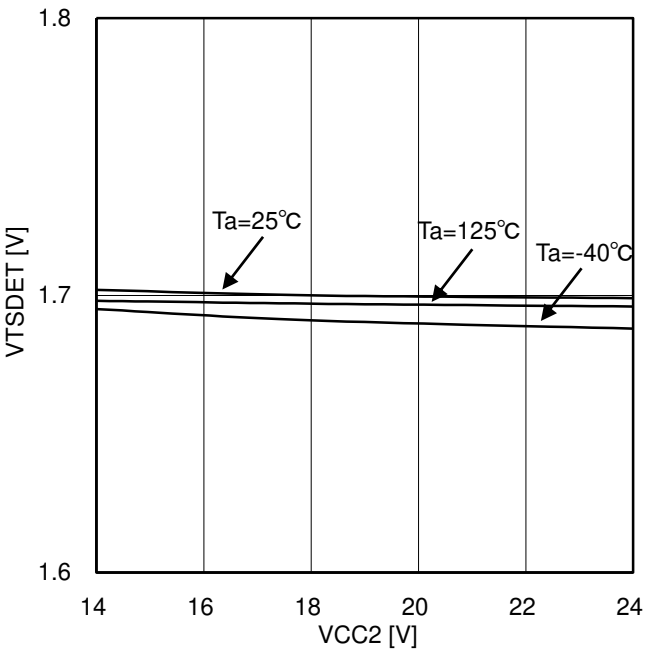


Figure 58. Thermal detection voltage

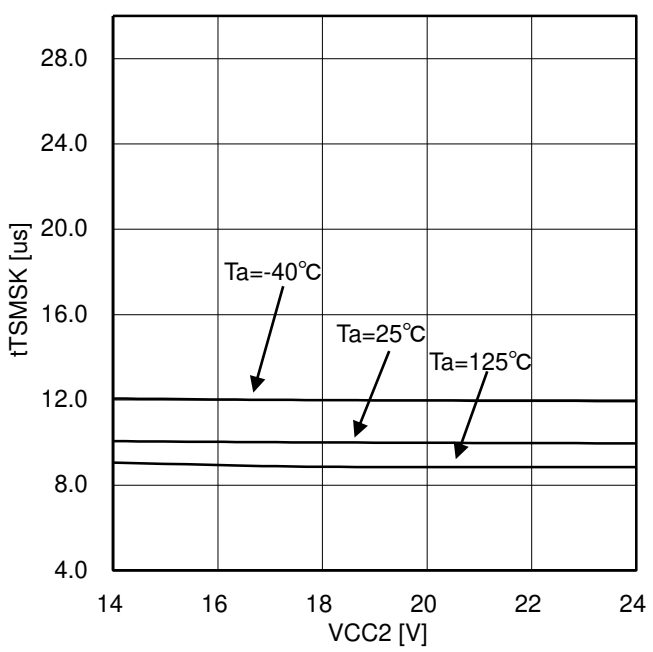


Figure 59. Thermal detection mask time

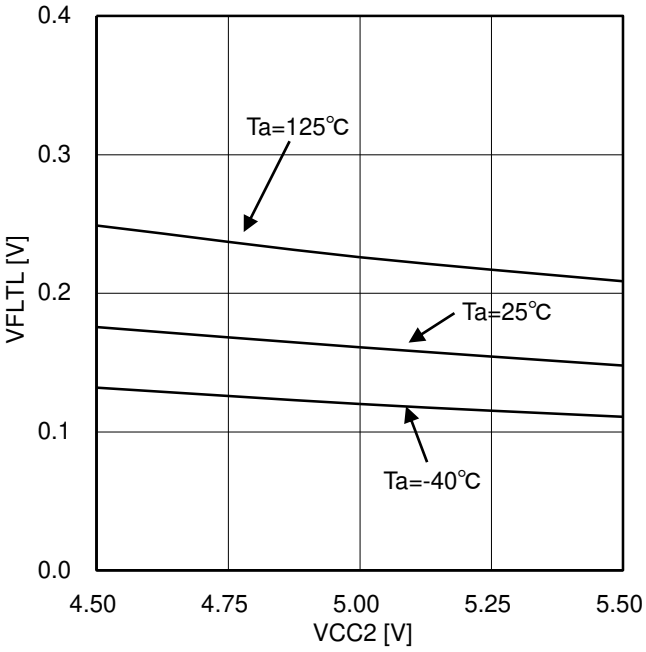


Figure 60. FLT output low voltage (IFLT=5mA)

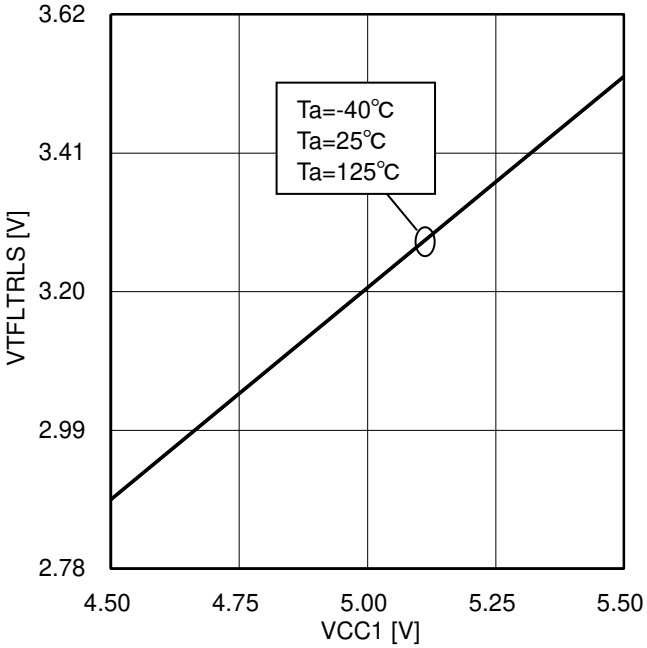


Figure 61. FLTRLS threshold

●Selection of Components Externally Connected

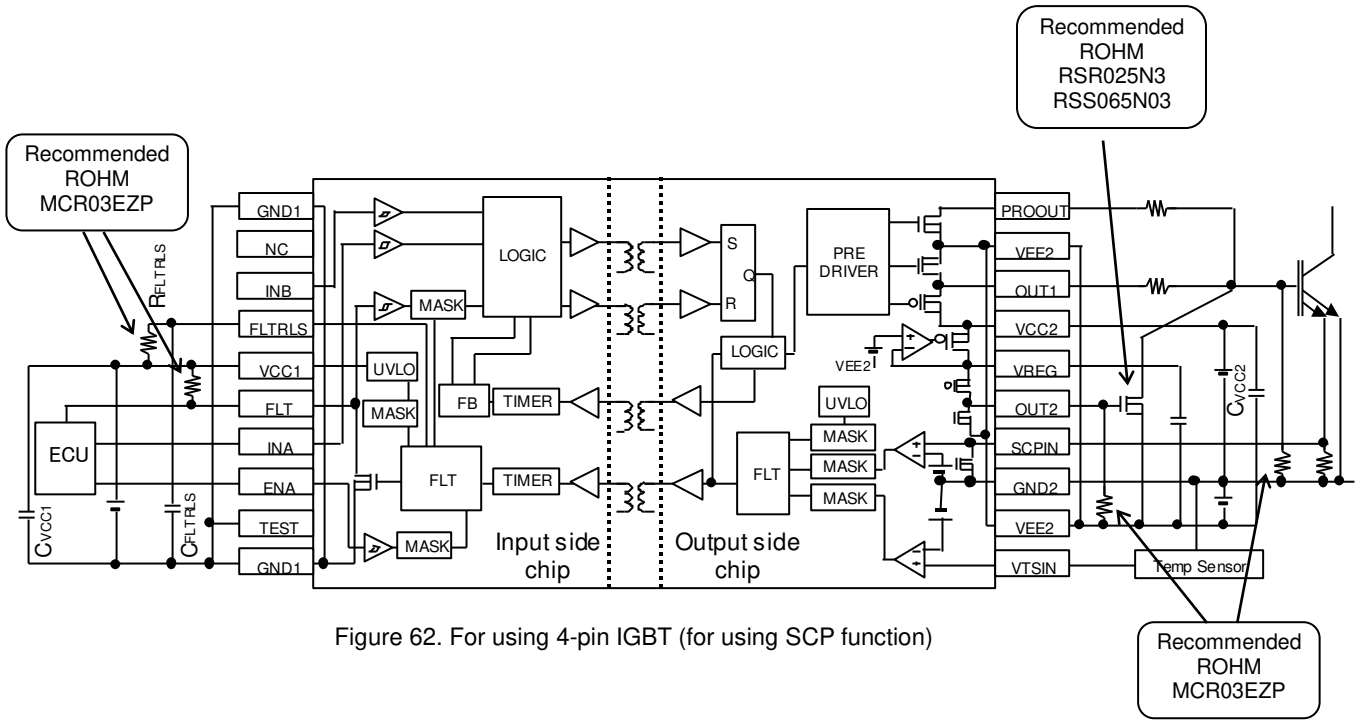


Figure 62. For using 4-pin IGBT (for using SCP function)

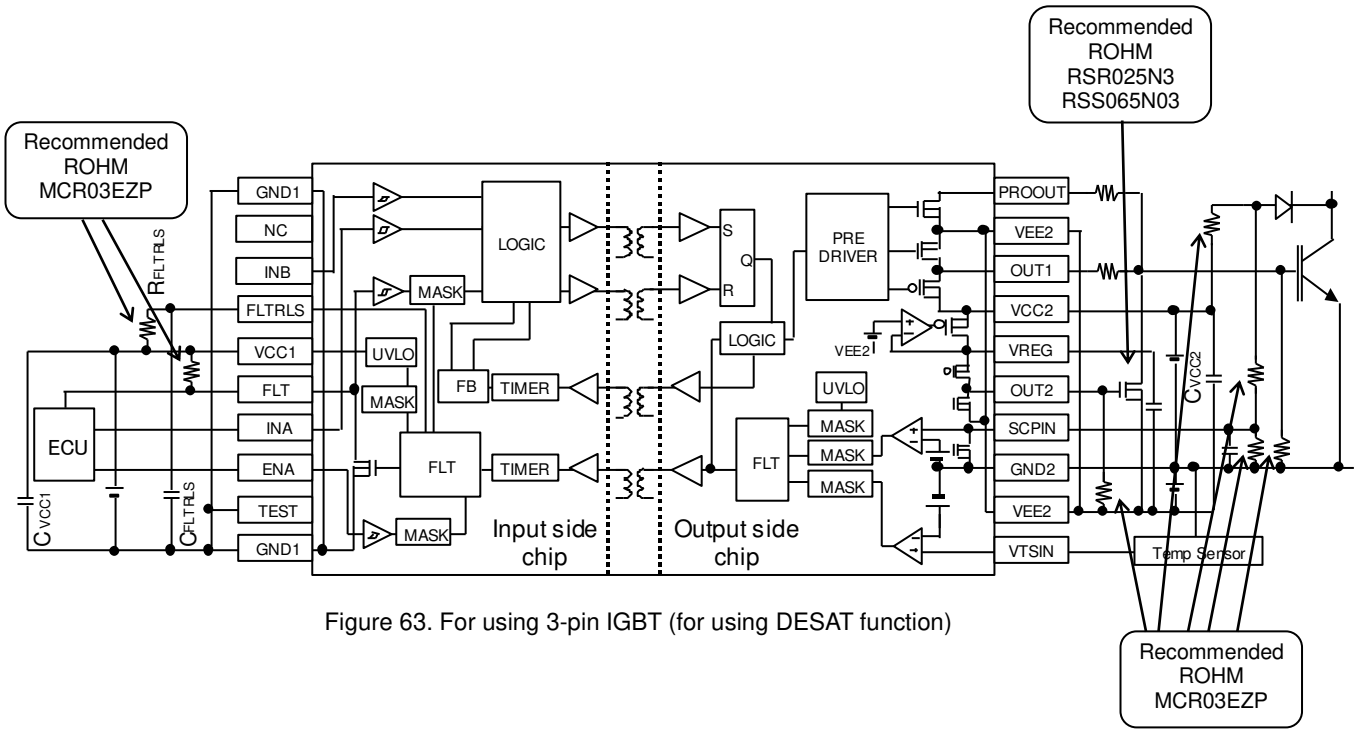


Figure 63. For using 3-pin IGBT (for using DESAT function)