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MOD5441X

Single & Dual Port Ethernet Core Module

MOD54415 (100 Version with RJ-45 | 200 Version with 10-pin header)
MOD54417 (100 Version with 2 X RJ-45 | 200 Version with 20-pin header)

NetBurner

DATASHEET

Key Points

- Use as a high-performance single board computer or add Ethernet connectivity to a new or existing design
- Industrial temperature range (-40°C to 85°C)
- MOD54417 can function as a switch or as two independent ports, each with its own MAC address
- Customize with development kit

Device Connectivity

- Up to two 10/100Mbps Ethernet
- 8 UARTs, 4 I^2C, 2 CAN, 3 SPI, and 1-Wire® support
- SD/MMC and MicroSD flash card ready
- 42 digital I/Os and 2 additional digital inputs
- 16-bit address and data bus with 5 chip selects
- Eight 12-bit analog-to-digital converters (ADC)
- Two 12-bit digital-to-analog converters (DAC)
- Five pulse width modulators (PWM)

Performance and memory

- 32-bit 250 MHz Processor
- 64MB DDR2 RAM and 32MB Flash

Companion development kit

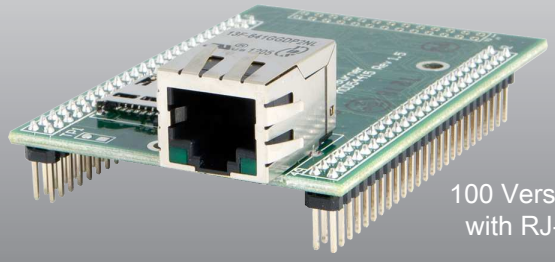
The following is available with the development kit:

- Customize any aspect of operation including web pages, data filtering, or custom network applications
- Development software: NB Eclipse IDE, Graphical debugger, deployment tools, and examples
- Communication software: TCP/IP stack, HTTP web server, FTP, E-mail, and flash file system
- System software: uC/OS RTOS, ANSI C/C++ compiler and linker

The following optional software modules are not included with kit and are sold separately:

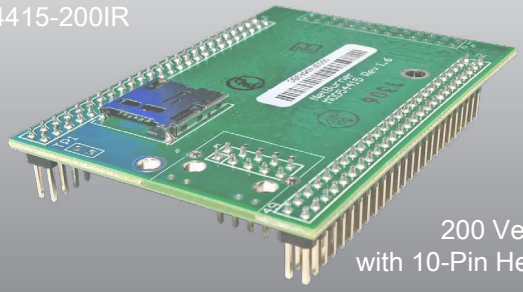
- Embedded SSL & SSH Security Suite (Module License Version)
- SNMP

MOD54415-100IR



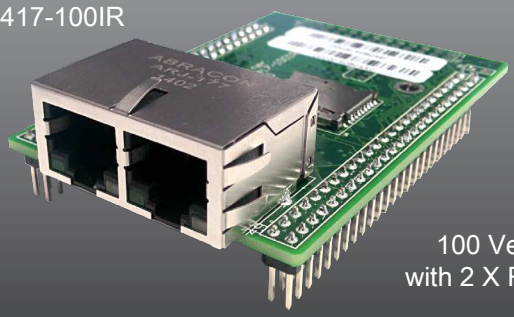
100 Version
with RJ-45

MOD54415-200IR



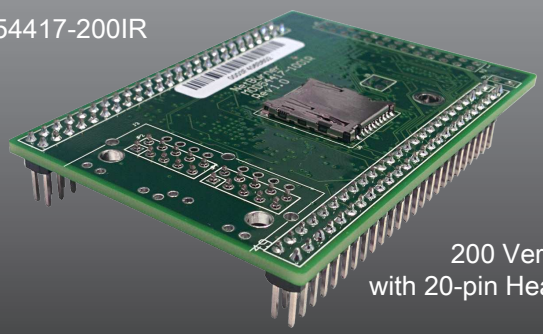
200 Version
with 10-Pin Header

MOD54417-100IR



100 Version
with 2 X RJ-45

MOD54417-200IR



200 Version
with 20-pin Header

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Specifications

Processor and Memory
32-bit Freescale ColdFire 54415 or 54417 running at 250MHz with 64MB DDR2 RAM and 32MB Flash

Network Interface
10/100 BaseT with RJ-45 connector (MOD54415-100IR Version)
10-pin header (MOD54415-200IR Version)
Two 10/100 BaseT with RJ-45 connectors (MOD54417-100IR Version)
Two 10-pin headers (MOD54417-200IR Version)

Data I/O Interface (J1)
- Up to 8 UARTs
- Up to 4 I^2C
- Up to 2 CAN 2.0b controllers
- Up to 3 SPI
- Up to 42 digital I/O + 2 digital inputs
- Up to eight 12-bit analog-to-digital converters (ADC)
- Up to two 12-bit digital-to-analog converters (DAC)
- Up to 5 pulse width modulators (PWM)
- Up to 4 external timer in or outputs
- MicroSD flash card ready
- 1-Wire® interface

Flash Card Support
FAT32 support for SD Cards up to 32GB (requires exclusive use of one SPI port).

Serial Configurations
The UARTs can be configured in the following way:
- 8 TTL ports
- Add external level shifter for RS-232
- Add external level shifter for RS-422/485 (up to two ports)

Note: UART 0/1 also provides RTS/CTS hardware handshaking signals.

LEDs
Link and Speed (100 Version only, on RJ-45)

Physical Characteristics
Dimensions (inches): 2.95” x 2.00”
Weight: 1 oz.
Mounting Holes: 3 x 0.125” dia.

Power
MOD54415 module
3.3VDC @ 410 mA with Ethernet | 3.3VDC @ 360 mA without Ethernet

MOD54415 module mounted on MOD-DEV-70
3.3VDC @ 450 mA with Ethernet | 3.3VDC @ 400 mA without Ethernet

MOD54417 module
3.3VDC @ 520mA with Ethernet | 3.3VDC @ 450 mA without Ethernet

MOD54417 module mounted on MOD-DEV-70
3.3VDC @ 530 mA with Ethernet | 3.3VDC @ 520 mA without Ethernet

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Environmental Operating Temperature
-40° to 85° C

RoHS Compliance
The Restriction of Hazardous Substances guidelines ensure that electronics are manufactured with fewer environment harming materials.

Part Numbers

MOD54415 Ethernet Core Module (100 Version, with RJ-45)
Part Number: MOD54415-100IR

MOD54415 Ethernet Core Module (200 Version, with 10-pin header)
Part Number: MOD54415-200IR

MOD54415 LC Development Kit
Part Number: NNDK-MOD54415LC-KIT
Kit includes all the hardware and software you need to customize the included platform hardware. See NetBurner Store product page for package contents.

MOD54417 Ethernet Core Module (100 Version, with 2 X RJ-45)
Part Number: MOD54417-100IR

MOD54417 Ethernet Core Module (200 Version, with 20-pin header)
Part Number: MOD54417-200IR

MOD54417 LC Development Kit
Part Number: NNDK-MOD54417LC-KIT
Kit includes all the hardware and software you need to customize the included platform hardware. See NetBurner Store product page for package contents.

Embedded SSL & SSH Security Suite (Module License Version)
Part Number: NBLIC-SSL-MODULE
Only required if you are using a development kit.

SNMP V1 (Module License Version)
Part Number: NBLIC-SNMP
Available as an option if you are using a development kit.

Ordering Information

E-mail: sales@netburner.com
Online Store: www.NetBurner.com
Telephone: 1-800-695-6828

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Pinout and Signal Description

The 200 version board has a 10-pin header instead of an RJ-45 jack. This header enables you to relocate the jack to another location or to add a different jack with power over ethernet (PoE) capabilities to your module.

Table 1: MOD54415-200IR Signal Descriptions for JP1 Header

Pin	Signal	Description
1	TX-	Transmit -
2	TX+	Transmit +
3	VCC	3.3V
4	RX+	Receive +
5	RX-	Receive -
6	VCC	3.3V
7	GND	Ground
8	N/C	Not Connected
9	LED	Link LED
10	LED	Speed LED

Table 2: MOD54417-200IR Signal Descriptions for JP1 & JP2 Headers

Pin	Signal	Description
1	TX-	Transmit -
2	TX+	Transmit +
3	RXCT	Receive Centertap
4	RX+	Receive +
5	RX-	Receive -
6	VCC	3.3V LED Power
7	GND	Ground
8	TXCT	Transmit Centertap
9	LED	Link LED
10	LED	Speed LED

Alternate Monitor Boot Jumper

The boot jumper is the unpopulated header ‘TP1’. It can be used to recover from a software or configuration fault.

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The module has two dual in-line 50 pin headers which enable you to connect to one of our standard NetBurner Carrier Boards, or a board you create on your own. Table 2 provides descriptions of pin function of the module header. The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO default to their GPIO functionality. See Table 2-1 in section 2.2 of the MCF5441x Reference Manual for a list of the exceptions.

Table 2: Pinout and Signal Descriptions for J1 Connector [1]

J1 Connector							
Pin	CPU Pin	Function 1	Function 2	Function 3	General Purpose I/O	Description	Max Voltage
1		GND				Ground	-
2		GND				Ground	-
3	E16	VSTBY				Input power 3.3 VDC	3.3VDC
4	G2	R/$\overline{W}$				Data Bus - Read / NOT Write	3.3VDC
5	E1	$\overline{CS1}$		$\overline{NFC\_CE}$	PB4	Data Bus - Chip Select 1 or NAND Flash Controller Chip Enable	3.3VDC
6	B1	$\overline{CS4}$	$\overline{DREQ1}$		PB5	Data Bus - Chip Select 4 or External DMA Request 1	3.3VDC
7	F2	$\overline{CS5}$	$\overline{DACK1}$		PB6	Data Bus - Chip Select 5 or External DMA Acknowledge 1	3.3VDC
8	F1	$\overline{OE/RE}$				Data Bus - Output Enable / Read Enable or Burst Transfer Indicator / Read Enable	3.3VDC
9	D1	$\overline{BE1}$	FB_TSIZE0		PA0	Byte Enable 1 for D16 to D23 (8 bits) or FlexBus Transfer Size 0	3.3VDC
10	F4	$\overline{BE0}$	FB_TSIZE1		PA1	Byte Enable 0 for D24 to D31 (8 bits) or FlexBus Transfer Size 1	3.3VDC
11		TIP Generated				Data Bus - Transfer in Progress[2]	3.3VDC
12	A5	D16				Data Bus - Data 16	3.3VDC
13	H3	$\overline{TA}$		NFC_R/$\overline{B}$	PA4	Data Bus - Transfer Acknowledge or NAND Flash Controller Flash Ready / NOT Busy	3.3VDC
14	D5	D18				Data Bus - Data 18	3.3VDC
15	C6	D17				Data Bus - Data 17	3.3VDC
16	A6	D20				Data Bus - Data 20	3.3VDC
17	B6	D19				Data Bus - Data 19	3.3VDC
18	A7	D22				Data Bus - Data 22	3.3VDC
19	D6	D21				Data Bus - Data 21	3.3VDC
20	B7	D24				Data Bus - Data 24	3.3VDC

Note:
1. Active low signals, such as $\overline{RESET}$, are indicated with an overbar.
2. The TIP signal is the logical AND of *CS1, *CS4 and *CS5. TIP can used to control an external data bus buffer for the data bus signals. An example circuit design can be found on the Module Development Board schematic. An external data bus buffer is recommended for any designs that use data bus signals D16-D31.

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J1 Connector (continued)							
Pin	CPU Pin	Function 1	Function 2	Function 3	General Purpose I/O	Description	Max Voltage
21	C7	D23				Data Bus - Data 23	3.3VDC
22	A8	D26				Data Bus - Data 26	3.3VDC
23	D7	D25				Data Bus - Data 25	3.3VDC
24	B8	D28				Data Bus - Data 28	3.3VDC
25	D8	D27				Data Bus - Data 27	3.3VDC
26	C8	D30				Data Bus - Data 30	3.3VDC
27	A9	D29				Data Bus - Data 29	3.3VDC
28	K15	$\overline{\text{RESET}}$				Processor Reset Input	3.3VDC
29	B9	D31				Data Bus - Data 31	3.3VDC
30	L16	$\overline{\text{RSTOUT}}$				Processor Reset Output	3.3VDC
31	G1	CLK			PB7	Internal Bus Clock[2]	3.3VDC
32	F3	A0				Data Bus - Address 0	3.3VDC
33	C2	A1				Data Bus - Address 1	3.3VDC
34	B2	A2				Data Bus - Address 2	3.3VDC
35	A2	A3				Data Bus - Address 3	3.3VDC
36	E3	A4				Data Bus - Address 4	3.3VDC
37	D3	A5				Data Bus - Address 5	3.3VDC
38	E4	A6				Data Bus - Address 6	3.3VDC
39	C3	A7				Data Bus - Address 7	3.3VDC
40	B3	A8				Data Bus - Address 8	3.3VDC
41	C4	A9				Data Bus - Address 9	3.3VDC
42	C5	A10				Data Bus - Address 10	3.3VDC
43	B4	A11				Data Bus - Address 11	3.3VDC
44	D4	A12				Data Bus - Address 12	3.3VDC
45	A3	A13				Data Bus - Address 13	3.3VDC
46	A4	A14				Data Bus - Address 14	3.3VDC
47	B5	A15				Data Bus - Address 15	3.3VDC
48		VCC3V				Input power 3.3 VDC	3.3VDC
49		GND				Ground	-
50		GND				Ground	-

Note:

1. Active low signals, such as $\overline{\text{RESET}}$, are indicated with an overbar.
2. Internal bus clock is one-half the core/system clock $f_{sys/2}$

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Table 3: Pinout and Signal Descriptions for J2 Connector [1]

J2 Connector								
Pin	CPU Pin	Rev	Function 1	Function 2	Fuction 3	General Purpose I/O	Description	Max Voltage
1			GND				Ground	-
2			VCC3V				Input power 3.3 VDC	3.3VDC
3	B10		UART0_RX	I2C4_SDA	SPI2_SIN	PF4	UART 0 Receive or I²C 4 Serial Data or SPI 2 Serial Data In[2,3]	3.3VDC
4	D11		UART0_TX	I2C4_SCL	SPI2_SOUT	PF3	UART 0 Transmit or I²C 4 Serial Clock or SPI 2 Serial Data Out[2,3]	3.3VDC
5	J4 H4		VDDA_DAC_ADC				ADC and DAC Supply Voltage 3.3V@24mA, By default VDDA_DAC_ADC is used as the analog reference. If you wish to use a different reference voltage value, the Iternate References inputs are: ADC_IN0 for ADC_IN1-3, ADC_IN4 for ADC_IN5-7	3.3VDC
6	H1		ADC_IN0				Analog to Digital Converter 0 Input	3.3VDC
7	J1		ADC_IN1				Analog to Digital Converter 1 Input	3.3VDC
8	J2		ADC_IN2				Analog to Digital Converter 2 Input	3.3VDC
9	K4		ADC_IN3	DAC0_OUT			Analog to Digital Converter 3 Input or Digital to Analog Coverter 0 Output	3.3VDC
10	G4		ADC_IN4				Analog to Digital Converter 4 Input	3.3VDC
11	J3		ADC_IN5				Analog to Digital Converter 5 Input	3.3VDC
12	H2		ADC_IN6				Analog to Digital Converter 6 Input	3.3VDC
13	K3		ADC_IN7	DAC1_OUT			Analog to Digital Converter 7 Input or Digital to Analog Converter 1 Output	3.3VDC
14	H5 J5		VSSA_ADC VSSA_DAC_ADC				ADC and DAC Reference Ground (required when using ADC or DAC)	-
15	A12		SSI0_MCLK	SSI_CLKIN	SIM1_CLK	PH4	SSI 0 Serial Master Clock or SSI Clock Input or SIM 1 Clock	3.3VDC
16	A13		SSI0_BCLK	UART7_RX	SIM1_PD	PH3	SSI 0 Serial Bit Clock or UART 7 Receive or SIM 1 Card Insertion Detect Signal[2]	3.3VDC
17	A14 A15	1.7+	USB0_DM USBH_DM			Input only	USB- On-the-Go (default configuration) USB- Host (see appnote for host mode configuration)	3.3VDC
	C12	1.6	SSI0_RX	I2C2_SDA	SIM1_VEN	PH7	SSI 0 Serial Receive or I²C 2 Serial Data or SIM 1 Power Supply Enable Signal[3]	3.3VDC
18	B14 B15	1.7+	USB0_DP USBH_DP			Input only	USB+ On-the-Go (default configuration) USB+ Host (see appnote for host mode configuration)	3.3VDC
	C13	1.6	SSI0_TX	I2C2_SCL	SIM1_DATA	PH6	SSI 0 Serial Transmit or I²C 2 Serial Clock or SIM 1 Bidirectional Transmit/ Receive Data Signal[3]	3.3VDC
19	N2		UART2_TX	PWM_B3	SSI1_TX	PE3	UART 2 Transmit or PWM B3 Output Signal/Input Capture or SSI 1 Serial Transmit[2]	3.3VDC
20	E15		SSI0_FS	UART7_TX	SIM1_RST	PH5	SSI 0 Serial Frame Sync or UART 7 Transmit or SIM 1 Reset Signal[2]	3.3VDC
21	C9		UART1_RX	I2C5_SDA	SPI3_SIN	PE0	UART 1 Receive or I²C 5 Serial Data or SPI 3 Serial Data In[2,3]	3.3VDC
22	D9		UART1_TX	I2C5_SCL	SPI3_SOUT	PF7	UART 1 Transmit or I²C 5 Serial Clock or SPI 3 Serial Data Out[2,3]	3.3VDC
23	D10		$\overline{\text{UART1\_RTS}}$	UART5_RX	SPI3_PCS0	PE1/RGPIO	UART 1 Request To Send or UART 5 Receive or SPI 2 Peripheral Select 0 Chip[2]	3.3VDC
24	C10		$\overline{\text{UART1\_CTS}}$	UART5_TX	SPI3_SCK	PE2/RGPIO	UART 1 Clear To Send or UART 5 Transmit or SPI 3 Serial Clock[2]	3.3VDC
25	A10		SDHC_CLK	PWM_A0	SPI1_SCK	PG5	SDHC Clock or PWM A0 Output Signal/Input or SPI 1 Serial Clock	3.3VDC

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J2 Connector (continued)							
Pin	CPU Pin	Function 1	Function 2	Function 3	General Purpose I/O	Description	Max Voltage
26	M1	$\overline{\text{IRQ3}}$	SPI0_PCS3	USBH_VBUS_EN	PC3	External Interrupt 3 or SPI 0 Chip Select 3 or USB Host VBUS Enable	3.3VDC
27	C11	SDHC_CMD	PWM_B0	SPI1_SIN	PG6	SDHC Command Line or PWM B0 Output Signal/Input Capture or SPI 1 Serial Data In	3.3VDC
28	B12	SDHC_DAT0	PWM_B2	SPI1_SOUT	G7	SDHC DAT0 Line or PWM B2 Output Signal/Input or Serial Data Out	3.3VDC
29	E13	$\overline{\text{UART0\_CTS}}$	UART4_TX	SPI2_SCK	PF6/RGPIO	UART 0 Clear To Send or UART 4 Transmit or SPI 2 Serial Clock[2]	3.3VDC
30	B13	SDHC_DAT3	PWM_A1	SPI1_PCS0	PF2	SDHC DAT3 Line / Card Detection or PWM A1 Output Signal/Input Capture or SPI 1 Chip Select 0	3.3VDC
31	P1	UART2_RX	PWM_A3	SSI1_RX	PE4	UART 2 Receive or PWM A3 Output Signal/Input Capture or SSI 1 Serial Receive[2]	3.3VDC
32	G13	T3IN/PWM_ EXTA3	T3OUT	USBO_VBUS_EN	PD2/RGPIO	Timer Input 3 / Alternate PWM control signal 3 or Timer Output 3 or USB On-The-Go VBUS Enable	3.3VDC
33	H14	T2IN/PWM_ EXTA2	T2OUT	SDHC_DAT2	PD1/RGPIO	Timer Input 2 / Alternate PWM control signal 2 or Timer Output 2 or SDHC DAT2 Line / Read Wait	3.3VDC
34	H13	T1IN/PWM_ EXTA1	T1OUT	SDHC_DAT1	PD0/RGPIO	Timer Input 1 / Alternate PWM control signal 1 or Timer Output 1 or SDHC DAT1 Line / Interrupt Detect	3.3VDC
35	D12	SDHC_DAT1	PWM_A2	SPI1_PCS1	PF0	SDHC DAT1 Line or PWM A2 Output Signal/Input Capture or SPI Chip Select 1	3.3VDC
36	H15	T0IN/PWM_ EXTA0	T0OUT	USBO_VBUS_OC	PE7/RGPIO	Timer Input 0 / Alternate PWM control signal 0 or Timer Output 0 or USB On-The-Go VBUS Over-Current	3.3VDC
37	N11	OW-DAT	$\overline{\text{DACK0}}$		PD3/RGPIO	1-Wire Data Signal or DMA Acknowledge 0	3.3VDC
38	B11	$\overline{\text{UART0\_RTS}}$	UART4_RX	SPI2_PCS0	PF5/RGPIO	UART 0 Request To Send or UART 4 Receive or SPI 2 Chip Select 0[1]	3.3VDC
39	G14	I2C0_SDA	UART8_RX	CAN0_RX	PB1	I²C 0 Serial Data or UART 8 Receive or CAN 0 Receive[2,3]	3.3VDC
40	E14	SDHC_DAT2	PWM_B1	SPI1_PCS2	PF1	SDHC DAT2 Line / Read Wait or PWM B1 Output Signal/Input Capture or SPI 1 Chip Select 2	3.3VDC
41	D15	CAN1_RX	UART9_RX	I2C1_SDA	PC7	CAN 1 Receive or UART 9 Receive or I²C 1 Serial Data[2,3]	3.3VDC
42	G15	I2C0_SCL	UART8_TX	CAN0_TX	PB2	I²C 0 Serial Clock or UART 8 Transmit or CAN 0 Transmit[2,3]	3.3VDC
43	M2	$\overline{\text{IRQ2}}$	SPI0_PCS2	USBH_VBUS_OC	PC2	External Interrupt 2 or SPI 0 Chip Select 2 or USB Host VBUS Over-Current	3.3VDC
44	D14	CAN1_TX	UART9_TX	I2C1_SCL	PB0	CAN 1 Transmit or UART 9 Transmit or I²C 1 Serial Clock[2,3]	3.3VDC
45	F13	$\overline{\text{IRQ1}}$			PC1	External Interrupt 1	3.3VDC
46		GND				Ground	-
47	N1	$\overline{\text{IRQ6}}$		USB_CLKIN	PC5	External Interrupt 6 or USB Clock In	3.3VDC
48	F12	$\overline{\text{IRQ7}}$			PC6	External Interrupt 7	3.3VDC
49		GND				Ground	-
50		VCC3V				Input power 3.3 VDC	3.3VDC

Note:
1. Active low signals, such as $\overline{\text{RESET}}$, are indicated with an overbar.
2. Each UART can be clocked from an internal or external source. For external clocks, each UARTn can be clocked by the corresponding DTn_IN vnput pin.
3. If using I2C, the module must add pull-up resistors to SDA/SCL.

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