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# **Power Amplifier**

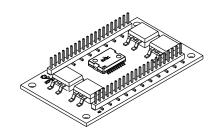


#### **FEATURES**

- Low Cost Integrated Solution
- Output Current > 10A within SOA
- Internal Power Dissipation 35W Per Channel
- 167V/μs Slew Rate

### **APPLICATIONS**

Piezoelectric Actuation For Ink Jet Printer Nozzles



### **DESCRIPTION**

The MP103 is a high voltage, high output current dual channel operational amplifier for driving capacitive loads such as piezo devices use in ink jet printing applications. The MP103 utilizes proprietary IC's combined with discrete semiconductor and passive elements on a thermally conductive insulated metal substrate, delivering very high power from a compact module. The amplifier gain is fixed at 65 V/V when the feedback pin is connected to the  $V_{OUT}$  pin. Internal compensation provides optimum slew rate and ensures stability. The only external components required are the current limit resistors  $R_{LIM}$ , a series isolation resistor  $R_{S}$  (when driving a capacitative load) and the power supply bypass capacitors.

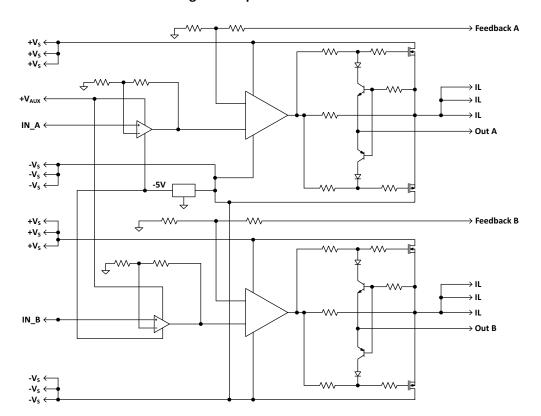
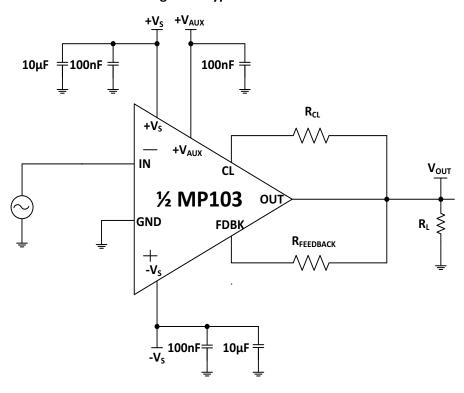


Figure 1: Equivalent Schematic



# **TYPICAL CONNECTION**

**Figure 2: Typical Connection** 





# PINOUT AND DESCRIPTION TABLE

**Figure 3: External Connections** 

1 2 3 4 5 6 7 8 9 10 11 12 13	NC NC	MP103 (viewed from backplate)	-Vs_A -Vs_A -Vs_A NC IN_A NC FBK_A NC HVAUX NC GND NC FBK_B NC IN_B	42 41 40 39 38 37 36 35 34 33 32 31 30 29
11 12 13 14 15	NC NC NC NC OUT_B	•	FBK_B	30 29 28 27 26
16 17 18 19 20	NC NC +V <sub>s</sub> _B +V <sub>s</sub> _B +V <sub>s</sub> _B		CL_B CL_B -Vs_B -Vs_B -Vs_B	25 24 23 22 21

Pin Number	Name	Description		
1, 2, 3	+Vs_A	The positive supply rail for channel A.		
4, 5, 6	CL_A	Connect to the current limit resistor. Output current flows into/out of these pins through $R_{\text{CL}}$ . The output pin and the load are connected to the other side of $R_{\text{CL}}$ .		
8	OUT_A	The output for channel A. Connect this pin to load and to the feedback resistor.		
15	OUT_B	The output for channel B. Connect this pin to load and to the feedback resistor.		
18, 19, 20	+Vs_B	The positive supply rail for channel B.		
21, 22, 23	-Vs_B	The negative supply rail for channel B. Internally connected to -Vs_A.		
24, 25, 26	CL_B	Connect to the current limit resistor. Output current flows into/out of these pins through $R_{\text{CL}}$ . The output pin and the load are connected to the other side of $R_{\text{CL}}$ .		
28	IN_B	The input for channel B.		
30	The feedback pin for channel B. This pin must be connected to OUT_B to feedback loop. When connected directly to OUT_B the closed loop volta channel B is 65 V/V. The gain can be increased by inserting a 1/4 W r between FBK_B and OUT_B.			
32	GND	Ground.		
34	Vaux	+24 V power supply pin. A 24 V supply is required for operation of front end small signal circuitry.		
feedback loop. When connected directly to OUT_A the closed loop voltage		The feedback pin for channel A. This pin must be connected to OUT_A to close the feedback loop. When connected directly to OUT_A the closed loop voltage gain of channel A is 65 V/V. The gain can be increased by inserting a 1/4 W resistor between FBK_A and OUT_A.		
38	IN_A	The input for channel A.		
40, 41, 42	-Vs_A	The negative supply rail for channel A. Internally connected to -Vs_B.		
All Others	NC	No connection.		



### **ELECTRICAL SPECIFICATIONS**

**Notes:** a) All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and  $T_C = 25$ °C.

**b)**  $+V_S$  and  $-V_S$  denote the positive and negative supply voltages to the output stages.  $+V_{AUX}$  denotes the positive supply voltage to the input stages.

### **ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage, +V <sub>S</sub> to -V <sub>S</sub>	+V <sub>S</sub> to -V <sub>S</sub>		200	V
Supply Voltage, –V <sub>S</sub>	-V <sub>S</sub>	-30		V
Supply Voltage, +V <sub>AUX</sub>	+V <sub>AUX</sub>		30	V
Output Current, pk, per Channel (Within SOA)	I <sub>O(PK)</sub>		15	А
Power Dissipation, internal, Each Channel	$P_{D}$		35	W
Input Voltage	V <sub>IN</sub>	-5	V <sub>AUX</sub>	V
Temperature, pin solder, 10s			225	°C
Temperature, junction <sup>1</sup>	T <sub>J</sub>		150	°C
Temperature Range, storage		-40	105	°C

<sup>1.</sup> Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.

### **INPUT**

Parameter	Test Conditions	Min	Тур	Max	Unit
Offset Voltage		-6.7	±2	6.7	mV
Offset Voltage vs. Temperature	Full temp range		±2		μV/°C
Bias Current, initial <sup>1</sup>		-6.6	±3.3	6.6	μΑ

<sup>1.</sup> Doubles for every 10°C of case temperature increase.

# **GAIN**

Parameter	Test Conditions	Min	Тур	Max	Unit
Fixed Gain	Feedback connected to V <sub>OUT</sub>	63.5	65	66.5	V/V
Gain Bandwidth, -3db	C <sub>L</sub> = 47nF		230		kHz
Power Bandwidth, 130 V <sub>p-p</sub>	+V <sub>S</sub> = 145V, -V <sub>S</sub> = -15V		230		kHz



# OUTPUT

Parameter	Test Conditions	Min	Тур	Max	Unit
Voltage Swing	I <sub>O</sub> = 10A	+V <sub>S</sub> - 15	+V <sub>S</sub> - 9		V
Voltage Swing	I <sub>O</sub> = 10A	-V <sub>S</sub> + 15	-V <sub>S</sub> + 14		V
Current, Peak, Source			12		А
Slew Rate	$R_s = 1 \Omega$ , $C_L = 47nF$ , $V_{in} \ge 8V_{p-p}$	167			V/µs

### **POWER SUPPLY**

Parameter	Test Conditions	Min	Тур	Max	Unit
Voltage, -V <sub>S</sub>		-7	-15	-20	V
Voltage, +V <sub>AUX</sub>			24	25	V
Voltage, +V <sub>S</sub>		-V <sub>S</sub> + 20	145	-V <sub>S</sub> + 200	V
Current, quiescent, -V <sub>S</sub>			19	26	mA
Current, quiescent, +V <sub>AUX</sub>			13.5	15	mA
Current, quiescent, +V <sub>S</sub>			1	5	mA

### THERMAL

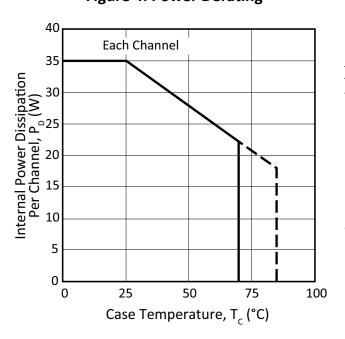
Parameter	Test Conditions	Min	Тур	Max	Unit
Resistance, AC, junction to case <sup>1</sup>	Full temp range, f ≥ 60 Hz		1.5	1.75	°C/W
Resistance, DC, junction to case	Full temp range, f < 60 Hz		3.1	3.6	°C/W
Resistance, junction to air	Full temp range		12.5	14	°C/W
Temperature Range, case		0		70	°C

<sup>1.</sup> Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

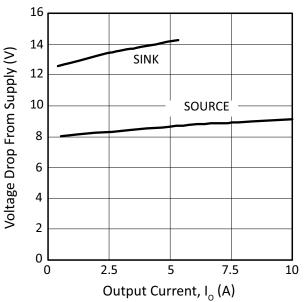


# **TYPICAL PERFORMANCE GRAPHS**

**Figure 4: Power Derating** 

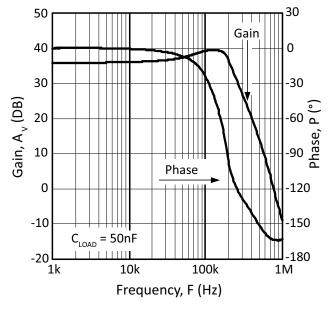


**Figure 5: Output Voltage Swing** 



**Figure 6: Frequency Response** 

**Figure 7: Quiescent Current** 



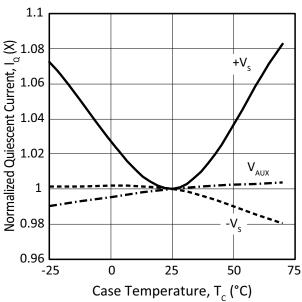




Figure 8: Offset Voltage vs. Temperature

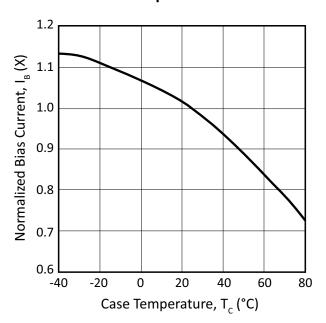


Figure 10: Max. Output Pulse Duty Cycle

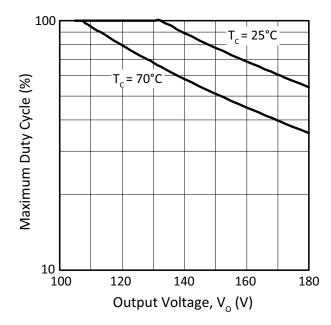


Figure 9: Max. DC Output Voltage

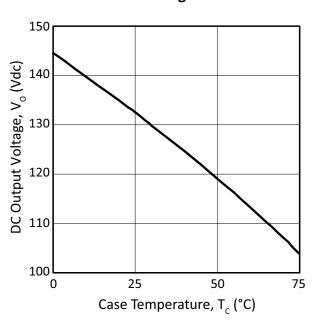


Figure 11: Input Bias Current vs.
Temperature

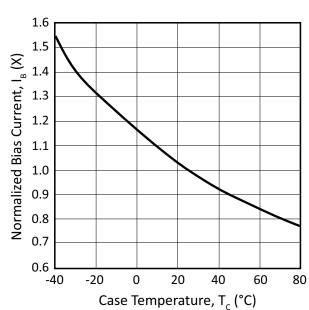




Figure 12: Offset Voltage vs. V<sub>s</sub>
Supply

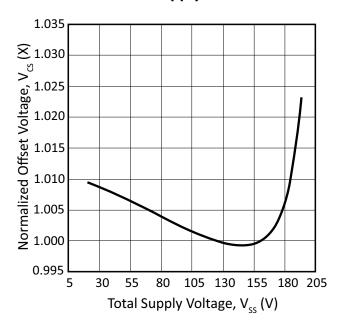


Figure 13: Offset Voltage vs. V<sub>Aux</sub> Supply

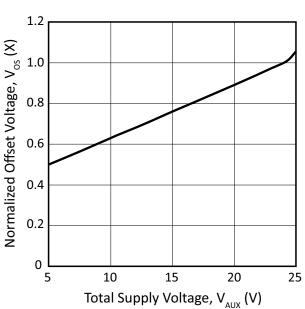


Figure 14: Input Bias Current vs. V<sub>Aux</sub> Supply

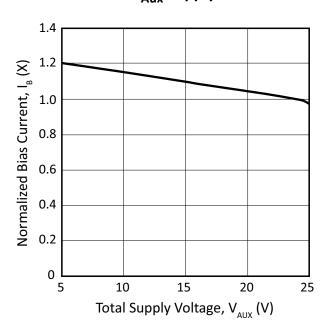


Figure 15: Input Bias Current vs. V<sub>SS</sub> Supply

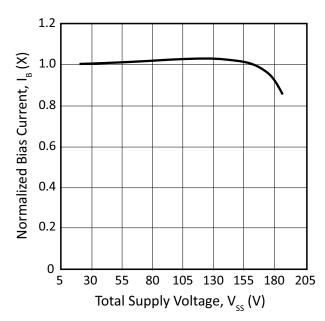




Figure 16: Amplifier Gain vs.  $R_{\text{FDBK}}$ 

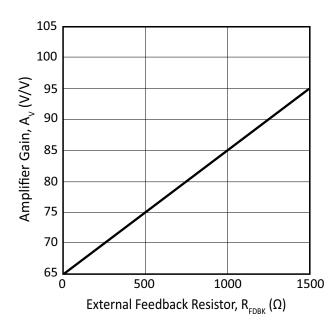
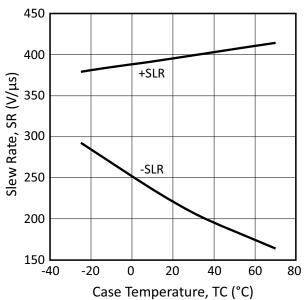


Figure 17: Slew Rate vs. Temperature

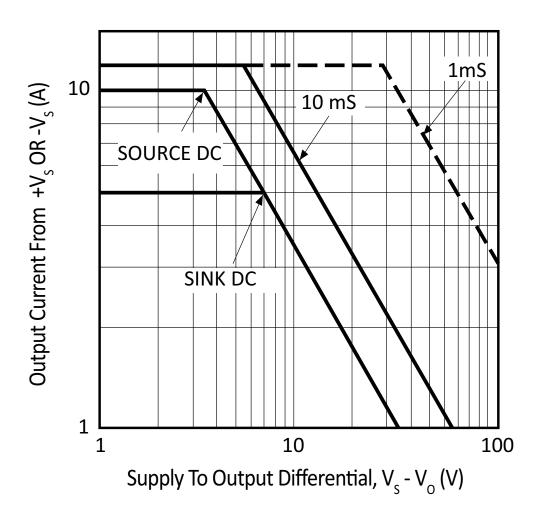




# **SAFE OPERATING AREA (SOA)**

The MOSFET output stage of the MP103 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback, external fast-recovery diodes must be used.

Figure 18: SOA





#### **GENERAL**

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology's complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

### **AMPLIFIER GAIN**

When the feedback pin for each channel is connected to the corresponding OUT pin, the gain of the amplifier is internally set to 65 V/V. The amplifier gain can be increased by connecting a resistor between the feedback and Out pin. The amplifier gain will be increased approximately 1 V/V for each additional 49.9  $\Omega$  added between the feedback and OUT pin.

### POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals  $+V_S$  and  $-V_S$  must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP103. Use electrolytic capacitors at least  $10\mu F$  per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R)  $0.1\mu F$  or greater. Duplicate the supply bypass for the supply terminals of each amplifier channel. A bypass capacitor of  $0.1\mu F$  or greater is recommended for the  $+V_{AUX}$  terminal.

# **CURRENT LIMIT**

For proper operation, the current limit resistor ( $R_{LIM}$ ) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30  $\Omega$ . The current limit function can be disabled by shorting the  $I_{I}$  pin to the OUT pin.

$$R_{LIM} = \frac{0.7V}{I_{LIM}}$$

### **POWER SUPPLY PROTECTION**

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

# SERIES ISOLATION RESISTOR, R<sub>S</sub>

To insure stability with all capacitive loads a series isolation resistor should be included between the output and the load as shown in the external connections drawing. A 1  $\Omega$  resistor works well for capacitive loads between 135pF and 44nF. The resistor will affect the rise and fall time of the output pulse at the capacitive load. This can be compensated for on the input signal.

# **MP103**



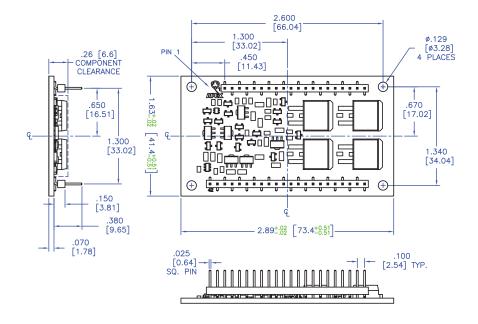
# **BACKPLATE GROUNDING**

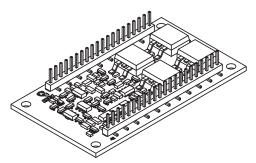
The substrate of the MP103 is an insulated metal substrate. It is required that it be connected to signal ground. This is accomplished when the ground pin (Pin 32) is properly connected to signal ground.



### PACKAGE OPTIONS

#### PACKAGE STYLE FC





#### NOTES:

- Dimensions are inches: alternate units are [mm]
- Recommended PCB hole diameter for pins: .050 [1.27]
- 2oz. copper over 600V dielectric over aluminum substrate. Tin over nickel plated phosphor bronze pins.
- Package weight:
- Mount with #4 or equivalent screws.
- It is not recommended that mounting of the package rely on the pins for mechanical support.

### **NEED TECHNICAL HELP? CONTACT APEX SUPPORT!**

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