Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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MP110

900V Offline Switching Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP110 is a flyback regulator with an integrated 900V MOSFET. Requiring a minimum number of external components, the MP110 provides excellent power regulation in AC-DC applications that require high reliability. These applications include smart meters, large appliances, industrial controls and products powered by unstable AC grids.

The regulator uses peak current mode control to provide excellent transient response and easy loop compensation. When the output power falls below a given level, the regulator enters burst mode to lower the stand-by power consumption.

The MPS proprietary 900V monolithic process enables an over temperature protection (OTP) that is on the same silicon of the 900V power FET, offering the most precise thermal protection. It also offers a full suite of protection features such as V_{CC} under-voltage lockout, over-load protection, over-voltage protection, and short-circuit protection.

The MP110 is designed to minimize electromagnetic interference for wireless communication in home and building automation applications. The operating frequency is externally programmed with a single resistor so that the power supply's radiated energy can be designed to avoid the interference to wireless communication.

In addition to the programmable frequency, the MP110 employs a frequency jittering function that not only greatly reduces the noise level, but also reduces the cost of EMI filter.

The MP110 is available in the PDIP8-7EP package.

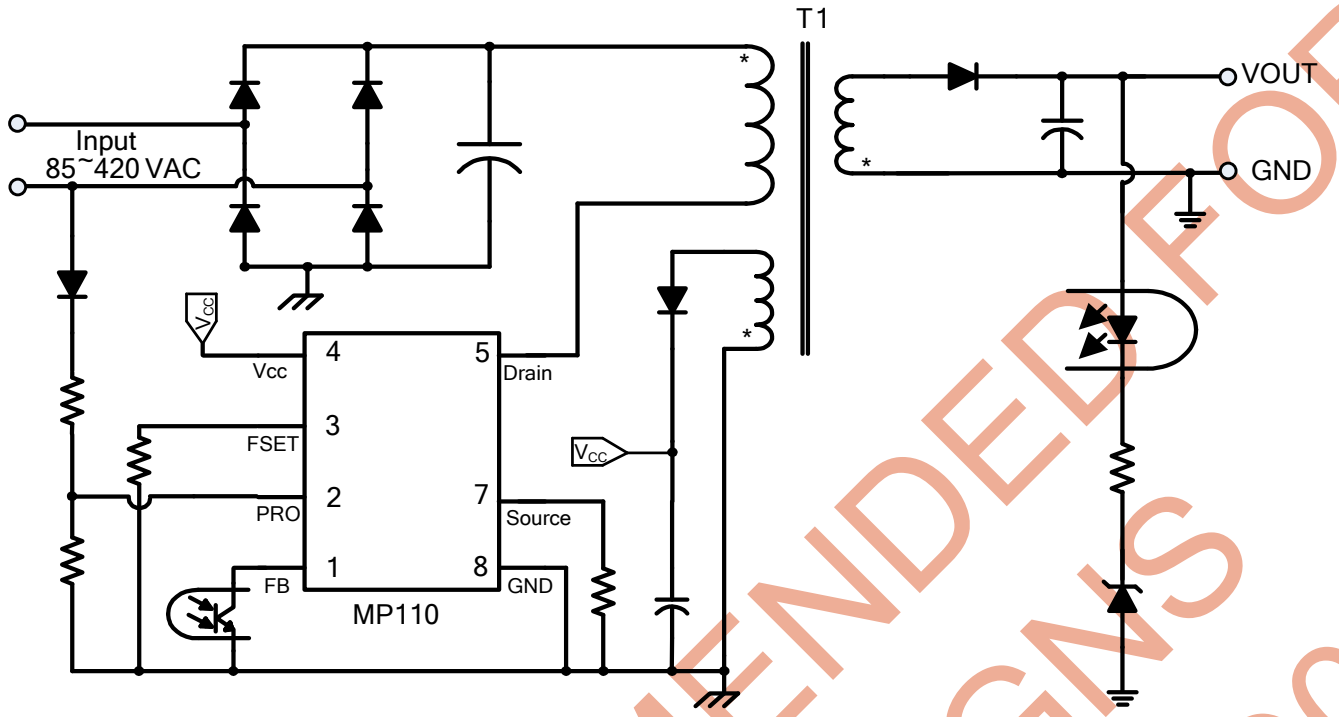
FEATURES

- Internal Integrated 900V MOSFET
- Programmable switching frequency up to 300kHz
- Frequency jittering
- Current-mode operation
- Internal high voltage current source
- Low standby power consumption via active burst mode
- Internal leading-edge blanking
- Built-in soft-start function
- Internal slope compensation
- Built-in PRO pin pull-up auto restart function
- Over-Temperature Protection (OTP)
- V_{CC} under-voltage lockout with hysteresis
- Over-Voltage Protection on V_{CC}
- Time-based overload protection
- Short-Circuit Protection (SCP)

APPLICATIONS

- Smart Power Meters
- Large Appliances
- Industrial Controls
- All AC-DC supplies sold where power grid may be unstable

TYPICAL APPLICATION

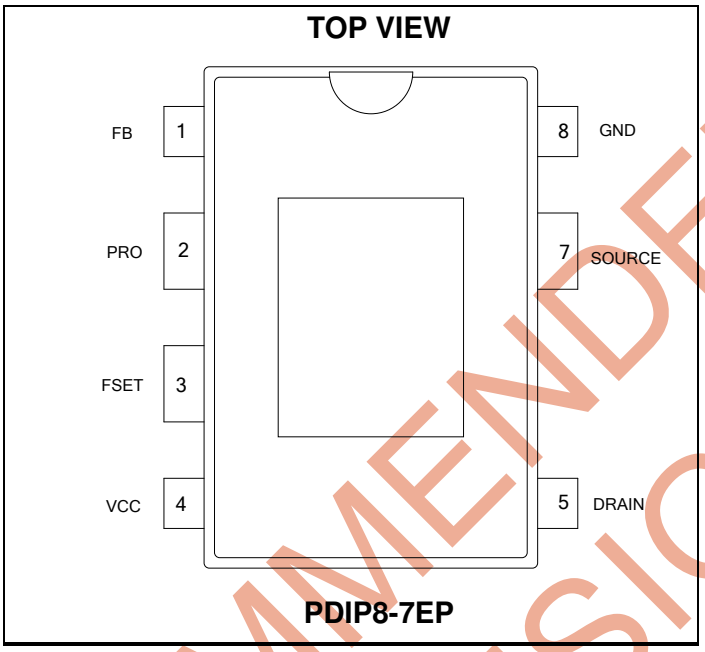


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP110GPR	PDIP8-7EP	MP110

* For Tape & Reel, add suffix –Z (e.g. MP110GPR–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Drain ..... –0.3V to 900V
Vcc ..... –0.3V to 30 V
All Other Pins ..... –0.3V to 7 V
Continuous Power Dissipation (T_A=+25°C) (2)
PDIP8-7EP 1.47W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -60°C to +150°C
Thermal Shut Down ..... 150°C
Thermal Shut Down Hysteresis ..... 30°C
ESD Capability Human Body Model 2.0kV
ESD Capability Machine Model 200V
Operating Temperature ..... –40°C to +85°C

Recommended Operation Conditions (3)

V_{CC} to GND ..... 9V to 20V
Operating Junction Temp (T_J) .. -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
PDIP8-7EP	68	7 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} =12V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise noted

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Start-up Current Source (Pin Drain)							
Supply Current from Drain	I_{Charge}	V_{CC} =6V; V_{Drain}=400V		1.5	2	2.9	mA
Leakage Current from Drain	I_{Leak}	V_{CC} =13V; V_{Drain}=400V			15	30	μA
Break-Down Voltage	$V_{(BR)DSS}$	$I_{leakage}$=100μA		900			V
On-State Resistance	$R_{DS(ON)}$	V_{CC} =10V; I_{Drain}=100mA;	T_J=25℃		13	17	Ω
			T_J=125℃		22	26	Ω
Supply Voltage Management (Pin V_{CC})							
V_{CC} Upper Level at which the IC Switch On	V_{CCH}			10.6	11.7	13.2	V
V_{CC} Lower Level at which the IC Switch Off	V_{CCL}			7	8	9	V
V_{CC} Hysteresis	V_{CC_HYS}			3	3.8	4.6	V
V_{CC} OVP Level	V_{OVP}			22.5	24	25.3	V
V_{CC} Re-Charge Level at which the Protection Occurs	V_{CCR}			4.5	5.3	6	V
Quiescent Current at Protection Phase	I_{Pro}	V_{CC}=6V; V_{pro}=4V				600	μA
Quiescent Current	I_Q	V_{CC}=13V			700	900	uA
Operation Current	I_{CC}	V_{CC}=13V; f_S=100kHz			1.7	2	mA
Feedback Management (Pin FB)							
Internal Pull-Up Resistor	R_{FB}				10		kΩ
Internal Pull-Up Voltage	V_{UP}			3.8	4.1	4.4	V
FB to Current-Set-Point Division Ratio	I_{div}				3.3	3.5	
Internal Soft-Start Time	T_{SS}				3		ms
FB Decreasing Level at which the Regulator Enters Burst Mode	V_{BURL}			0.4	0.5	0.6	V
FB Increasing Level at which the Regulator Leaves Burst Mode	V_{BURH}			0.58	0.7	0.86	V
Over-Load Set Point	V_{OLP}			3.6	3.8	4	V
Over-Load Delay Time	T_{Delay}	f_S=100kHz			82		ms

ELECTRICAL CHARACTERISTICS

V_{CC} =12V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise noted

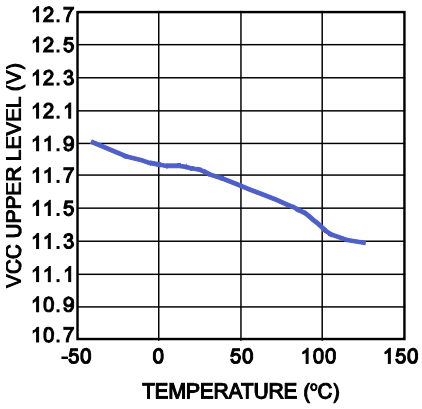
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing Resistor(Pin FSET)						
FSET Reference Voltage	V_{FSET}		1.16	1.23	1.29	V
Frequency Spectrum Jittering Range, in Percentage of Fs	$R_{Jittering}$	Example: f_S=100kHz, then jittering is ±4kHz		±4		%
Typical Operating Frequency	f_S	T_J=25°C, R_{FSET}=100kΩ	90	104	118	kHz
Current Sampling Management (Pin Source)						
Leading-Edge Blanking for Current Sensor	T_{LEB1}			650		ns
Leading-Edge Blanking for SCP	T_{LEB2}			600		ns
Maximum Current Set Point	V_{CS}		0.90	0.96	1.02	V
Short-Circuit Protection Set Point	V_{SC}		1.32	1.42	1.62	V
Slope Compensation Ramp	S_{Ramp}	f_S=100kHz		40		mV/μs
Protection Management (Pin PRO)						
Protection Voltage	V_{PRO}		2.95	3.1	3.3	V
Protection Hysteresis	V_{HY}			0.2		V
Thermal Shutdown						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Recovery Hysteresis				30		°C

PIN FUNCTIONS

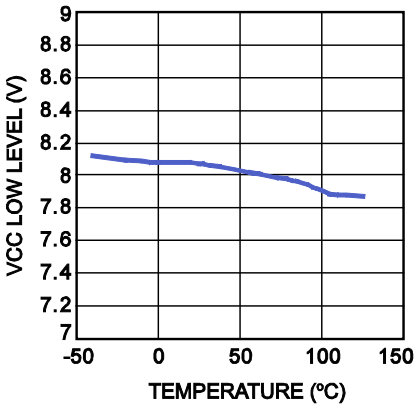
Pin #	Name	Description
1	FB	Feedback. The output voltage from the external compensation circuit is fed into this pin. This pin and the current sense signal from Source determines the PWM duty cycle. A feedback voltage of V_{OLP} triggers over-load protection, while V_{BURL} triggers burst-mode operation. The regulator exits burst-mode operation and enters normal operation when the FB voltage reaches V_{BURH}.
2	PRO	Protection. Pull-up PRO to shut down the IC with hysteresis.
3	FSET	Switching converter frequency set. Connect a resistor to GND to set the switching frequency up to 300kHz.
4	V_{CC}	Supply voltage. Connect a 22μF bulk capacitor and a 0.1uF ceramic capacitor for most applications. When V_{CC} rises to V_{CCH}, the IC starts switching; when it falls below V_{CCL}, the IC stops switching.
5	Drain	Drain of the internal MOSFET. Input for the start-up high voltage current source.
7	Source	Source of the internal MOSFET. Input of the primary current sense signal.
8	GND	The IC Ground.

TYPICAL CHARACTERISTICS

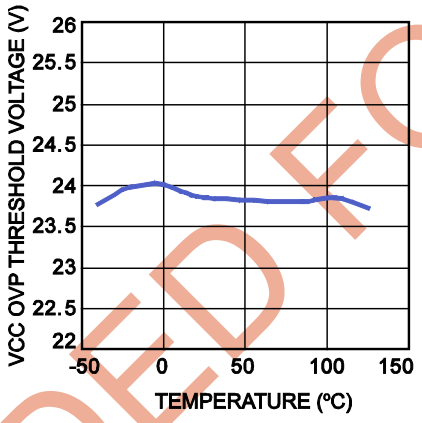
VCC Upper Level vs. Temperature



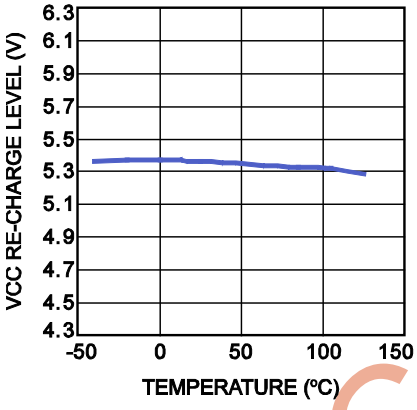
VCC Low Level vs. Temperature



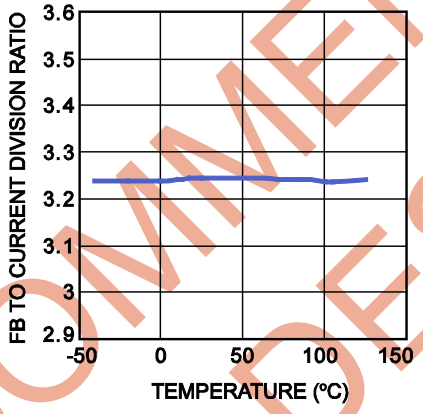
VCC OVP Threshold Voltage vs. Temperature



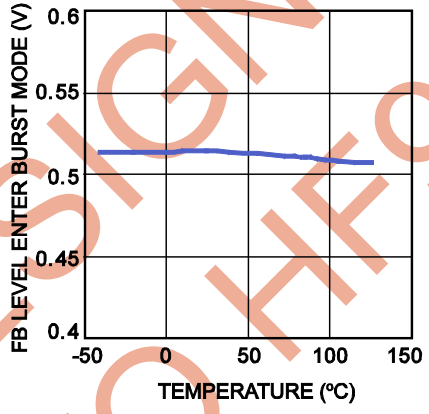
VCC Re-Charge Level vs. Temperature



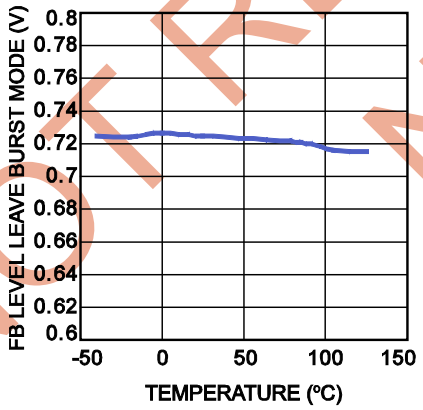
FB to Current Division Ratio vs. Temperature



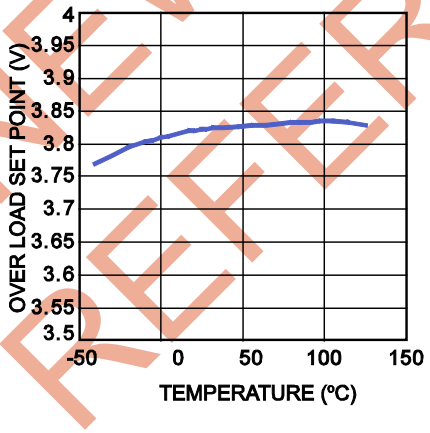
FB Level Enter Burst Mode vs. Temperature



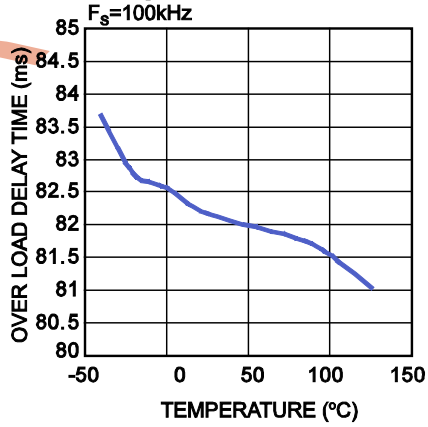
FB Level Leave Burst Mode vs. Temperature



Over Load Set Point vs. Temperature

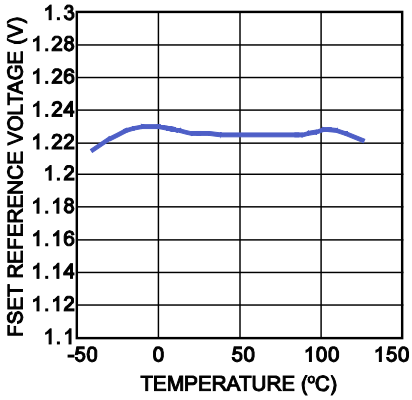


Over Load Delay Time vs. Temperature

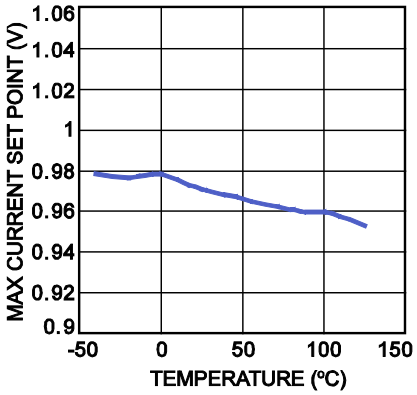


TYPICAL CHARACTERISTICS *(continued)*

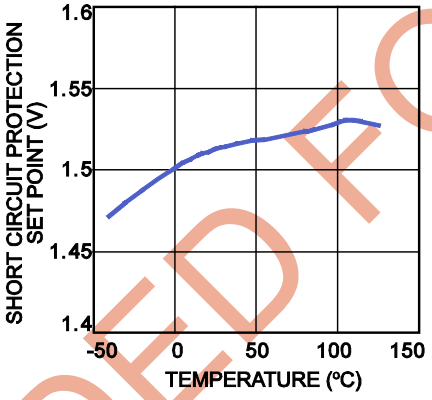
Fset Reference Voltage vs. Temperature



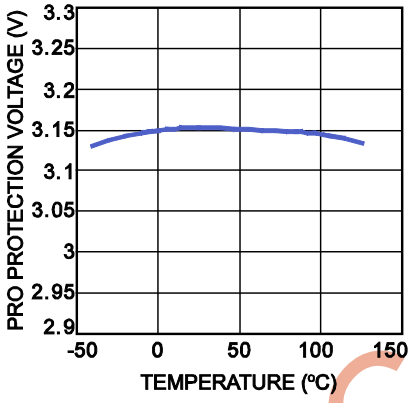
Max Current Set Point vs. Temperature



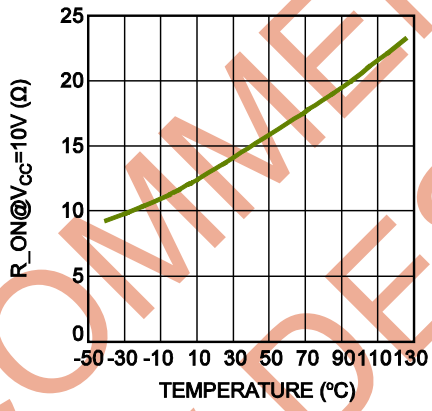
Short Circuit Protection Set Point vs. Temperature



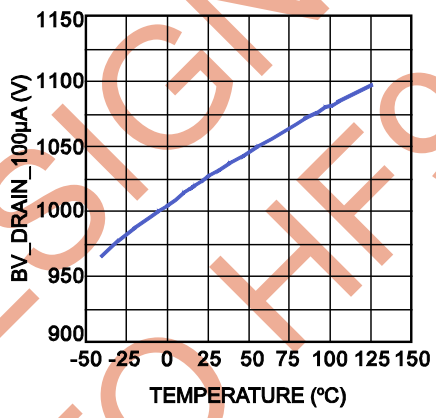
Pro Protection Voltage vs. Temperature



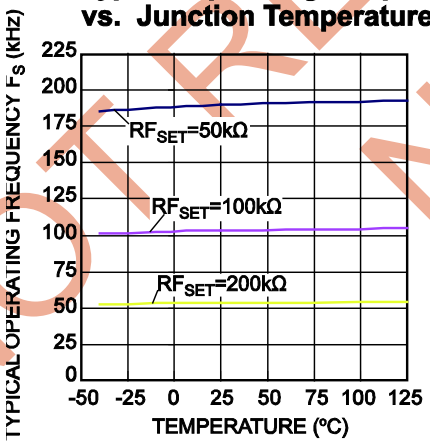
R_ON@V_{CC}=10V vs. Temperature



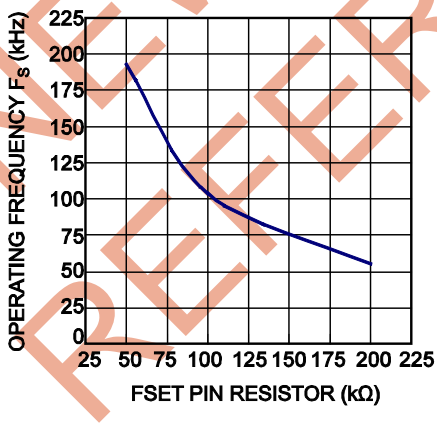
BV_Drain_100µA vs. Temperature



Typical Operating Frequency vs. Junction Temperature



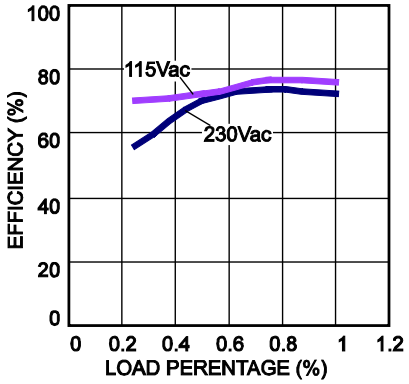
Typical Operating Frequency when T_J=25ºC



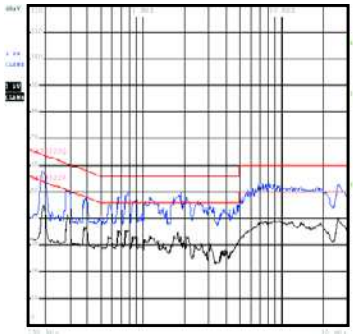
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230V, V_{OUT1} = 12.5V, V_{OUT2} = 5V, Primary Inductance=2.5mH, N_P:N_{AUX}:N_{S1}:N_{S2} = 125:14:14:9, T_A = 25°C, unless otherwise noted.

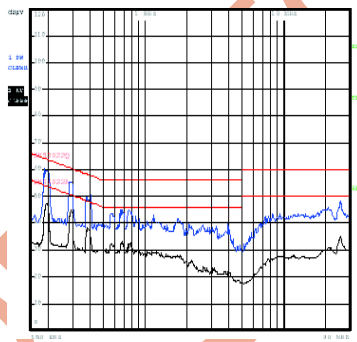
Efficiency



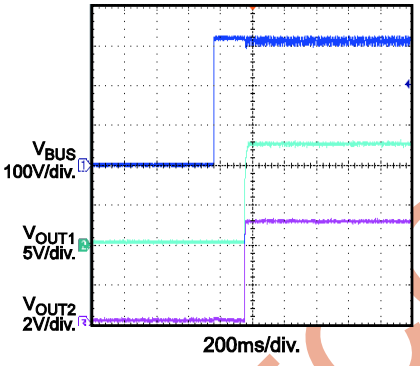
EMI
230Vac, Full Load, L Line



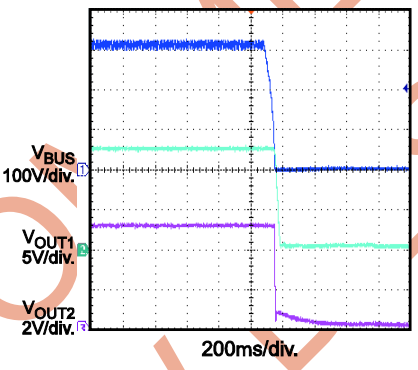
EMI
230Vac, Full Load, N Line



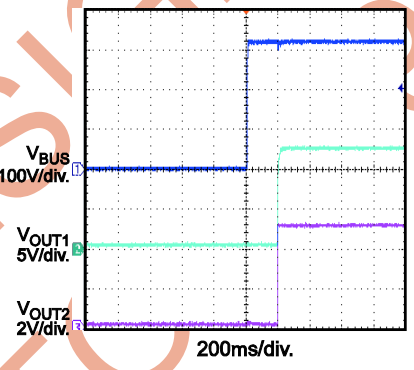
Startup
230Vac, Full Load



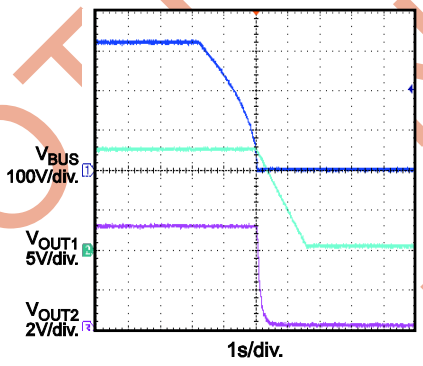
Shutdown
230Vac, Full Load



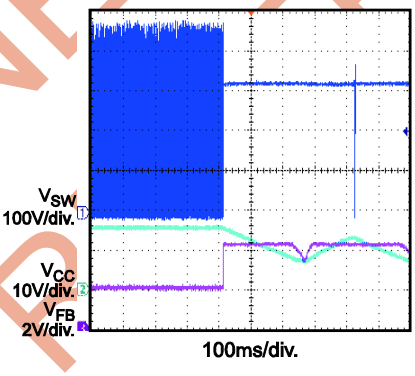
Startup
230Vac, No Load



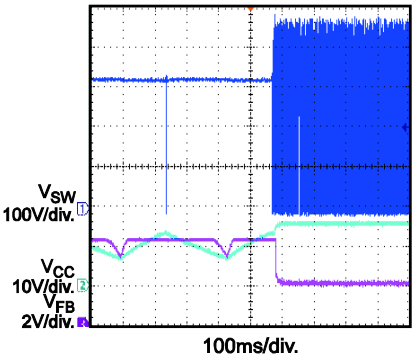
Shutdown
230Vac, No Load



SCP Entry
230Vac, Full Load



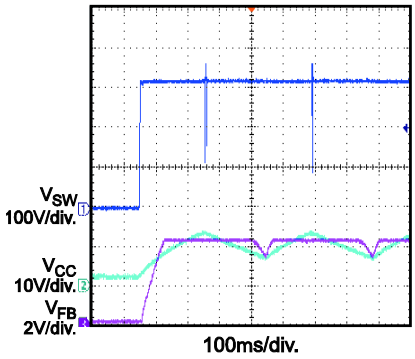
SCP Recovery
230Vac, Full Load



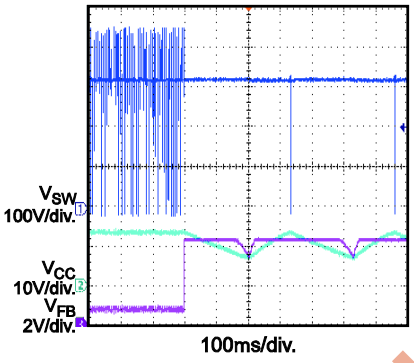
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 230V, V_{OUT1} = 12.5V, V_{OUT2} = 5V, Primary Inductance=2.5mH, N_P:N_{AUX}:N_{S1}:N_{S2} = 125:14:14:9, T_A = 25°C, unless otherwise noted.

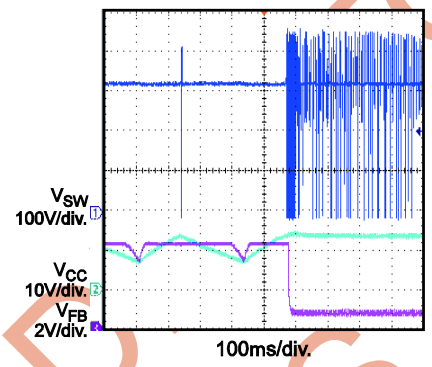
SCP Startup
230Vac, Full Load



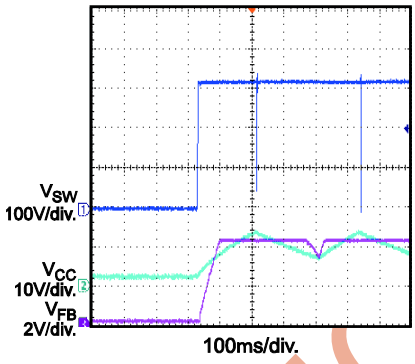
SCP Entry
230Vac, No Load



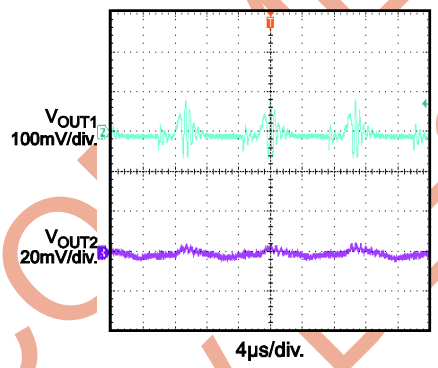
SCP Recovery
230Vac, No Load



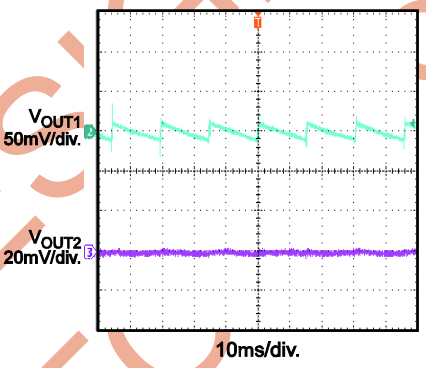
SCP Startup
230Vac, No Load



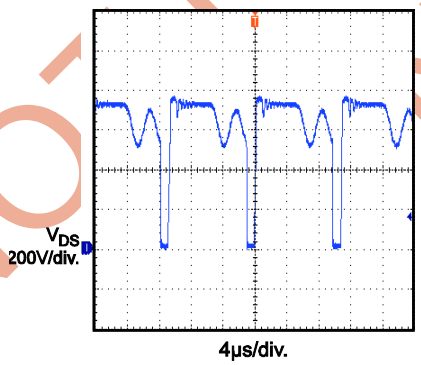
Output Ripple
230Vac, Full Load



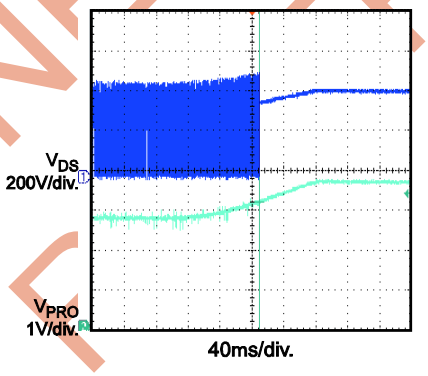
Output Ripple
230Vac, No Load



Stress
420Vac, Full Load



Pro Protection
230Vac, 300Vac Protection, Full Load



FUNCTIONAL BLOCK DIAGRAM

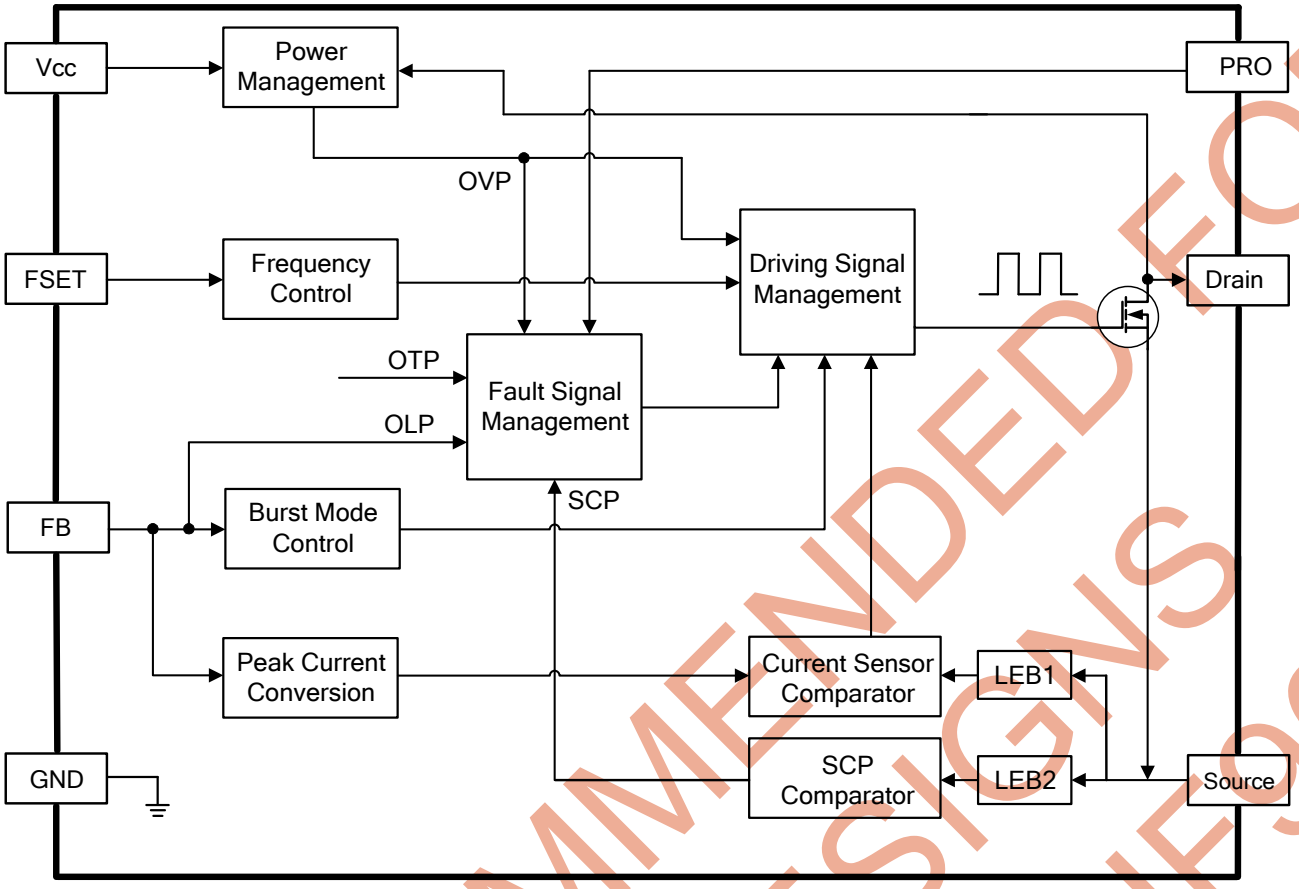


Figure 1: Internal Function Block Diagram

OPERATION

The MP110 incorporates all the necessary features required by a reliable switch mode power supply. The proprietary 900V monolithic integration enables a highly integrated power supply solution. It has burst mode operation to minimize the stand-by power consumption at light load. Protection features such as auto-recovery for over-load protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), and thermal shutdown for over-temperature protection (OTP) - contribute to a safer converter design with minimal external components. .

PWM Operation

The MP110 employs peak current mode control. On the secondary side, the output voltage is divided down by a voltage divider network. This voltage is fed back to the primary side as voltage on the FB pin using an opto-coupler and a shunt regulator. The voltage at the FB pin is compared to the V_{Sense} voltage which measures MOSFET switching current. The integrated MOSFET turns on at the beginning of each clock cycle. The current in the transformer magnetizing inductance increases until it reaches the value set by the FB voltage, and then the integrated MOSFET turns off.

Start-up and V_{CC} UVLO

Initially, the IC is driven by the internal current source which is drawn from the high-voltage Drain pin. The IC starts switching and the internal high-voltage current source turns off as soon as the voltage on pin V_{CC} reaches 11.7V (V_{CCH}, typical value). At this point, the supply of the IC is taken over by the auxiliary winding of the transformer. When V_{CC} falls below 8V (V_{CCL}, typical value), the regulator stops switching and the internal high-voltage current source turns on again.

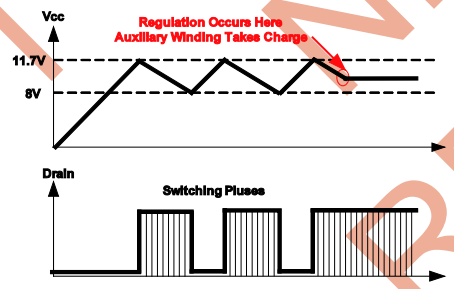


Figure 2: V_{CC} UVLO

The lower threshold of VCC UVLO decreases from 8V (V_{CCL}, typical value) to 5.3V (V_{CCR}, typical value) when fault conditions happen, such as SCP, OLP, OVP, and OTP.

Soft-Start

The MP110 implements an internal soft-start circuit in order to reduce stress on the primary side MOSFET, secondary diode and smoothly establish the output voltage during start-up. The internal soft-start circuit gradually increases the primary current sense threshold which determines the MOSFET peak current during start-up. The pulse width of the power switching device is progressively increased to establish correct operating conditions until the feedback control loop takes charge.

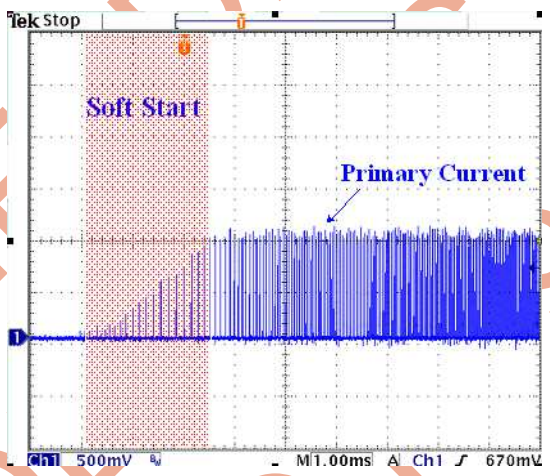


Figure 3: Soft Start

Switching Frequency

The switching frequency of MP110 can be set by FSET pin. The frequency can be set by a resistor between FSET pin and GND pin. The oscillator frequency can be attained below:

$$f_S = \frac{1}{200\times10^{-9} + 112.5\times10^{-12}\times\frac{R_{FSET}}{V_{FST}}}\ Hz$$

V_{FST} (1.23V) is the FSET pin reference voltage.

Over Voltage Protection (OVP)

Monitoring the V_{CC} pin voltage via a 20us time constant filter allows the MP110 to enter OVP during an over-voltage condition, typically when V_{CC} goes above 24V. The regulator will resume operation after the fault disappears.

Over Load Protection (OLP)

MP110 shuts when the power supply undergoes an overload. OLP is achieved by continuously monitoring the FB voltage. A fault signal is triggered when FB pulls up to 3.8V (V_{OLP}, typical value) and after 82ms delay (8192 switching cycle, f_S=100kHz), if the fault signal is still present, MP110 shuts down. When the fault disappears, the power supply resumes operation. The OLP delay time can be attained below.

$$T_{Delay} = \frac{82ms \times 100kHz}{f_S}$$

Short Circuit Protection (SCP)

By monitoring the CS Pin, MP110 shuts down when the voltage rises higher than 1.42V (V_{SC}, typical value) to indicate a short circuit. The MP110 enters a safe low-power mode that prevents any thermal damage or stress damage. As soon as the fault disappears, the power supply resumes operation.

Thermal shutdown (OTP)

When the junction temperature of the IC exceeds 150℃, the over temperature protection is activated and stops output driver switching to prevent MP110 from any thermal damage. As soon as the junction temperature drops below 120℃, the regulator resumes operation. During the protection period, the regulator enters auto-recovery mode. The VCC voltage is discharged to V_{CCR} and is re-charged to V_{CCH} by the internal high voltage current source.

Burst Operation

To minimize stand-by power consumption, the MP110 implement burst mode at no load and light load. As the load decreases, the FB voltage decreases. The IC stops switching when the FB voltage drops below 0.5V (V_{BRUL}, typical value). As the load power increases, the output voltage drops at a rate dependent on the load. This causes the FB voltage to rise again due to the negative feedback control loop. Once the FB voltage exceeds 0.7V (V_{BRUH}, typical value), the switching pulse resumes. The FB voltage then decreases and the whole process repeats. Burst-mode operation alternately enables and disables the switching pulse of the MOSFET. Hence switching loss at no load and light load conditions is greatly reduced. Figure 4 shows the burst mode operation of MP110.

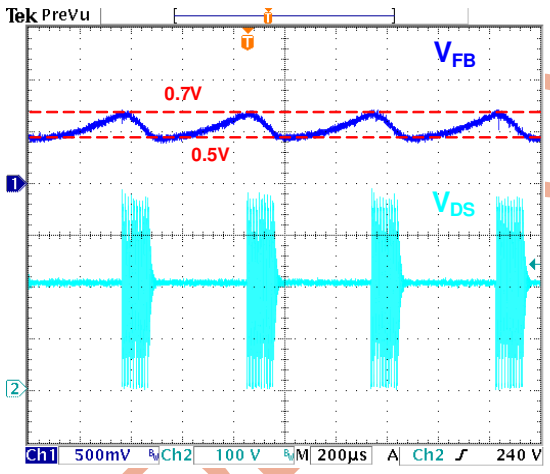


Figure 4: Burst Mode Operation

PRO Pin

The PRO pin provides extra protection against abnormal conditions. Use the PRO pin for input OVP or other protections (input UVP, over-temperature protection for key component and so on). If the PRO pin voltage exceeds 3.1V (V_{PRO}, typical value), the IC shuts down to enter auto-recovery mode. As soon as the fault disappears, the power supply resumes operation.

Peak Current Limit

In normal operation, the primary peak current is sensed by a sensing resistor between the Source pin and Ground. The turn-off threshold of the MOSFET is set by FB voltage, $V_{Sense}=V_{FB}/I_{div}$. When the sensing resistor voltage reaches the V_{Sense}, the MOSFET turns off. The I_{div} is the FB to current-set-point division ratio.

During over-load condition, the primary peak current threshold is internally limited to the maximum value 0.96V (V_{CS}, typical value) even if V_{FB} voltage exceeds 3.2V to avoid excessive output power and lower the switch voltage rating.

During start-up period, the primary peak current threshold internally increases to the maximum current set point V_{CS} gradually.

Leading Edge Blanking

In order to avoid turning off the MOSFET from mis-trigger spikes shortly after the switch turns

on, the IC implements leading-edge blanking. During the blanking time, any trigger signal on source pin is blocked. An internal leading-edge blanking(LEB) unit containing two LEB times is employed between the Source pin and the current comparator input to avoid premature switching pulse termination due to the parasitic capacitances. During the blanking time, the current comparator is disabled and can not turn off the MOSFET.

Current sensor leading edge blanking inhibits the current limitation comparator during 650ns (T_{LEB1}, typical value) and SCP leading edge blanking inhibits the SCP current comparator during 600ns (T_{LEB2}, typical value). Figure 5 shows the primary current sense waveform and the leading edge blanking.

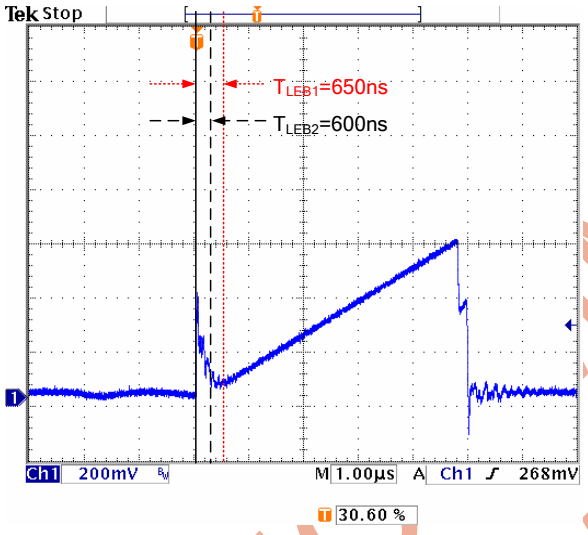


Figure 5: Leading Edge Blanking

APPLICATION INFORMATION

Input Capacitor Choose

The bulk capacitors after the rectifier bridge filter the rectified AC input which supply the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of full bridge rectifier.

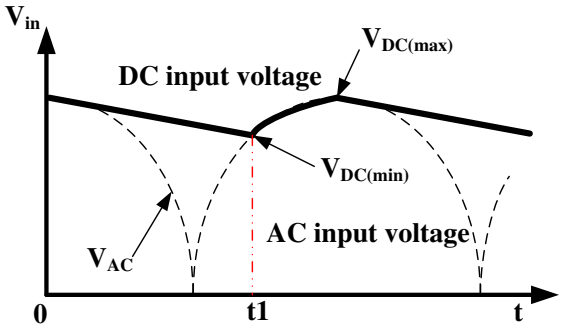


Figure 6: Input voltage waveform

When the full-bridge rectifier is used, the input capacitor is usually set as 2μF/W for the universal input condition (85~265V_{AC}). Halve the capacitor values for high voltage input (>185VAC) application. The input power P_{in} can be estimated as follow.

$$P_{in} = \frac{V_O \times I_O}{\eta}$$

Where V_O is the output voltage, I_O is the rated output current, η is the estimated efficiency. Generally, η is between 0.75 and 0.85 depending on the input range and output application.

From the waveform above, the AC input voltage V_{AC} and DC input voltage V_{DC} can be got as follow.

$$V_{DC}(V_{AC},t) = \sqrt{2 \times V_{AC}^2 - \frac{2 \times P_{in}}{C_{in}} \times t}$$

By setting V_{AC}=V_{DC}, t1 where DC bus voltage reaches to its minimum value can be calculated. So the minimum DC voltage is as follow.

$$V_{DC(min)} = V_{DC}(V_{AC(min)},t1)$$

Very low DC input voltage could cause thermal problem in full load. It's recommend the minimum DC voltage is higher than 70V, or the input capacitor value should be increased.

As a 900V offline regulator, MP110 is very suitable for very high voltage input application. But the general input capacitors with 400V voltage rating can not satisfy the safety requirement. Thus the stack capacitors could be used in very high input voltage application such as 420VAC input which refers to the Figure7.

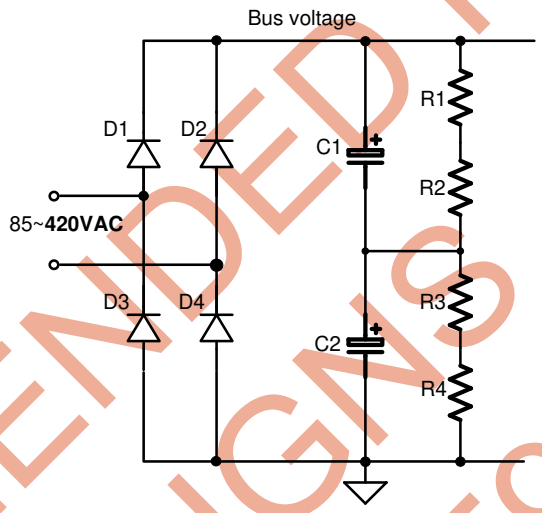


Figure 7: Input Stack Capacitor Circuit

The C1 and C2 endure the half of input DC voltage rating respectively. The R1~R4 should be use the same value resistor to equalize the C1, C2 voltage stress. And the R1~R4 is recommended to use the 1206 package to satisfy safety requirement. Also, the R1~R4 value should be large enough for energy saving. For example, the total value of R1~R4 is 20MΩ which consumes about 18mW in 600VDC bus voltage.

Primary-Side Inductor Design (L_m)

Normally, the converter is designed to operate in CCM under low input voltage. CCM is needed to satisfy the output energy requirement in universal input condition. With built-in slope compensation function, MP110 can support CCM when duty cycle exceeds 50%. Set the ratio (K_P) of the primary inductor ripple current amplitude vs. the peak current value to 0<K_P≤1, where K_P=1 for DCM. Figure 8 shows the relevant waveforms. A larger inductor leads to a smaller K_P, which can

reduce RMS current but increase transformer size. For 5W application, an optimal K_P value is usually between 0.8 and 1 for the universal input range and 1 for a 230VAC input range.

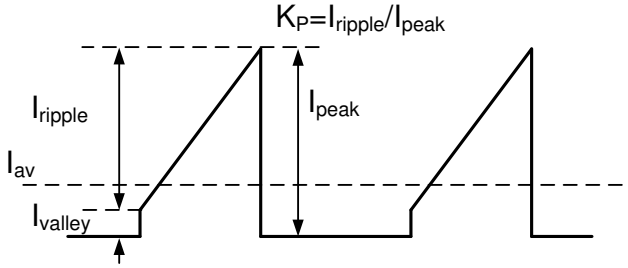


Figure 8: Typical Primary-Current Waveform

For CCM at minimum input, the converter duty cycle is:

$$D = \frac{(V_O + V_F) \times N}{(V_O + V_F) \times N + V_{DC(min)}}$$

Where:

V_F is the secondary diode's forward voltage,

N is the transformer turns ratio.

The MOSFET turn-on time is

$$T_{ON} = \frac{D}{f_S}$$

f_S is operating frequency.

The input average current, ripple current, peak current and valley current of the primary side are described as follows:

$$I_{AV} = \frac{P_{in}}{V_{DC(min)}}$$

$$I_{ripple} = K_P \times I_{peak}$$

$$I_{peak} = \frac{I_{AV}}{(1 - \frac{K_P}{2}) \times D}$$

$$I_{valley} = (1 - K_P) \times I_{peak}$$

The following equation estimates L_m as

$$L_m = \frac{V_{DC(min)} \times T_{ON}}{I_{ripple}}$$

Current-Sense Resistor

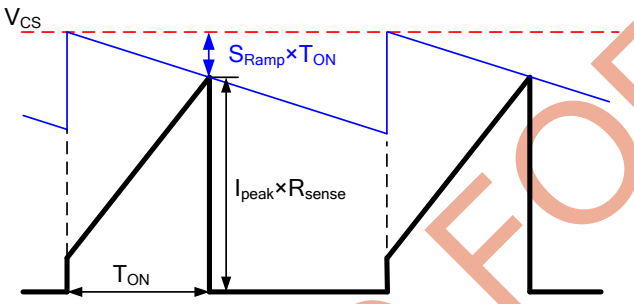


Figure 9: Slope Compensation waveform

Figure 9 shows the slope compensation waveform. When the sum of the sense resistor voltage and the slope compensation voltage reaches the peak current limit V_{CS}, MP110 turns off the internal MOSFET. The maximum peak current limit is 0.96V (V_{CS}, typical value) and the slope compensation slew rate is 40mV/us. Considering the margin, use $0.95 \times V_{CS}$ as the peak current limit at full load. The voltage on sense resistor is given by the following equation: .

$$V_{sense} = 0.95 \times V_{CS} - S_{Ramp} \times T_{ON}$$

So the value of the sense resistor is

$$R_{sense} = \frac{V_{sense}}{I_{peak}}$$

Select the current sense resistor with appropriate power rating based on the power loss:

$$P_{sense} = \left[\left(\frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} \times \left(I_{peak} - I_{valley} \right)^2 \right] \times D \times R_{sense}$$

PRO pin

Extra protection can be enable thru the MP110 PRO pin. A typical input over-voltage protection circuitry is shown in figure 10.

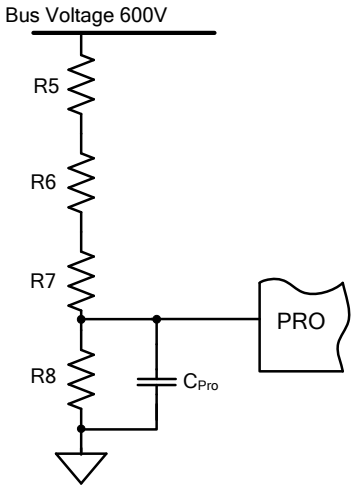


Figure 10: Input Over Voltage Protection Setup

The input over voltage protection point can be calculated by the following function:

$$V_{INOVP} = V_{PRO} \times \frac{R5 + R6 + R7 + R8}{R8}$$

1206 packages should be used for resistors R5~R8 for safety consideration and the total value should be larger than 10MΩ for energy saving purpose.
The switching voltage noise could be introduced by large R5~R8 value which disturbs the PRO pin protection action. One ceramic cap with around 1nF should be paralleled with PRO pin and GND pin. It should be located near the IC to decouple the switching voltage noise.

Frequency Jittering

MP110 provides the frequency jittering function which simplifies the input EMI filter design and also decreases the system cost. MP110 has the optimized frequency jittering with ±4% frequency deviation range and $256T_S$ carrier cycle which can effectively improve EMI by spreading the energy dissipation over the frequency range.

Thermal

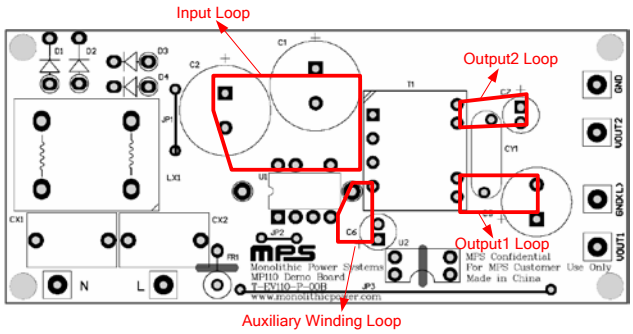
MP110 is popular for high input voltage application with 900V integrated MOSFET. The thermal is the key factor to influence the output power especially the high input voltage and high operating frequency. The turn-on loss is dominant in high input voltage caused by the parasitic cap of secondary side diode and transformer, which bring about the IC very high junction temperature.

In order to deliver maximum power, a proper heatsink for MP110 should be designed for optimum thermal performance. In addition, it's recommended to set the operating frequency less than 150kHz in order to achieve better thermal performance and better EMI in application.

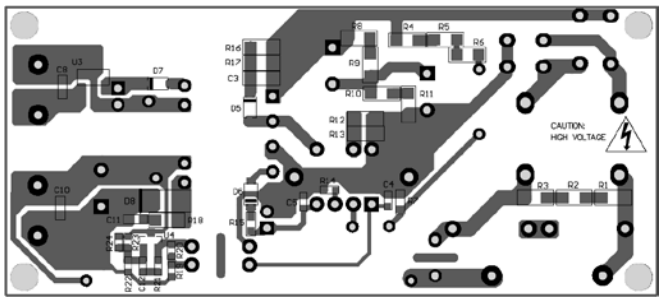
PCB Layout Guide

PCB layout is important to achieve reliable operation, good EMI performance, and good thermal performance. Follow these guidelines to optimize performance.

1) Minimize the power stage switching stage loop area. This includes the input loop (C2–C1-T1–U1–R12/R13–C2), the auxiliary winding loop (T1–D6–C6–T1), the output loop (T1–D8–C9–T1 and T1–D7–C7–T1) and the RCD loop (T1–D5–R16/R17/C3–T1)
2) The input loop GND and control circuit should be separate and only connect at C2.
3) Connecting the heatsink to the primary GND plane improves EMI and thermal dissipation.
4) Place the control circuit capacitors (such as those for FB, PRO and VCC pins) close to IC to decouple switching voltage noise.
5) Enlarge the GND pad near the IC for good thermal dissipation.
6) Keep the EMI filter far away from the switching point.
7) The two outputs clearance distance should satisfy the insulation requirement.



a) Top



b) Bottom

Figure 11: PCB Layout

Design Example

The following is a design example using the application guidelines for the given specifications:

V_{IN}	85 to 420VAC
V_{OUT1}	12.5V
I_{OUT1}	0.4A
V_{OUT2}	5V
I_{OUT2}	0.05A
f_S	100kHz

The detailed application schematic is shown in Figure 12. The typical performance and circuit waveforms have been shown in the typical performance characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

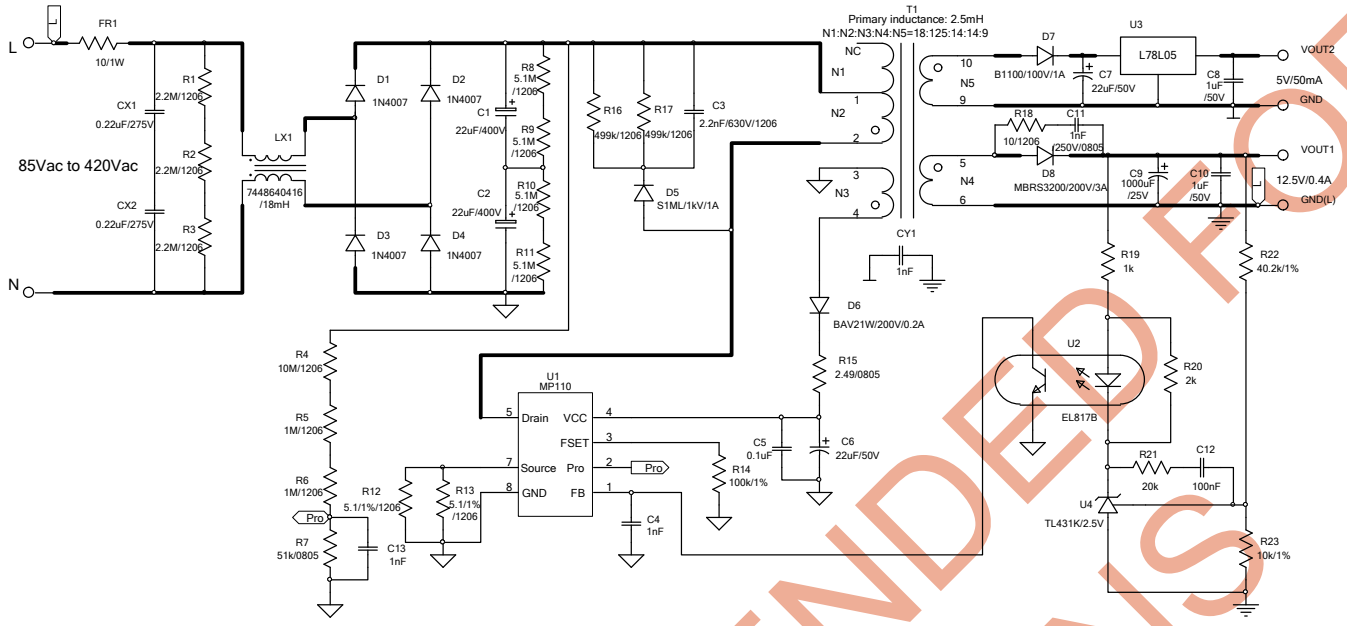
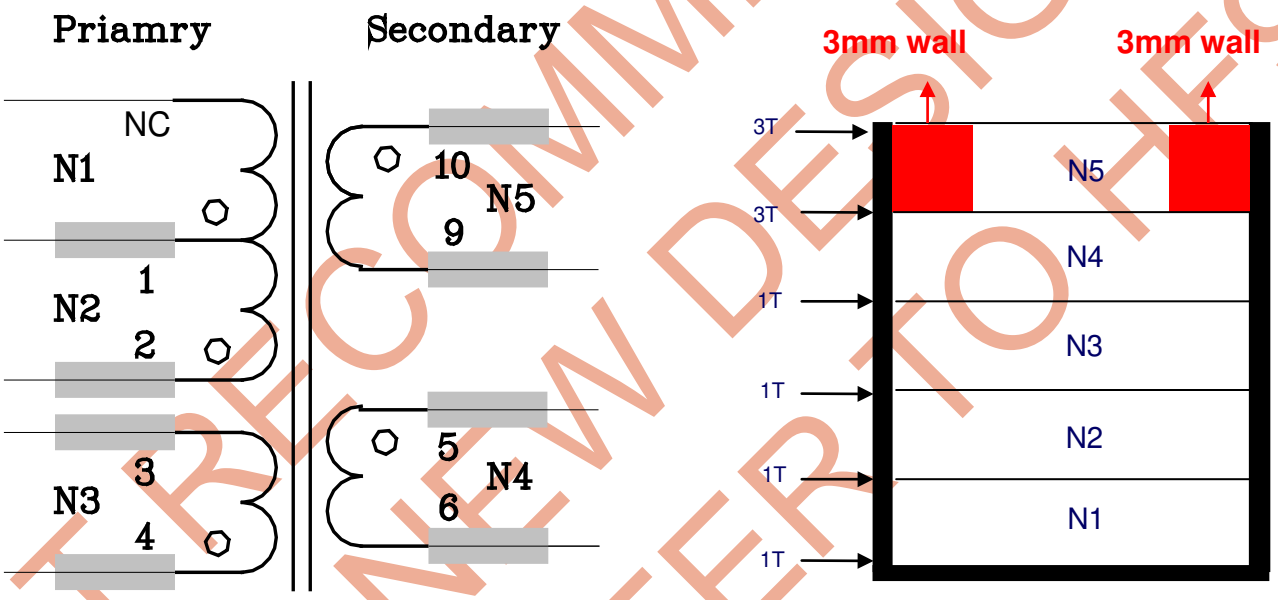


Figure 12: Typical Application Schematic



a) Connection Diagram

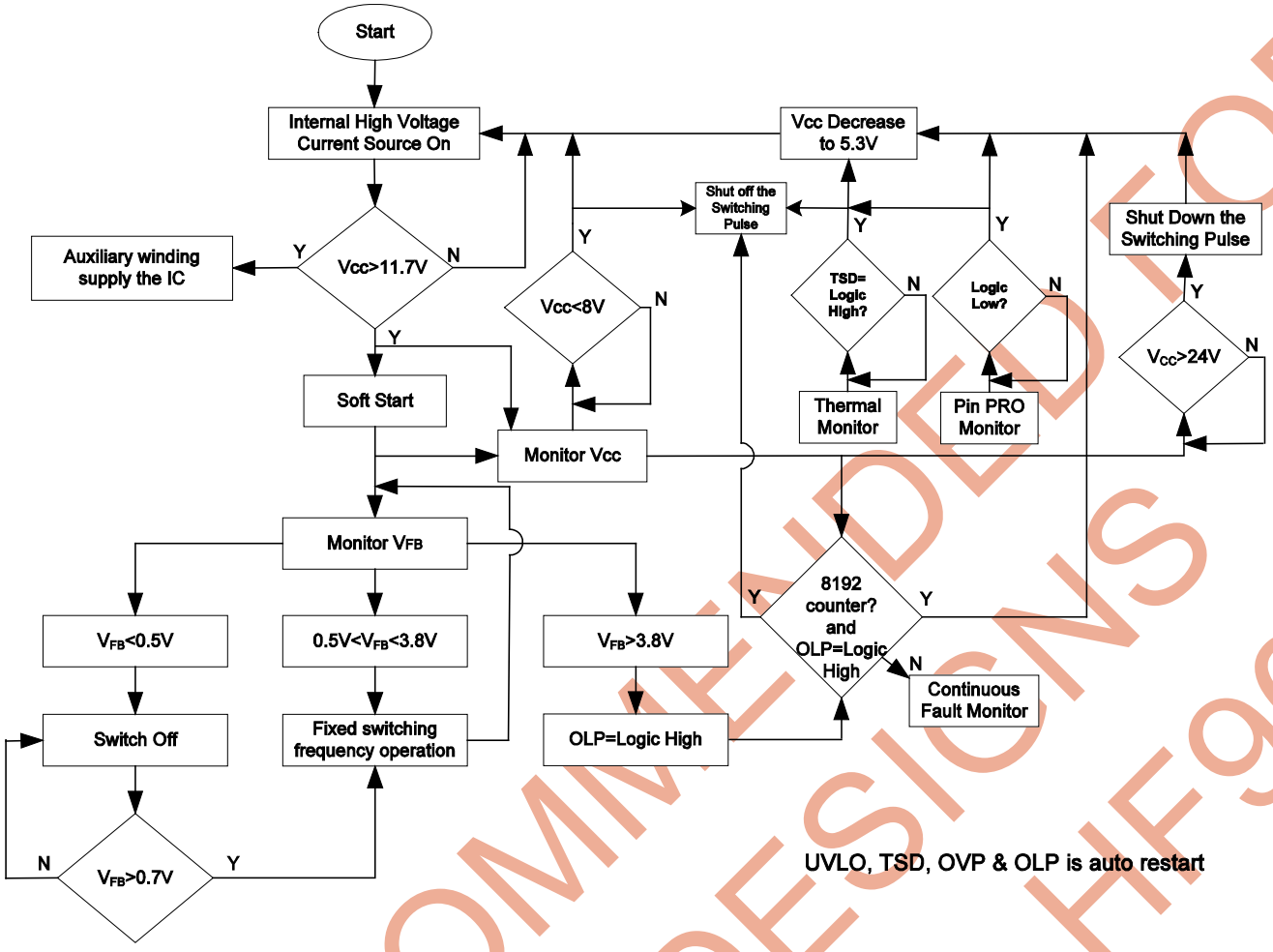
b) Winding Diagram

Figure 13: Transformer Structure

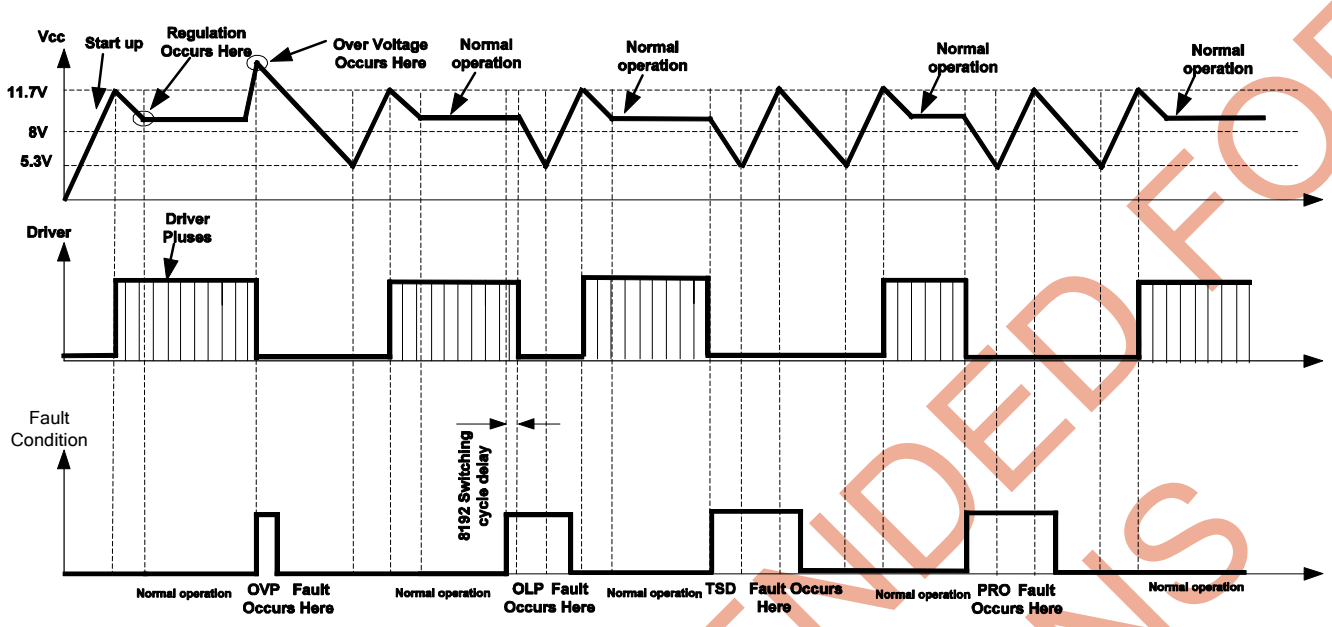
Table 2—Winding Order

Tape (T)	Winding	Margin Wall PRI side	Terminal Start—>End	Margin Wall SEC side	Wire Size (φ)	Turns (T)
1	N1	0mm	1—>NC	0mm	0.18mm*2	18
1	N2	0mm	2—>1	0mm	0.18mm*1	125
1	N3	0mm	4—>3	0mm	0.15mm*1	14
1	N4	0mm	5—>6	0mm	0.4mm*1	14
3	N5	3mm	10—>9	3mm	0.2mm*1	9
3						

FLOW CHART

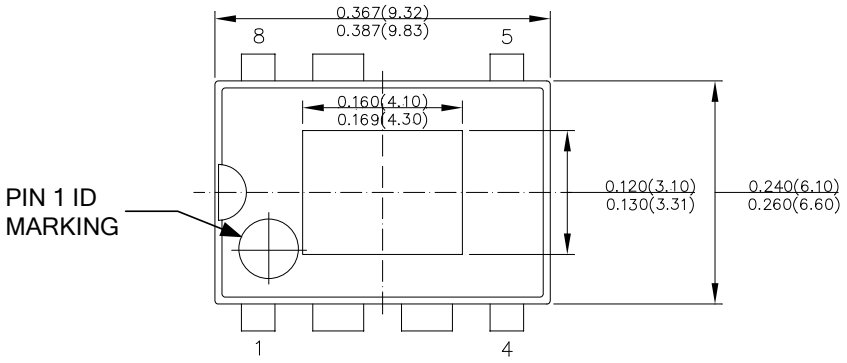


EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

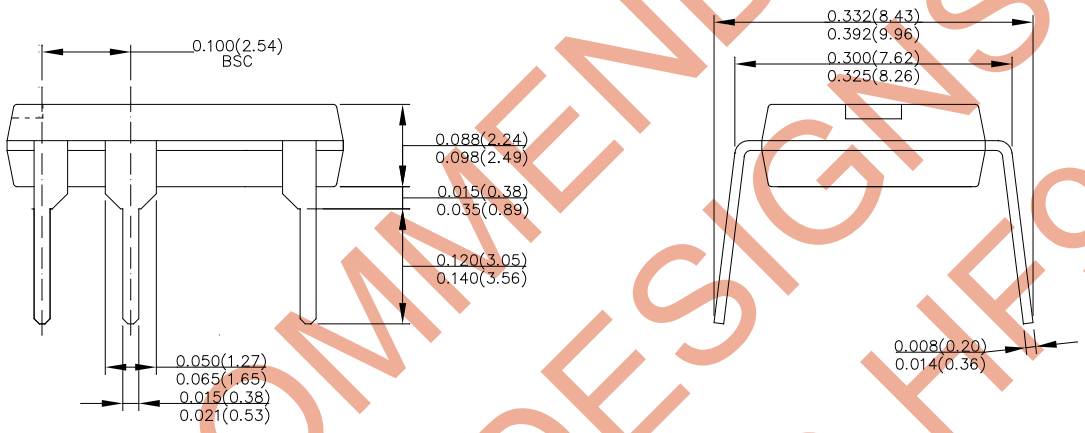


PACKAGE INFORMATION

PDIP8-7EP



TOP VIEW



SIDE VIEW

NOTE :

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS .
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH ,OR PROTRUSIONS.
3) JEDEC REFERENCE IS MS-001, VARIATION BA .
4) DRAWING IS NOT TO SCALE .