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Printhead Driver Module

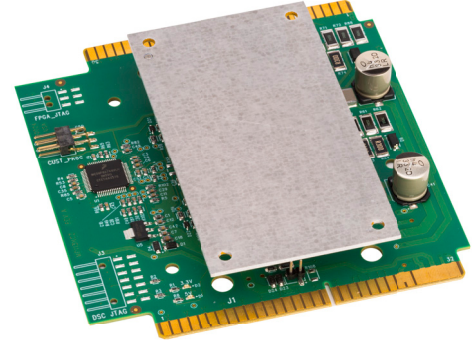
FEATURES

2 Power, Analog Output Channels

- High Output Voltage: Up To 135Vpp
- High Output Current: 3A Continuous, 7A Peak (Per Channel)
- High Output Slew Rate: Up To 45V/ μ s
- 100W Dissipation Capability (Per Channel)
- Over-temperature Protection
- Temperature Sense

Integrated Digital Printing Data Converter

- LVDS Serial Data Input, 1- Or 2-bits Per Nozzle
- Up To 1024 Nozzles
- Output Waveform Frequency: Up To 50kHz



APPLICATIONS

- Industrial Inkjet Printers

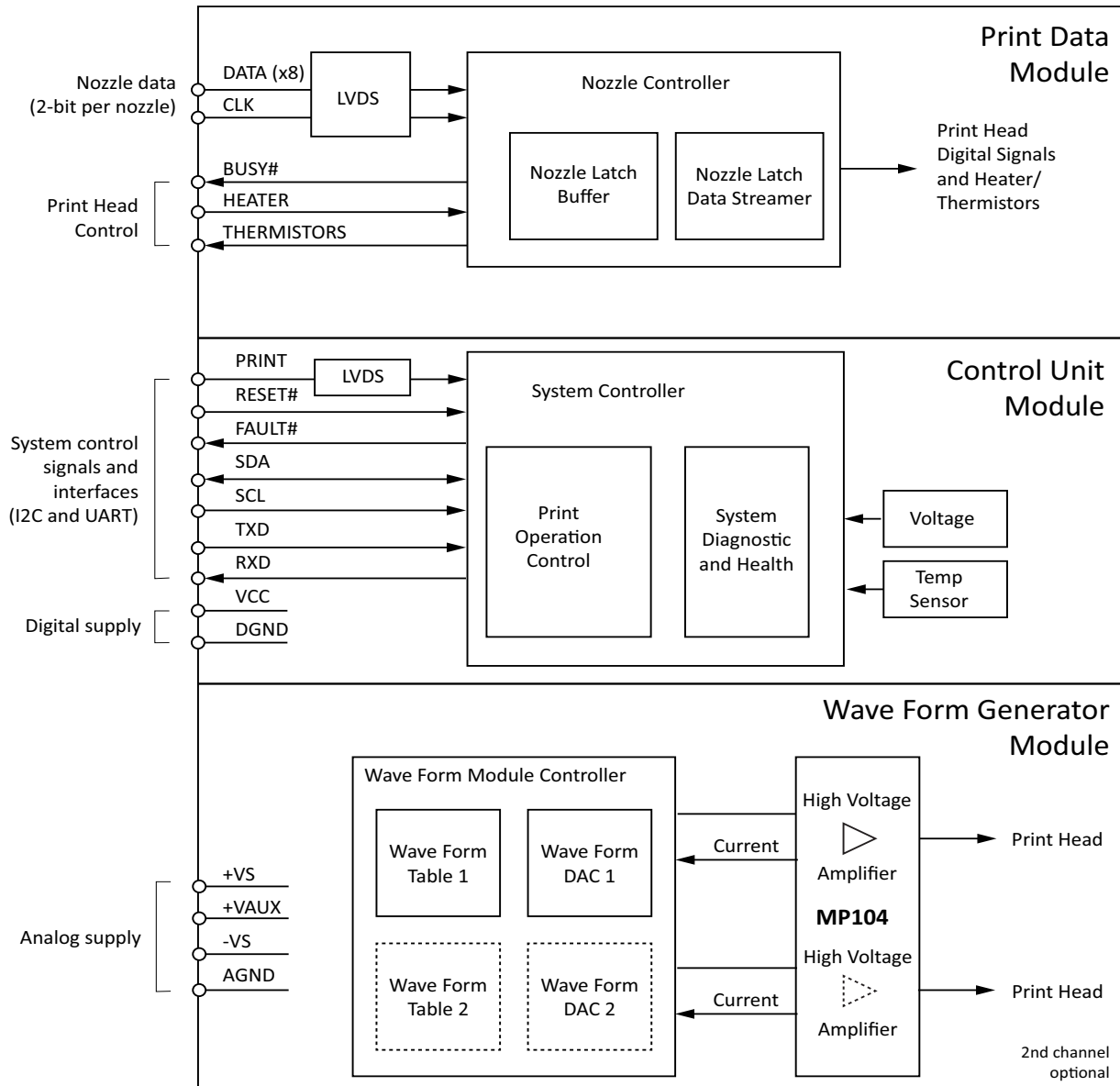
DESCRIPTION

MP113 is an inkjet printhead driver intended for use with Fujifilm Dimatix SG-class printheads. It can also be used with Q-class print heads and compatible printheads of other brands.

MP113 contains an analog and a digital section. The analog section consists of two independent power amplifiers, each of which capable of producing the fire pulses needed to drive up to 512 inkjet nozzles. The digital section converts 1- or 2-bit, digital printing data into bit streams for the printhead's output latches, and exactly timed analog input signals for the power op amps.

The analog section plugs into the digital section and is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink. The digital section has card edge connectors for connection to the printhead(s) and to digital printing control.

Figure 1: Equivalent Schematic



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage	+V _S		165	V
	-V _S	-20		V
	+V _{AUX}		25	V
Digital Supply Voltage	V _{CC}		5.5	V
Fire Pulse Output Current, peak, (within SOA) ¹	I _O (PK)		7.5	A
Power Dissipation, internal ¹	P _D		100	W
Temperature, junction	T _J		150	°C
Temperature Range, storage	T _S	-40	105	°C

Notes:

1. Rating applies to each amplifier channel

ANALOG SPECIFICATIONS

Unless otherwise noted, the analog output of the MP113 has been characterized under the following conditions:

1. Cable lengths to the print head up to 160cm
2. Temperature from 0 to 85°C
3. +V_S at 160V

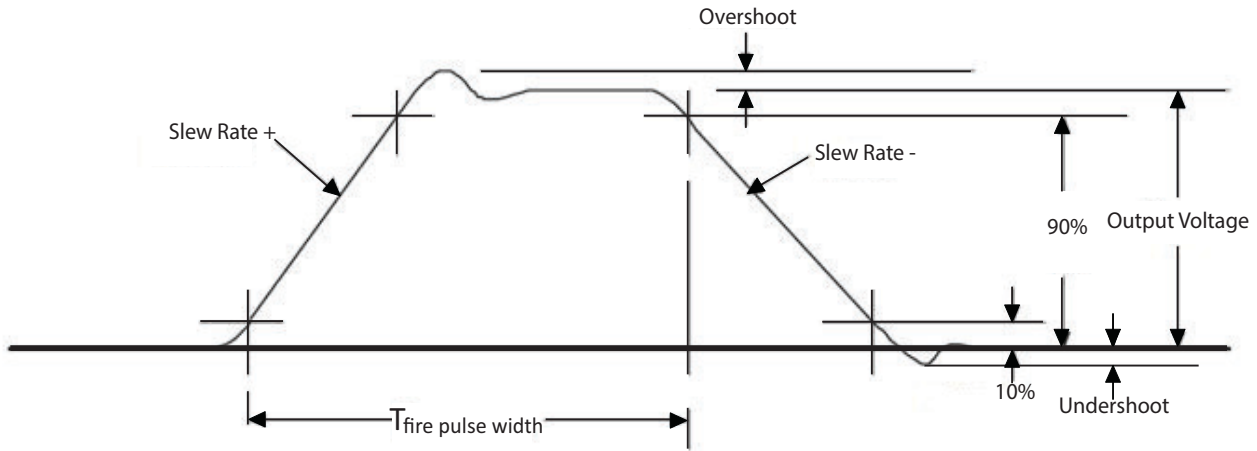
OUTPUT (PER AMPLIFIER CHANNEL)

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Swing	I _{OUT} =4.7A	0 to +V _S -12	0 to +V _S -10		V
Voltage, output accuracy ¹	V _{OUT} =50 to 130V, T _J =25°C ²			1	V
Current, continuous ³				4.7	A
Overshoot ¹	Full temperature range			10	%
Undershoot ¹	Full temperature range			1	V
Slew Rate	C _{LOAD} =75nF	45			V/μs
Capacitive Load				75	nF

Notes:

1. Refer to figure 2 for definition of this parameter. Figure 2 is also defined in Appendix 1 of FFDM's Application Notes: Electronics Design for VersaDrop Jetting with SG-Class Printerheads, figure A1 waveform characteristics.
2. If better precision is required at a different temperature, the unit will need to be re-calibrated at that temperature.
3. The continuous current is internally limited.

Figure 2: Waveform Characteristics



RISE/FALL TIME ERROR

The MP113 analog output will vary from the input waveform uploaded to the module. Rise and fall times vary over amplitude and slew rate requirements. Use the graphs below to adjust input waveforms for rise and fall time error. The data in the graphs below were taken using an SG-1024 print-head operating at 50% load.

Figure 3: Rise Time Error vs Amplitude

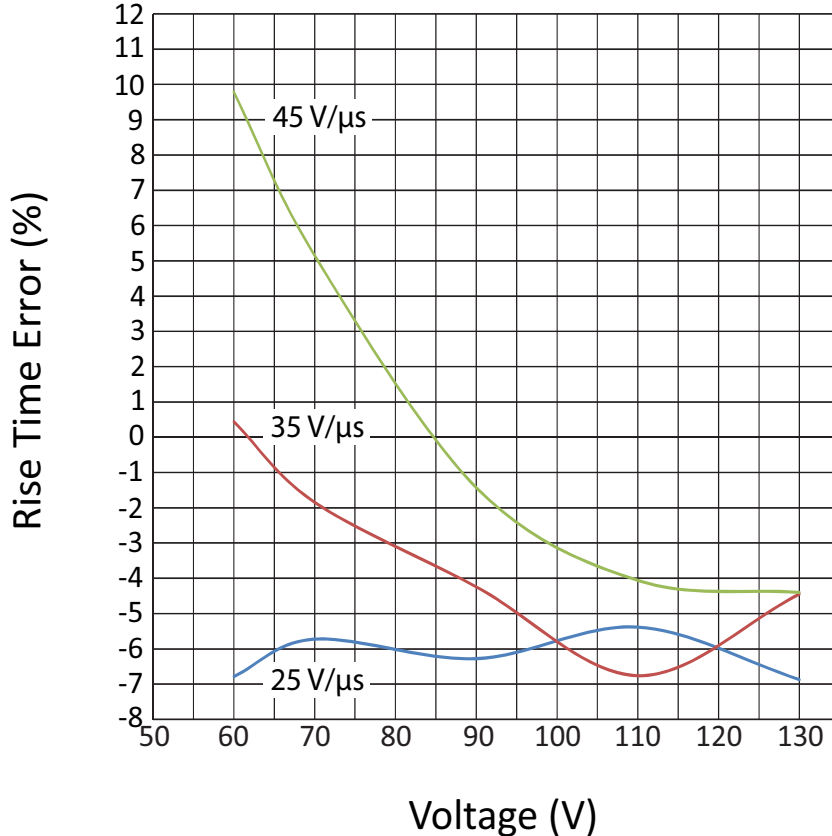
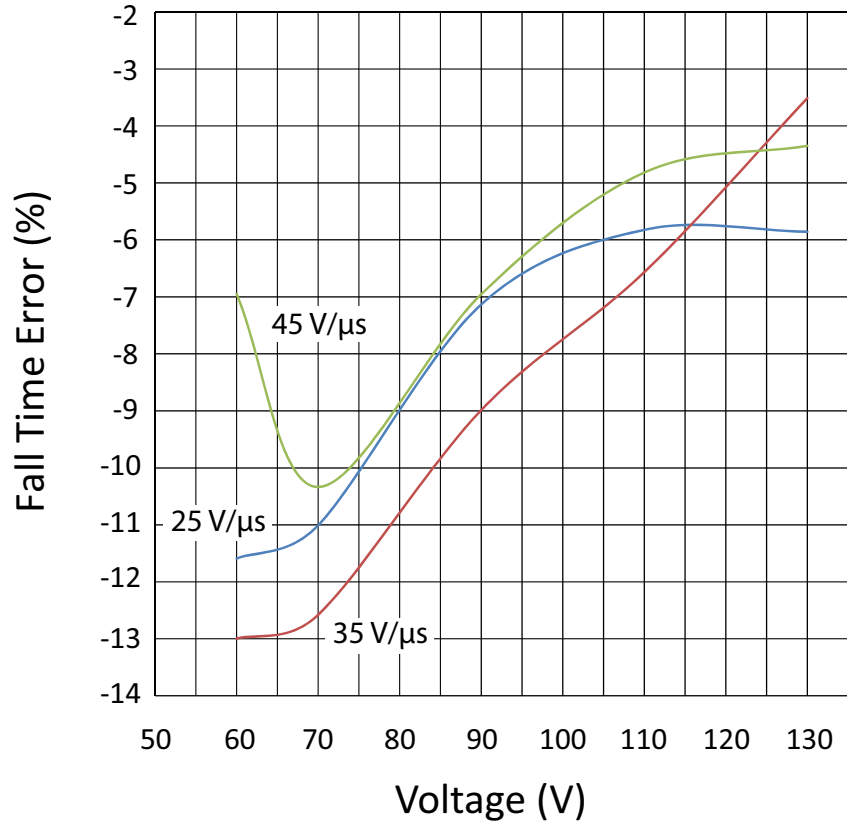


Figure 4: Fall Time Error vs Amplitude



POWER SUPPLY REQUIREMENTS

Parameter		Test Conditions	Min	Typ	Max	Units
Voltage, +V _s			70		160	V
Voltage, -V _s			-20	-18	-15	V
Voltage, V _{AUX}			+20	+24	+25	V
Voltage, V _{CC} ¹			4.75	5.0	5.5	V
Current, quiescent	+V _s to HVGND	+V _s =160V, V _{AUX} =24V, -V _s =-18V		5	7	mA
	V _{AUX} to AGND			18		mA
	-V _s to AGND			-48		mA
Current Consumption, operation	V _{AUX} to AGND	10 kHz, C _L =150nF		22	25	mA
	-V _B to AGND			-58	-60	mA
	V _{CC} to DGND ¹			225	230	mA

Notes:

1. The 5V supply powers the MP113 and the print-head. The V_{CC} continuous current value does NOT include any current used by the print-head.

HIGH VOLTAGE POWER SUPPLY CURRENT USAGE

The current draw on the high voltage power supply (+VS) is determined by the output waveform and pulse repeat frequency. Use figure 6 below to gauge the required output current when selecting a power supply.

All values below were collected at 25°C, +VS = 160V. The MP113 was connected to an SG1024 print-head with all nozzles switched ON, or full load (C_L=150nF). The test waveform was 130V peak at 45 V/us (see figure 5 below).

Figure 5: Waveform Used for Current Testing

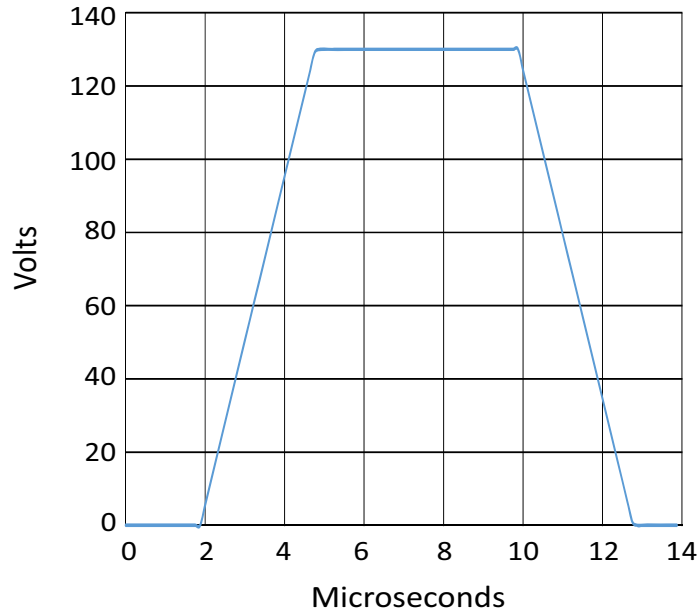
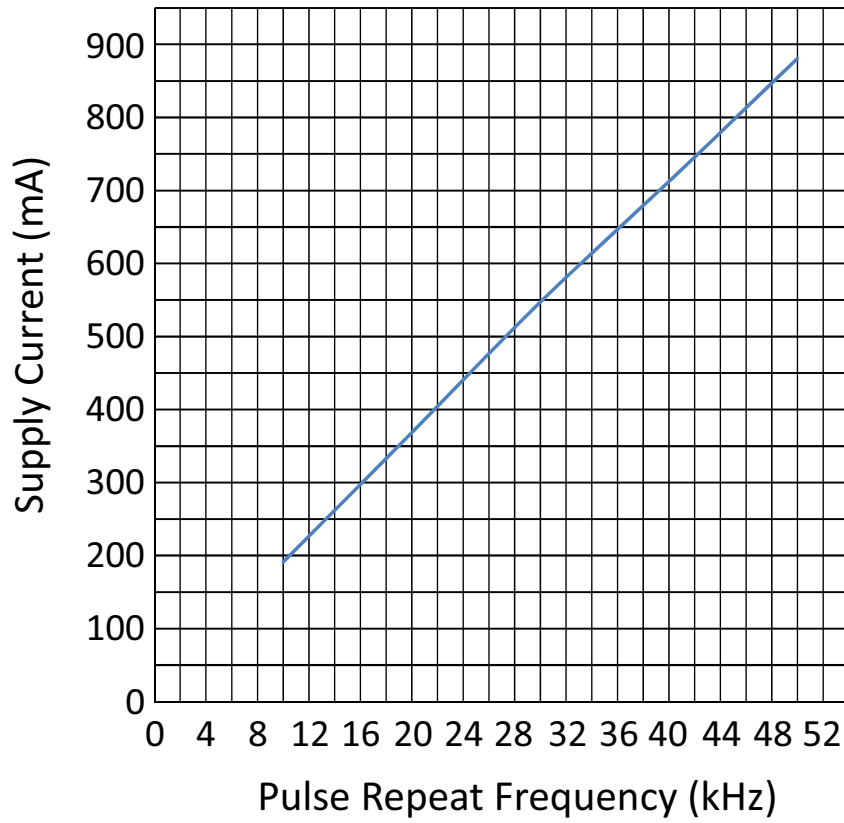


Figure 6: Supply Current vs Pulse Repeat Frequency



SYSTEM PROTECTION

Parameter	Test Conditions	Min	Typ	Max	Units
Temperature Accuracy	$T_C=0^{\circ}\text{C}$ to 85°C^1			± 2	$^{\circ}\text{C}$
Thermal System Shut-down Temperature, TSD			85		$^{\circ}\text{C}$
Thermal System Warning Temperature			70		$^{\circ}\text{C}$
Thermal Shutdown Temperature, Hysteresis			2		$^{\circ}\text{C}$

Notes:

1. T_C is substrate temperature of the analog section (module)

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Resistance, AC junction to case	Full temperature range f>60Hz			1.0	°C/W
Resistance, DC junction to case	Full temperature range f<60Hz			1.25	°C/W
Resistance, junction to ambient				13	°C/W
Temperature Range, case	Meets full range specifications	0		85	°C

DIGITAL SPECIFICATIONS

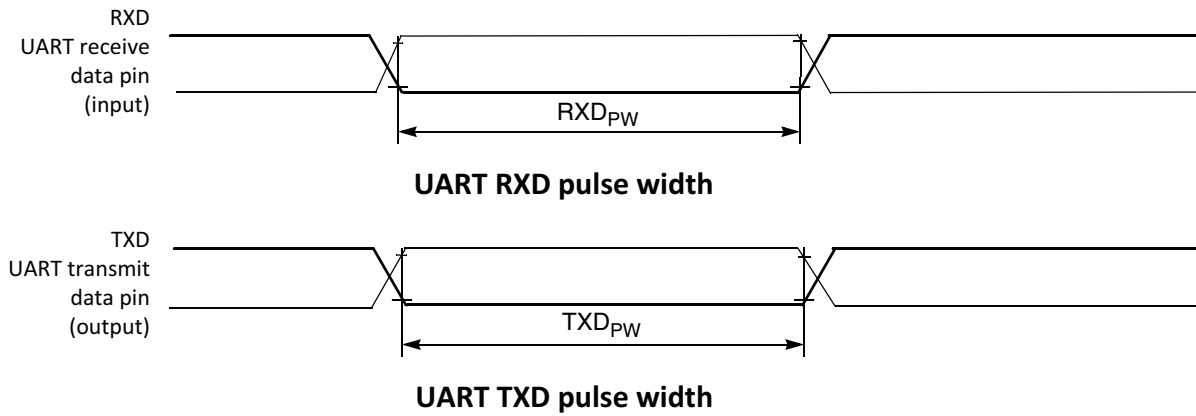
PRINT CONTROL SIGNALS

Parameter	Test Conditions	Min	Typ	Max	Units
Control Output Low Level Voltage, V_{OL}				0.9	V
Control Output High Level Voltage, V_{OH}		2.5			V
Control Input Low Level Voltage, V_{IL}		-0.3		0.8	V
Control Input High Level Voltage, V_{IH}		2.5		3.6	V
LVDS Serial Data Clock Frequency, CLKIN				16	MHz
LVDS Differential Input Threshold, V_{THD}		±100			mV
LVDS Input Voltage, V_{INP} , V_{INM}		0		2.6	V

ASYNCHRONOUS SERIAL COMMUNICATION INTERFACE (UART)

Parameter	Test Conditions	Min	Typ	Max	Units
Baud rate			9600		bit/s
RXD Pulse Width	RXD _{PW}	100.52		108.33	μs
TXD Pulse Width	TXD _{PW}	100.52		108.33	μs

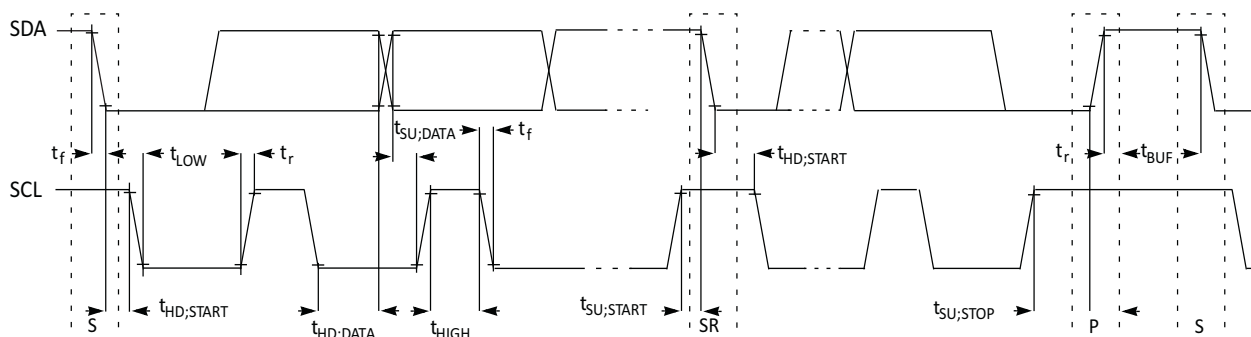
Figure 7: UART Timing



INTER-INTEGRATED CIRCUIT INTERFACE (I²C)

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency		0		100	kHz
Low Period of the SCL Clock	t_{LOW}	4.7			μs
High Period of the SCL Clock	t_{HIGH}	4			μs
Setup Time for Repeat START Condition	$t_{SU;START}$	4.7			μs
Data Hold Time for I ² C Bus Devices	$t_{HD;DATA}$			3.45	μs
Data Setup Time	$t_{SU;DATA}$	0.25			μs
Rise Time of SDA and SCL Signals	t_r			1.0	μs
Fall Time of SDA and SCL Signals	t_f			0.3	μs
Setup Time for STOP Condition	$t_{SU;STOP}$	4			μs
Bus Free Time Between STOP and START	t_{BUF}	4.7			μs

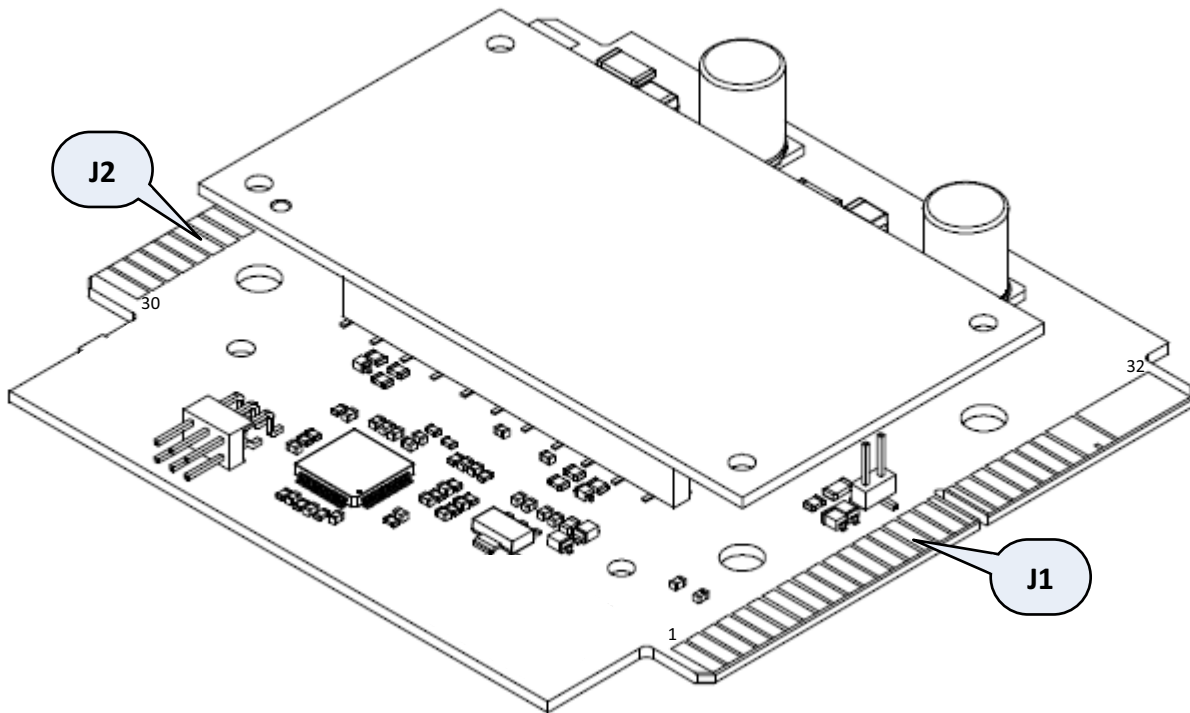
Figure 8: I²C Timing



PINOUT AND DESCRIPTION TABLE

Two sides of the digital section of the MP113 have contact pads to mate with card edge connectors, see figure below. While silk screen pin numbers show 1 through 32 for J1 and 1 through 30 for J2 on the top of the board, pins on the top of the board correspond to odd numbered pins, as shown by the pinout tables below, while pins on the bottom of the board correspond to even numbered pins.

Figure 9: External Connections



J1 64-Positions Card Edge Connector - for Connecting MP113 to Print Control					
J1Pin Number	Card Edge Number	Description	J1 Pin Number	Card Edge Number	Description
1	1	CLKIN_P	2	64	V _{AUX}
3	2	CLKIN_N	4	63	-V _S
5	3	DINO_P	6	62	-V _S
7	4	DINO_N	8	61	-V _S
9	5	DIN1_p	10	60	-V _S
11	6	DIN1_N	12	59	-V _S
13	7	DIN2_P	14	58	-V _S
15	8	DIN2_N	16	57	-V _S
17	9	DIN3_P	18	56	-V _S
19	10	DIN3_N	20	55	HVGND
21	11	DIN4_P	22	54	HVGND
23	12	DIN4_N	24	53	HVGND
25	13	DIN5_P	26	52	HVGND
27	14	DIN5_N	28	51	HVGND
29	15	DIN6_P	30	50	HVGND
31	16	DIN6_N	32	49	HVGND
33	17	DIN7_P	34	48	HVGND
35	18	DIN7_N	36	47	AGND
37	19	PRINT_P	38	46	+V _S
39	20	PRINT_N	40	45	+V _S
41	21	SDA	42	44	+V _S
43	22	SCL	44	43	+V _S
45	23	RESET #	46	42	+V _S
47	24	BUSY#	48	41	+V _S
49	25	FAULT#	50	40	+V _S
51	26	VCC	52	39	+V _S
53	27	VCC	54	38	HTRA
55	28	DGND	56	37	HTRB
57	29	DGND	58	36	HTRA
59	30	DGND	60	35	HTRB
61	31	DGND	62	34	THA
63	32	DGND	64	33	THB

- Notes:**
- a) DGND...ground signal for VCC
 - b) HVGND...ground signal for +V_S
 - c) AGND...ground signal for V_{AUX} and -V_S

It is recommended to keep the ground signals separate to avoid ground loops (which decrease signal quality).

J2 60-Positions Card Edge Connector - for Connecting MP113 to Print Head				
Pin Number	Connection	Pin Number	Connection	Note
1	GND	60	FP7	60 and 59 are Twisted Pair
2	VCC	59	GND	
3	GND	58	FP6	58 and 57 are Twisted Pair
4	VCC	57	GND	
5	CONFIG	56	FP5	56 and 55 are Twisted Pair
6	GND	55	GND	
7	C1_CLK_N	54	FP4	54 and 53 are Twisted Pair
8	C1_CLK_P	53	GND	
9	C2_CLK_N	52	FP3	52 and 51 are Twisted Pair
10	C2_CLK_P	51	GND	
11	C1_LAT_N	50	FP2	50 and 49 are Twisted Pair
12	C1_LAT_P	49	GND	
13	D0_N	48	FP1	48 and 47 are Twisted Pair
14	D0_P	47	GND	
15	D1_N	46	FP0	46 and 45 are Twisted Pair
16	D1_P	45	GND	
17	D2_N	44	GND	
18	D2_P	43	GND	
19	D3_N	42	HTRA	
20	D3_P	41	HTRB	
21	D4_N	40	GND	
22	D4_P	39	GND	
23	D5_N	38	HTRA	
24	D5_P	37	HTRB	
25	D6_N	36	THA	
26	D6_P	35	THB	
27	D7_N	34	SDA	
28	D7_P	33	GND	
29	C2_LAT_N	32	SCL	
30	C2_LAT_P	31	GND	

INPUT DATA AND WAVEFORM TIMING (GRAYSCALE MODE)

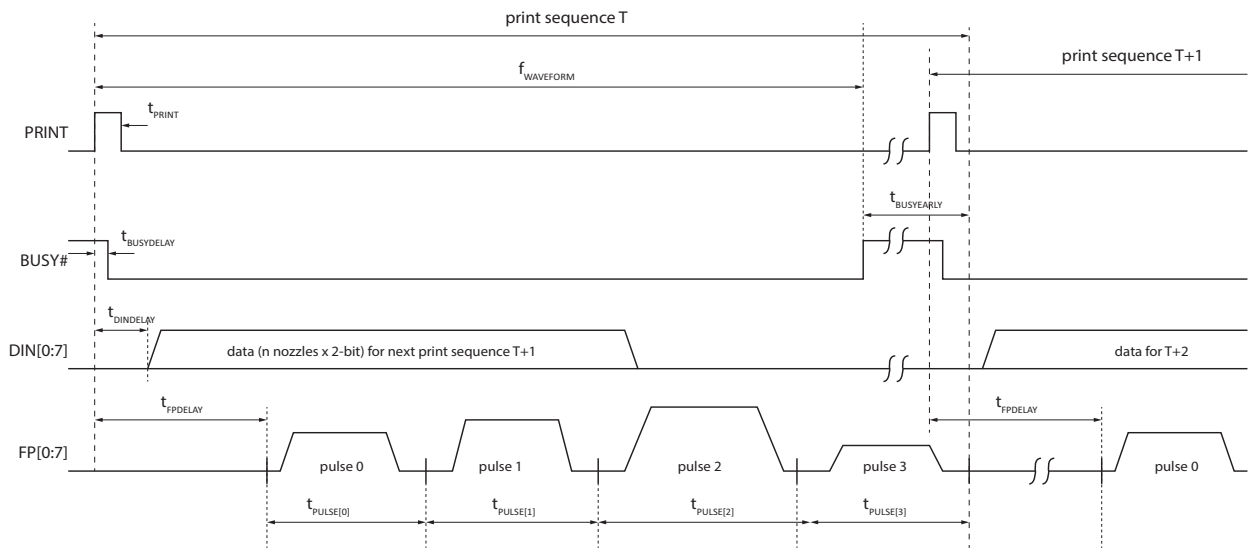
Parameter	Symbol	Min	Typ	Max	Units
Print Pulse Width	t _{PRINT}	70		1000	ns
Busy Signal Delay	t _{BUSYDELAY}			100	ns
Print to Fire Pulse Start Delay	t _{FPDELAY}		13.8		μs
Print to Next Data in Delay	t _{DINDELAY}	300			ns
Busy Signal Release to Fire Pulse End	t _{BUSYEARLY}		3.5		μs
Minimum Pulse Duration	t _{PULSE[n]}	10.0			μs
Waveform Frequency, single pulse	f _{WAVEFORM}			50	kHz

- Notes:** a) A PRINT pulse is ignored while the BUSY# signal is active (low level)
b) The maximum possible printing frequency of a waveform can be calculated as:

$$f = \frac{1}{9\mu s + \sum t_{PULSE[n]}}$$

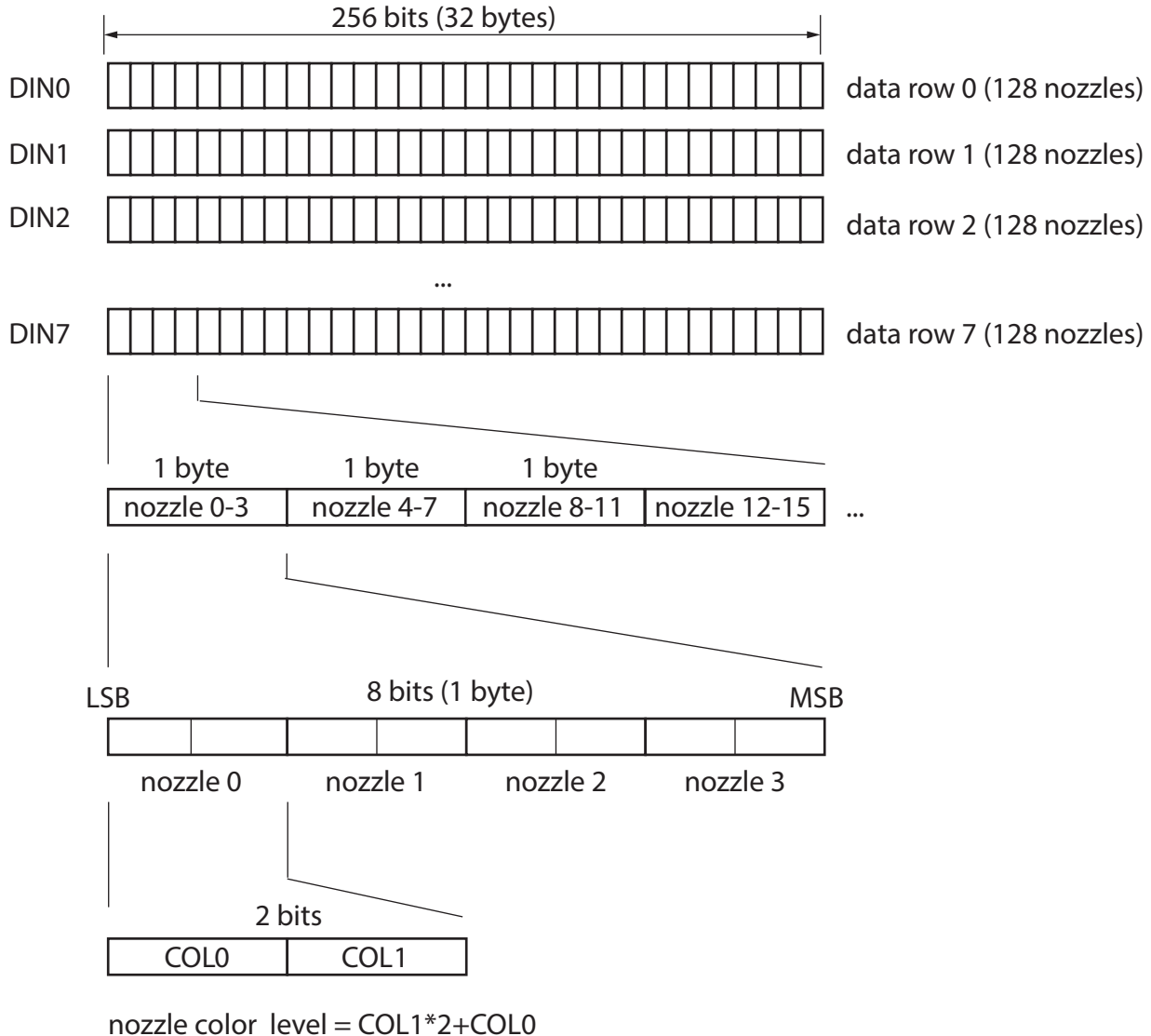
- c) The system can start a new print sequence while the current print sequence is still active once the BUSY# signal becomes inactive (high level). The minimum effective delay between two fire pulses is therefore 9μs.

Figure 10: Signal Timing Diagram



INPUT DATA STREAM FORMAT (DIN[7:0])

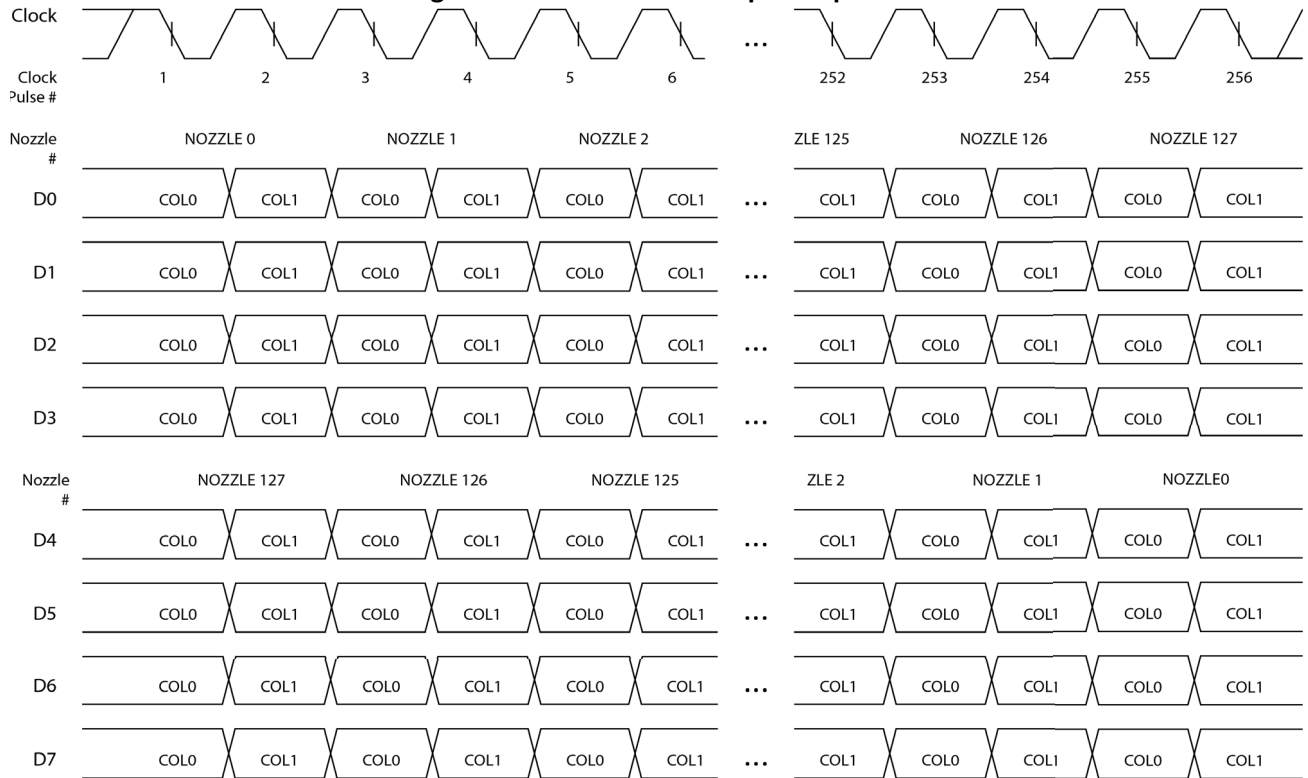
Figure 11: Input Data Stream



The timing diagram below shows the data and clock sequence for a SG-1024 nozzle print head. Data is fetched by the MP113 at the falling edge of the clock signal. The inversion of D4-D7 (nozzle 127 first, nozzle 0 last) is specific to the SG-1024 print head and not caused by MP113. MP113 handles the input data same as the connected print head.

Data is shifted in by nozzle row. Please refer to the print head specification to understand the organization of nozzles (or print jets) and rows. For each nozzle, 2 bits (COL0, COL1) are used to define the intensity level of the nozzle (L0 – L3). The intensity level of each nozzle is calculated as $L = \text{COL1} * 2 + \text{COL0}$. The clock signal at the beginning of the shift sequence can be either low or high, as the MP113 only uses the falling edge to fetch data.

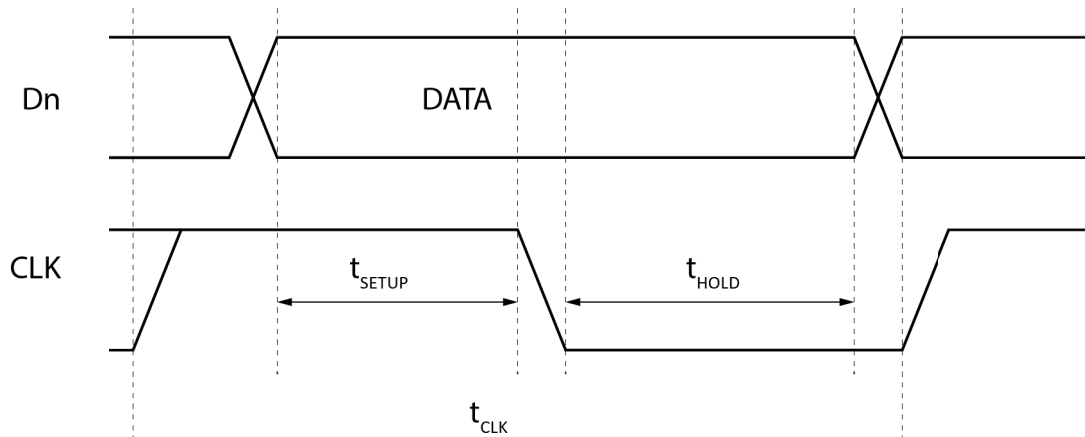
Figure 12: Data and Clock Input Sequence



SG-1024 Grayscale Mode

Parameter	Symbol	Min	Typ	Max	Units
Data Setup Time	t_{SETUP}	20			ns
Data Hold Time	t_{HOLD}	10			ns
Clock Period	t_{CLK}	62.5			ns

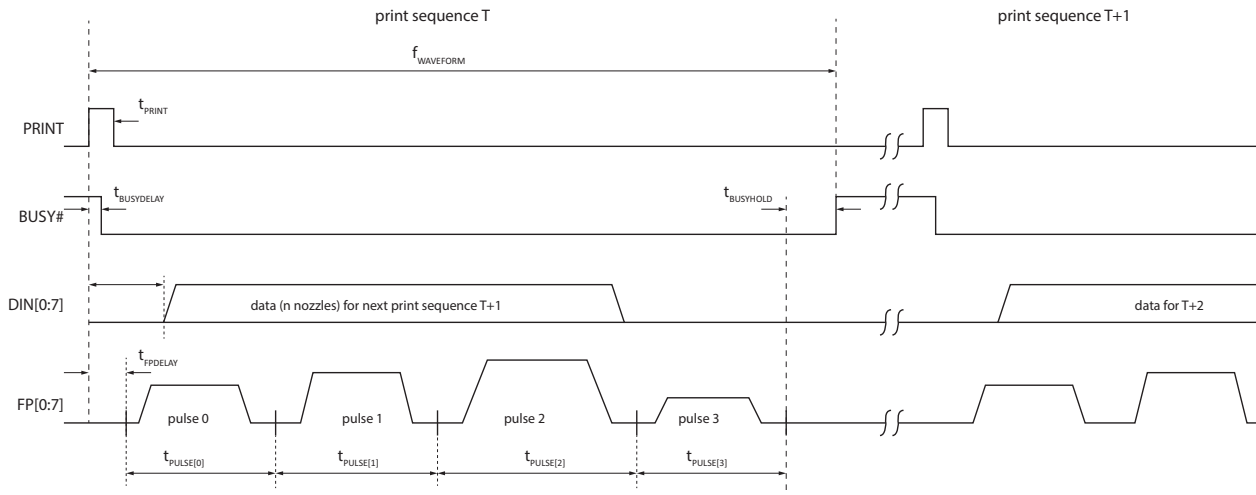
Figure 13: Data Input Timing



INPUT DATA AND WAVEFORM TIMING (BINARY MODE)

For systems where grayscale mode is not needed, MP113 also offers a binary mode. In binary mode, a nozzle is either ON or OFF during a print sequence.

Figure 14: Binary Mode Signal Timing Diagram

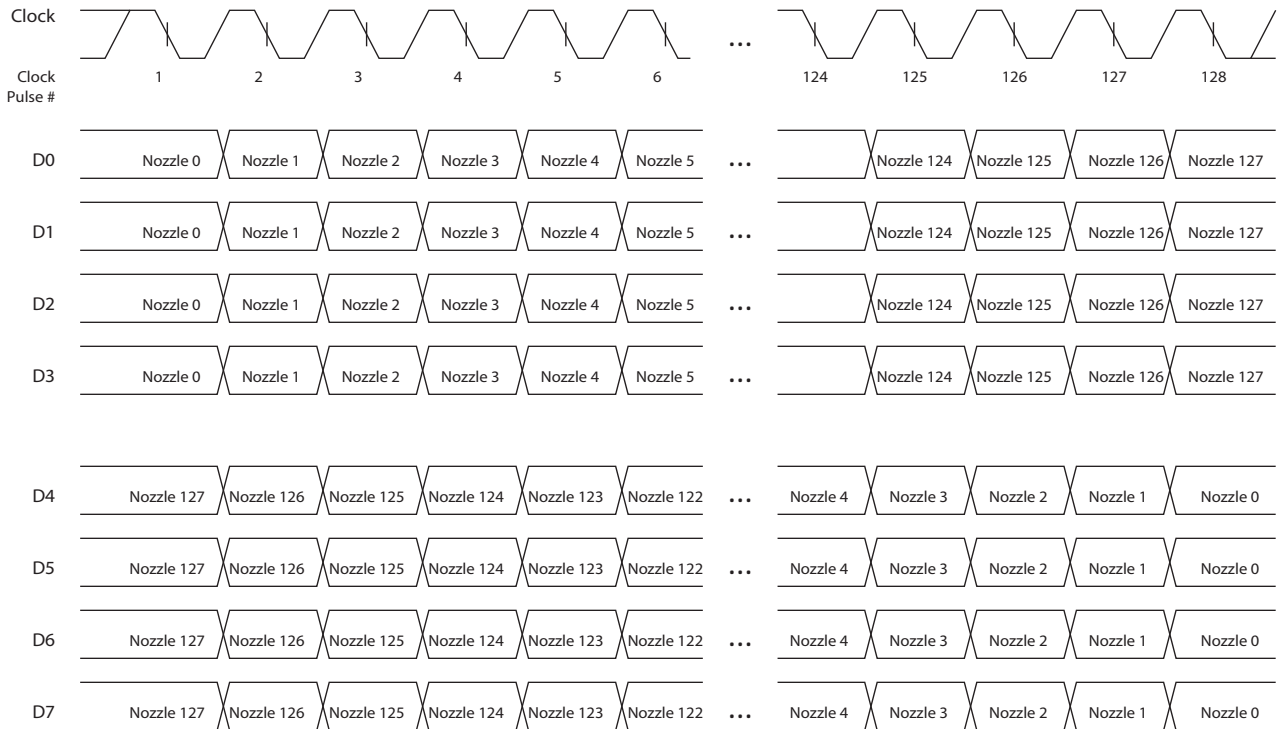


Parameter	Symbol	Min	Typ	Max	Units
Print Pulse Width	t_{PRINT}	70		1000	ns
Busy Signal Delay	$t_{BUSYDELAY}$			100	ns
Print to Fire Pulse Start Delay	$t_{FPDELAY}$		13.8		μs
Print to Next Data in Delay	$t_{DINDELAY}$	300			ns
Busy Signal Release to Fire Pulse End	$t_{BUSYEALRY}$		3.5		μs
Minimum Pulse Duration	$t_{PULSE[n]}$	10.0			μs
Waveform Frequency, single pulse	$f_{WAVEFORM}$			50	kHz

- Notes:**
- a) A PRINT pulse is ignored while the BUSY# signal is active (low level)
 - b) The maximum possible printing frequency of a waveform can be calculated as:

$$f = \frac{1}{9\mu s + \sum t_{PULSE[n]}}$$

Figure 15: Binary Mode Data Input Sequence



SG-1024 Binary Mode

The timing diagram above shows the data and clock sequence for a SG-1024 nozzle print head. The data and clock lines are direct pass-through from the input connector to the output connector. Therefore, the data and clock timing requirements of the input lines are same as the lines would be connected directly to the print head.

The print head is operated in latched mode. The print input signal is connected to the LATCH signal of the print head. Data for the next print sequence can be shifted in while a print sequence is active.

Data is shifted in by nozzle row. Please refer to the print head specification to understand the organization of nozzles (or print jets) and rows.

POWER SUPPLY SEQUENCING

For reliable operation it is suggested that the power supplies be turned on and off in the following sequence;

Power on sequence: V_{CC} , V_{AUX} , $-V_S$, $+V_S$

Power off sequence: $+V_S$, $-V_S$, V_{AUX} , V_{CC}

HEAT SINK MOUNTING

The IMS board provides a very low thermal resistance path for the heat generated by the high power of the fire pulse amplifier. This IMS board must be attached to a heat sink of adequate size for heat dissipation and reliable operation. Mounting holes for mounting the IMS board to the heat sink are located in each corner of the IMS board. There are access holes through the main board coincident to the IMS board mounting holes to allow screwdriver access for tightening mounting screws through the IMS board into the heat sink.

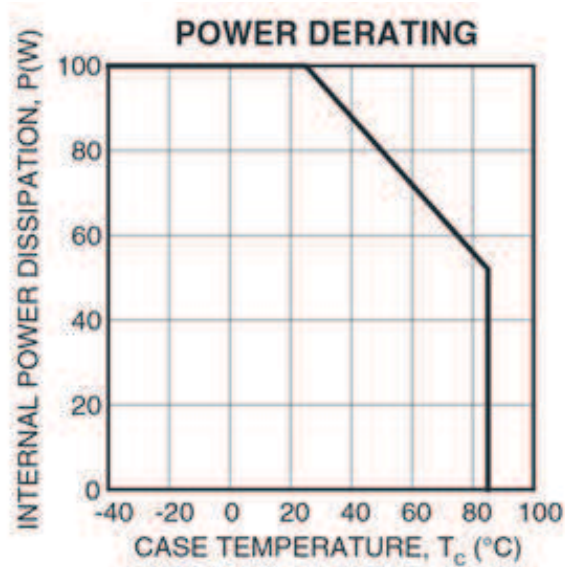
Thermal grease must be used between the back side of the IMS board and the heat sink. The IMS board must sit flush to the heat sink with no gaps between the IMS board and heat sink.

INTERNAL POWER DISSIPATION

The internal power dissipation in each channel of MP113 is limited to 100W at a case temperature of 25°C. Each channel drives half of the fire pulse lines to the print head. Channel A drives FP0 – FP3 and Channel B drives FP4 – FP7.

The allowed power dissipation is de-rated by 0.75W/°C increase in case temperature. See the power derating curve.

Figure 16: Power Derating Curve



The IMS board must be mounted to a heat sink with low enough thermal resistance to ambient to maintain the case temperature at a safe level. For example, with ambient temperature of 25°C and average internal power dissipation of 55W the maximum allowable case temperature is 80°C. A heat sink with a thermal resistance rating of 1 °C/W is needed.

Internal Power Dissipation, P_D = 55W

Allowable Case Temperature, T_C = 80°C

Ambient Temperature, T_A = 25°C

Heat Sink Thermal Resistance,

$$R_{TH} = \frac{T_C - T_A}{PD} = \frac{80^\circ C - 25^\circ C}{55W} = 1^\circ C/W$$

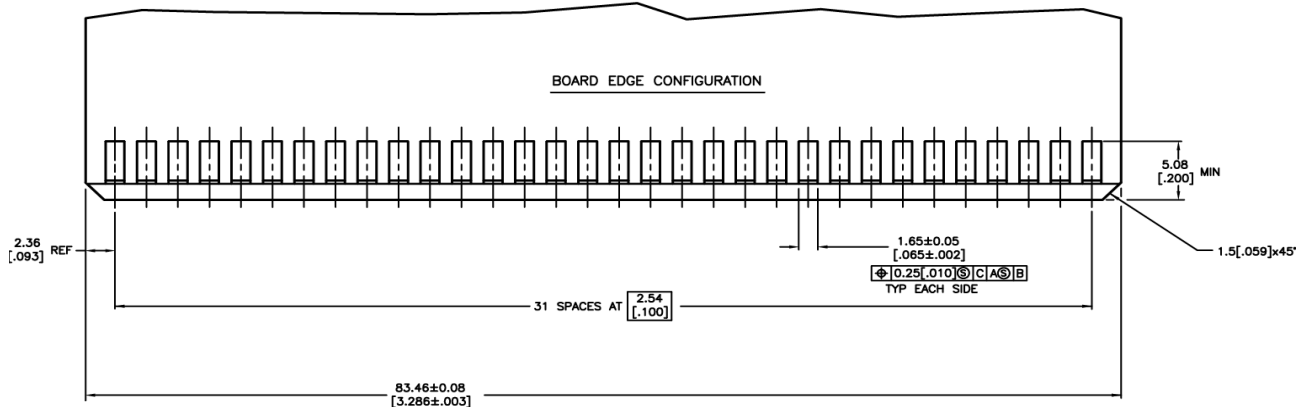
Heat sink thermal resistance can be improved by using active cooling such as forced air or liquid cooling. The average internal power dissipation can be reduced by decreasing the duty cycle of the fire pulse wave form (lower frequency).

OVERVOLTAGE PROTECTION

Some applications will need over voltage protection devices connected between the power supply rails and ground. Unidirectional transient voltage suppressor diodes are recommended. The TVS diodes clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether TVS diodes are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

PACKAGE OUTLINE

Figure 17: Card Edge Dimensions



PACKAGE OPTIONS

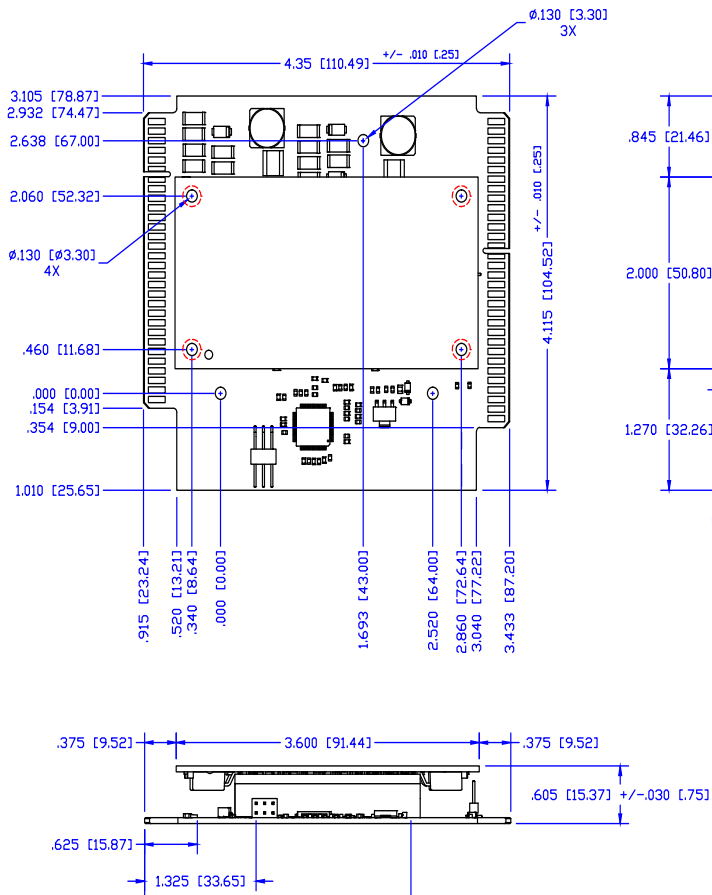
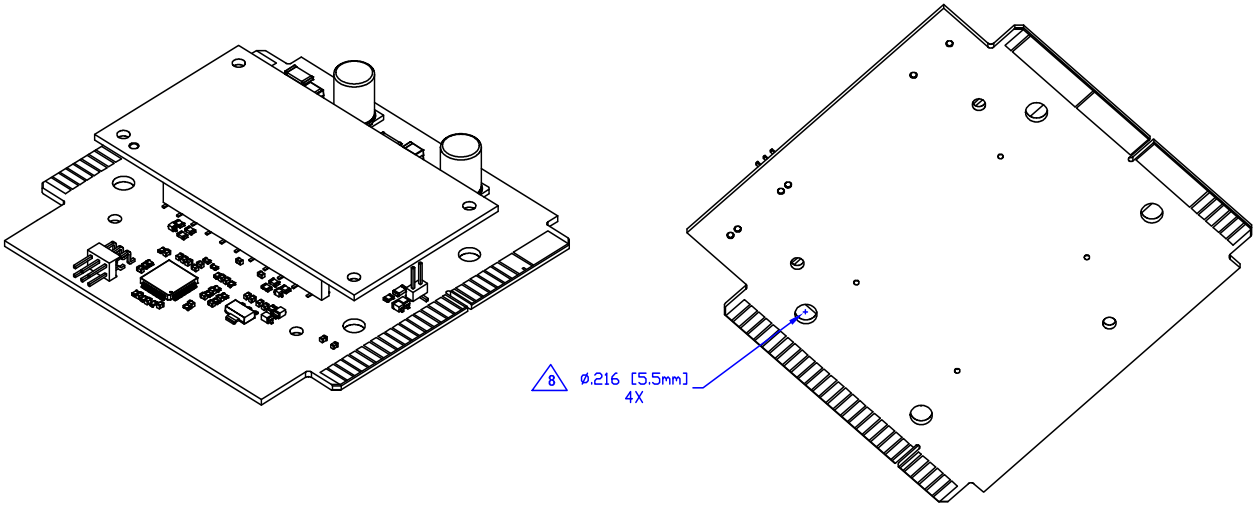
Part Number	Apex Package Style	Description
MP113	NC	Module Edge Conn 60P, 64P

Recommended card edge connectors:

60-pin: Sullins CONN EDGE CARD 60POS .100 EYELET, part number ACC30DREH

64-pin: TE Connectivity, part number 1761469-1

PACKAGE STYLE NC



NOTES:

1. Dimensions are inches; alternate units are [mm].
2. Recommended mating edge connector or equivalent:
 64-pin TE Connectivity p/n 1761469-1
 60-pin TE Connectivity p/n 1-5530843-8
3. Material:
 Digital unit - .062 [1.57] thick FR-4, 2 oz. Cu conductors.
 Analog unit - .062 [1.57] thick, 2 oz. Cu conductors over 600V dielectric over aluminum substrate.
4. Hard gold plating on edge connector contacts.
5. Not recommended that mating connectors between digital and analog unit be used as mechanical support.
6. When designing or choosing a heatsink, allow adequate space for components on the digital unit.
7. Use #4 or equivalent screws for analog unit to heatsink.
8. Four holes in digital unit used to secure mounting holes.

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