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MP2106

1.5A, 15V, 800kHz Synchronous Buck Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2106 is a 1.5A, 800kHz synchronous buck converter designed for low voltage applications requiring high efficiency. It is capable of providing output voltages as low as 0.9V, and integrates top and bottom switches to minimize power loss and component count. The 800kHz switching frequency reduces the size of filtering components, further reducing the solution size.

The MP2106 includes cycle-by-cycle current limiting and under voltage lockout. The internal power switches, combined with the tiny 10-pin MSOP and QFN packages, provide a solution requiring a minimum of surface area.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV2106DQ/DK-00A	2.5"X x 2.0"Y x 0.5"Z

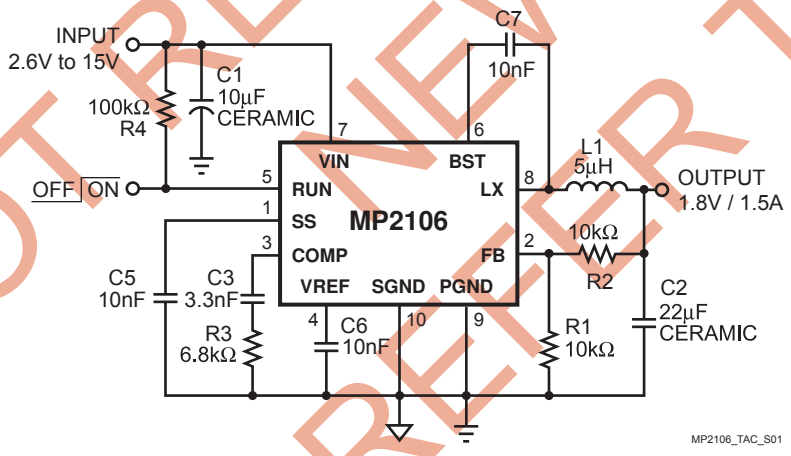
FEATURES

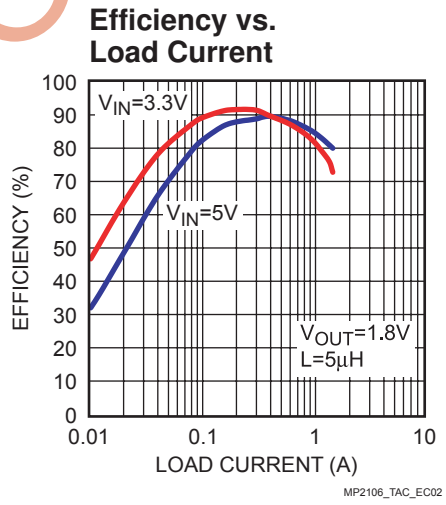
- 1.5A Output Current
- Synchronous Rectification
- Internal 210mΩ and 255mΩ Power Switches
- Input Range of 2.6V to 15V
- >90% Efficiency
- Zero Current Shutdown Mode
- Under Voltage Lockout Protection
- Soft-Start Operation
- Thermal Shutdown
- Internal Current Limit (Source & Sink)
- Tiny 10-Pin MSOP or QFN Package

APPLICATIONS

- DC/DC Regulation from Wall Adapters
- Portable Entertainment Systems
- Set Top Boxes
- Digital Video Cameras, DECT
- Networking Equipment
- Wireless Modems

TYPICAL APPLICATION



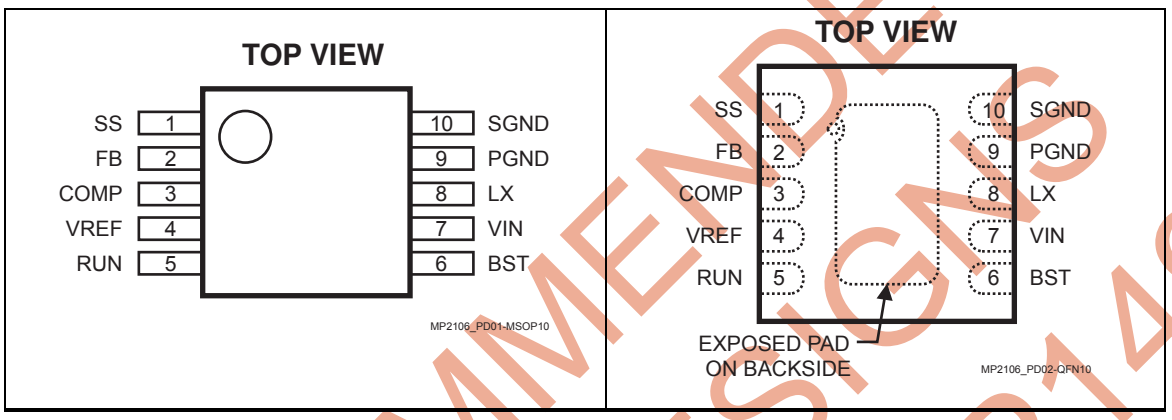


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2106DK*	MSOP10	2106D	-40°C to +85°C
MP2106DQ**	QFN10 (3x3mm)	C4	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2106DK–Z).
For Lead Free, add suffix –LF (e.g. MP2106DK–LF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP2106DQ–Z).
For Lead Free, add suffix –LF (e.g. MP2106DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Supply Voltage V_{IN} 16V
LX Voltage V_{LX} ..... -0.3V to V_{IN} + 0.3V
BST to LX Voltage ..... -0.3V to +6V
Voltage on All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
MSOP10 ..... 0.83W
QFN10 ..... 2.5W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operating Conditions (3)

Input Supply Voltage V_{IN} ..... 2.6V to 15V
Output Voltage V_{OUT} ..... 0.9V to V_{IN} x 80%
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
MSOP10	150	65	°C/W
QFN10 (3x3mm)	50	12	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.6		15	V
Input Under Voltage Lockout				2.2		V
Input Under Voltage Lockout Hysteresis				100		mV
Shutdown Supply Current		V_{RUN} ≤ 0.3V		0.5	1.0	µA
Operating Supply Current		V_{RUN} > 2V, V_{FB} = 1.1V		1.2	1.8	mA
VREF Voltage	V_{REF}	V_{IN} = 2.6V to 15V		2.4		V
RUN Input Low Voltage	V_{IL}				0.4	V
RUN Input High Voltage	V_{HL}		1.5			V
RUN Hysteresis				100		mV
RUN Input Bias Current					1	µA
Oscillator						
Switching Frequency	f_{SW}		700	800	900	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	85			%
Minimum On Time	t_{ON}			200		ns
Error Amplifier						
Voltage Gain	A_{VEA}			400		V/V
Transconductance	G_{EA}			300		µA/V
COMP Maximum Output Current				±30		µA
FB Regulation Voltage	V_{FB}		875	895	915	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.895V		-100		nA
Soft-Start						
Soft-Start Current	I_{SS}			2		µA
Soft-Start Period		C_{SS} = 0.1µF		15		ms
Output Switch On-Resistance						
Switch On Resistance		V_{IN} = 5V		255		mΩ
		V_{IN} = 3V		315		mΩ
Synchronous Rectifier On Resistance		V_{IN} = 5V		210		mΩ
		V_{IN} = 3V		255		mΩ
Switch Current Limit (Source)			2.0	2.5	3.2	A
Synchronous Rectifier Current Limit (Sink) (5)				350		mA
Thermal Shutdown				160		°C

Note:

5) Guaranteed by design.

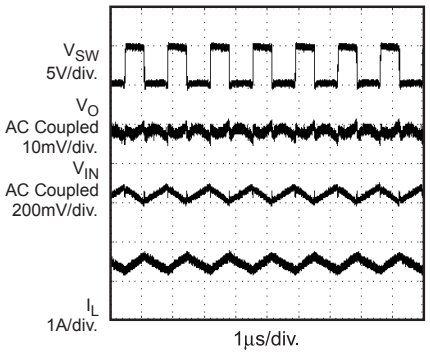
PIN FUNCTIONS

Pin #	Name	Description
1	SS	Soft-Start Input. Place a capacitor from SS to SGND to set the soft-start period. The MP2106 sources 2μA from SS to the soft-start capacitor at startup. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during startup.
2	FB	Feedback Input. FB is the inverting input of the internal error amplifier. Connect a resistive voltage divider from the output voltage to FB to set the output voltage value.
3	COMP	Compensation Node. COMP is the output of the error amplifier. Connect a series RC network to compensate the regulation control loop.
4	VREF	Internal 2.4V Regulator Bypass. Connect a 10nF capacitor between VREF and SGND to bypass the internal regulator. Do not apply any load to VREF.
5	RUN	On/Off Control Input. Drive RUN high to turn on the MP2106; low to turn it off. For automatic startup, connect RUN to VIN via a pullup resistor.
6	BST	Power Switch Boost. BST powers the gate of the high-side N-Channel power MOSFET switch. Connect a 10nF or greater capacitor between BST and LX.
7	VIN	Internal Power Input. VIN supplies the power to the MP2106 through the internal LDO regulator. Bypass VIN to PGND with a 10μF or greater capacitor. Connect VIN to the input source voltage.
8	LX	Output Switching Node. LX is the source of the high-side N-Channel switch and the drain of the low-side N-Channel switch. Connect the output LC filter between LX and the output.
9	PGND	Power Ground. PGND is the source of the N-Channel MOSFET synchronous rectifier. Connect PGND to SGND as close to the MP2106 as possible.
10	SGND	Signal Ground.

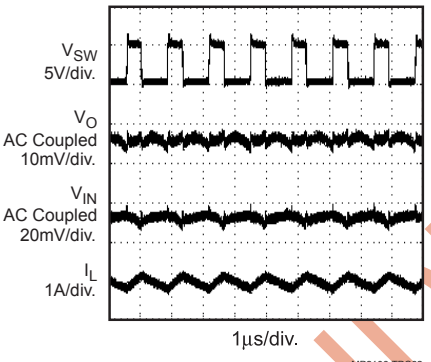
TYPICAL PERFORMANCE CHARACTERISTICS

Circuit of Figure 2, V_{IN} = 5V, V_{OUT} = 1.8V, L1 = 5µH, C1 = 10µF, C2 = 22µF, T_A = +25°C, unless otherwise noted.

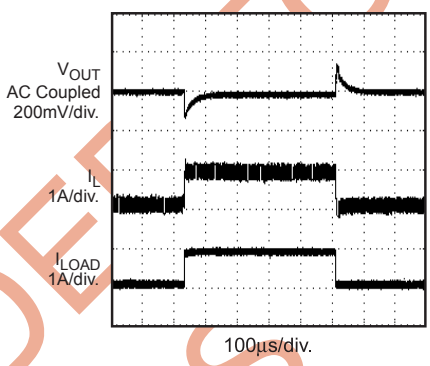
Steady State Operation
1.5A Load



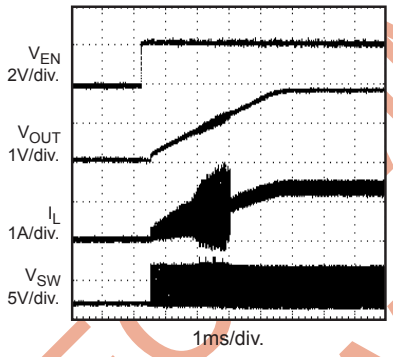
Steady State Operation
No Load



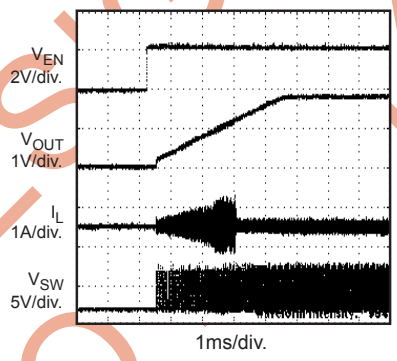
Load Transient



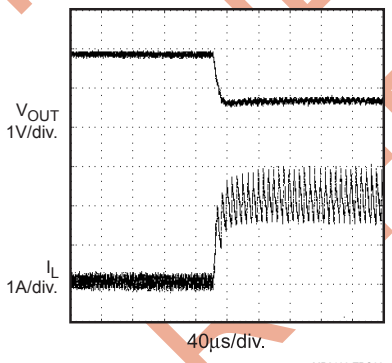
Startup from Shutdown
1.5A Resistive Load



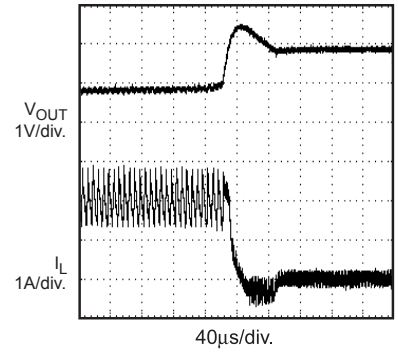
Startup from Shutdown
No Load



Short Circuit Protection



Short Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM

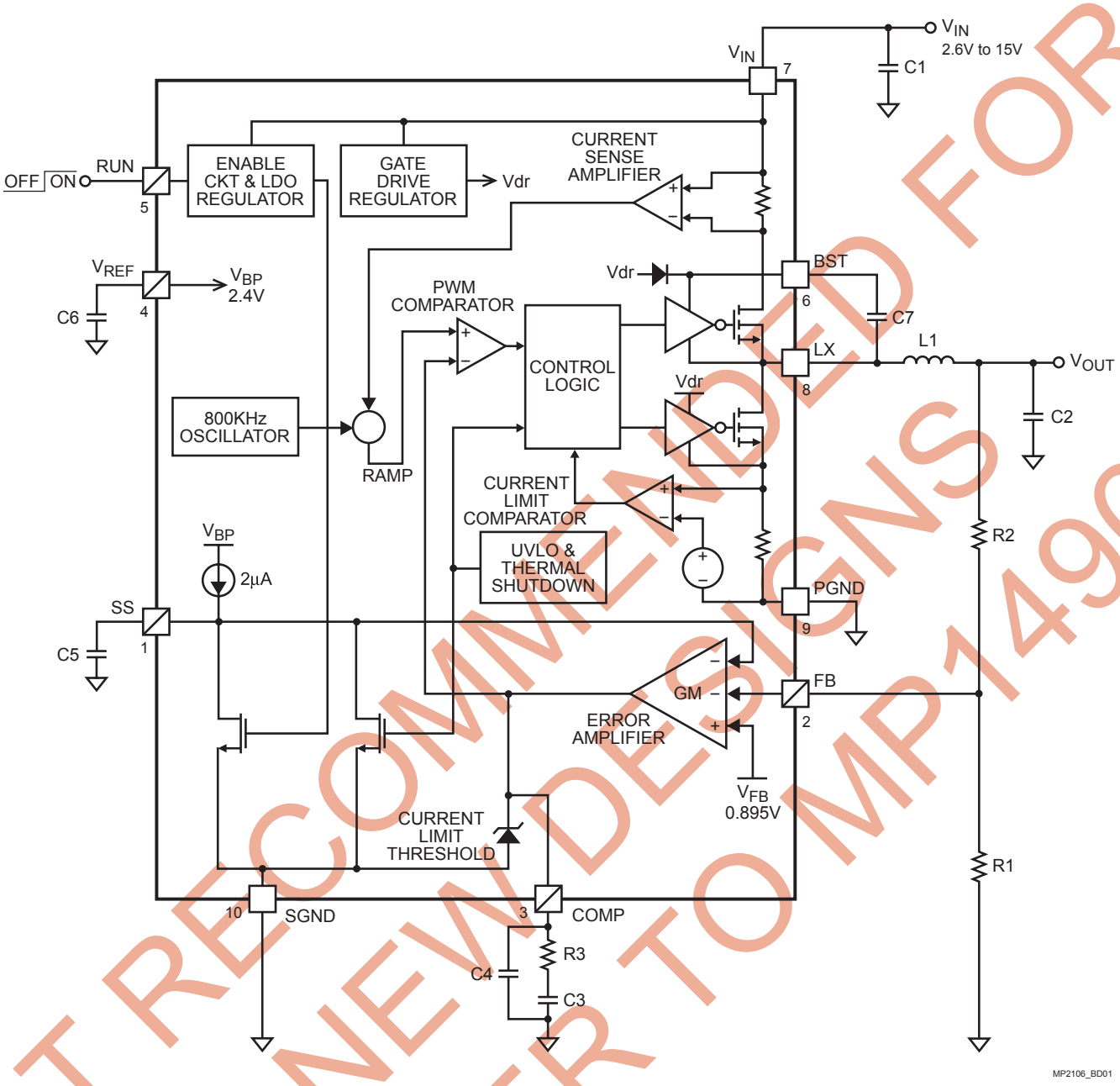


Figure 1—Functional Block Diagram

OPERATION

The MP2106 measures the output voltage through an external resistive voltage divider and compares that voltage to the internal 0.9V reference in order to generate the error voltage at COMP. The current-mode regulator uses the voltage at COMP and compares it to the inductor current to regulate the output voltage. The use of current-mode regulation improves transient response and improves control loop stability.

At the beginning of each cycle, the high-side N-Channel MOSFET is turned on, forcing the inductor current to rise. The current at the drain of the high-side MOSFET is internally measured and converted to a voltage by the current sense amplifier.

That voltage is compared to the error voltage at COMP. When the inductor current rises sufficiently, the PWM comparator turns off the high-side switch and turns on the low-side switch, forcing the inductor current to decrease. The average inductor current is controlled by the voltage at COMP, which in turn is controlled by the output voltage. Thus the output voltage controls the inductor current to satisfy the load.

Since the high-side N-Channel MOSFET requires voltages above V_{IN} to drive its gate, a bootstrap capacitor from LX to BST is required to drive the high-side MOSFET gate. When LX is driven low (through the low-side MOSFET), the BST capacitor is internally charged. The voltage at BST is applied to the high-side MOSFET gate to turn it on, and maintains that voltage until the high-side MOSFET is turned off and the low-side MOSFET is turned on, and the cycle repeats. Connect a 10nF or greater capacitor from BST to SW to drive the high-side MOSFET gate.

APPLICATION INFORMATION

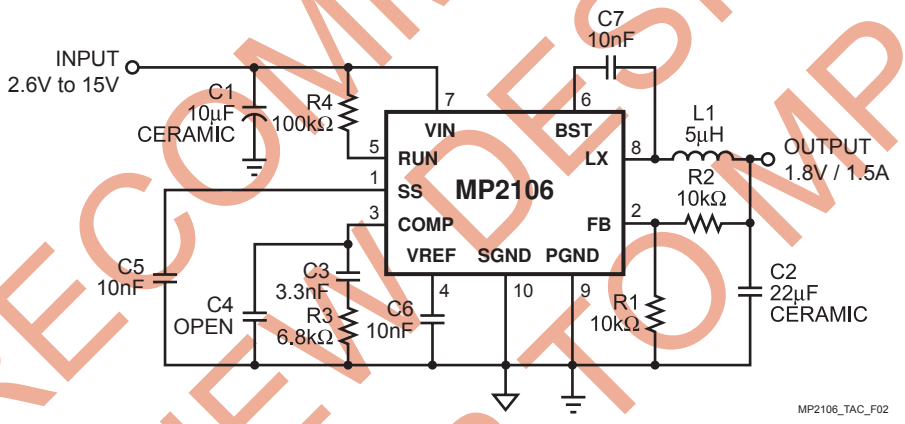


Figure 2—Typical Application Circuit

APPLICATION INFORMATION

Internal Low-Dropout Regulator

The internal power to the MP2106 is supplied from the input voltage (VIN) through an internal 2.4V low-dropout linear regulator, whose output is VREF. Bypass VREF to SGND with a 10nF or greater capacitor for proper operation. The internal regulator can not supply more current than is required to operate the MP2106. Therefore, do not apply any external load to VREF.

Soft-Start

The MP2106 includes a soft-start timer that slowly ramps the output voltage at startup to prevent excessive current at the input.

When power is applied to the MP2106, and RUN is asserted, a 2μA internal current source charges the external capacitor at SS. As the capacitor charges, the voltage at SS rises. The MP2106 internally limits the feedback threshold voltage at FB to that of the voltage at SS. This forces the output voltage to rise at the same rate as the voltage at SS, forcing the output voltage to ramp linearly from 0V to the desired regulation voltage during soft-start.

The soft-start period is determined by the equation:

$$t_{SS} = 0.45 \times C5$$

Where C5 (in nF) is the soft-start capacitor from SS to GND, and t_{SS} (in ms) is the soft-start period. Determine the capacitor required for a given soft-start period by the equation:

$$C5 = 2.22 \times t_{SS}$$

Use values between 10nF and 22nF for C5 to set the soft-start period (between 4ms and 10ms).

Setting the Output Voltage (see Figure 2)

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.895V feedback voltage. Use 10kΩ for the low-side resistor of the voltage divider. Determine the high-side resistor by the equation:

$$R2 = \left(\frac{V_{OUT}}{0.895V} - 1\right) \times R1$$

Where R2 is the high-side resistor, V_{OUT} is the output voltage and R1 is the low-side resistor.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and so a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors may also suffice.

The capacitor can be electrolytic, tantalum or ceramic. Because it absorbs the input switching current it must have an adequate ripple current rating. Use a capacitor with RMS current rating greater than 1/2 of the DC load current.

For stable operation, place the input capacitor as close to the IC as possible. A smaller high quality 0.1μF ceramic capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP2106. For most applications, a 10μF ceramic capacitor will work.

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

The output voltage ripple is:

$$V_{RIPPLE} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right)$$

Where V_{RIPPLE} is the output voltage ripple, f_{SW} is the switching frequency, V_{IN} is the input voltage, R_{ESR} is the equivalent series resistance of the

output capacitors and f_{SW} is the switching frequency.

Choose an output capacitor to satisfy the output ripple requirements of the design. A 22µF ceramic capacitor is suitable for most applications.

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current that will result in lower output ripple voltage. However, the larger value inductor is likely to have a larger physical size and higher series resistance. Choose an inductor that does not saturate under the worst-case load conditions. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30% to 40% of the maximum load current. Make sure that the peak inductor current (the load current plus half the peak-to-peak inductor ripple current) is below 2.5A to prevent loss of regulation due to the current limit.

Calculate the required inductance value by the equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I}$$

Where ΔI is the peak-to-peak inductor ripple current. It is recommended to choose ΔI to be 30%~40% of the maximum load current.

Compensation

The system stability is controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC loop gain is:

$$A_{VDC} = \left(\frac{V_{FB}}{V_{OUT}}\right) \times A_{VEA} \times G_{CS} \times R_{LOAD}$$

Where V_{FB} is the feedback voltage, A_{VEA} is the transconductance error amplifier voltage gain, G_{CS} is the current sense transconductance (roughly the output current divided by the voltage at COMP) and R_{LOAD} is the load resistance:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}}$$

Where I_{OUT} is the output load current.

The system has 2 poles of importance, one is due to the compensation capacitor (C3), and the other is due to the load resistance and the output capacitor (C2), where:

$$f_{P1} = \frac{G_{EA}}{2\pi \times A_{VEA} \times C3}$$

P1 is the first pole, and G_{EA} is the error amplifier transconductance (300µA/V) and

$$f_{P2} = \frac{1}{2\pi \times R_{LOAD} \times C2}$$

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). The zero is:

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C3}$$

If large value capacitors with relatively high equivalent-series-resistance (ESR) are used, the zero due to the capacitance and ESR of the output capacitor can be compensated by a third pole set by R3 and C4. The pole is:

$$f_{P3} = \frac{1}{2\pi \times R3 \times C4}$$

The system crossover frequency (the frequency where the loop gain drops to 1, or 0dB, is important. Set the crossover frequency to below one tenth of the switching frequency to insure stable operation. Lower crossover frequencies result in slower response and worse transient load recovery. Higher crossover frequencies degrade the phase and/or gain margins and can result in instability.

Table 1—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT}	C2	R3	C3	C4
1.8V	22µF Ceramic	6.8kΩ	3.3nF	None
2.5V	22µF Ceramic	9.1kΩ	2.2nF	None
3.3V	22µF Ceramic	12kΩ	1.8nF	None
1.8V	47µF Tantalum (300mΩ)	13kΩ	2nF	1nF
2.5V	47µF Tantalum (300mΩ)	18kΩ	1.2nF	750pF
3.3V	47µF Tantalum (300mΩ)	24kΩ	1nF	560pF

Choosing the Compensation Components

The values of the compensation components given in Table 1 yield a stable control loop for the given output voltage and capacitor. To optimize the compensation components for conditions not listed in Table 1, use the following procedure.

Choose the compensation resistor to set the desired crossover frequency. Determine the value by the following equation:

$$R3 = \frac{2\pi \times C2 \times V_{OUT} \times f_C}{G_{EA} \times G_{CS} \times V_{FB}}$$

Where f_C is the desired crossover frequency (preferably 33kHz).

Choose the compensation capacitor to set the zero below one fourth of the crossover frequency. Determine the value by the following equation:

$$C3 > \frac{2}{\pi \times R3 \times f_C}$$

Determine if the second compensation capacitor, C4 is required. It is required if the ESR zero of the output capacitor happens at less than half of the switching frequency. Or:

$$\pi \times C2 \times R_{ESR} \times f_{SW} > 1$$

If this is the case, then add the second compensation capacitor.

Determine the value by the equation:

$$C4 = \frac{C2 \times R_{ESR(max)}}{R3}$$

Where $R_{ESR(MAX)}$ is the maximum ESR of the output capacitor.

External Boost Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.3

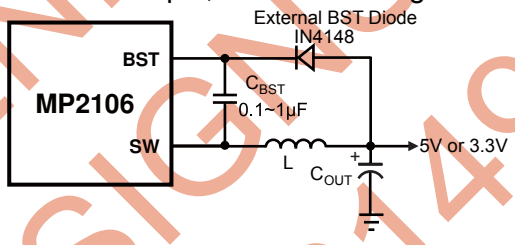


Figure 3—Add Optional External Bootstrap Diode to Enhance Efficiency

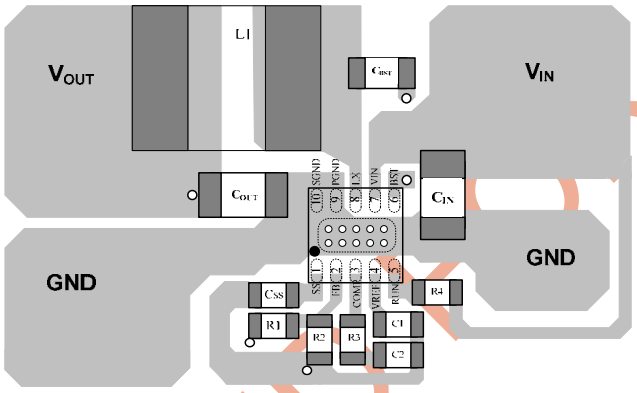
The recommended external BST diode is IN4148, and the BST cap is 0.1~1µF.

PCB Layout Guide

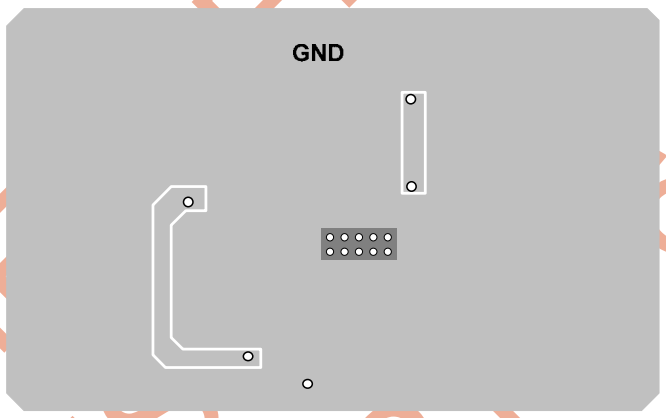
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure4 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the V_{IN} Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer

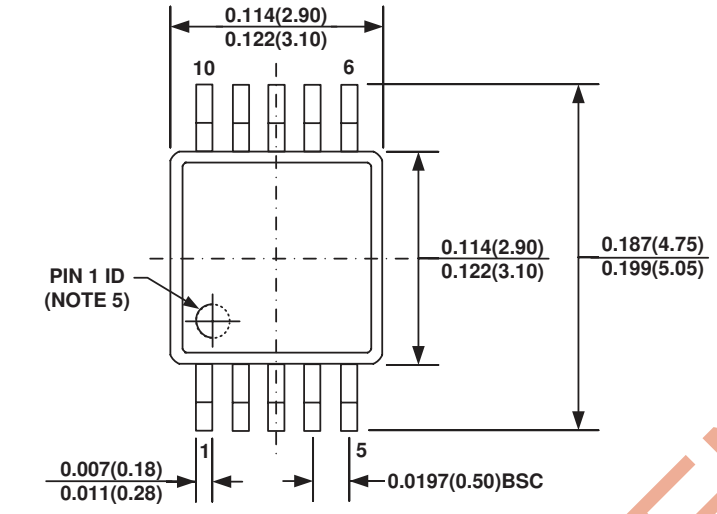


Bottom Layer

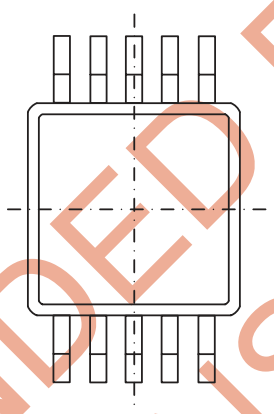
Figure4—PCB Layout (Double Layers)

PACKAGE INFORMATION

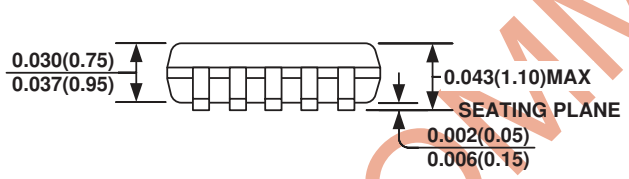
MSOP10



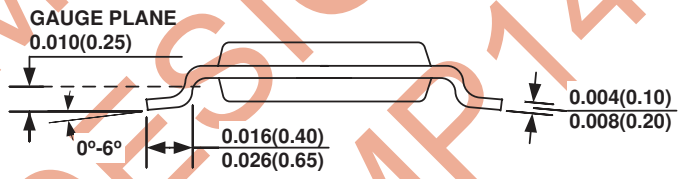
TOP VIEW



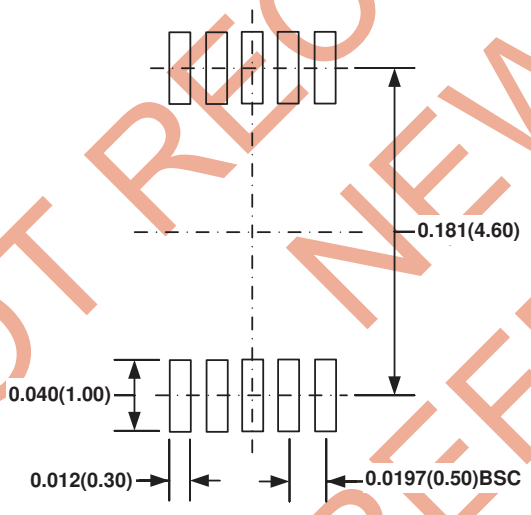
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

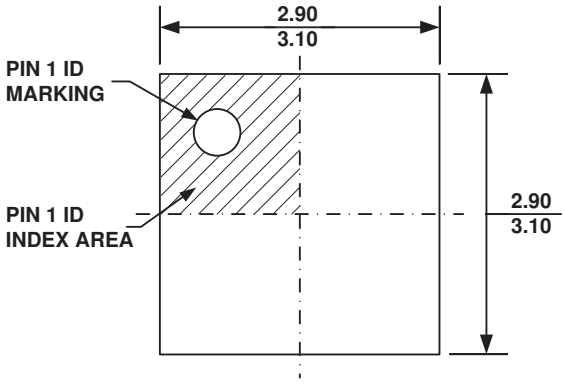


RECOMMENDED LAND PATTERN

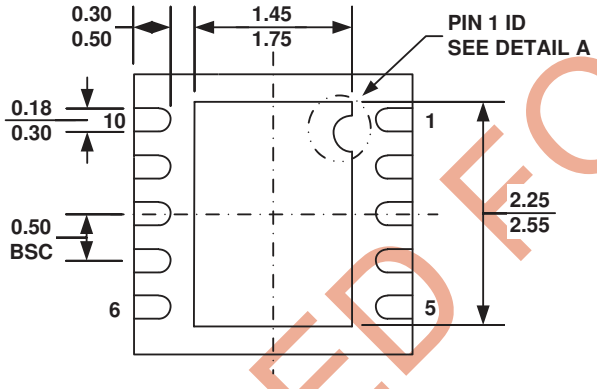
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

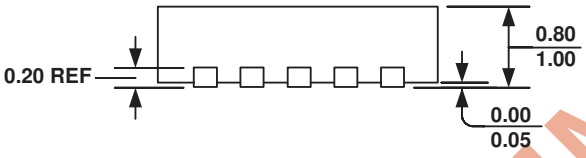
QFN10 (3mm x 3mm)



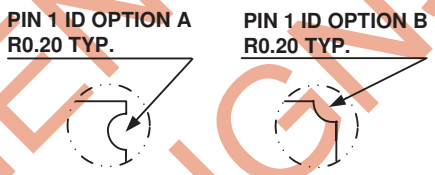
TOP VIEW



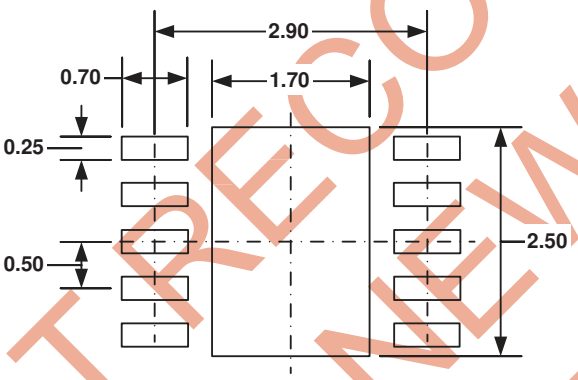
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.