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MP2235

High-Efficiency, 3A, 16V, 800kHz Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2235 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 3A continuous output current with excellent load and line regulation over a wide input supply range. The MP2235 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shut down.

The MP2235 requires a minimal number of readily-available standard external components, and is available in a space-saving 8-pin TSOT23 package.

FEATURES

- Wide 4.5V-to-16V Operating Input Range
- 80mΩ/30mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Fixed 800kHz Switching Frequency
- Synchronizes from a 300kHz-to-2MHz External Clock
- Power-Save Mode at Light Load
- External Soft-Start
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- Distributed Power Systems

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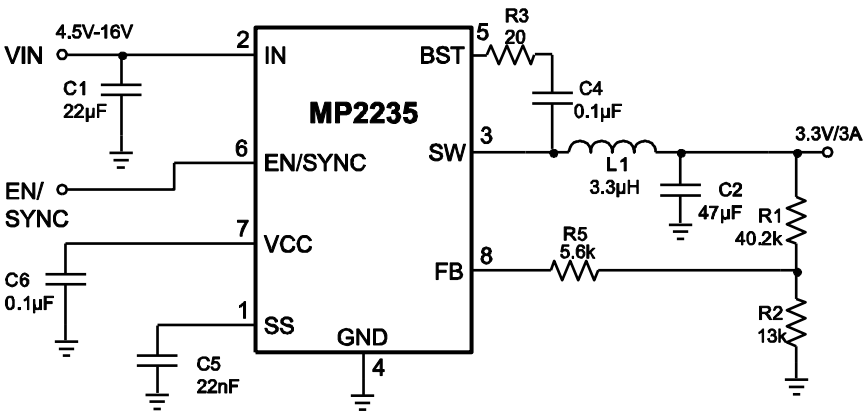
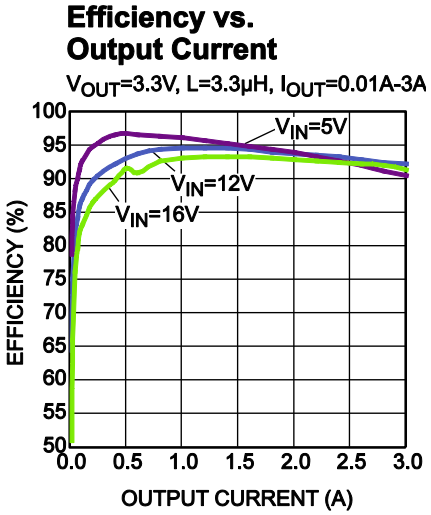
TYPICAL APPLICATION





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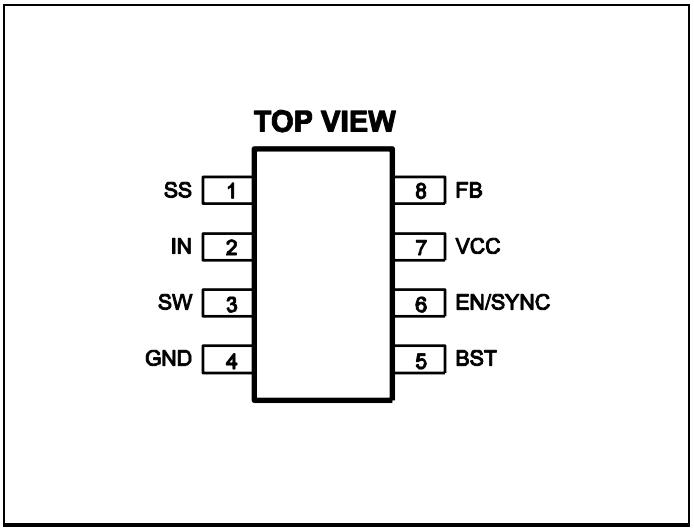
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2235GJ	TSOT-23-8	AFL

* For Tape & Reel, add suffix –Z (e.g. MP2235GJ–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 17V
V_{SW} .....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins.....-0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
.....1.25W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN}..... 4.5V to 16V
Output Voltage V_{OUT}.....0.8V to V_{IN} x 90%
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
TSOT-23-8	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to Page 9, Enable/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.6	0.8	mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		80		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		30		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			0.3	μA
Current Limit	I_{LIMIT}	Under 40% Duty Cycle	4	5	6	A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V	690	800	870	kHz
Fold-Back Frequency	f_{FB}	V_{FB}<400mV		0.25		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV	90	95		%
Minimum On Time(6)	$\tau_{ON\ MIN}$			40		ns
Sync Frequency Range	f_{SYNC}		0.3		2	MHz
Feedback Voltage	V_{FB}	T_A =25°C	791	807	823	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	$V_{EN\ RISING}$		1.2	1.4	1.6	V
EN Hysteresis	$V_{EN\ Hysteresis}$		110	175	240	mV
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0		0		μA
EN Turn-Off Delay	EN_{td-off}		3	5	7	μs
VIN Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$		3.7	3.9	4.1	V
VIN Under-Voltage Lockout Threshold—Hysteresis	$INUV_{HYS}$		530	610	690	mV
VCC Regulator	V_{CC}		4.6	4.9	5.2	V
VCC Load Regulation		I_{CC}=5mA		1.5	3	%
Soft-Start Current	I_{SS}		8	11	14	μA
Thermal Shutdown (6)				150		°C
Thermal Hysteresis (6)				20		°C

Notes:

6) Guaranteed by design.

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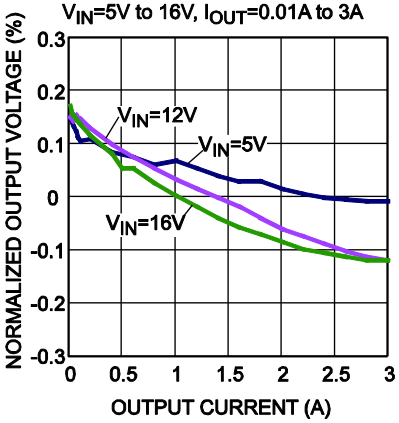
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L=3.3µH, T_A = 25°C, unless otherwise noted.

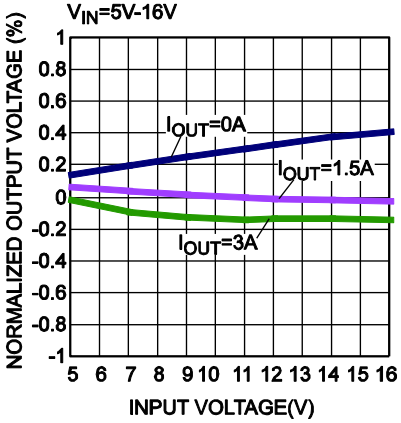
Load Regulation

V_{IN}=5V to 16V, I_{OUT}=0.01A to 3A

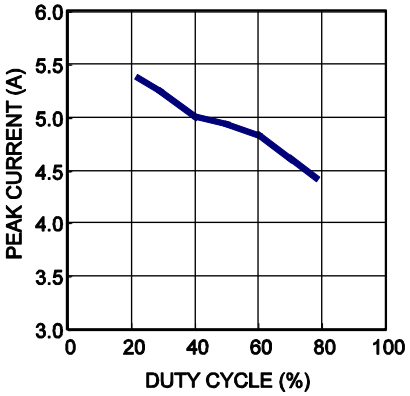


Line Regulation

V_{IN}=5V-16V

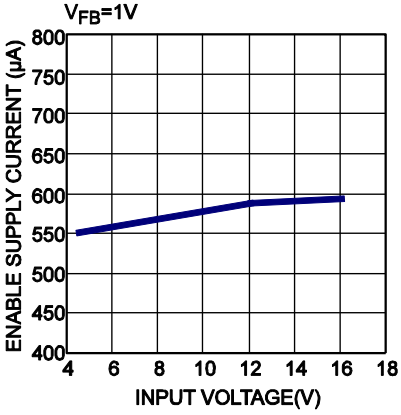


Current Limit vs. Duty Cycle



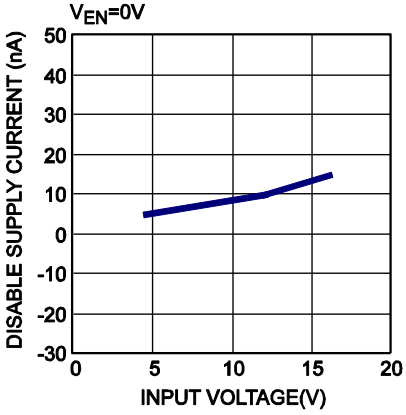
Enabled Supply Current vs. Input Voltage

V_{FB}=1V

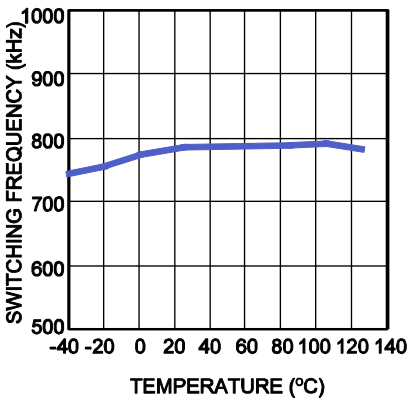


Disabled Supply Current vs. Input Voltage

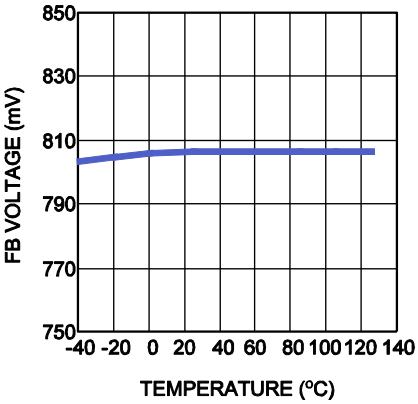
V_{EN}=0V



Switching Frequency vs. Temperature



FB Voltage vs. Temperature



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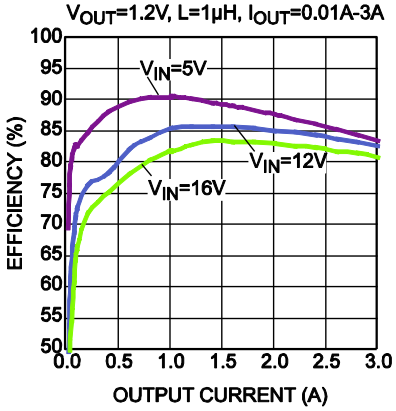
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L=4.7µH, T_A = 25°C, unless otherwise noted.

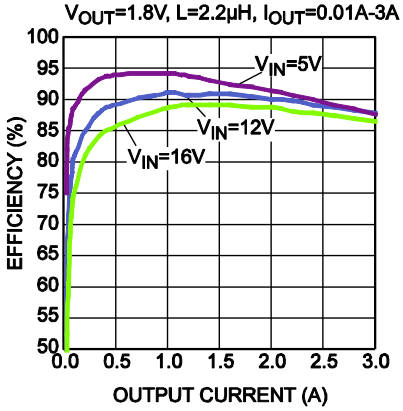
Efficiency vs. Output Current

V_{OUT}=1.2V, L=1µH, I_{OUT}=0.01A-3A



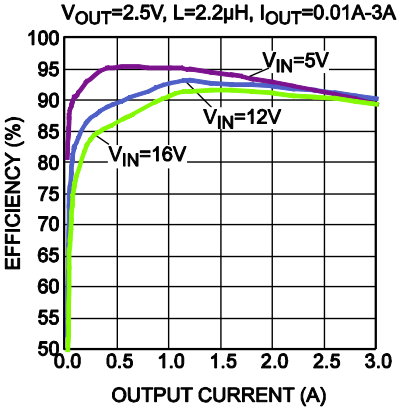
Efficiency vs. Output Current

V_{OUT}=1.8V, L=2.2µH, I_{OUT}=0.01A-3A



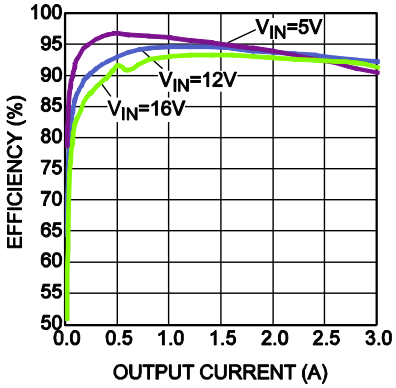
Efficiency vs. Output Current

V_{OUT}=2.5V, L=2.2µH, I_{OUT}=0.01A-3A



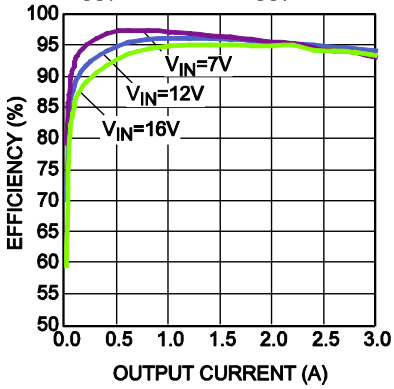
Efficiency vs. Output Current

V_{OUT}=3.3V, L=3.3µH, I_{OUT}=0.01A-3A



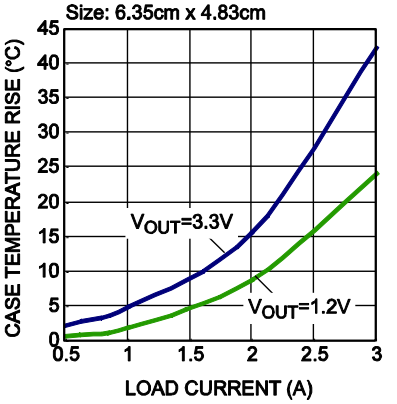
Efficiency vs. Output Current

V_{OUT}=5V, L=3.3µH, I_{OUT}=0.01A-3A



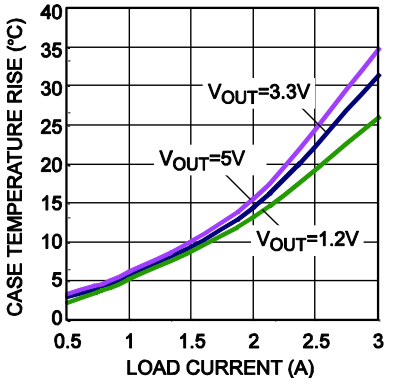
Case Temperature Rise vs. Output Current

V_{IN}=5V, I_{OUT}=0.5A-3A, 2 Layers PCB, Size: 6.35cm x 4.83cm



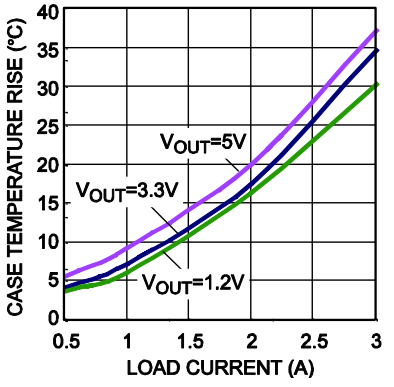
Case Temperature Rise vs. Output Current

V_{IN}=12V, I_{OUT}=0.5A-3A, 2 Layers PCB, Size: 6.35cm x 4.83cm



Case Temperature Rise vs. Output Current

V_{IN}=16V, I_{OUT}=0.5A-2A, 2 Layers PCB, Size: 6.35cm x 4.83cm



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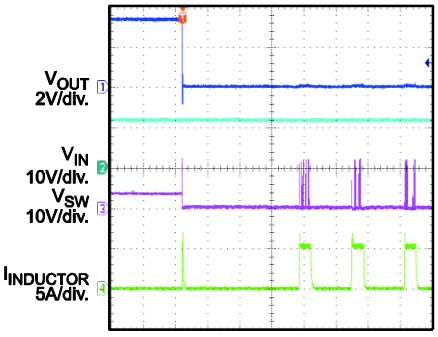
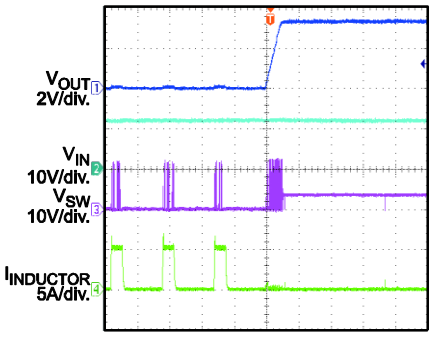
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L=3.3µH, T_A = 25°C, unless otherwise noted.

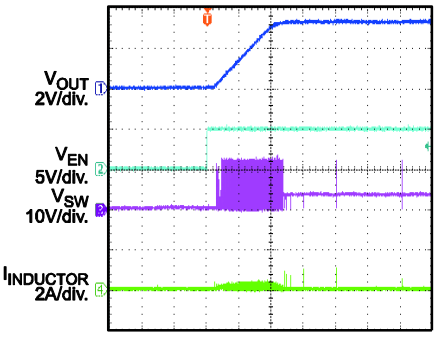
Short Entry
I_{OUT}=0A



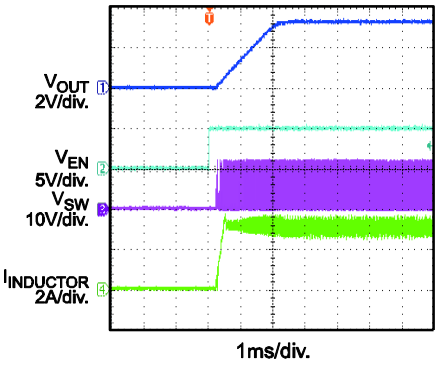
Short Recovery
I_{OUT}=0A



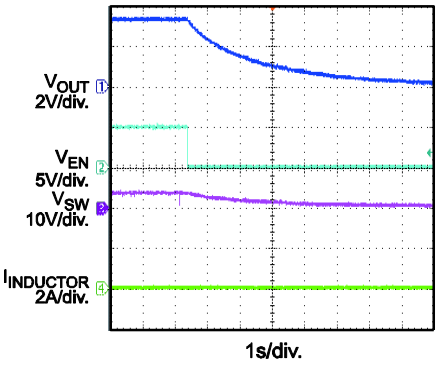
Startup through Enable
I_{OUT}=0A



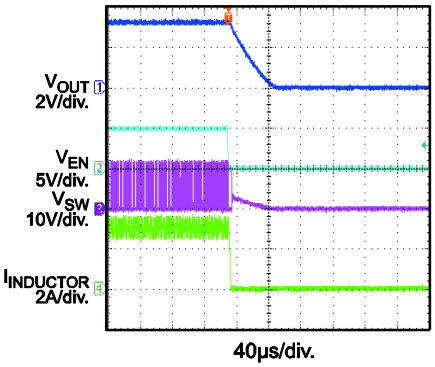
Startup through Enable
I_{OUT}=3A



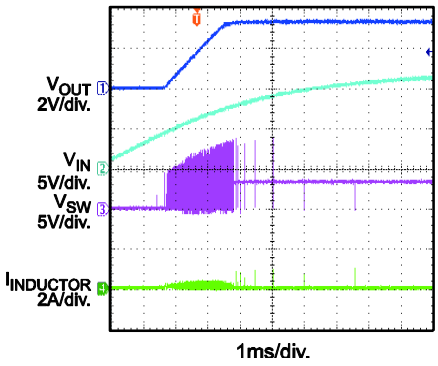
Shutdown through Enable
I_{OUT}=0A



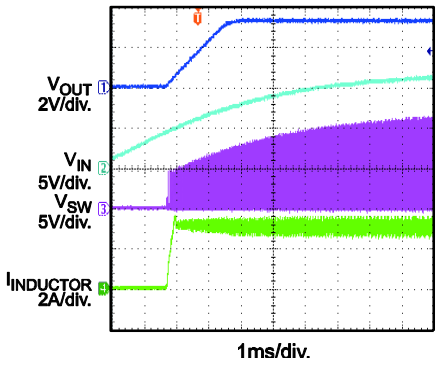
Shutdown through Enable
I_{OUT}=3A



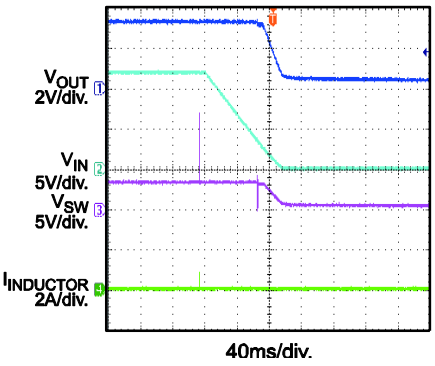
Startup through Input Voltage
I_{OUT}=0A



Startup through Input Voltage
I_{OUT}=3A



Shutdown through Input Voltage
I_{OUT}=0A



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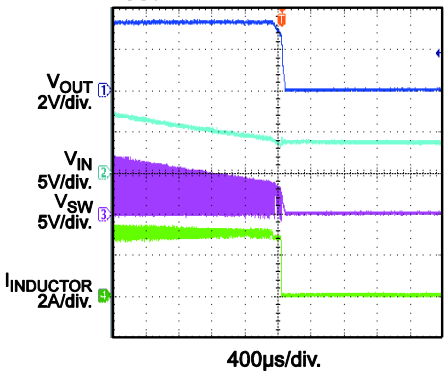
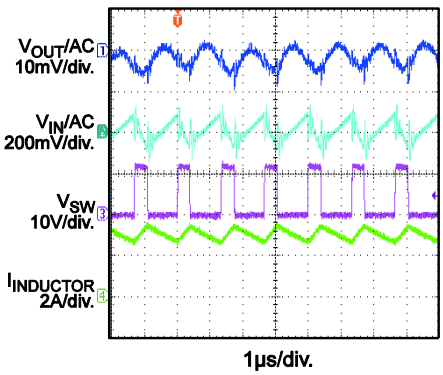
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L=3.3µH, T_A = 25°C, unless otherwise noted.

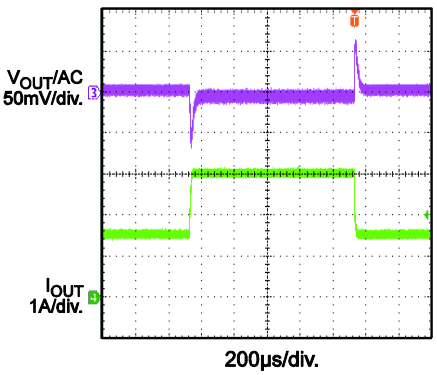
Shutdown through Input Voltage
I_{OUT}=3A



Input / Output Ripple
I_{OUT}=3A



Load Transient Reponse
I_{OUT}=1.5A to 3A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	SS	Soft-Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
2	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP2235 operates from a +4.5V to +16V input rail. Requires a low-ESR, and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
3	SW	Switch Output. Connect to the inductor and bootstrap capacitor. This pin is driven up to V_{IN} by the high-side switch during the PWM duty cycle ON time. The inductor current drives the SW pin negative during the OFF time. The ON resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect using wide PCB traces and multiple vias.
4	GND	System Ground. Reference ground of the regulated output voltage. PCB layout Requires extra care. For best results, connect to GND with copper and vias.
5	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
6	EN/SYNC	Enable. EN=high to enable the MP2235. Apply an external clock change the switching frequency. For automatic start-up, connect EN pin to V_{IN} with a 100kΩ resistor.
7	VCC	Internal 5V LDO output. Powers the driver and control circuits. Decouple with 0.1μF-to-0.22μF capacitor. Do not use a capacitor ≥0.22μF.
8	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short circuit fault. Place the resistor divider as close to the FB pin as possible. Avoid placing vias on the FB traces.

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FUNCTIONAL BLOCK DIAGRAM

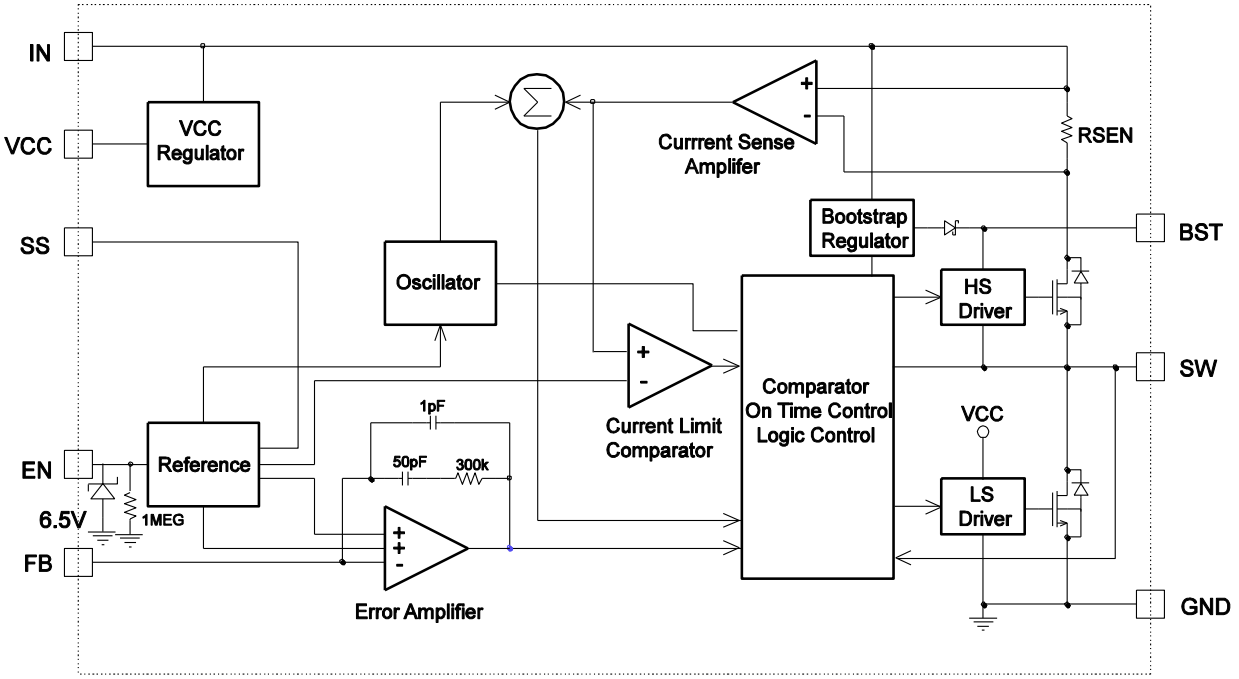

Figure 1: Functional Block Diagram

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OPERATION

The MP2235 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves a 3A continuous output current with excellent load and line regulation over a wide input supply range.

The MP2235 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until the current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, within 95% of one PWM period, the current in the power MOSFET does not reach the value set by the COMP value, the power MOSFET is forced off.

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. When V_{IN} is less than 5.0V, the output decreases, and the part requires a 0.1µF ceramic decoupling capacitor.

Error Amplifier

The error amplifier compares the FB pin voltage to the internal 0.807V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. An internal 1MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

The EN pin is clamped internally using a 6.5V series-Zener-diode as shown in Figure 2. Connecting the EN input pin through a pullup resistor to the voltage on the IN pin limits the EN input current to less than 100µA.

For example, with 12V connected to IN, R_{PULLUP} ≥ (12V – 6.5V) ÷ 100µA = 55kΩ.

Connecting the EN pin is directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

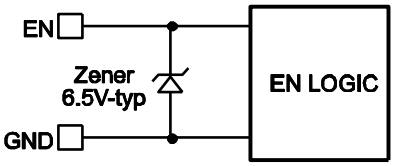

Figure 2: 6.5V Zener Diode Connection

For external clock synchronization, connect a clock with a frequency range between 300kHz and 2MHz 2ms after the output voltage is set: The internal clock rising edge will synchronize with the external clock rising edge. Select an external clock signal with a pulse width less than 1.2µs.

Under-Voltage Lockout (UVLO)

The MP2235 has under-voltage lock-out protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold voltage, the MP2235 powers up. It shuts off when the VCC voltage drops below the UVLO falling threshold voltage. This is non-latch protection.

The MP2235 is disabled when the input voltage falls below 3.25V. If an application requires a higher under-voltage lockout (UVLO) threshold, use the EN pin as shown in Figure 3 to adjust the input voltage UVLO by using two external resistors. For best results, set the UVLO falling threshold (VSTOP) above 4.5V using the enable resistors. Set the rising threshold (VSTART) to provide enough hysteresis to allow for any input supply variations.

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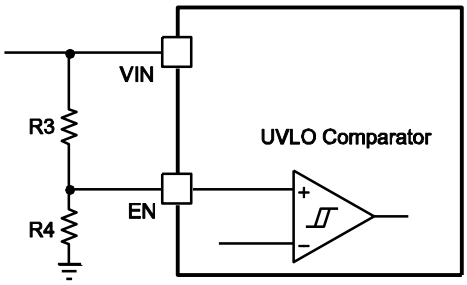

Figure 3: **Adjustable UVLO**

Soft-Start

Adjust the soft-start time by connecting a capacitor from SS pin to ground. When the soft-start begins, an internal 11μA current source charges the external capacitor. During soft-start, the soft-start capacitor connects to the non-inverting input of the error amplifier. The soft-start period continues until the voltage on the soft-start capacitor exceeds the 0.8V reference. Then the non-inverting amplifier uses the reference voltage takes as the input. Use the following equation to calculate the soft-start time:

$$t_{SS}(ms) = \frac{0.8V \times Css(nF)}{11\mu A}$$

Power Save Mode for Light Load Condition

The MP2235 has AAM (Advanced Asynchronous Modulation) power save mode for light load. The AAM voltage is set at 0.6V internally. Under the heavy load condition, the V_{COMP} is higher than V_{AAM}. When clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time when V_{COMP} is higher than V_{AAM}.

Under the light load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}, during this time, the internal clock is blocked, thus the MP2235 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

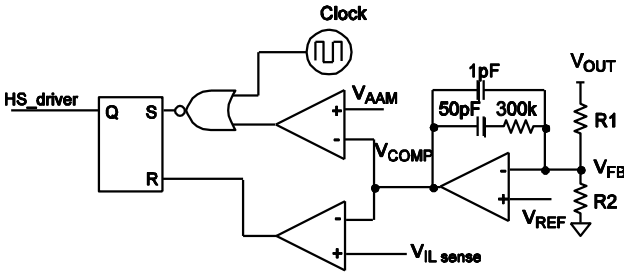

Figure 4: **Simplified AAM Control Logic**

When the load current is light, the inductor peak current is set internally which is about 0.9A for V_{IN}=12V, V_{OUT}=3.3V, and L=3.3μH.

Over-Current-Protection and Hiccup

The MP2235 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until V_{FB} is below the Under-Voltage (UV) threshold—typically 50% below the reference. Once UV is triggered, the MP2235 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground, and greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator. The MP2235 exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 150°C, it shuts down the whole chip. When the temperature drops below its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, R3, C4, L1 and C2 (Figure 5). If (V_{IN}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4. A 20Ω resistor placed between SW and BST cap. is strongly recommended to reduce SW spike voltage.

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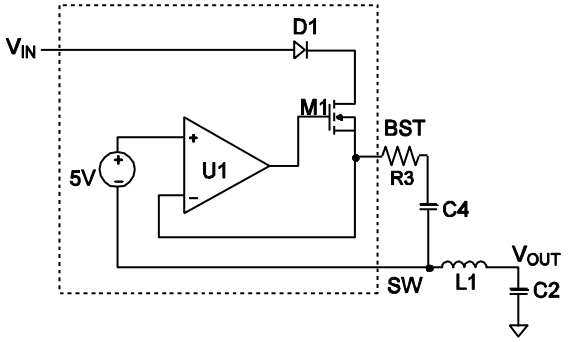

Figure 5: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{EN} low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1).

Choose R1 around 40kΩ for V_{OUT}>1.2V then R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1}$$

The T-Type resistor R5 is used to control the bandwidth of control loop which will be introduced below.

Control Loop Compensation

MP2235 employs peak current mode control for easy compensation and fast transient response. To simplify the compensation design and minimize external components, MP2235 integrates internal compensation. Figure 6 shows an equivalent model for the device control loop.

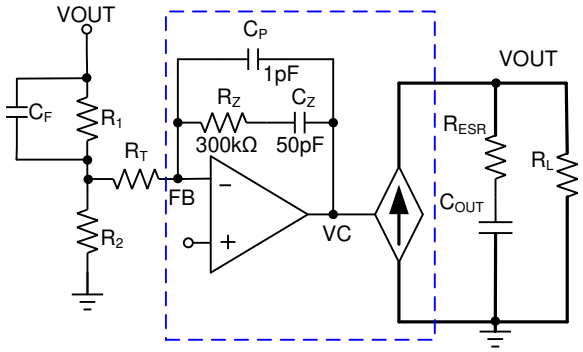

Figure 6: Equivalent Control Loop Model

The device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control (V_C) to output (V_{OUT}) transfer function is shown as below:

$$\frac{V_{OUT}}{V_C} = A_{DC} \times \frac{1 + \frac{s}{2\pi f_{Z1}}}{1 + \frac{s}{2\pi f_{P1}}}$$

$$A_{DC} = \frac{R_L}{R_i}$$

feedback loop has the unity gain is important. Lower crossover frequency results in slower line and load transient responses, while higher

$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

$$f_{P1} = \frac{1}{2\pi R_L C_{OUT}}$$

Where A_{DC} is the DC gain of power stage, R_L is the load resistance, R_i is the current sense resistance (R_i=0.22Ω). R_{ESR} is the equivalent series resistance of output capacitor. C_{OUT} is the output capacitance.

MP2235 uses voltage type amplifier for the feedback error amplifier and integrates compensation to ease the system design. The output to control transfer function is given by:

$$\frac{V_C}{V_{OUT}} = -A_{EA} \frac{(1 + \frac{s}{2\pi f_{Z2}})(1 + \frac{s}{2\pi f_{Z3}})}{s(1 + \frac{s}{2\pi f_{P2}})(1 + \frac{s}{2\pi f_{P3}})}$$

$$A_{EA} = \frac{R_2}{(C_Z + C_P)(R_1 R_T + R_1 R_2 + R_2 R_T)}$$

$$f_{Z2} = \frac{1}{2\pi R_Z C_Z}$$

$$f_{Z3} = \frac{1}{2\pi R_1 C_F}$$

$$f_{P2} = \frac{1}{2\pi R_Z C_P}$$

$$f_{P3} = \frac{1}{2\pi (R_1 // R_2 // R_T) C_Z}$$

Where R_1, R_2 are the feedback resistors, R_T is the T-type resistor between feedback resistor divider and FB pin. C_F is the type III compensation feed forward capacitor. R_Z, C_Z and C_P are internal compensation resistor and capacitors.

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the crossover frequency could cause system instability. A good rule of thumb is to set the

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crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose high-side feedback resistor R1 and calculate the value of low-side resistor R2 according to desired output voltage. Suggest choosing R1 around 40kΩ for >1.2V output condition.

2. Choose the T-Type resistor R_T to set the desired crossover frequency. Determine the R_T value by the following equation:

$$R_T = \frac{V_{FB} \times R_Z}{V_{OUT} \times R_i \times 2\pi \times f_C \times C_{OUT}} - \frac{R_1 \times R_2}{R_1 + R_2}$$

R_Z is the internal compensation resistor, which equals to 300kΩ. f_C is the desired crossover frequency which is typically one tenth of the switching frequency. R_i is the current sense resistance, 0.22Ω.

3. Choose feed forward capacitor C_F to achieve sufficient phase margin especially for large output inductor condition. In theory there is no need to add type III zero for peak current mode control, but in real circuit there are some parasitic capacitors or filters internal which induces poles into the control loop. Fortunately, those poles are locating at high frequency range which won't affect the step 2 bandwidth calculation while it affects the phase margin. For applications with typical inductor values (<4.7μH), setting the compensation zero, f_{Z3} (formed by R_1 and C_F) around 1.5 times of crossover frequency f_C. Then the C_F value can be calculated by following equation:

$$C_F = \frac{1}{3\pi \times R_1 \times f_C}$$

If electrolytic capacitor is used or the output capacitor has large ESR, the feed forward capacitor C_F is not needed any more since there is already one ESR zero in the loop.

If large output inductor is used, like 22μH, the phase margin will decrease a lot due to the half switching frequency pole moves towards crossover frequency. In this condition, it's suggested increasing feed forward capacitor value of C_F to get enough phase margins while it's better to keep the feed forward zero frequency higher than half of crossover frequency.

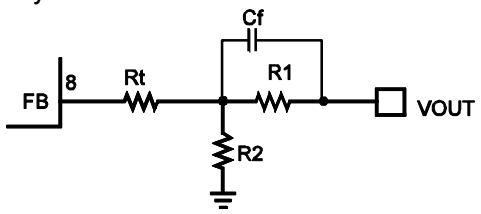

Figure 7: T-Type Network

Table 1 lists the recommended resistors and compensation values for common output voltages (refer to Figure 7).

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	Cf(pF)	L(μH)
1	20.5	84.5	34	33	1
1.2	30.1	61.9	24	33	1
1.8	40.2	32.4	15	33	2.2
2.5	40.2	19.1	6.8	33	2.2
3.3	40.2	13	5.6	33	3.3
5	40.2	7.68	2	33	3.3

For more accurate control loop design, visit MPS website and run the online bode plot simulation by DC/DC designer.

Selecting the Inductor

Use a 1μH-to-22μH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2235 can be optimized for a wide range of capacitance and ESR values.

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External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases, add an external BST diode from the VCC pin to BST pin, as shown in Figure 8.

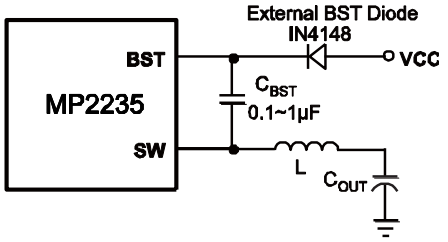

Figure 8: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1µF to 1µF.

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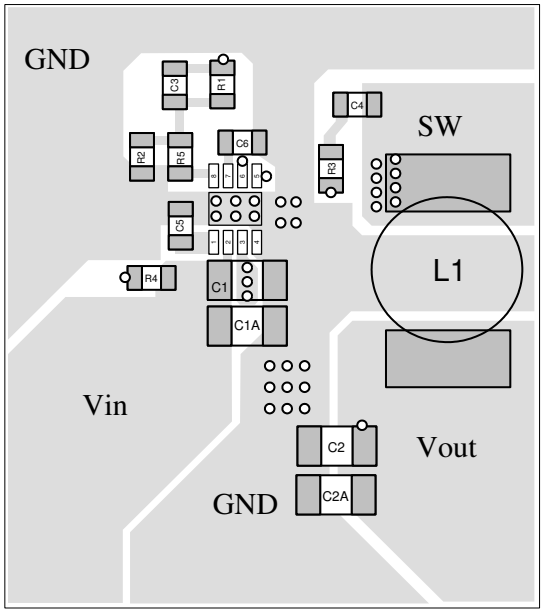
PC Board Layout [8]

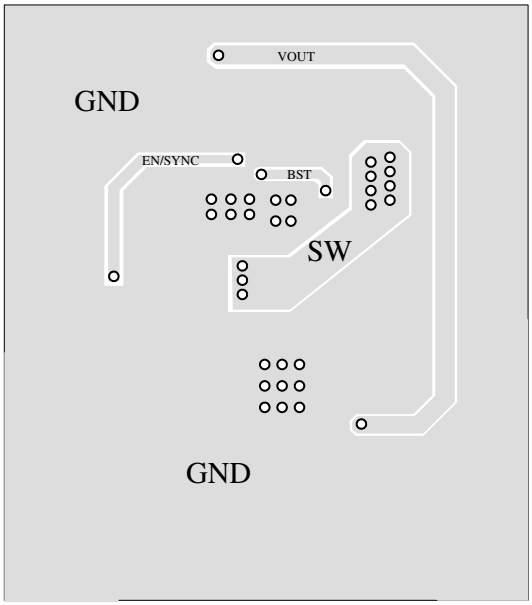
PCB layout is very important to achieve stable operation especially for VCC capacitor and input capacitor placement. For best results, follow these guidelines:

1. Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.
2. Place the VCC capacitor to VCC pin and GND pin as close as possible. Make the trace length of VCC pin-VCC capacitor anode-VCC capacitor cathode-chip GND pin as short as possible.
3. Place the ceramic input capacitor close to IN and GND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.
4. Route SW, BST away from sensitive analog areas such as FB. It's not recommended to route SW, BST trace under chip's bottom side.
5. Place the T-type feedback resistor R5 close to chip to ensure the trace which connects to FB pin as short as possible

Notes:

8) The recommended layout is based on the Figure 8 Typical Application circuit on the next page.





Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	3A

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

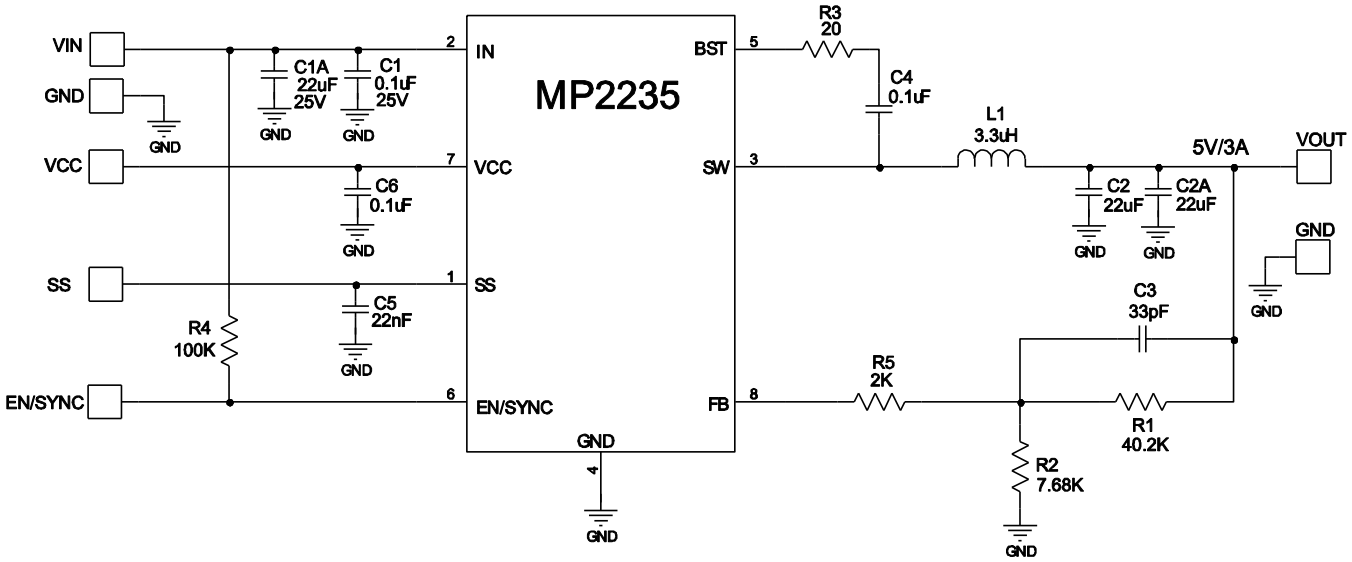

Figure 9: $12V_{IN}$, 5V/3A Output

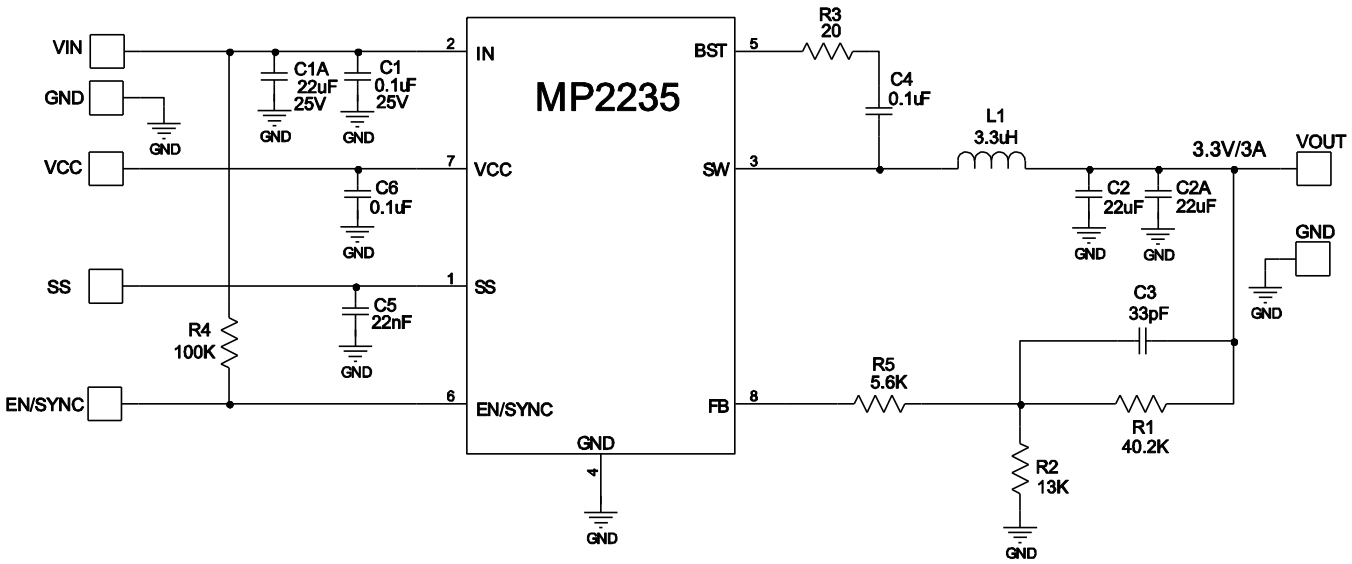

Figure 10: $12V_{IN}$, 3.3V/3A Output

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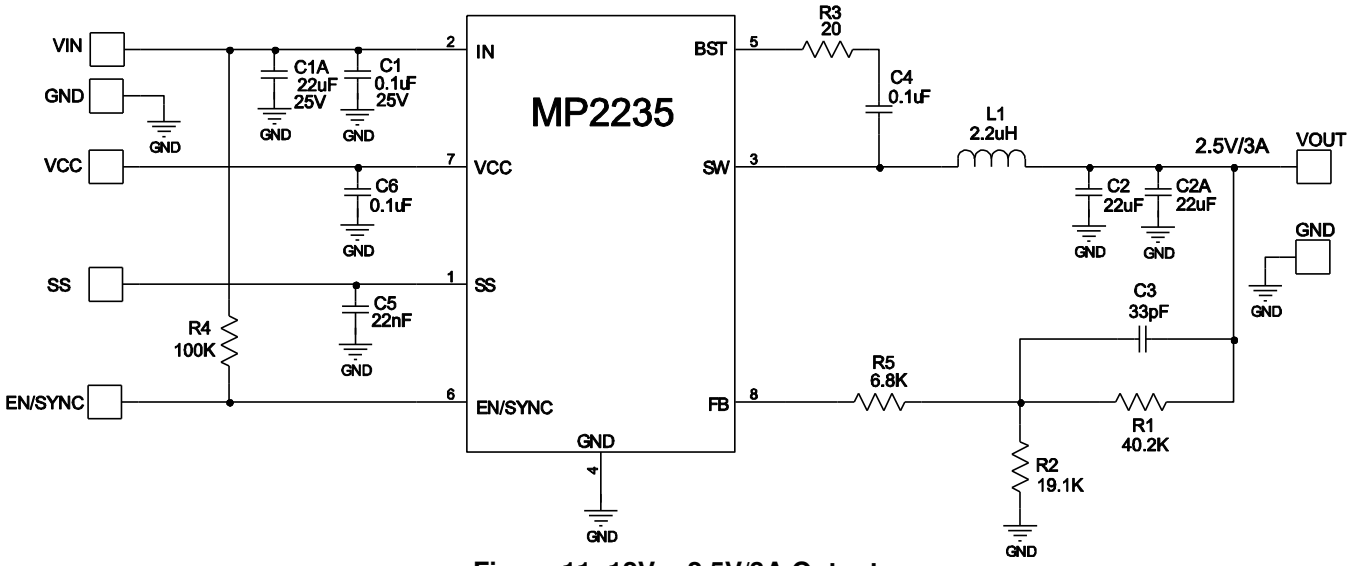

Figure 11: $12V_{IN}$, 2.5V/3A Output

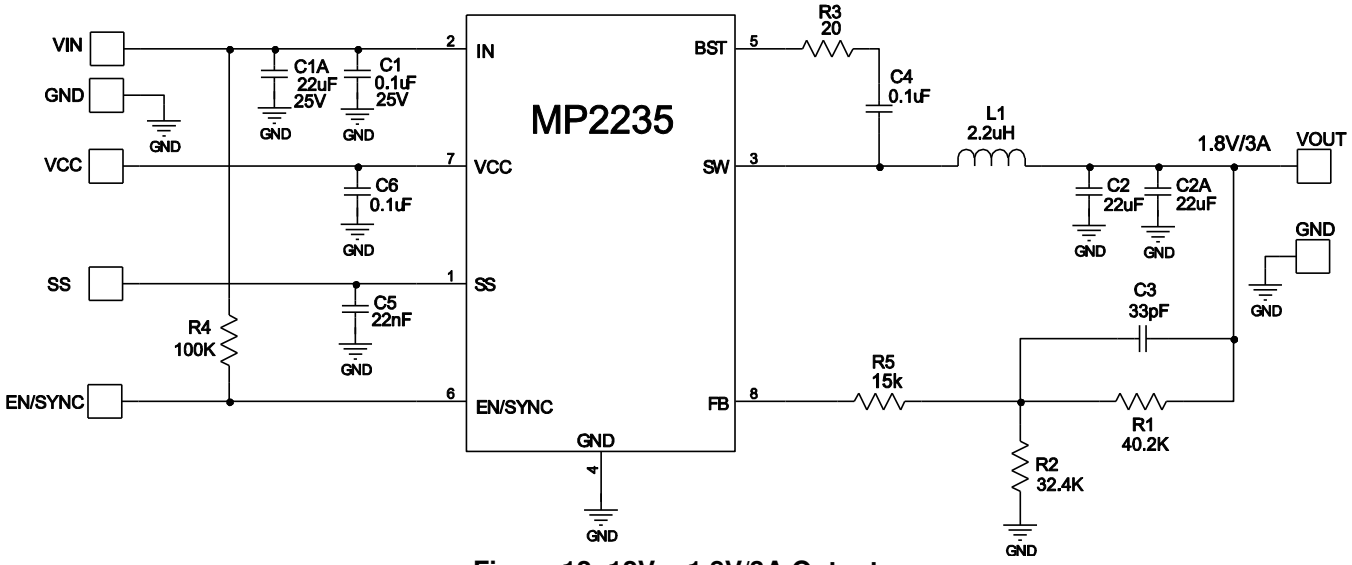

Figure 12: $12V_{IN}$, 1.8V/3A Output

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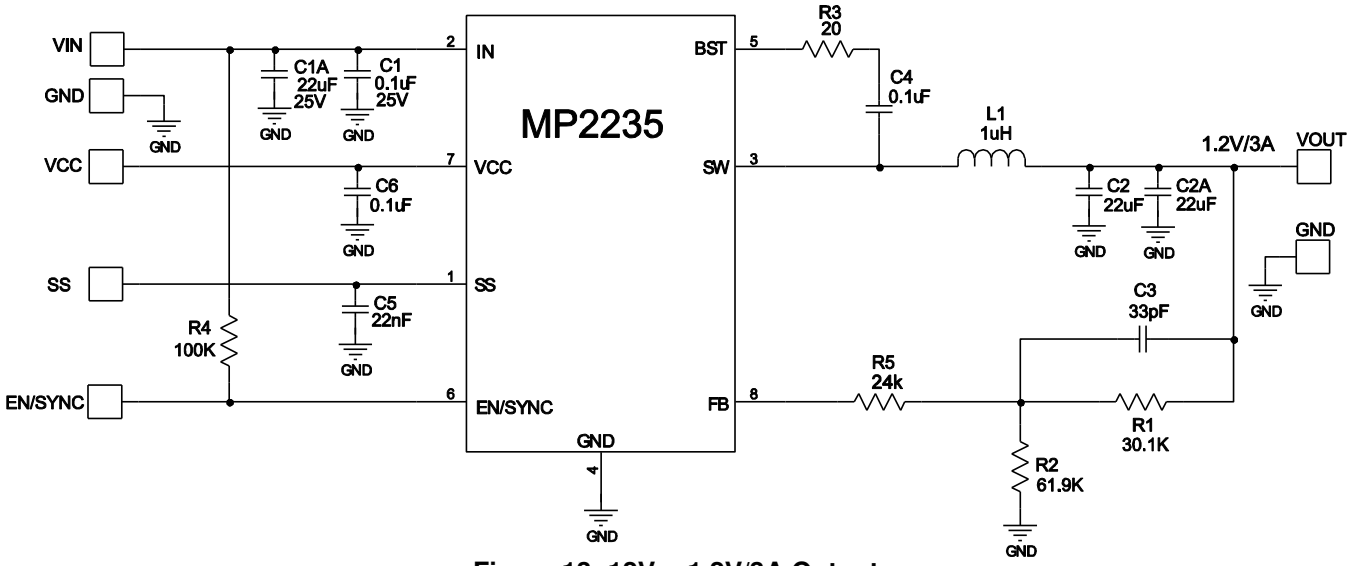

Figure 13: $12V_{IN}$, 1.2V/3A Output

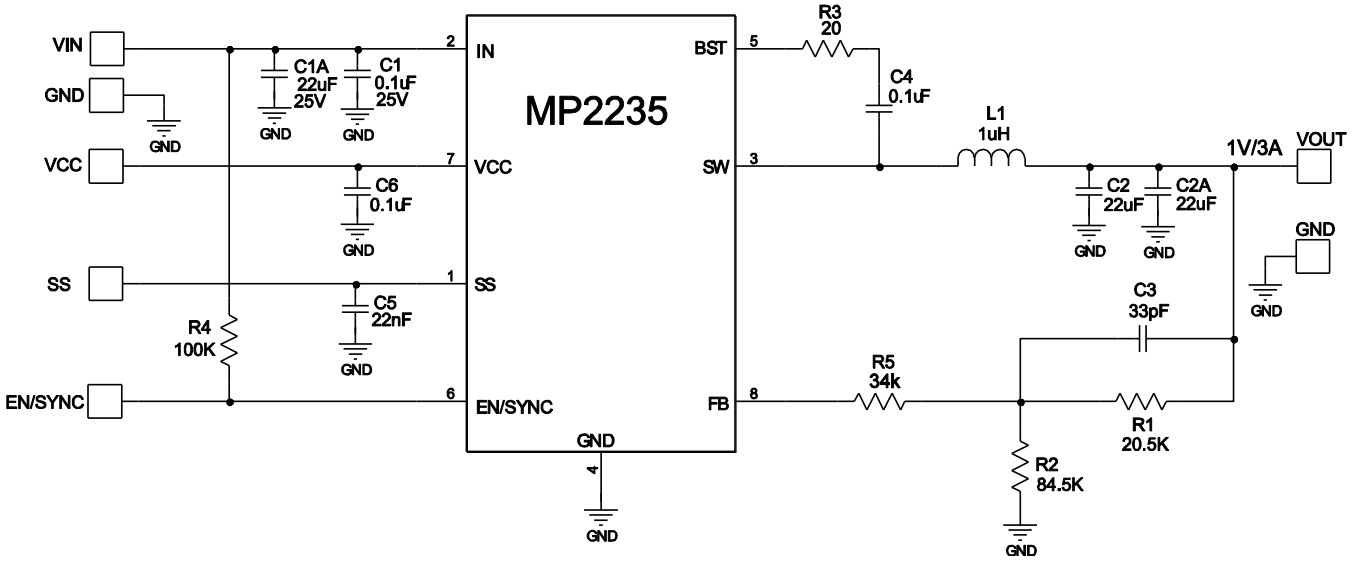

Figure 14: $12V_{IN}$, 1V/3A Output

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PACKAGE INFORMATION

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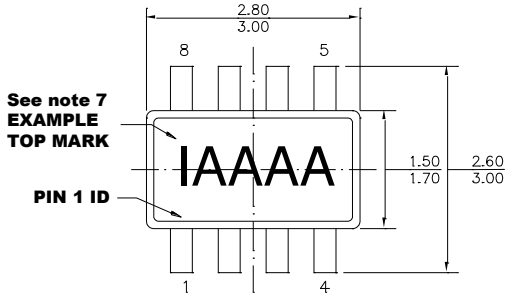
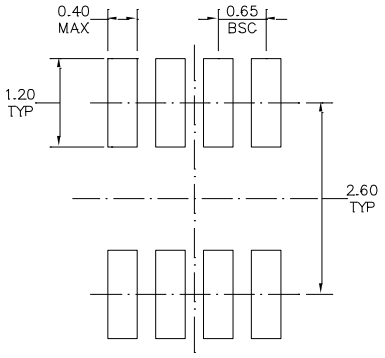
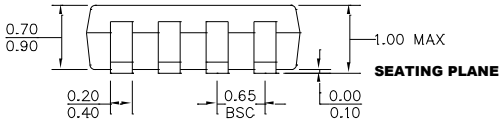


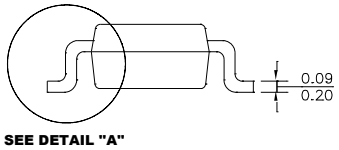
TOP VIEW



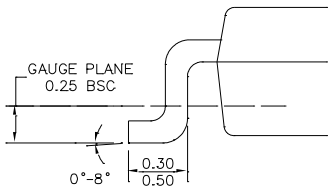
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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