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## DESCRIPTION

The MP24830 is a 90V white LED driver suitable for either step-down or inverting step-up/down applications. It supports a wide input range with excellent load and line regulation. Its programmable current limit provides customized applications with a wide power range. Current mode operation provides a fast transient response and eases loop stabilization. Fault condition protection includes thermal shutdown, cycle-by-cycle peak-current limiting, open-string protection, and output short-circuit protection.

The MP24830 incorporates both DC and PWM dimming onto a single control pin. The separate input reference ground pin allows for direct enable and/or dimming control for a positive-to-negative power conversion.

The MP24830 requires a minimal number of readily-available external components. It is available in 14-pin SOIC and QFN packages.

## FEATURES

- Programmable Maximum Output Current
- Unique Step-Up/Down Operation (Buck-Boost Mode)
- Wide 4.5V-to-90V Operating Input Range for Step-Down Applications (Buck Mode)
- Adjustable Switching Frequency
- Analog and PWM Dimming
- 0.2V Reference Voltage
- 10 $\mu$ A Shutdown Mode
- No Minimum LED Quantity Required
- Stable with Low ESR Output Ceramic Capacitors
- Cycle-by-Cycle Over-Current Protection
- Thermal Shutdown Protection
- Open-String Protection
- Output Short-Circuit Protection
- Available in 14-Pin SOIC and QFN Packages

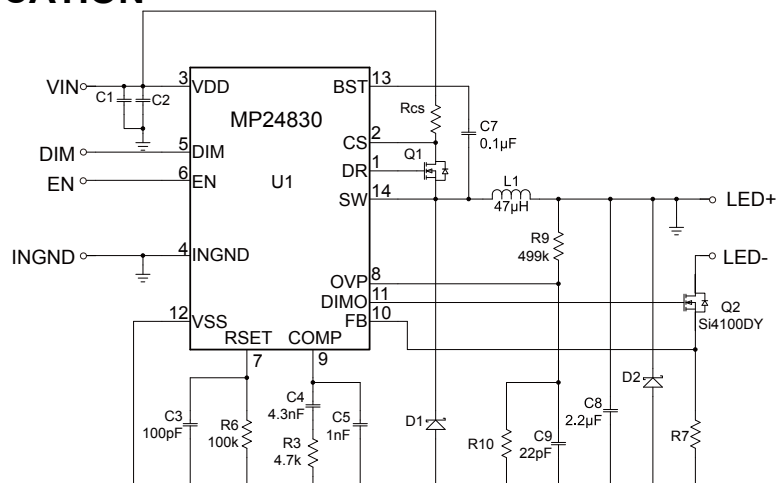
## APPLICATIONS

- General LED Illumination
- Automotive LED Lighting
- LCD Backlight

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## TYPICAL APPLICATION



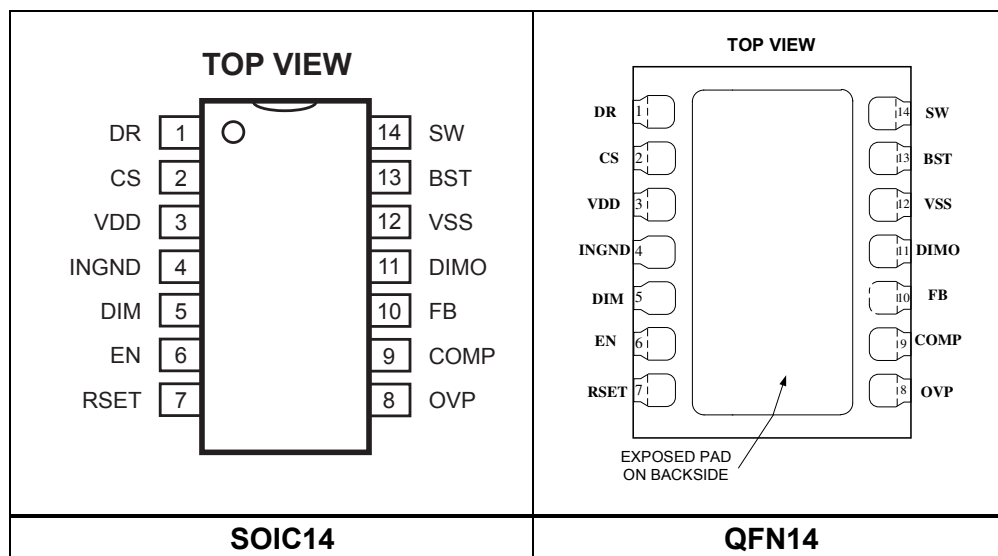
## ORDERING INFORMATION

Part Number	Package	Top Marking
MP24830HS*	SOIC-14	MP24830
MP24830HL**	QFN-14	24830

\* For Tape & Reel, add suffix –Z (e.g. MP24830HS–Z);  
For RoHS Compliant Packaging, add suffix –LF (e.g. MP24830HS–LF–Z)

\*\* For Tape & Reel, add suffix –Z (e.g. MP24830HL–Z);  
For RoHS Compliant Packaging, add suffix –LF (e.g. MP24830HL–LF–Z)

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply Voltage  $V_{DD} - V_{SS}$ ,  $V_{CS} - V_{SS}$  ..... 90V  
 $V_{SW} - V_{SS}$  ..... -0.3V to  $V_{IN} + 0.3V$   
 $V_{BST}$ ,  $V_{DR}$  .....  $V_{SW} + 6V$   
 $V_{EN} - V_{INGND}$ ,  $V_{DIM} - V_{INGND}$  ..... -0.3V to +6V  
 $V_{INGND} - V_{SS}$  ..... -0.3V to 90V  
 Other pins –  $V_{SS}$  ..... -0.3V to +6V  
 Continuous Power Dissipation ( $T_A = +25^\circ C$ ) <sup>(2)</sup>  
 SOIC-14 ..... 1.4W  
 QFN-14 ..... 2.6W  
 Junction Temperature ..... 150°C  
 Lead Temperature ..... 260°C  
 Storage Temperature ..... -65°C to +150°C

### Recommended Operating Conditions <sup>(3)</sup>

Supply Voltage  $V_{DD} - V_{SS}$  ..... 4.5V to 85V  
 Operating Junction Temp. ( $T_J$ ) -40°C to +125°C

### Thermal Resistance <sup>(4)</sup> $\theta_{JA}$ $\theta_{JC}$

SOIC-14 ..... 86 ..... 38 ... °C/W  
 QFN-14 ..... 49 ..... 10 ... °C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) –  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device function is not guaranteed outside of the recommended operating conditions.
- Measured on JESD51-7, 4-layer PCB.



# ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = +25^{\circ}C$ , all voltages with respect to  $V_{SS}$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	$V_{FB}$	$4.5V \leq V_{IN} \leq 90V$	0.192	0.2	0.208	V
Feedback Current	$I_{FB}$	$V_{FB} = 0.22V$	-50		50	nA
Under Voltage Lockout Threshold Rising	$V_{UVLOTH}$		3.7	4.1	4.4	V
Under Voltage Lockout Threshold Hysteresis	$V_{UVLOHY}$			160		mV
Operation Current (Quiescent)	$I_Q$	$V_{EN} = 2V$ , $V_{FB} = 0.25V$		0.8	1.1	mA
Supply Current (Quiescent) at EN Off	$I_{OFF}$	$V_{EN}=0V$		10	23	$\mu A$
Gate Driver Pull-Up Impedance	$R_{PULL\ UP}$			25		$\Omega$
Gate Driver Pull-Down Impedance	$R_{PULL\ Down}$			7		$\Omega$
Gate Driver Output-High to SW	$V_{OH-SW}$	$I_{DR}=10mA$	5.6	5.8		V
Gate Driver Output-Low to SW	$V_{OL-SW}$	$I_{DR}=10mA$		0.1	0.3	V
DIMO Source Current	$I_{DIMOSC}$			0.05		A
DIMO Sink Current	$I_{DIMOSK}$			0.05		A
DIMO Output High	$V_{DIMOH}$	$I_{DR}=10mA$	4.6	5		V
DIMO Output Low	$V_{DIMOL}$	$I_{DR}=10mA$		0.4	0.5	V
Oscillator Frequency	$f_{SW}$	$V_{FB} = 0.15V$ , $R_{SET}=100k\Omega$	145	215	265	kHz
Min. Oscillator Frequency	$f_{SWMIN}$	$V_{FB} = 0.15V$ , $R_{SET}=380k\Omega$	30	50	75	kHz
Max. Oscillator Frequency	$f_{SWMAX}$	$V_{FB} = 0.15V$ , $R_{SET}$ open	245	365	465	kHz
Foldback Frequency	$f_{SWFB}$	$V_{FB} = 0V$ , $V_{OVP}=0V$ , $R_{SET}=100k\Omega$		30		kHz
GM of Error Amplifier	GM			80		$\mu s$
Error Amplifier Output Current	$I_{Oamp}$			40		$\mu A$
Current Sensing Gain	$G_{CS}$			20		
High-Side Current Limit Threshold	$V_{CLTH}$			45		mV
Min. Off-Time	$t_{OFFMIN}$	$V_{FB} = 0.19V$ , $R_{SET}=100k\Omega$		280		ns
Min. On-Time <sup>(5)</sup>	$t_{ON}$			100		ns
EN Input Current	$I_{ENIN}$	$V_{EN} = 3.3V$		3.7		$\mu A$
EN OFF Threshold (w/Respect to INGND)	$V_{ENOFFTH}$	$V_{EN}$ Falling	0.4			V
EN ON Threshold (w/Respect to INGND)	$V_{ENONTH}$	$V_{EN}$ Rising			1.4	V
Min. DIM Threshold	$V_{DIMTHL}$	$V_{FB} = 0.2V$	0.6	0.7	0.8	V
Max. DIM Threshold	$V_{DIMTHH}$	$V_{FB} = 0.2V$	1.55	1.75	1.95	V
LED-Short Threshold for Immediate Latch-Off				600		mV
LED Short Delay for Latch-Off				450		$\mu s$
LED Short Threshold				300		mV
Thermal Shutdown <sup>(5)</sup>	$T_{TSHD}$			160		$^{\circ}C$
Open LED OV Threshold	$V_{OVPTH}$		1.1	1.2	1.3	V
Open LED OV Hysteresis	$V_{OVPHY}$			50		mV

## Notes:

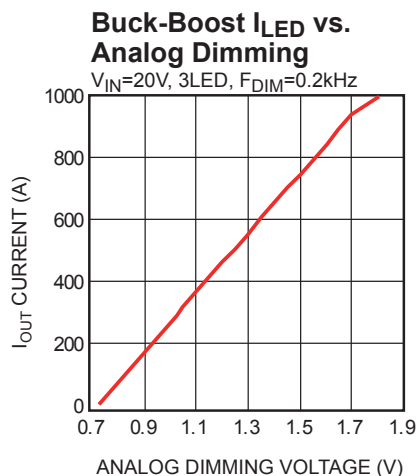
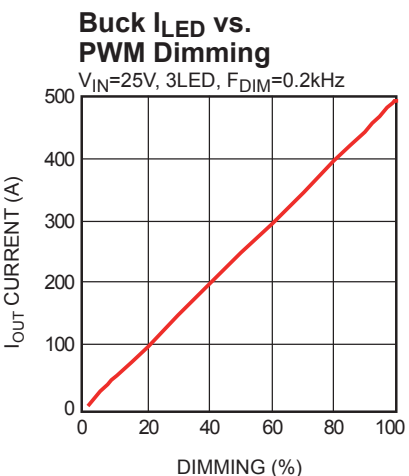
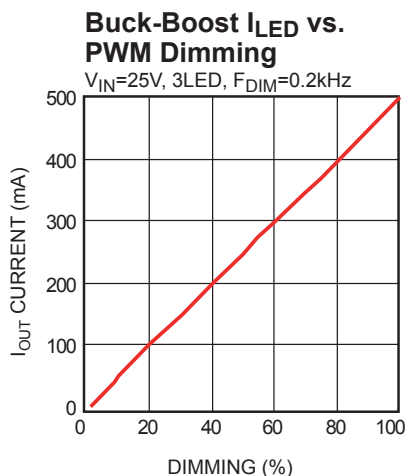
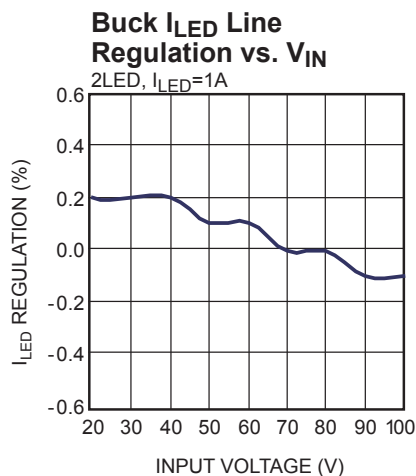
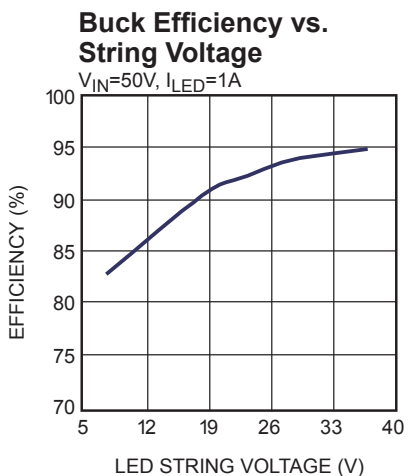
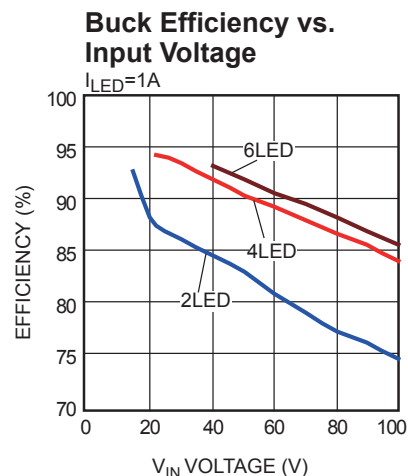
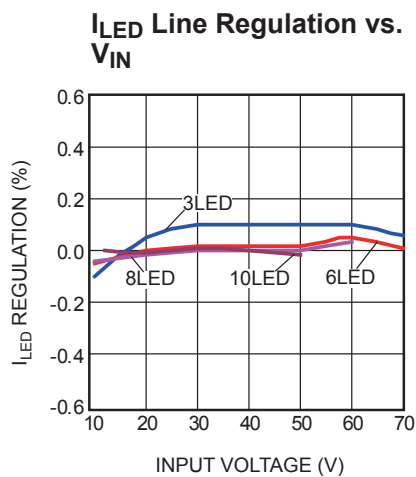
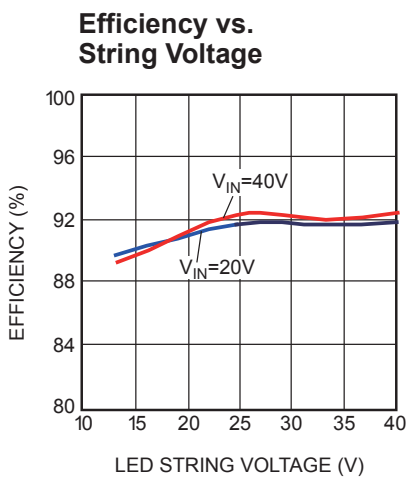
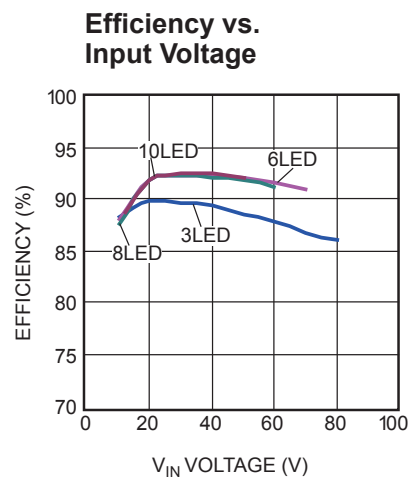
5) Guaranteed by design.

## PIN FUNCTIONS

SOIC14	Name	Description
1	DR	Driver Output. Connect it to the high-side MOSFET gate.
2	CS	High-Side Current Sense. For over-current protection and current-mode control.
3	VDD	Supply Voltage. Operates from a 4.5V-to-85V unregulated input (with respect to VSS). Needs C1 to prevent large input voltage spikes.
4	INGND	Input Ground Reference. Reference for the EN/DIM signal.
5	DIM	Dimming Command Input. Selects for DC or PWM dimming. When the DIM pin voltage (with respect to INGND) rises from 0.6V to 1.95V, the LED current changes from 0% to 100% of the maximum LED current. For PWM dimming, apply a 100Hz-to-2kHz square wave with an amplitude greater than 2V. For combined analog and PWM dimming, apply a 100Hz-to-2kHz square wave signal with amplitude from 0.6V to 1.95V.
6	EN	Enable.
7	RSET	Frequency Set. Connect a resistor to VSS to set the switching frequency, and a 1nF capacitor to VSS to bypass the noise. Leaving this pin open for the 350kHz default operating frequency.
8	OVP	Over-Voltage Protection. Use a voltage divider to program OVP threshold. When the OVP pin voltage reaches the 1.2V shutdown threshold, the switch turns off and recovers when the OVP voltage decreases sufficiently. When the OVP pin voltage (with respect to VSS) falls below 0.4V and the FB pin voltage falls below 0.1V, the chip interprets this as a short circuit and the operating frequency will fold back. Program the OVP pin voltage from 0.4V to 1.2V for normal operation.
9	COMP	Error Amplifier Output. Connect a 1nF or larger capacitor on COMP and an RC network from FB to COMP to improve the stability and to provide soft-start and PWM dimming.
10	FB	LED Current Feedback Input. A current-sensing resistor between FB and VSS provides circuit feedback. The regulation voltage is 0.2V. Short-circuit protection triggers if the FB voltage exceeds 300mV for 450μs or the FB voltage exceeds 600mV.
11	DIMO	DIM Output. Provides for accurate PWM dimming control following DIM logic. Connect to the gate of the external dimming MOSFET. Leave floating if dimming accuracy is not a concern.
12	VSS	Power Return. Connect to the circuit's point of lowest potential, which is typically the anode of the Schottky rectifier. Acts as the voltage reference for the regulated output voltage, and layout requires extra consideration. Place this node outside of the D1-to-C1 ground path to prevent switching current spikes from inducing voltage noise. Connect the exposed pad to this pin.
13	BST	Bootstrap. Connect a capacitor between the SW and BST pins to form a floating supply across the power switch driver. Use a 100nF or larger ceramic capacitor to provide sufficient energy to drive the power switch's gate above the supply voltage.
14	SW	Switch. Connect to the source of the external MOSFET

# TYPICAL PERFORMANCE CHARACTERISTICS

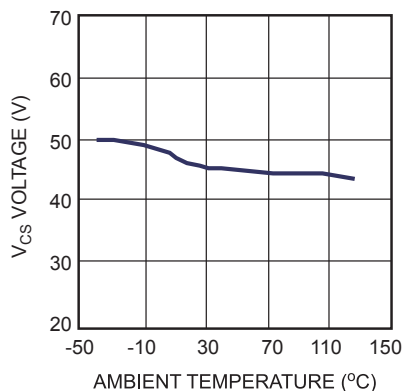
$V_{EN}=5V$ ,  $V_{IN}=5V$  to  $85V$ ,  $I_{OUT}=0.5A$ ,  $L=47\mu H$ ,  $T_A=25^\circ C$ , unless otherwise noted.



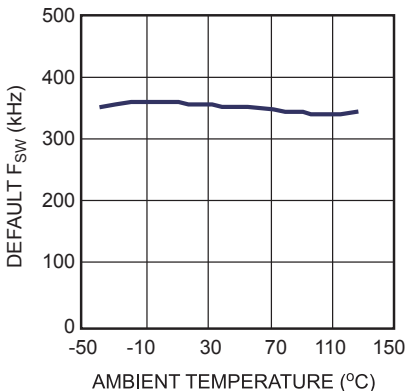
# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{EN}=5V$ ,  $V_{IN}=5V$  to  $85V$ ,  $I_{OUT}=0.5A$ ,  $L=47\mu H$ ,  $T_A=25^\circ C$ , unless otherwise noted.

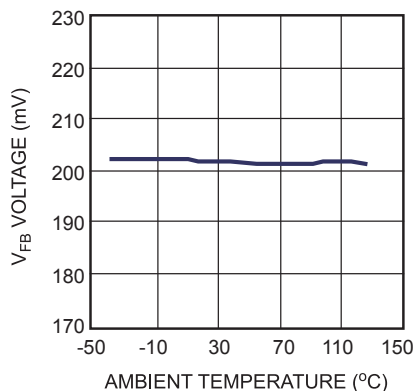
**$V_{CS}$  vs. Temperature**



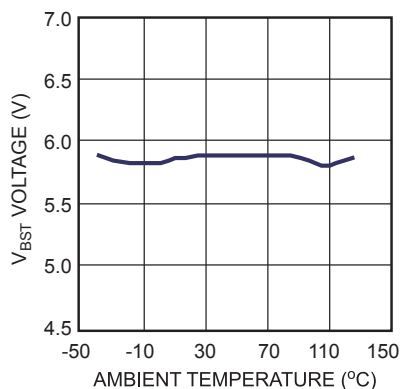
**$F_{SW}$  vs. Temperature**



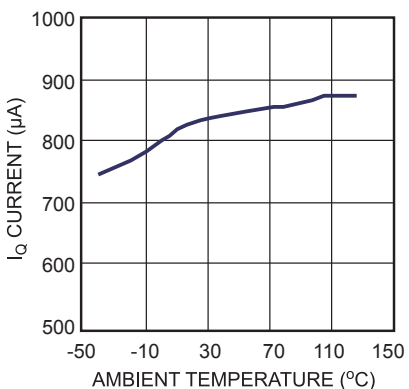
**$V_{FB}$  vs. Temperature**



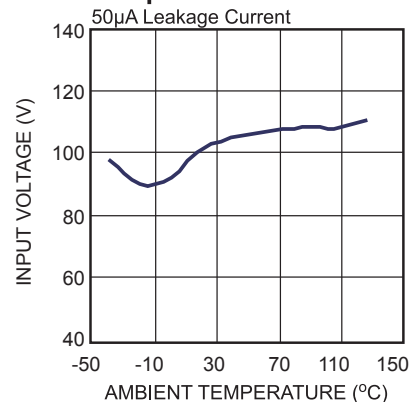
**$V_{BST}$  vs. Temperature**



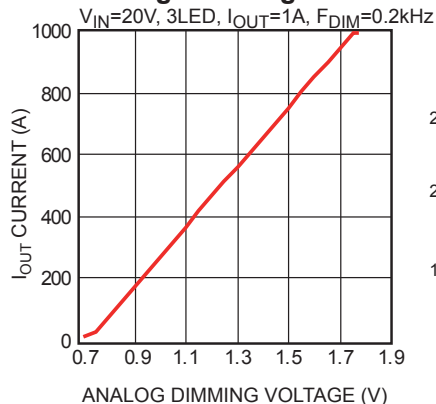
**$I_Q$  Current vs. Temperature**



**Input Voltage vs. Temperature**

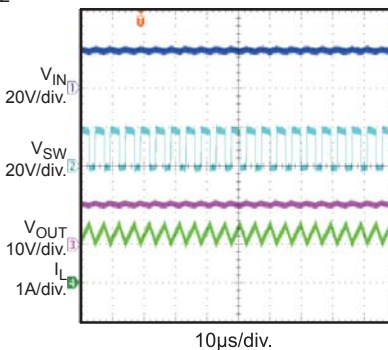


**Buck ILED vs. Analog Dimming**



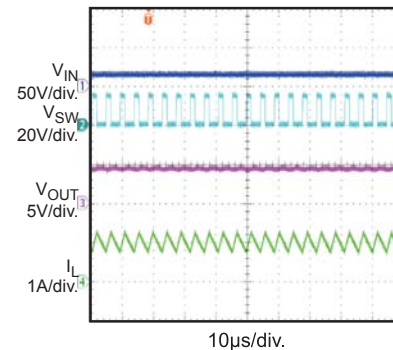
**Buck-Boost Steady State**

$V_{IN} = 8V$ , 3LED,  $I_{OUT} = 1A$



**Buck Steady State**

$V_{IN} = 14V$ , 1LED,  $I_{OUT} = 1A$

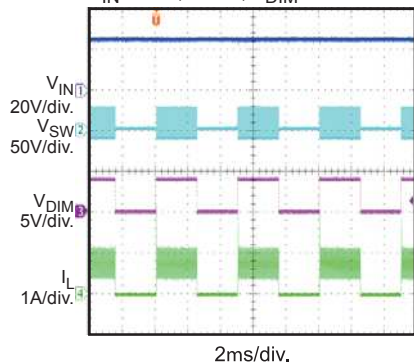


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{EN}=5V$ ,  $V_{IN}=5V$  to  $85V$ ,  $I_{OUT}=0.5A$ ,  $L=47\mu H$ ,  $T_A=25^\circ C$ , unless otherwise noted.

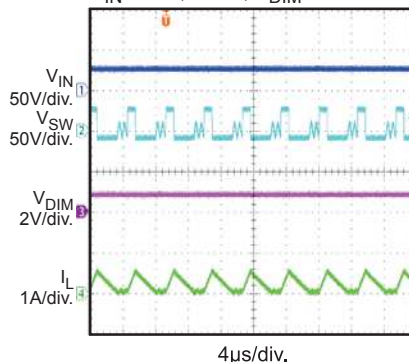
### Buck-Boost PWM Dimming

$V_{IN} = 25V$ , 3LED,  $F_{DIM} = 200Hz/50\%$



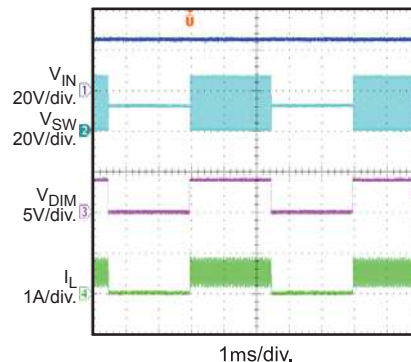
### Buck-Boost Analog Dimming

$V_{IN} = 25V$ , 3LED,  $V_{DIM} = 0.9A$



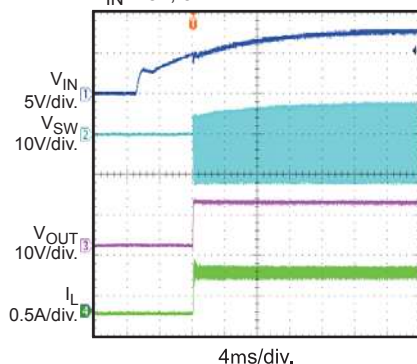
### Buck PWM Dimming

$V_{IN} = 25V$ , 3LED,  $F_{DIM} = 200Hz/50\%$



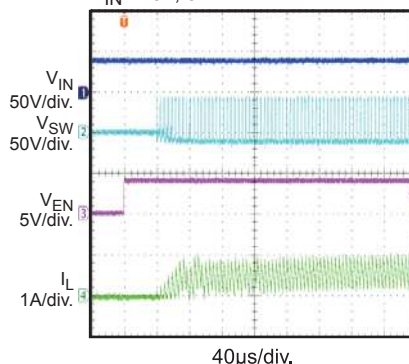
### Buck-Boost Power Ramp Up

$V_{IN} = 8V$ , 3LED



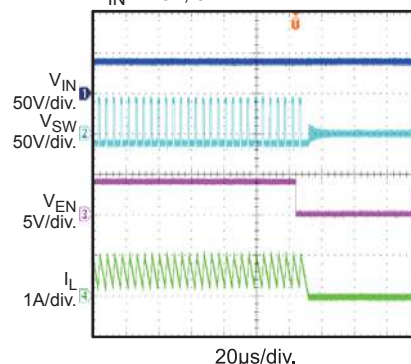
### Buck-Boost Enable Power Up

$V_{IN} = 40V$ , 3LED



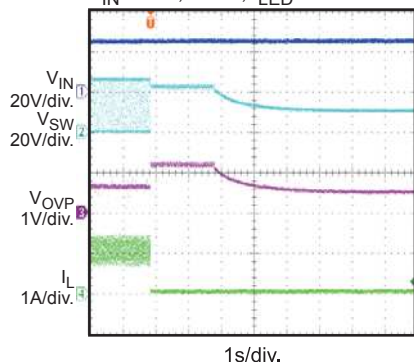
### Buck-Boost Enable Power Down

$V_{IN} = 40V$ , 3LED



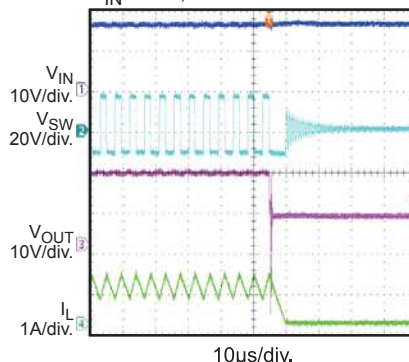
### Buck-Boost Open LED Protection

$V_{IN} = 25V$ , 3LED,  $I_{LED} = 1A$



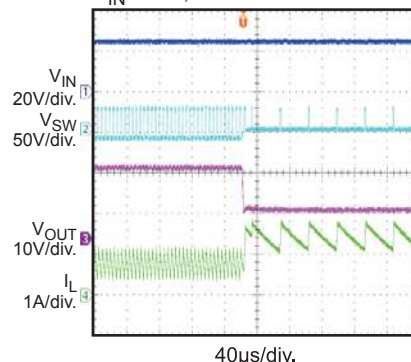
### Buck-Boost Short LED Protection

$V_{IN} = 16V$ , 3LED



### Buck-Boost Short LED to VSS

$V_{IN} = 25V$ , 3LED





## FUNCTIONAL BLOCK DIAGRAM

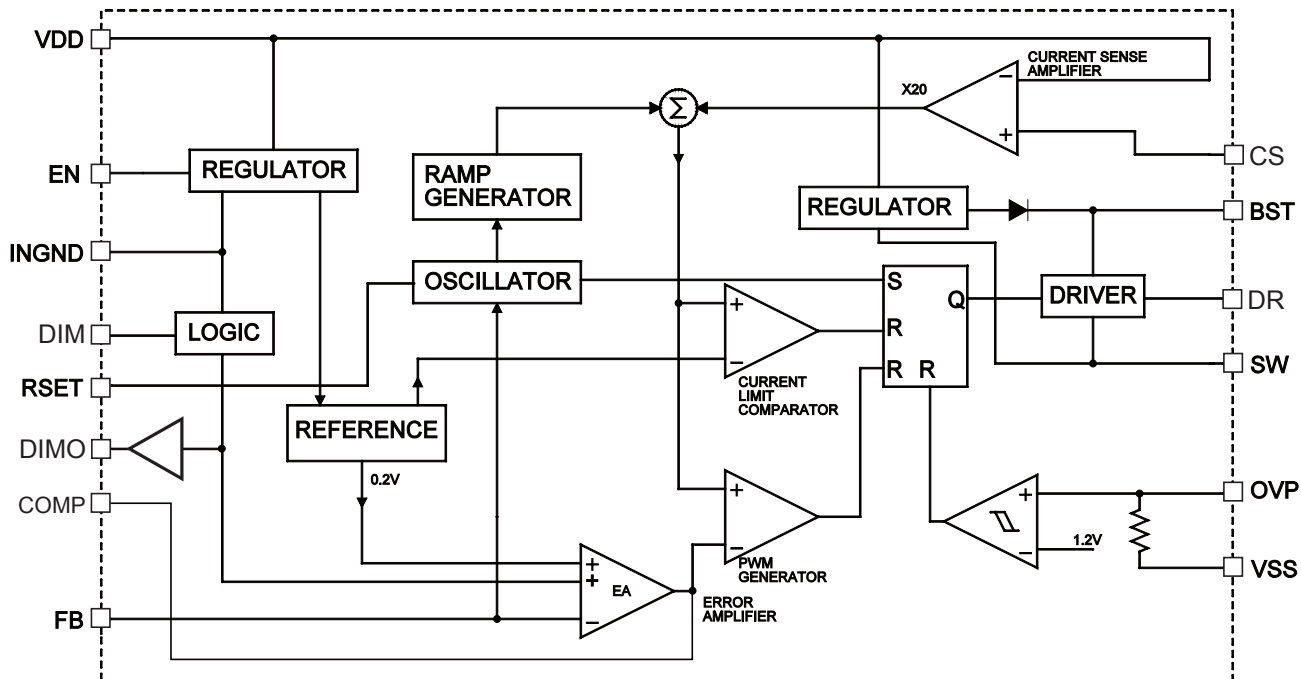


Figure 1: Functional Block Diagram

## OPERATION

The MP24830 is a current-mode regulator. The error amplifier (EA) output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage exceeds the current sense amplifier output, and the current comparator's output is low. The rising edge of the CLK signal (its frequency equals the switching frequency) triggers the RS flip-flop. The driver turns on the external MOSFET, thus connecting the SW pin and inductor to the input supply.

The current-sense amplifier (CSA) senses the increasing inductor current. The PWM comparator compares the sum of the ramp generator and the CSA output against the output of the error amplifier. When the sum of the CSA output and the ramp generator signal exceeds the EA output voltage, the RS flip-flop resets and driver turns off the external MOSFET. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the CSA output and the ramp compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the flip-flop.

The output of the EA integrates the voltage difference between the feedback and the 0.2V reference: A value of  $0.2V - V_{FB}$  increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, increasing its voltage also increases the current delivered to the output.

### LED Open Protection

If the LED is open, there is no voltage on the FB pin. The duty cycle increases until OVP-VSS reaches the shutdown threshold set by the external resistor divider. The top switch remains off until the voltage OVP-VSS drops below 1.2V.

### LED Short Protection

If the FB voltage exceeds 600mV, the IC latches off immediately and DIMO goes low. If the FB voltage exceeds 300mV for 450μs, the IC latches off and DIMO is pulled low. The EN needs to reset to restart the IC.

### Dimming Control

The MP24830 allows both DC and PWM dimming on the DIM pin. For analog dimming, a voltage range from 0.6V to 1.95V linearly sets the LED current from 0% to 100% of the maximum LED current. DIM voltages exceeding 2V results in the maximum LED current. For PWM dimming, use a square signal with an amplitude ( $V_{DIM} - V_{INGND}$ ) that exceeds 1.95V. For good dimming linearity, select a PWM frequency in range of 100Hz to 2kHz. For a higher dimming frequency or dimming ratio, use the DIMO pin to control an external dimming MOSFET. For combined analog and PWM dimming, apply a PWM signal with amplitude of 0.6V to 1.95V on the DIM pin.

### Output Short-Circuit Protection

The MP24830 integrates output short-circuit protection (SCP) to foldback the operating frequency and decrease power consumption when the output is shorted to VSS. Such shorts cause the voltage on the OVP pin to drop below 0.4V, and the FB pin senses no voltage ( $<0.1V$ ) as no current goes through the WLED.

In buck-boost applications, when there is a possibility that LED+ short-circuits to VSS, add a diode from VSS to INGND to protect the IC, as shown in below in Figure 2.

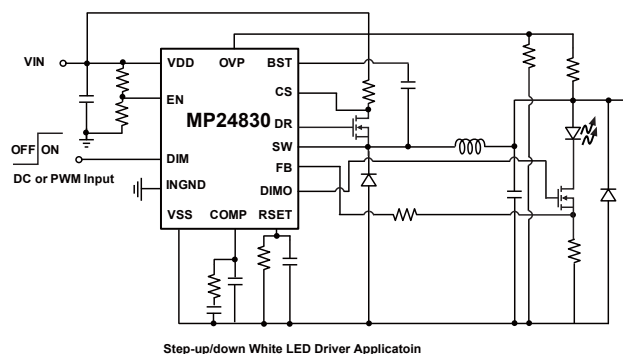


Figure 2: Buck-Boost Application with Possible LED+ Short to VSS

## APPLICATION INFORMATION

The MP24830 can be used in buck mode and buck-boost mode applications.

### Setting the LED Current

An external resistor  $R_{FB}$  sets the maximum LED current as per the equation:

$$R_{FB} = \frac{0.2V}{I_{LED}}$$

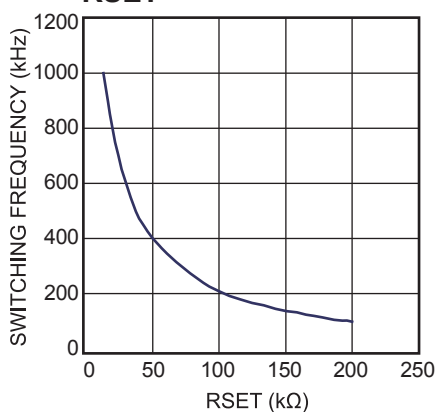
### Setting the Switching Frequency

The switching frequency is set by an external resistor,  $R_{SET}$ , connected from the RSET pin to VSS. The relationship between the switching frequency and the programming resistor is as per the following table and shown in Figure 3.

**Table 1  $R_{SET}$  and  $f_{SW}$  Relationship**

$f_{SW}$ (kHz)	$R_{SET}$ (k $\Omega$ )
100	200
125	165
210	100
400	50.4
600	30.3
800	19.9
1000	13.2
350	Open

**Switching Frequency vs.  $R_{SET}$**



**Figure 3: Switching Frequency vs.  $R_{SET}$**

The MP24830 implements current mode control by sensing the inductor current through a current sensing resistor  $R_{CS}$ , as calculated by:

$$R_{CS} = \frac{0.9 \times V_{CL}}{I_{L\_PK\_Max}}$$

Where the  $V_{CL}$  is the current limit,  $V_{CL}=50mV$ , and  $I_{L\_PK\_Max}$  is the maximum peak current in the inductor.

Calculate  $R_{CS}$  using the minimum input voltage, the maximum output voltage and the maximum output current.

### Setting the Over-Voltage Protection

The MP24830 detects output over-voltage via the OVP pin. The OVP pin monitors the output voltage through a voltage divider ( $R_{OVP1}$  and  $R_{OVP2}$ ): When the OVP voltage exceeds 1.24V, the IC triggers OVP.

Select the resistor value ratio using the following equation:

$$\frac{R_{OVP1}}{R_{OVP2}} = \frac{V_{OUT\_OVP}}{V_{th\_OVP}} - 1$$

The OVP trip-point is set between 0.4V and 1.24V.

### Setting the Compensation

The MP24830 implements current-mode control to regulate the LED current feedback through the compensation network on the COMP pin. For most applications, use an RCC compensation network to ensure current accuracy and the system stability, as shown in Figure 4.

Its DC gain is:

$$DCGain_{EA} = \frac{gm \times R_{FB}}{C_z + C_p}$$

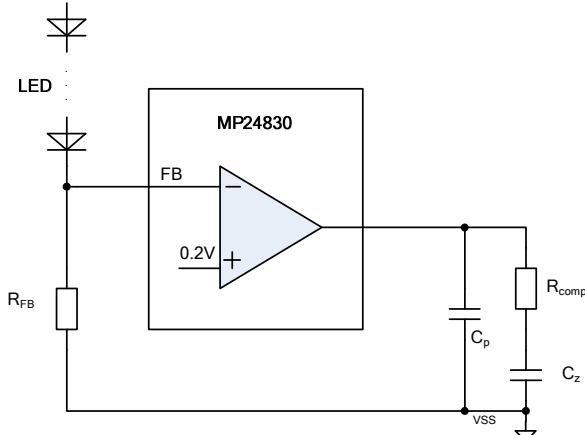
Where  $gm$  is error amplifier's transconductance of  $80\mu A/V$ .

The zero of the compensation network is:

$$f_{z\_EA} = \frac{1}{2\pi \times R_{COMP} \times C_z}$$

The pole of the compensation network is:

$$f_{p\_EA} = \frac{1}{2\pi \times R_{COMP} \times \frac{C_z \times C_p}{C_z + C_p}}$$



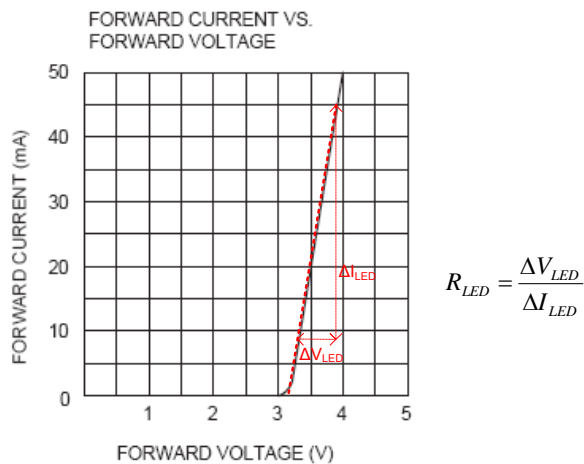
**Figure 4: RCC Compensation Network on COMP Pin**

### (1) Compensation network for Buck-boost application

The DC modulator gain of the buck-boost power stage (from the output current to the control voltage on COMP pin) is:

$$DCGain\_PS = \frac{\frac{V_{OUT} \times V_{IN}}{V_{OUT} + V_{IN}}}{20 \times R_{CS} \times \left( \frac{V_{OUT}}{R_{FB} + R_{LED}} + \frac{I_{OUT} \times V_{OUT}}{V_{OUT} + V_{IN}} \right) \times (R_{FB} + R_{LED})}$$

Where  $R_{CS}$  is the switch current sensing resistor on CS pin,  $R_{LED}$  is the equivalent dynamic resistance of the LED load, as shown in Figure 5.



**Figure 5: LED Dynamic Resistance Equivalent**  
The dominant low-frequency pole of the buck-boost power stage is:

$$f_{P\_PS} = \frac{\frac{V_{OUT}}{R_{FB} + R_{LED}} + \frac{I_{OUT} \times V_{OUT}}{V_{OUT} + V_{IN}}}{2\pi V_{OUT} \times C_{OUT}}$$

The right-half plane (RHP) zero of the buck-boost power stage is:

$$f_{Z\_RHP} = \frac{V_{IN}^2}{2\pi \times L \times I_{OUT} \times (V_{OUT} + V_{IN})}$$

Step 1: Select  $R_{COMP}$

Choose a crossing frequency,  $f_c$ , below  $1/3 \times f_{Z\_RHP}$  to derive the compensation network as follow (assume  $C_Z \gg C_P$ ):

$$R_{COMP} = \frac{f_c}{gm \times R_{FB} \times DCGain\_PS \times f_{P\_PS}}$$

That is:

$$R_{COMP} = \frac{2\pi f_c \times C_{OUT} \times 20 \times R_{CS} \times (R_{FB} + R_{LED}) (V_{OUT} + V_{IN})}{gm \times R_{FB} \times V_{IN}}$$

Use the maximum input voltage and minimum output voltage to calculate  $R_{COMP}$ .

Step 2: Select  $C_Z$

Set the zero of the compensation network to cancel the minimum pole of the power stage to get:

$$C_Z = \frac{1}{2\pi \times f_{P\_PS} \times R_{COMP}}$$

Choose  $C_Z$  with the maximum input voltage and maximum output voltage.

Step 3: Select  $C_P$

Set the pole of the compensation network to cancel the minimum RHP zero to get:

$$C_P \approx \frac{1}{2\pi \times f_{Z\_RHP} \times R_{COMP}}$$

Choose  $C_P$  with the minimum input voltage and maximum output voltage.



## (2) Compensation network for Buck application

The DC modulator gain of the buck power stage (from the output current to the control voltage) is:

$$\text{DCGain\_Buck} = \frac{1}{20 \times R_{CS}}$$

The dominant, low frequency pole of the buck power stage is:

$$f_{p\_Buck} = \frac{1}{2\pi \times (R_{FB} + R_{LED} + R_{ESR}) \times C_{OUT}}$$

The zero produced by the ESR of the output capacitor is:

$$f_{z\_ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

Where  $R_{ESR}$  is the ESR of the output capacitor.

Step 1: Select  $R_{COMP}$

Choose a crossing frequency,  $f_c$ , below  $1/5 \times f_c$  to derive the compensation network as follows (assume  $C_z \gg C_p$ ):

$$R_{COMP\_Buck} = \frac{f_c}{gm \times R_{FB} \times \text{DCGain\_Buck} \times f_{p\_Buck}}$$

That is:

$$R_{COMP\_Buck} = \frac{2\pi f_c \times C_{OUT} \times 20 \times R_{CS} \times (R_{FB} + R_{LED} + R_{ESR})}{gm \times R_{FB}}$$

Step 2: Select  $C_z$

Set the zero of the compensation network to cancel the minimum pole of the Buck power stage to get:

$$C_{z\_Buck} = \frac{1}{2\pi \times f_{p\_Buck} \times R_{COMP\_Buck}}$$

Step 3: Select  $C_p$

Set the pole of the compensation network to cancel the ESR zero. If the ESR zero is too high, set this pole at around 3 to 5 times  $f_c$ :

$$C_p \approx \max\left(\frac{1}{2\pi \times f_{z\_ESR} \times R_{COMP\_Buck}}, \frac{1}{2\pi \times 5f_c \times R_{COMP\_Buck}}\right)$$

## Selecting the Inductor

Select the inductor based on the input voltage, the output voltage, and the LED current. Select the inductor to make the circuit operate in continuous current mode (CCM). Select the inductor current rating to ensure that the inductor does not saturate and with consideration to power consumption based on the DC resistance.

(1) Selecting the Inductor for Buck-Boost Applications

For buck-boost applications, select the inductor based on the following equation:

$$L = \frac{V_{IN} \times V_{OUT}}{f_{SW} \times (V_{IN} + V_{OUT}) \times \Delta I_L}$$

Where  $\Delta I_L$  is the peak-to-peak inductor current ripple. Design  $\Delta I_L$  to be between 30% and 60% of the average current of the inductor, which is:

$$I_{L\_AVG} = I_{LED} \times \left(1 + \frac{V_{OUT}}{V_{IN}}\right)$$

Select the inductor with a DC current rating that ensurew that the inductor does not saturated at the peak current of:

$$I_{L\_PK} = I_{L\_AVG} + 0.5\Delta I_L$$

(2) Selecting the Inductor for Buck Applications

For buck applications, derive the inductance value from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to around 30% to 60% of the maximum load current. The maximum inductor peak current is calculated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

## Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. For best results, use

ceramic capacitors with X7R dielectrics with low ESR and small temperature coefficients.

Select a large-enough capacitor to limit input the voltage ripple,  $\Delta V_{IN}$ , to less than 5% to 10% of the DC value.

$$C_{IN} > \frac{I_{L\_AVG} \times V_{OUT}}{f_{SW} \times \Delta V_{IN} \times (V_{IN} + V_{OUT})}$$

### Selecting the Output Capacitor

The output capacitor limits the output voltage ripple,  $\Delta V_{OUT}$  (normally less than 1% to 5% of the DC value), and ensures feedback loop stability. Use an output capacitor with impedance at the switching frequency. Use ceramic capacitors with low ESR characteristics.

$$C_{OUT} > \frac{I_{LED} \times V_{OUT}}{f_{SW} \times \Delta V_{OUT} \times (V_{IN} + V_{OUT})}$$

### PC Board Layout

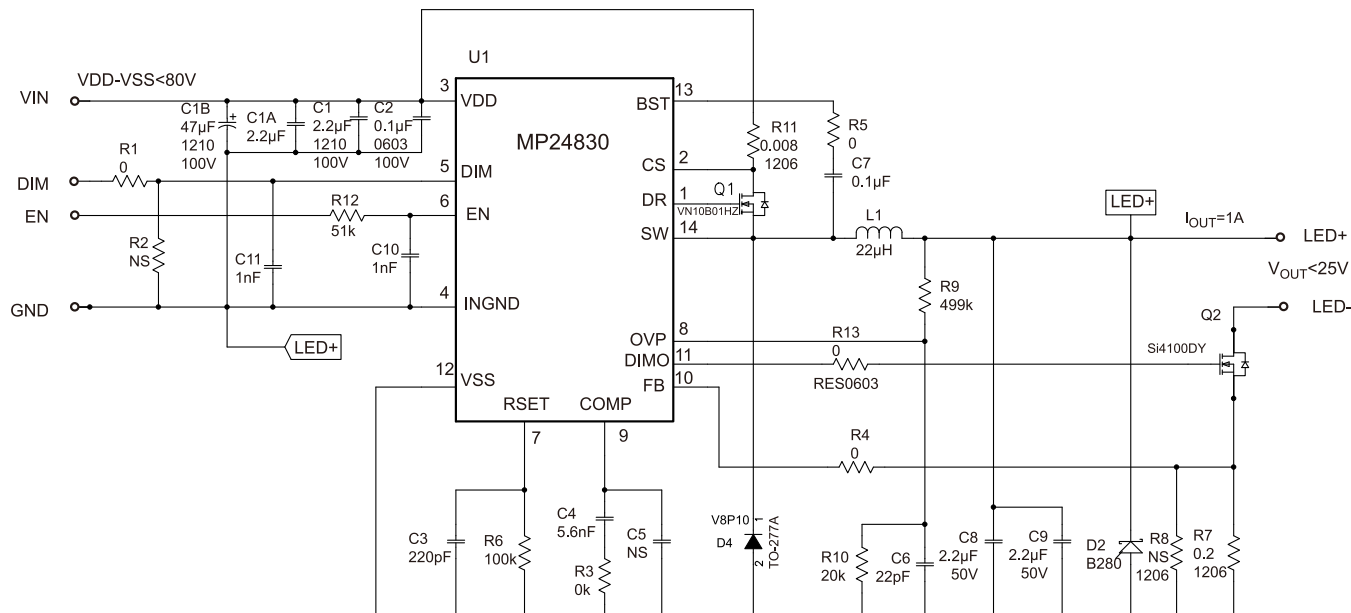
Place the high-current paths (VSS, VDD and SW) very close to the device with short, direct, and wide traces. Place the input capacitor as close as possible to the VDD and VSS pins. Place the external feedback resistors next to the FB pin. Keep the switch node traces short and away from the feedback network.

Pay special attention is required to the switching frequency loop layout, which should be as small as possible.

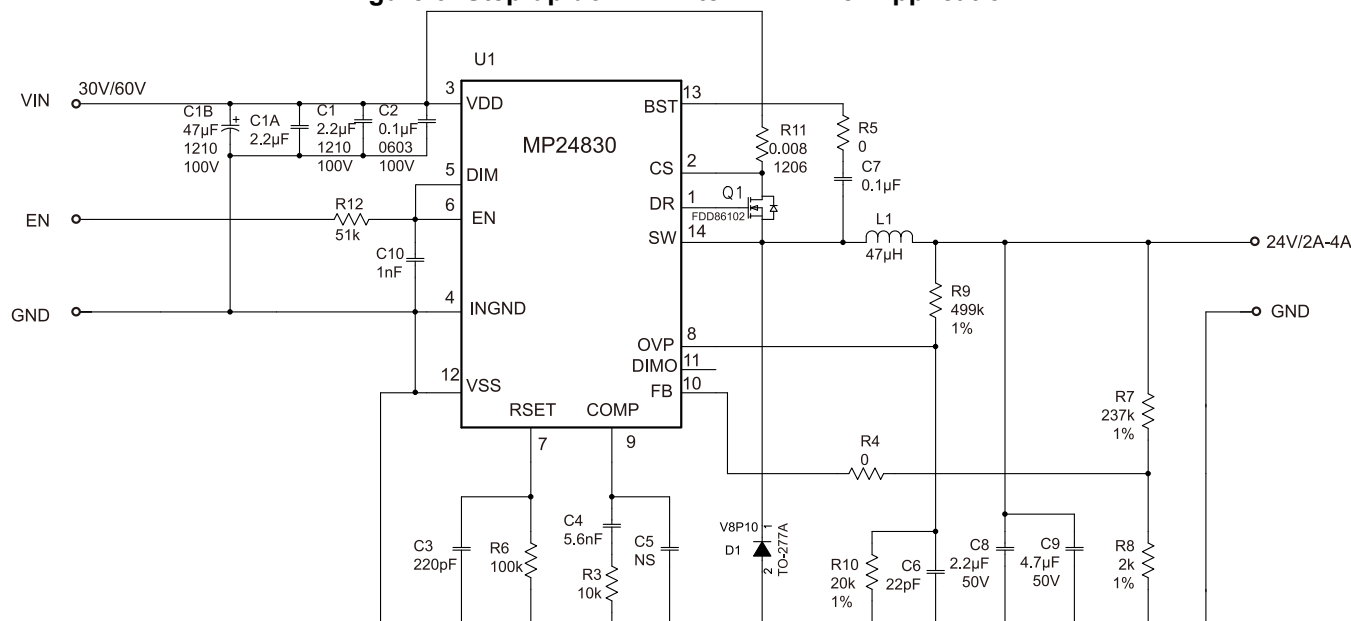
For buck applications, the switching frequency loop is composed of the input capacitor, the power MOSFET and the Schottky diode. Place the Schottky diode close to the power MOSFET and the input capacitor.

For buck-boost or boost applications, the switching frequency loop is composed of the input capacitor, the power MOSFET, the Schottky diode and the output capacitor. Make this component loop as small as possible. For most applications, place the output capacitor close to the input capacitor and the power MOSFET.

## TYPICAL APPLICATION CIRCUIT



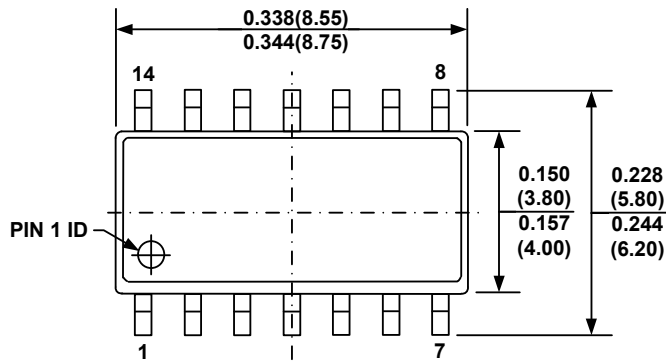
**Figure 6: Step-up/down White LED Driver Application**



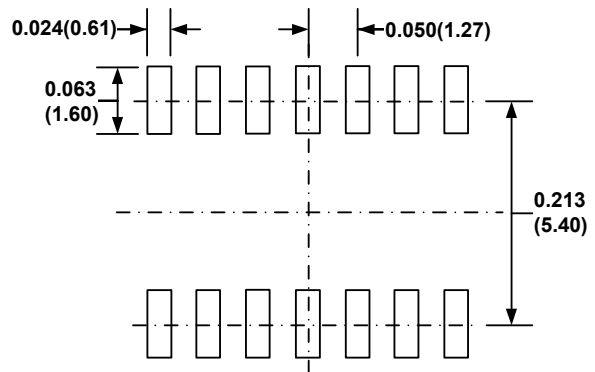
**Figure 7: Step-down Constant Voltage Converter Application**

## PACKAGE INFORMATION

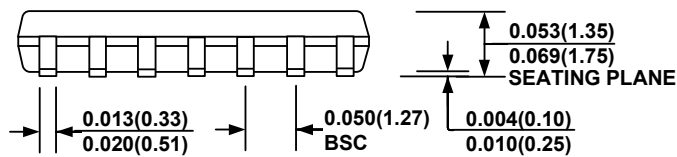
### SOIC-14



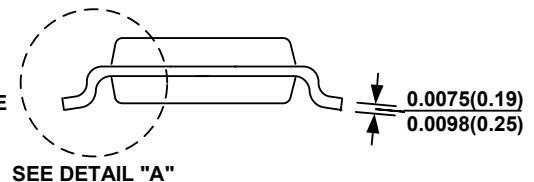
**TOP VIEW**



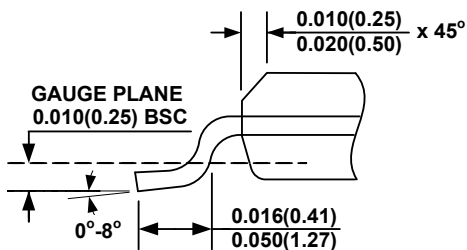
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



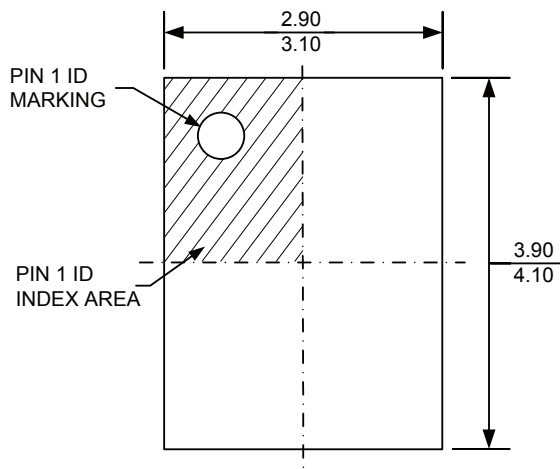
**DETAIL "A"**

#### NOTE:

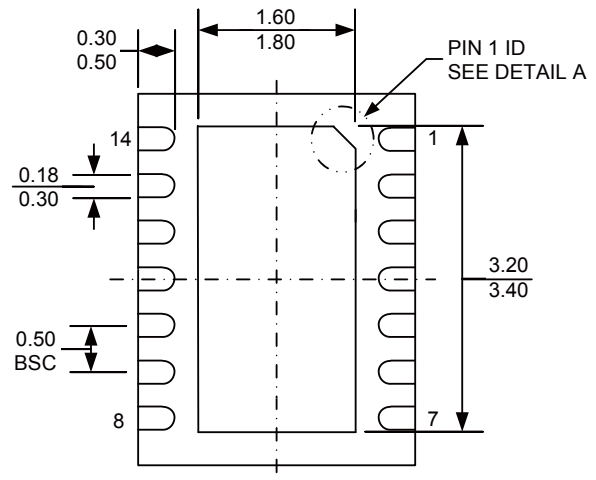
- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.



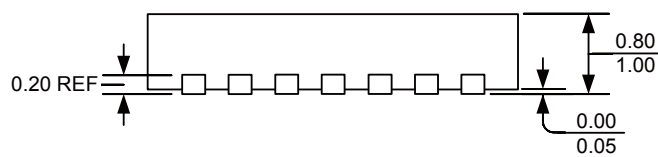
**QFN-14**



TOP VIEW

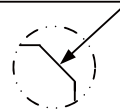


BOTTOM VIEW



SIDE VIEW

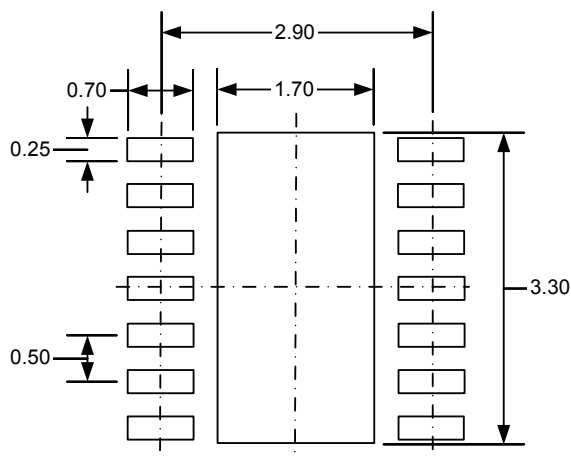
PIN 1 ID OPTION A  
0.30x45° TYP.



PIN 1 ID OPTION B  
R0.20 TYP.



DETAIL A



RECOMMENDED LAND PATTERN

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-229, VARIATION VGED-4.
- 5) DRAWING IS NOT TO SCALE.

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