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MP2624

I²C Controlled 4.5A Single Cell USB / Adaptor Charger with Narrow VDC Power Path Management USB OTG and Shipping Mode

DESCRIPTION

The MP2624 is a 4.5A, highly integrated, switching-mode battery charger IC for single-cell Li-ion or Li-polymer batteries. This device supports NVDC architecture with power path management suitable for different portable applications, such as tablets, MID, and smart phones. Its low impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. The I²C serial interface with charging and system settings allows the device to be controlled flexibly.

The MP2624 supports a wide range of input sources, including standard USB host ports and wall adapters. The MP2624 detects the input source type according to the USB Battery Charging Spec 1.2 (*BC1.2*) and then informs the host to set the proper input current limit. Also, this device is compliant with USB2.0 and USB3.0 power specifications by adopting a proper input current and voltage regulation scheme. In addition, the MP2624 supports USB On-The-Go operation by supplying 5V with current up to 1.3A.

The power path management regulates the system voltage slightly above the set maximum voltage between the battery voltage and the I²C programmable lowest voltage level (e.g. 3.6V). With this feature, the system is able to operate even when the battery is depleted completely or removed. When the input source current or voltage limit is reached, the power path management reduces automatically the charge current to meet the priority of the system power requirement. If the system current continues increasing, even when the charge current is reduced to zero, the supplement mode allows the battery to power both the system and the input power supply at the same time.

The MP2624 is available in a QFN-22 3mm x 4mm package.

FEATURES

- High Efficiency 4.5A 1.5MHz Buck Charger and 1.5MHz 1.3A Boost Mode to Support OTG
  - 94% Efficiency @ 2A
  - Fast Charge Time by Battery Path Impedance Compensation
  - USB OTG
  - 94% Efficiency @ 5V, 1.2A OTG
  - Selectable OTG Current Outputs
- 3.9V to 7.0V Operating Input Voltage Range
- Highest Battery Discharge Efficiency with 10mΩ Battery Discharge MOSFET up to 9A
- Single Input USB Compliant Charge
- Narrow System Bus Voltage Power Path Management
  - Instant On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplemental Mode
- Constant-Off-Time Control to Reduce Charging Time under Lower Input Voltages
- High Accuracy of Charging Parameter
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Full DISC Control to Support Shipping Mode
- High Integration
  - Fully Integrated Power Switches and No External Blocking Diode and Sense Resistor Required
  - Built-In Robust Charging Protection including Battery Temperature Monitor and Programmable Timer
  - Built-In Battery Disconnection Function
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±5% Input Current Regulation
  - ±2% Output Regulation in Boost Mode
- Safety
  - Battery Temperature Sensing for Charge Mode
  - Battery Charging Safety Timer

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- Thermal Regulation and Thermal Shutdown
- Battery/System Over-Voltage Protection
- MOSFET Over-Current Protection
- Charging Operation Indicator
- Thermal Limiting Regulation on Chip
- Tiny QFN-22 3mm x 4mm Package

APPLICATIONS

- Tablet PCs
- Smart Phones
- Mobile Internet Devices

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.
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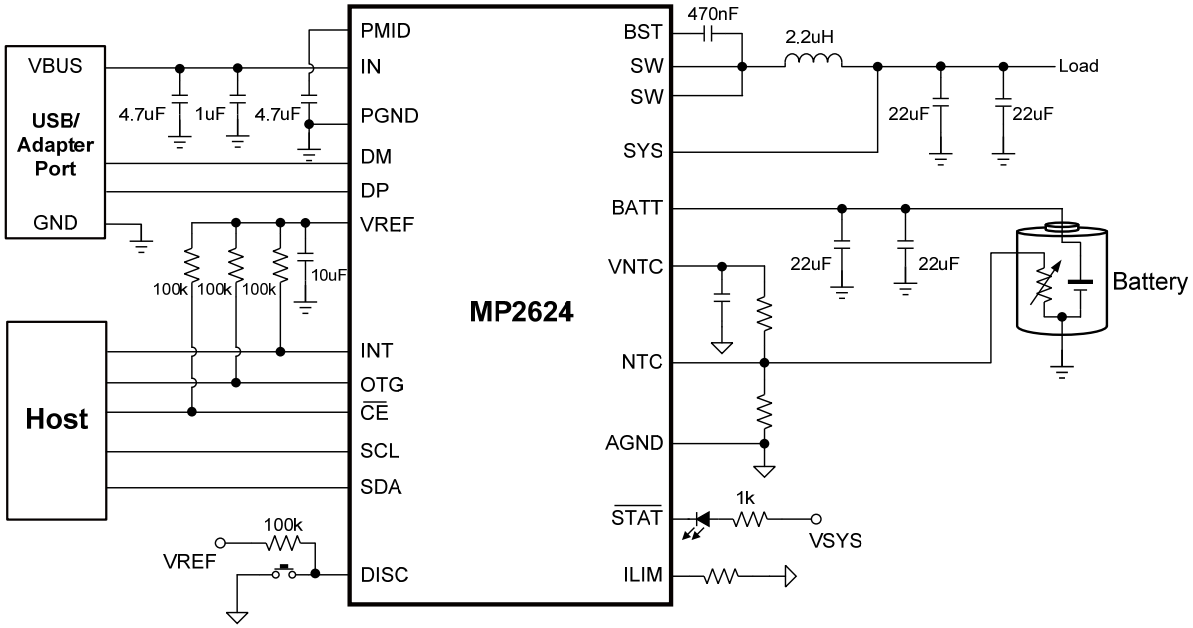
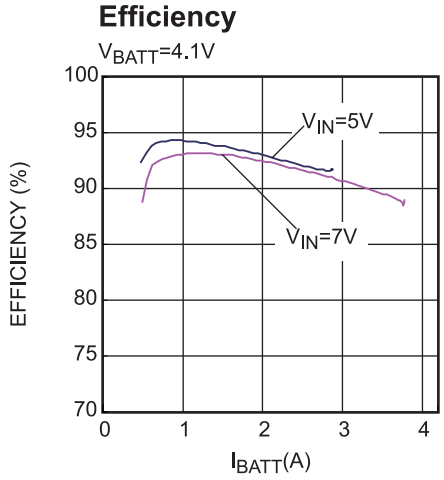
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2624GL	QFN-22 (3mm x 4mm)	*See Below*
EVKT-2624	Evaluation Kit	

* For Tape & Reel, add suffix –Z (e.g. MP2624GL–Z)

TOP MARKING

MPYW
2624
LLL

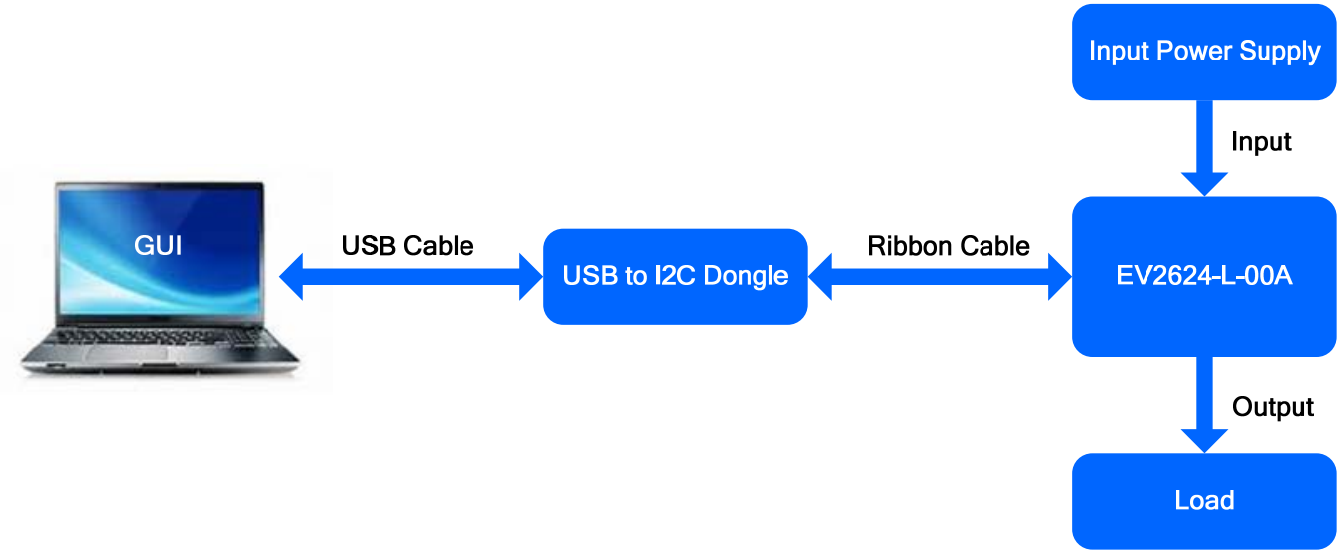
MP: MPS prefix
Y: Year code
W: Week code
2624: First four digits of the part number
LLL: Lot number

EVALUATION KIT EVKT-2624

EVKT-2624 Kit contents: (Items can be ordered separately).

#	Part Number	Item	Quantity
1	EV2624-L-00A	MP2624 Evaluation Board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I2C Dongle, one USB Cable, and one Ribbon Cable	1
3	Tdrive-2624	USB Flash drive that stores the GUI installation file and supplemental documents	1

Order direct from MonolithicPower.com or our distributors



EVKT-2624 Evaluation Kit Set-Up

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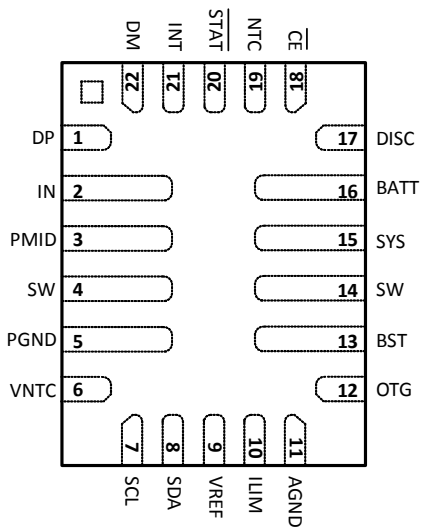
PACKAGE REFERENCE

TOP VIEW



QFN-22 (3mm x 4mm)

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PIN FUNCTIONS

Package Pin #	Name	Type	Description
1	DP	I	**Positive pin of the USB data line pair.** DP and DM achieve USB host/charging port detection automatically.
2	IN	Power	**Power input of the IC from the adapter or USB.** Place a 1µF ceramic capacitor from IN to PGND as close as possible to the IC.
3	PMID	Power	**Internal Power Pin**. Connect to the drain of the reverse-blocking MOSFET and the drain of the high-side MOSFET. Bypass with a 4.7µF capacitor from PMID to PGND as close as possible to the IC.
4, 14	SW	Power	**Switching node.**
5	PGND	Power	**Power ground.**
6	VNTC	O	**Pull-up voltage bias of the NTC comparator resistive divider for both the feedback and the reference.**
7	SCL	I/O	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
8	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
9	VREF	P	**PWM low-side driver output.** Connect a 10µF ceramic capacitor from VREF to AGND as close as possible to the IC.
10	ILIM	I	**Programmable input current limit.** A resistor is connected from ILIM to ground to set the minimum input current limit. The actual input current limit is the lowest setting by ILIM and I²C.
11	AGND	I/O	**Analog ground.**
12	OTG	I	**Boost mode enable control or input current limiting selection pin.** The On-The-Go is enabled through I²C. During boost operation, OTG low suspends boost operation. If the input is detected as the USB host, OTG is used as the input current limiting selection pin. When OTG = high, I_{IN_LMT} = 500mA. When OTG = low, I_{IN_LMT} = 100mA.
13	BST	P	**Bootstrap.** Connect a 470nF bootstrap capacitor between BST and SW to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage.
15	SYS	P	**System output.** Connect a 2x22µF ceramic capacitor from SYS to PGND as close as possible to the IC.
16	BATT	P	**Battery positive terminal.** Connect a 2x22µF ceramic capacitor from BATT to PGND as close as possible to the IC.
17	DISC	I	**Battery disconnection control.**
18	$\overline{CE}$	I	**Active low charge enable.** Battery charging is enabled when the corresponding register is set to active, and $\overline{CE}$ is low.
19	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VNTC to NTC to AGND. The charge is suspended when NTC is out of range.
20	$\overline{STAT}$	O	**Indicator for charging operation.**
21	INT	O	**Open-drain interrupt output.** INT sends the charging status, and the fault interrupts the host.
22	DM	I	**Negative pin of the USB date line pair.** DM and DP achieve USB host/charging port detection automatically.

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ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, STAT to GND .....-0.3V to +20V
SW to GND .....-0.3V (-2V for 20ns) to +20V
BST to GND……..... SW to +6V
BATT, SYS to GND……..-0.3V to +6V
All other pins to GND .....-0.3V to +6V
STAT, INT sink current 10mA
Continuous power dissipation (T_A = +25°C)(2)
..... 2.6W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature…. ..... -65°C to +150°C

Recommended Operating Conditions (3)

V_{IN} to GND ....3.9V to 7.0V(4)
I_{IN}.....Up to 3A
I_{SYS} .....Up to 4.5A
I_{CHG}.....Up to 4.5A
V_{BATT}.....Up to 4.425V
I_{DCHG} .....(Continuous) up to 6A
I_{DCHG} .....(Pulse) up to 9A
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-22 (3mm x 4mm).....	48	11....	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The inherent switching noise voltage should not exceed the absolute maximum rating on either BST or SW. A tight layout minimizes switching loss.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Step-Down Converter						
Input voltage range	V_{IN}		3.9		7.0	V
Input shutdown current		V_{IN} = 5V, both DC/DC and battery FET are disabled			65	μA
Input quiescent current		$V_{IN} > V_{IN\_UVLO}$, $V_{IN} > V_{BATT}$, charge disabled, switching, SYS float		3	5	mA
		$V_{IN} > V_{IN\_UVLO}$, $V_{IN} > V_{BATT}$, charge enabled, switching BATT and SYS float		3	5	
Input under-voltage lockout	V_{IN_UVLO}	V_{IN} rising		3.45	3.6	V
V_{IN_UVLO} hysteresis		V_{IN} falling		200		mV
V_{IN} vs. V_{BATT} headroom		V_{IN} rising	200	250	300	mV
		V_{IN} falling	65	90	115	mV
Internal reverse-blocking MOSFET on resistance	$R_{IN\ to\ PMID}$	Measure from IN to PMID		25	35	mΩ
High-side NMOS on resistance	R_{H_DS}	Measure from PMID to SW		25	35	mΩ
Low-side NMOS on resistance	R_{L_DS}	Measure from SW to PGND		28	35	mΩ
High-side NMOS peak current limit				7.5		A
Low-side NMOS peak current limit				7		A
Switching frequency		V_{BATT} = 4.2V, I_{CHG} = 2A	1.4	1.7	2.0	MHz
SYS Output						
Minimum system regulation voltage [I²C]	V_{SYS_MIN}	I_{SYS} = 0, V_{BATT} = 3.4V, POR default, REG01[2:0] = 110		3.6		V
System regulation voltage	V_{SYS_MAX}	50mV or 100mV (REG01[0]) higher than V_{BATT_FULL} depends on the I²C setting	3.53		4.525	V
Ideal diode forward voltage in supplement mode	V_{F_IDD}	50mA discharge current		24		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SYS/BAT comparator		V_{SYS} falling		40		mV
Battery good comparator (Threshold compared with V_{SYS_MIN})		V_{BATT} rising to the battery FET being turned on fully		60		mV
		V_{BATT} falling		-40		mV
Battery Charger						
Battery charge full voltage [I²C]	V_{BATT_FULL}	Depends on the I²C setting default (REG04[7:2] = 110000): 4.2V	3.48		4.425	V
Charge voltage regulation accuracy		V_{BATT_FULL} = 4.2V	-0.5		0.5	%
Constant current charge current [I²C]		Depends on the I²C setting	0.512		4.544	A
Charge current regulation accuracy		I_{CHG} = 2A	-5		5	%
Battery pre-charge threshold [I²C]	V_{BATT_PRE}	REG04[4]=1, V_{BATT} rising	2.8	3.0	3.1	V
Battery pre-charge hysteresis		V_{BATT} falling		220		mV
Battery short threshold	V_{BATT_SHORT}	V_{BATT} rising	2.0	2.1	2.2	V
Battery short threshold hysteresis		V_{BATT} falling		130		mV
Trickle-charge current	I_{TC}	V_{BATT} = 1.8V		128		mA
Pre-charge current [I²C]	I_{PRE}	Depends on the I²C setting	64		1024	mA
Pre-charge current accuracy		V_{BATT} = 2.6V, I_{PRE} = 256mA	-25		25	%
Termination current [I²C]	I_{BF}	Depends on the I²C setting	128		1024	mA
Termination current accuracy		V_{BATT_FULL} = 4.2V, I_{BF} = 512mA	-30		30	%
		V_{BATT_FULL} = 4.2V, I_{BF} = 128mA	15	98	250	mA
Recharge threshold below V_{BATT_FULL}	V_{RECH}	REG04[0] = 1		180		mV
Recharge threshold delay				20		ms
BATT to SYS FET on resistance	R_{BATFET}	V_{BATT} = 3.8V		10	15	mΩ
Battery discharge peak current limit	I_{DSG_LMT}	V_{IN} = 0V, V_{BATT} = 3.8V, OTG disabled, I_{SYS} rising		11		A
Battery discharge function controlled by DISC	t_{DISC}	DISC pulled low time period to turn off the battery discharge function		6.6		s
		DISC pulled high and low time period to turn on the battery discharge function		0.5		

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage and Input Current Based Power Path						
Input voltage regulation threshold [I²C]	V_{IN_REG}		3.9		5.1	V
Input voltage regulation accuracy		REG00[6:3] = 1011, $V_{IN\ REG}$ = 4.76V	-4		4	%
Input current limit	I_{IN_LMT}	USB100		70	100	mA
		USB150		120	150	
		USB500	400		500	
		USB900	750		900	
Input current limit accuracy		I_{IN_LMT} = 1.8A, REG00[2:0] = 101	1450		1800	mA
Protection						
Battery over-voltage protection	V_{BATT_OVP}	Rising. Compared to $V_{BATT\ FULL}$		200		mV
Battery over-voltage protection hysteresis		Compared to V_{BATT_FULL}		68		mV
Thermal shutdown rising threshold(6)	T_{J_SHDN}	T_J rising		184		ºC
Thermal shutdown hysteresis (6)				20		ºC
NTC low temp rising threshold	V_{COLD}	As percentage of V_{VNTC}	70.9	71.5	72.1	%
NTC low temp rising threshold hysteresis		As percentage of V_{VNTC}		1.4		%
NTC cool temp rising threshold	V_{COOL}	As percentage of V_{VNTC}	68.6	69.2	69.8	%
NTC cool temp rising threshold hysteresis		As percentage of V_{VNTC}		1.3		%
NTC warm temp falling threshold	V_{WARM}	As percentage of V_{VNTC}	55.9	56.5	57.1	%
NTC warm temp falling threshold hysteresis		As percentage of V_{VNTC}		1.4		%
NTC hot temp falling threshold	V_{HOT}	As percentage of V_{VNTC}	47.9	48.5	49.1	%
NTC hot temp falling threshold hysteresis		As percentage of V_{VNTC}		1.3		%

NOTE:

6) Guaranteed by design.

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VREF LDO						
VREF LDO output voltage		V_{IN} = 10V, I_{VREF} = 40mA	4.82	5		V
		V_{IN} = 5V, I_{VREF} = 20mA		4.8		
VREF LDO current limit		V_{VREF} = 4V	50			mA
OTG Boost Mode						
Battery operating range	V_{BATT_OTG}		2.5		4.5	V
Battery discharge current	I_{BATT_OTG}	V_{IN} < V_{IN_UVLO}, V_{BATT_OTG} = 4.2V, battery FET is off			20	µA
		V_{IN} < V_{IN_UVLO}, V_{BATT_OTG} = 4.2V, battery FET is on			35	µA
OTG output voltage	V_{IN_OTG}	I_{OTG} = 0A		5.15		V
OTG output voltage accuracy		As percentage of V_{IN_OTG}, I_{OTG} = 0A.	-2		2	%
Battery operation UVLO	V_{BATT_UVLO}	V_{BATT} falling		2.5		V
Battery operation UVLO hysteresis				200		mV
OTG output voltage protection threshold	V_{OTG_OVP}	V_{BATT} = 3.7V, OTG is enabled, force a voltage at IN until switching is off		5.75		V
OTG output voltage protection threshold hysteresis				175		mV
OTG output current limit [I²C]	I_{OLIM}	REG02[1:0] = 00, V_{BATT} = 3.7V	0.5	0.6	0.7	A
		REG02[1:0] = 01, V_{BATT} = 3.7V	1.3	1.5	1.7	
DP/DM USB Detection						
DP voltage source	V_{DP_SRC}		0.5	0.6	0.7	V
Data connect detect current source	I_{DP_SRC}		7		13	µA
DM sink current	I_{DM_SINK}		50	100	150	µA
Leakage current input DP/DM	I_{DP_LKG}		-1		1	µA
	I_{DM_LKG}		-1		1	µA
Data detect voltage	V_{DAT_REF}		0.25		0.4	V
Logic low	V_{LGC_LOW}				0.8	V
Session valid to connect time for powered up peripheral					45	mins

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic I/O Characteristics						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
I²C Interface (SDA, SCL)						
Input high threshold level		$V_{PULL\ UP}$ = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.4	V
I²C clock frequency	F_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Digital clock 1	F_{DIG1}	VREF LDO enabled	1400	1700	2000	kHz
Digital clock 2	F_{DIG2}			39		kHz
Watchdog timer	t_{WDT}	REG05 [5:4] = 11		160		s

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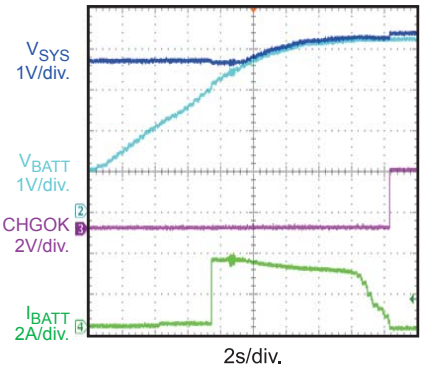
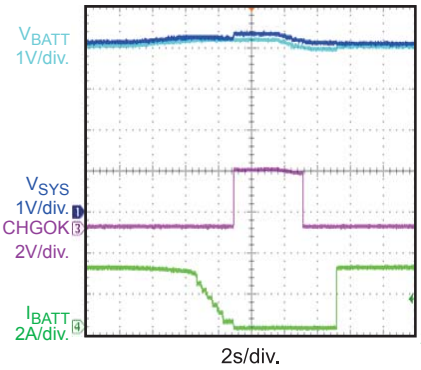
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = full range, I²C controlled, I_{CHG} = 4.5A, I_{IN_LMT} = 3.0A, V_{IN_REG} = 4.36V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

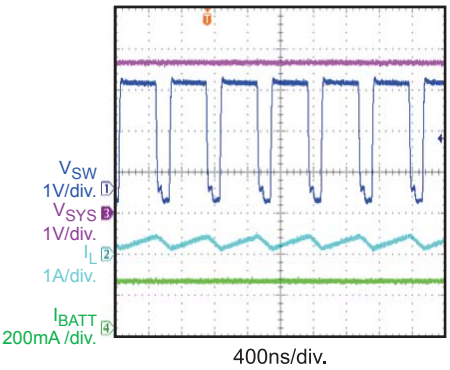
Battery Charge Curve
V_{IN}=5V, I_{SYS}=0A



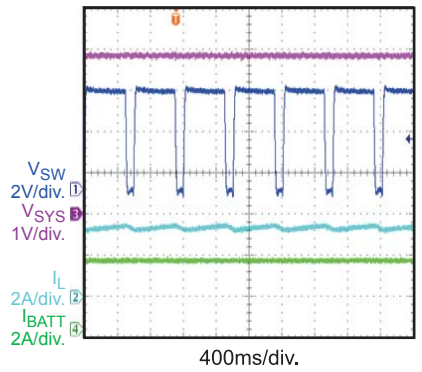
Auto Recharge
V_{IN}=5V, I_{SYS}=0A



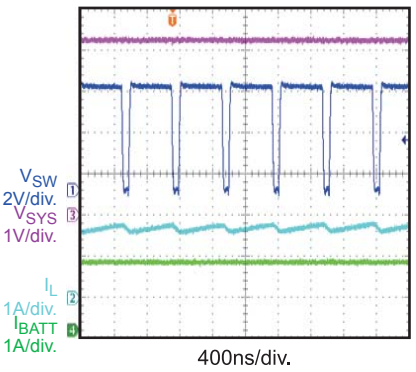
Trickle Charge Steady State
V_{IN}=5V, V_{BATT}=2.8V



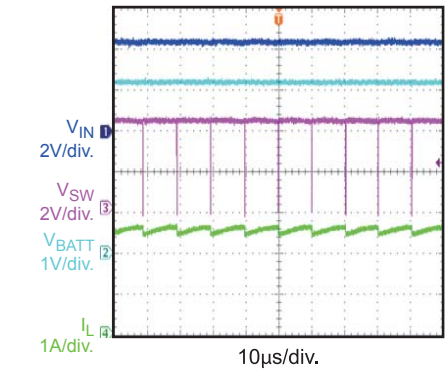
Constant Current Charge Steady State
V_{IN}=5V, V_{BATT}=3.6V



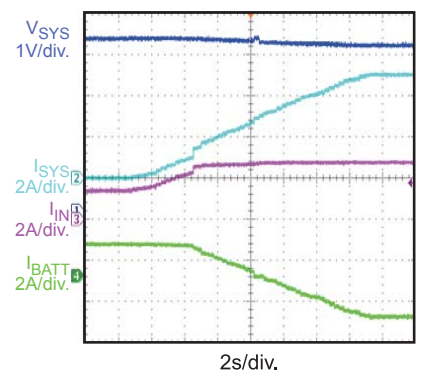
Constant Voltage Charge Steady State
V_{IN}=5V, V_{BATT}=4.2V



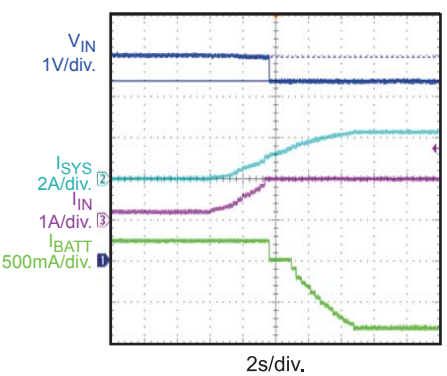
COT Operation
V_{IN}=4.5V



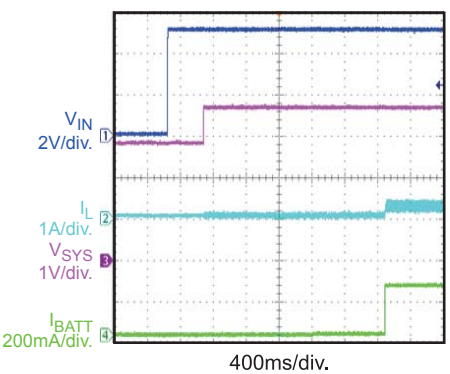
Input Current Limit
V_{IN}=5V, V_{BATT}=4.2V, I_{CHG}=3.5A



Input Voltage Limit
V_{IN}=5V/1.0A, V_{BATT}=2.8V, I_{CHG}=2A



Power On
V_{IN}=5V, V_{BATT}=3.7V



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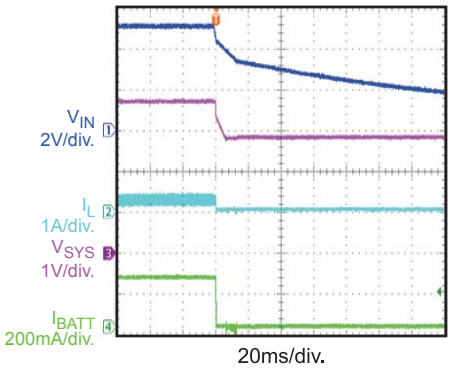
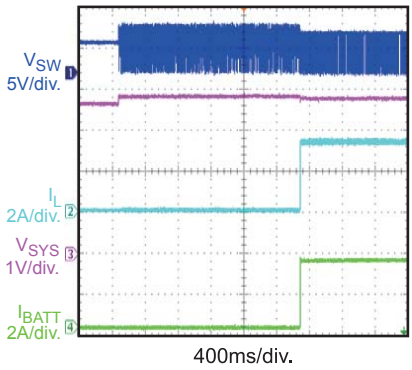
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I^2C controlled, I_{CHG} = 4.5A, I_{IN_LMT} = 3.0A, V_{IN_REG} = 4.36V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

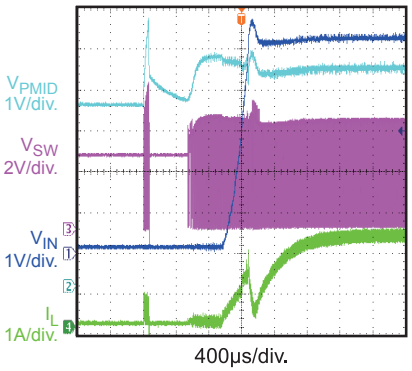
Power Off
V_{IN}=5V, V_{BATT}=3.7V



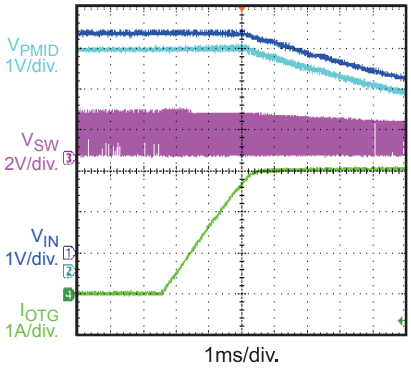
EN On
V_{IN}=5V, V_{BATT}=3.7V



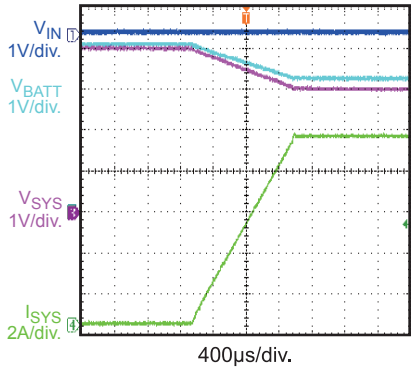
OTG Mode Start-Up
V_{IN_OTG}=5V,V_{BATT_OTG}=3.6V, I_{OTG}=1.3A



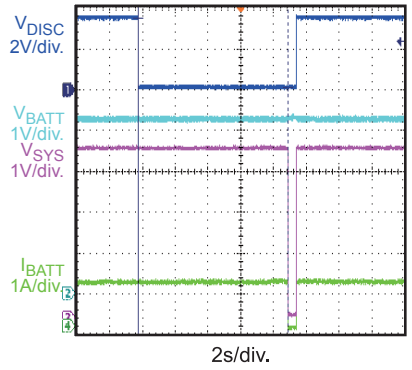
OTG Output CC Mode
V_{IN_OTG}=5V,V_{BATT_OTG}=3.6V, I_{OTG}=1.3A



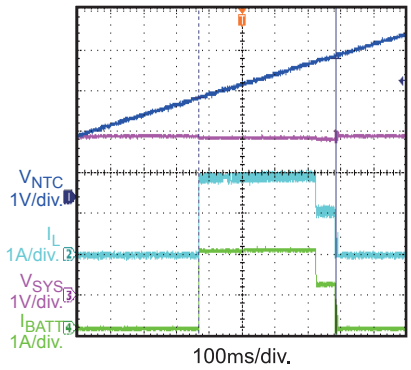
Battery Discharge Current
V_{IN}=Float, I_{SYS}=9A,V_{BATT}=4.0V



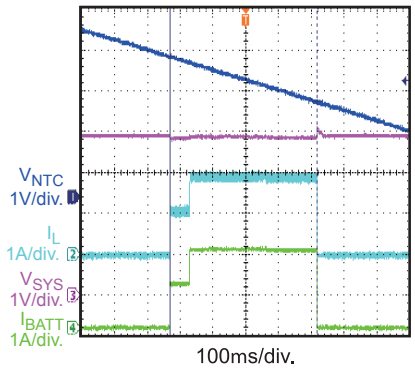
DISC Function
V_{IN}=Float, I_{SYS}=1A,V_{BATT}=4.2V



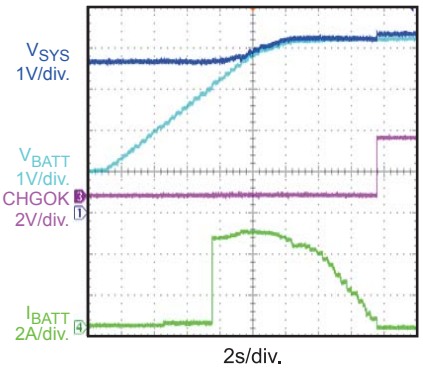
NTC Function
V_{IN}=5V,V_{BATT}=3.8V, I_{CHG}=2A



NTC Function
V_{IN}=5V,V_{BATT}=3.8V, I_{CHG}=2A



Battery Charge Curve
V_{IN}=9V, I_{SYS}=0A



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FUNCTIONAL BLOCK DIAGRAM

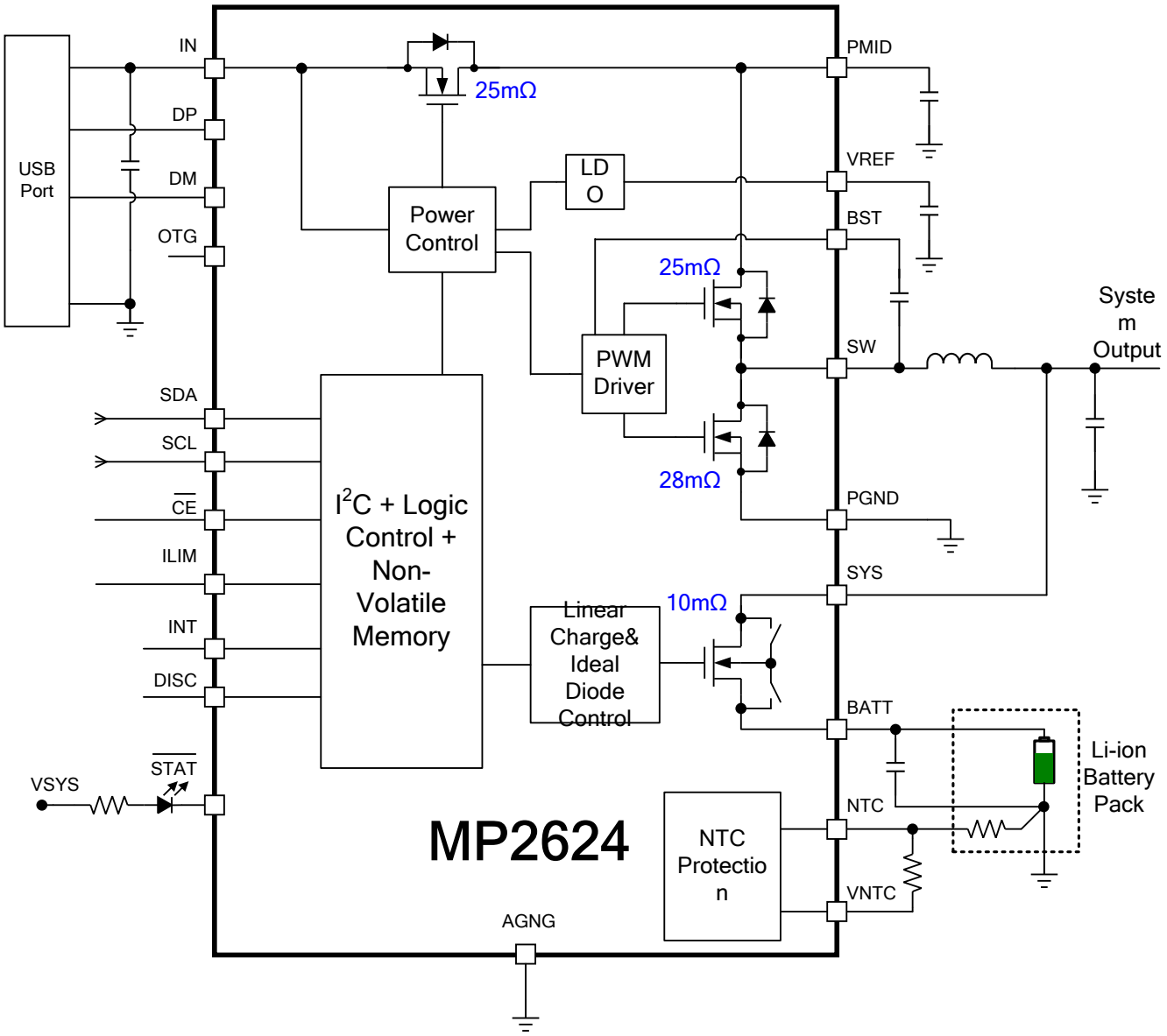

Figure 1: Functional Block Diagram

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OPERATION

Introduction

The MP2624 is a highly integrated I²C controlled switching-mode battery charger IC with NVDC power path management for single-cell lithium-ion or lithium-polymer battery applications. The MP2624 integrates a reverse blocking FET, a high-side switching FET, a low-side switching FET, and a battery FET between SYS and BATT. Its low impedance and high efficiency allows higher current (4.5A) capacity for a given package size.

Power Supply

The internal bias circuit of the MP2624 is powered from the higher voltage of V_{IN} and V_{BATT}. When V_{IN} or V_{BATT} rises above the respective UVLO threshold, the sleep comparator, battery depletion comparator, and the battery FET driver are active; the I²C interface is ready for communication and all the registers are reset to the default value. The host can access all the registers.

Input Power Status Indication

The MP2624 qualifies the voltage and current of the input source before start-up. The input source has to meet the following requirements:

1. $V_{IN} > V_{BATT} + 250mV$
2. $V_{IN\_UVLO} < V_{IN}$
3. OTG is not enabled by host

Once the input power source meets the conditions above, the system status register REG08 Bit [2] asserts that the input power is good, and the DP/DM detection starts (if enabled). Then the step-down converter is ready to operate.

The conditions above are monitored continuously, and the charge cycle is suspended if a condition is outside one of the limits (see Figure 2).

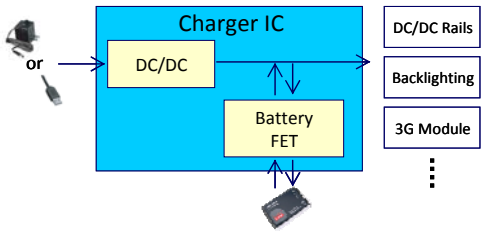

Figure 2: NVDC Power Path Management Structure

Narrow VDC Power Structure

The MP2624 employs a narrow VDC (NVDC) power structure with the battery FET decoupling the system from the battery, thus allowing separate control between the system and the battery. The system is always given priority to start-up even with a deeply-discharged or missing battery. When the input power is available (even with a depleted battery), the system voltage is always above the preset minimum system voltage (V_{SYS_MIN}) set by the I²C register REG01 Bit [3:1].

As depicted in Figure 2, the NVDC power structure is composed of a front-end, step-down DC/DC converter and a battery FET between SYS and BATT.

The DC/DC converter is a 1.5MHz step-down switching regulator adopting constant-off-time (COT) control to provide power to the system, which drives the system load directly and charges the battery through the battery FET.

For system voltage control:

(1) A minimum system voltage (V_{SYS_MIN}) can be set via the register REG01 Bit [3:1]. When the battery voltage is lower than V_{SYS_MIN} + 60mV, the system voltage is regulated at Max (V_{SYS_MIN}, V_{BATT}) + ΔV, and the battery FET works linearly to charge the battery with trickle-charge, pre-charge, or fast-charge current through the battery FET, depending on the battery voltage. ΔV can be set to 50mV or 100mV via the I²C register REG01 Bit [0].

(2) When the battery voltage exceeds V_{SYS_MIN} + 60mV, the system voltage tracks the battery voltage with a voltage differential of $I_{CHG} \cdot R_{BATFET}$, where the R_{BATFET} is the on resistance of the battery FET.

(3) When the charging is suspended or completed, the system voltage is regulated at ΔV higher than Max (V_{SYS_MIN}, V_{BATT}). ΔV can be set to 50mV or 100mV via the I²C register REG01 Bit [0].

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V_{SYS} regulation is shown in Figure 3.

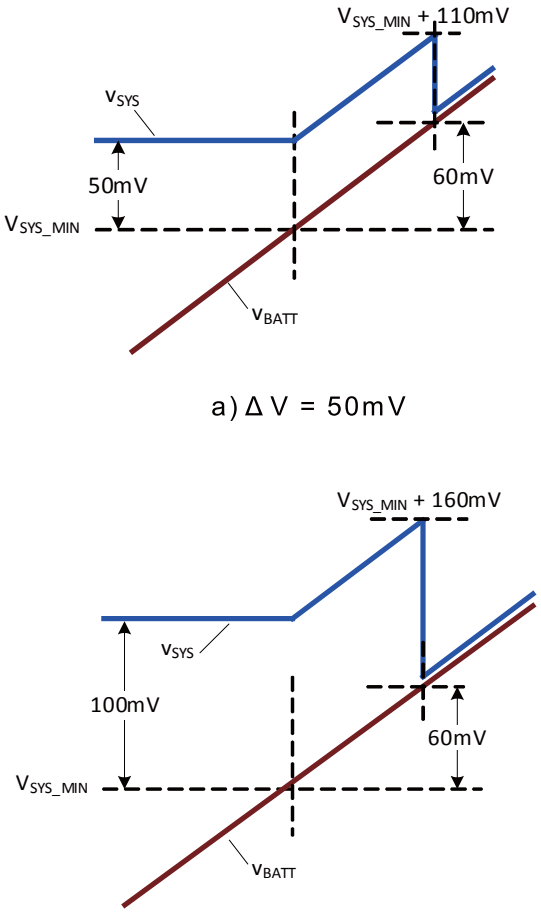

Figure 3: V_{SYS} Variation with V_{BATT}

The MP2624 monitors continuously the voltage at SYS. Once the system voltage is 100mV over V_{BATT_FULL} + ΔV, it is detected as a V_{SYS} OVP condition. The MP2624 will turn off the DC/DC converter, and then the system will be powered by the battery.

Battery Charge Profile

The MP2624 provides four main charging phases: trickle charge, pre-charge, constant-current charge, and constant-voltage charge.

Phase 1 (Trickle Charge):

When the input power is qualified as a good power supply, the MP2624 checks the battery voltage to decide if trickle charge is required. If the battery voltage is lower than V_{BATT_SHORT} (2.1V), a charging current of 128mA is applied on the battery, which helps reset the protection circuit in the battery pack.

Phase 2 (Pre-Charge):

When the battery voltage exceeds the V_{BATT_SHORT}, the MP2624 starts to pre-charge safely the deeply depleted battery until the battery voltage reaches the "pre-charge to fast-charge threshold" (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer expires, the charge cycle ends, and a corresponding timeout fault signal is asserted. The pre-charge current can be programmed via the I²C register REG03 Bit [7:4].

Phase 3 (Constant-Current Charge)

When the battery voltage exceeds V_{BATT_PRE} set via the REG04 Bit [1], the MP2624 enters a constant-current charge (fast charge) phase. The fast-charge current can be programmed as high as 4.5A via the REG02 Bit [7:2].

Phase 4 (Constant-Voltage Charge)

When the battery voltage rises to the pre-programmable charge full voltage (V_{BATT_FULL}) set via the REG04 Bit [7:2], the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the battery full termination threshold (I_{BF}) set via the REG03 Bit [3:0], assuming the termination function is enabled by REG05[7] = 1. If I_{BF} is not reached before the safety charge timer expires (see "Safety Timer" section), the charge cycle ends, and the corresponding timeout fault signal is asserted.

Figure 4 shows the battery charge profile.

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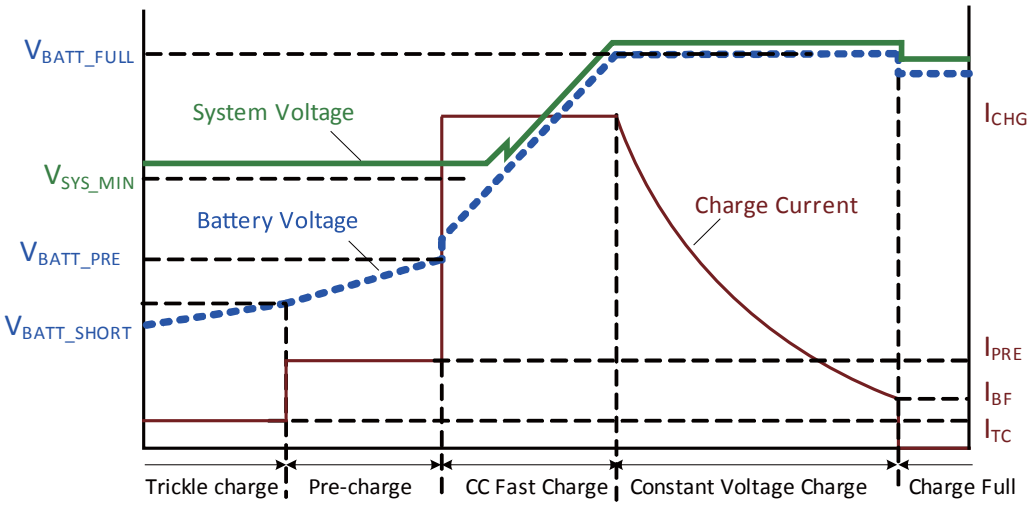

Figure 4: Battery Charge Profile

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations like dynamic power management (DPM) regulation (input current limit or input voltage regulation loop), or thermal regulation. Thermal regulation reduces the charge current, so the IC junction temperature does not exceed the pre-set limit. The multiple thermal regulation thresholds (from 60ºC to 120ºC) help system design meet thermal requirements for different applications. The junction temperature regulation threshold can be set via the REG06 Bit [1:0].

A new charge cycle starts when the following conditions are valid:

- The input power is re-plugged.
- Battery charging is enabled by I²C, and $\overline{CE}$ is forced to a low logic.
- No thermistor fault.
- No safety timer fault.
- No battery over voltage.
- The BATT FET is not forced to turn off.

Automatic Recharge

When the battery is charged full or the charging is terminated, the battery may be discharged because of the system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold, automatically the MP2624 starts a new charging cycle.

$\overline{CE}$ Control

$\overline{CE}$ is a logic input pin for enabling or disabling battery charging by turning on/off the DC/DC or restarting a new charging cycle. The battery charging is enabled when the REG01 Bit [5:4] is set to 01, and $\overline{CE}$ is pulled to low logic.

Indication

Apart from multiple status bits designed in the I²C registers, the MP2624 also has a hardware status output pin ($\overline{STAT}$). The status STAT in different states is shown in Table 1.

Table 1: Operation Indications

Charging State	STAT
Charging	Low
Charging complete, sleep mode, charge disable	High
Charging suspended	Blinking at 1Hz

Battery Over-Voltage Protection

The MP2624 is designed with built-in battery over-voltage protection. When the battery voltage exceeds V_{BATT_FULL} + 160mV, the MP2624 suspends immediately the charging and asserts a fault. When battery over-voltage protection occurs, only the charging is disabled, and the DC/DC will keep operating.

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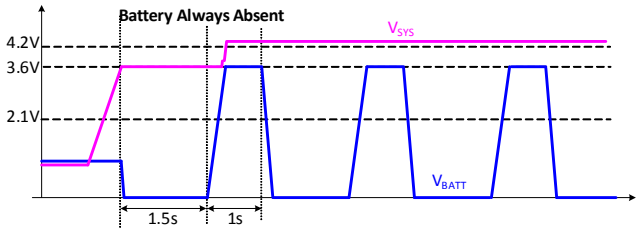
Battery Floating Detection

The MP2624 is capable of detecting whether a battery is connected or not. The following conditions initiate battery float detection:

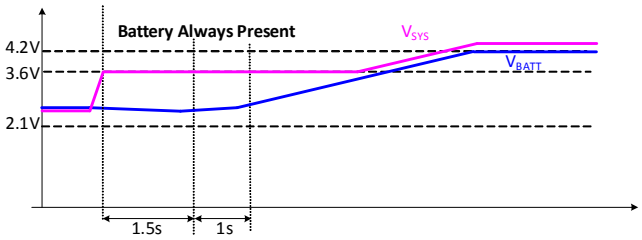
- Charging is enabled.
- Auto-recharge is triggered.
- Battery OVP recovery.

Before a charging cycle is initiated, the MP2624 will implement battery floating detection (see Figure 5). Under this condition, the detection block sinks a 3mA current for 1.5 seconds to check if V_{BATT} is lower than 2.1V. If V_{BATT} is higher than 2.1V, the battery present will be detected. Otherwise, the MP2624 will continue to source a 3mA current and start a 1 second timer to check when V_{BATT} exceeds 3.6V. If V_{BATT} is still lower than 3.6V when the 1 second timer expires, the battery present is asserted. The system regulation voltage is set to Max (V_{SYS_MIN}, V_{BATT}) + ΔV, and the charging begins to soft start. Before the 1 second timer expires (as soon as V_{BATT} rises up to 3.6V), the 3mA sink current source will be disabled, and the battery absent is detected. In this case, the charging is disabled, and the system regulation voltage is set to V_{BATT_FULL} + ΔV.

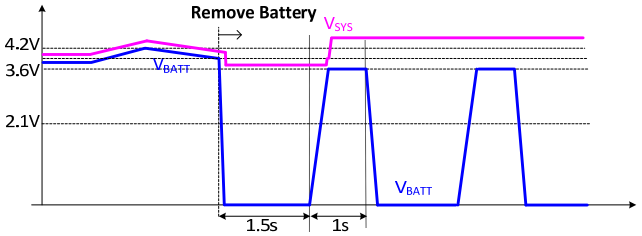
Battery floating detection flow is shown in Figure 6.



(a) Charging Start-Up with Battery Absent



(b) Charging Start-Up with Battery Present



(c) Remove Battery during Charging

Figure 5: Battery Float Detection Examples

System Over-Voltage Protection

The MP2624 always monitors the voltage at SYS. When system over-voltage is detected (V_{SYS} > V_{BATT_FULL}+ ΔV +100mV), the DC/DC converter is turned off, and the system is powered by the battery via the battery FET.

ΔV can be set to 50mV or 100mV via the I²C register REG01 Bit[0].

During heavy system load transient, System OVP often happens when load transient from heavy to light. The timer is suspend when system OVP, so the timer may transfer between normal and suspend frequently, the timer counter will receive a fault timer clock signal, then fault timer out may happen under this condition.

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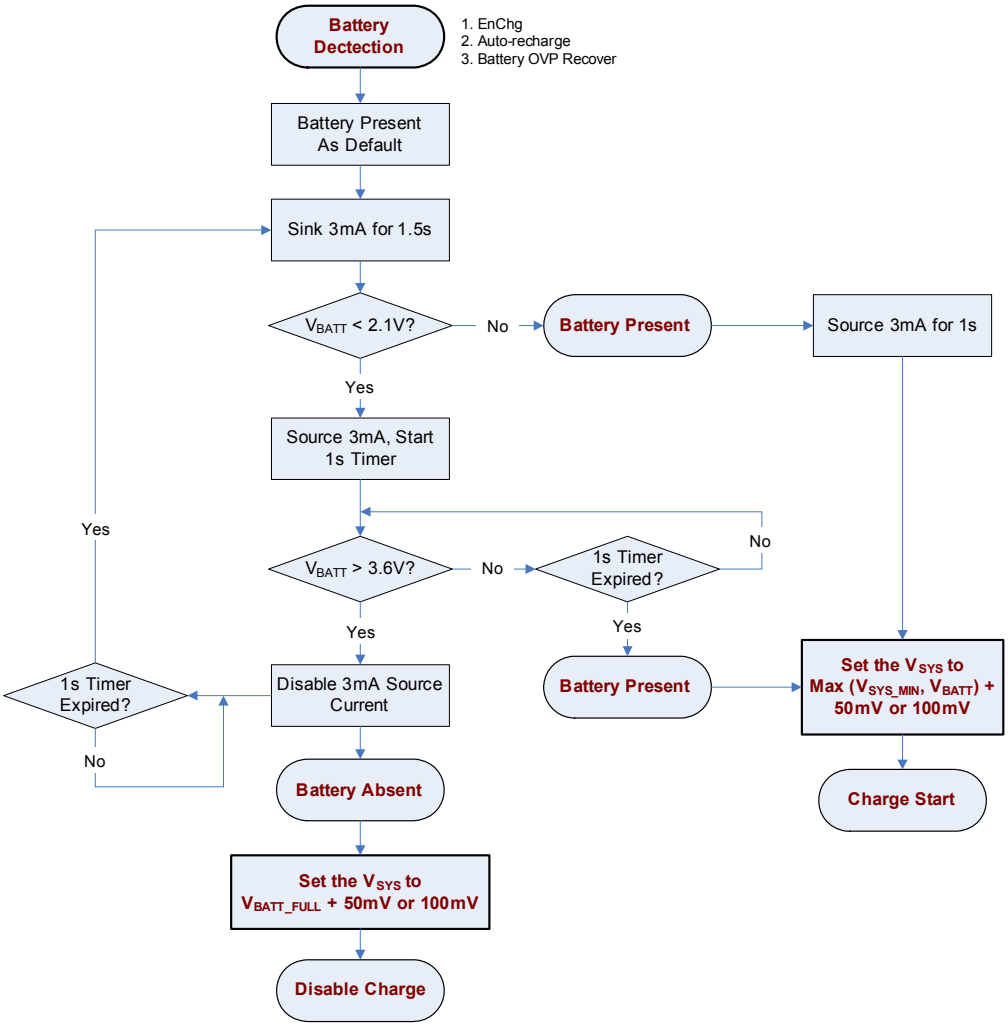

Figure 6: Battery Float Detection Flow

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Input Voltage Based and Input Current Based Power Management

To meet the maximum current limit for the USB specification and avoid overloading the adapter, the MP2624 features both input current and input voltage power management by continuously monitoring the input current and input voltage. The total input current limit is programmable to prevent the input source from being overloaded. When the input current hits the limit, the charge current tapers off to keep the input current from increasing further.

If the pre-set input current limit is higher than the rating of the adapter, the back-up input voltage based power management works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation threshold, due to the heavy load, the charge current is reduced to keep the input voltage from dropping further.

During CV mode, while battery voltage has been charged to the value only 100mV lower than the battery full threshold, if the power path management happens and charge current drops be lower than I_{BF}, the charge full will be fault detected.

The operation of the power path management is applied in the following two cases:

As mentioned in the "NVDC Power Structure" section,

a) When $V_{BATT} < V_{SYS\_MIN} + 60mV$, the system voltage is regulated at Max (V_{SYS_MIN}, V_{BATT}) + ΔV. If the input current or voltage regulation threshold is reached, the system voltage loop will lose the control of the DC/DC converter, which will cause system voltage drops. Once the system voltage drops by 2%·V_{SYS_MIN}, the charge current will be decreased to keep the system voltage from dropping further.

b) When $V_{BATT} > V_{SYS\_MIN} + 60mV$ (since the battery is connected to the system directly due to the free transition between each control loop), the charge current will decrease automatically when the input current limit or the voltage regulation threshold is reached.

Battery Supplement Mode

During battery supplement mode, the charge current is reduced to keep the input current or input voltage from dropping when DPM occurs. If the input source is still overloaded, even when the charge current has decreased to zero, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the MP2624 enters battery supplement mode. The battery will power both the system and the DC/DC converter simultaneously.

An ideal diode mode is designed in the MP2624 to optimize the control transition between the battery FET and DC/DC converter. The battery FET will enter ideal diode mode under the following conditions:

a) Charging start-up when $V_{BATT} > V_{SYS\_MIN} + \Delta V$.

b) When $V_{BATT} < V_{SYS\_MIN} + \Delta V$, if the system voltage drops below the battery voltage, the battery FET will enter ideal diode mode.

During ideal diode mode, the battery FET operates as an ideal diode. When the system voltage is 40mV below the battery voltage, the battery FET turns on and regulates the gate drive of the battery FET; the V_{DS} of the battery FET remains around 20mV. As the discharge current increases, the battery FET obtains a stronger gate drive and a smaller R_{DS} until the battery FET is fully on.

NTC (Negative Temperature Coefficient) Thermistor

"Thermistor" is the generic name given to a thermally sensitive resistor. Generally, a negative temperature coefficient thermistor is called a thermistor. Depending on the manufacturing method and the structure, there are many thermistor shapes and characteristics for various applications. The thermistor resistance values, unless otherwise specified, are classified at a standard temperature of 25ºC. The resistance of a temperature is solely a function of its absolute temperature.

Refer to the thermistor datasheet. The mathematical expression, which relates to the resistance and the absolute temperature of a thermistor, is shown in Equation (1):

$$R_1 = R_2 \cdot e^{\beta \cdot \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (1)$$

Where R1 is the resistance at the absolute temperature T1, R2 is the resistance at the

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absolute temperature T2, and β is a constant, which depends on the material of the thermistor.

In charge mode, the MP2624 monitors continuously the battery's temperature by measuring the voltage at NTC. This voltage is determined by the resistive divider whose ratio is produced by the different resistances of the NTC thermistor under the different ambient temperatures of the battery.

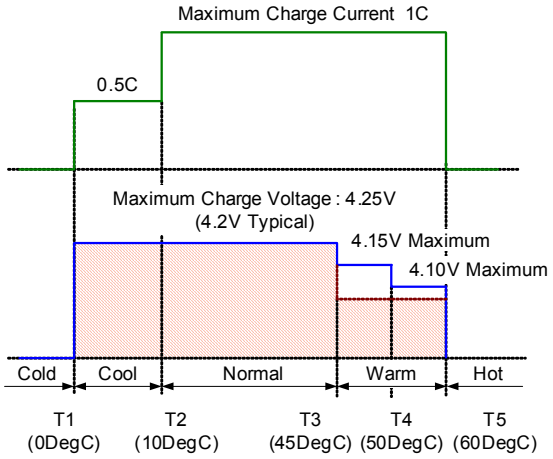

Figure 7: NTC Window

MP2624 sets internally a pre-determined upper and lower bound of the range. If the voltage at NTC goes out of this range, which means the temperature is outside the safe operating limit, the charging is ceased unless the operating temperature returns to a safe range.

To satisfy the JEITA requirement, the MP2624 monitors four temperature thresholds: the cold battery threshold (T_{NTC}<0ºC), the cool battery threshold (0ºC<T_{NTC}<10ºC), the warm battery threshold (45ºC<T_{NTC}<60ºC), and the hot battery threshold (T_{NTC}>60ºC). For a given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}. When V_{NTC} < V_{HOT} or V_{NTC} > V_{COLD}, the charging is suspended, and the timers are suspended. When V_{HOT} < V_{NTC} < V_{WARM}, the charge-full voltage (V_{BATT_FULL}) is reduced by 150mV compared to the programmable threshold. When V_{COOL} < V_{NTC} < V_{COLD}, the charging current is reduced to half of the programmable charge current. Figure 7 shows the JEITA control.

Separate Pull-Up Pin VNTC for NTC Protection

As shown in Figure 8, a separate pull-up VNTC is designed as the internal pull-up terminal of the resistive divider for the NTC comparator. Both the reference divider and the feedback divider are connected together to VNTC. The VNTC is connected to VREF via an internal switch (in charge mode only).

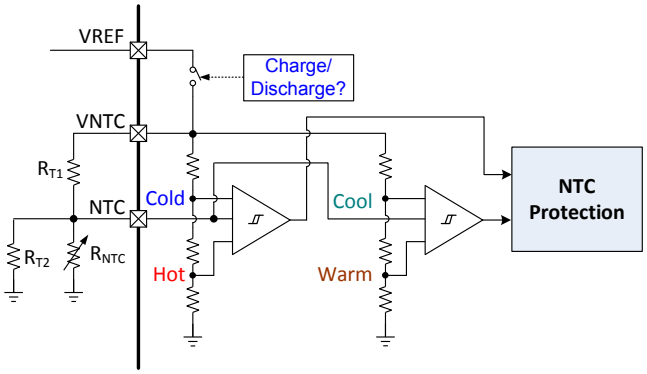

Figure 8: NTC Protection Circuit

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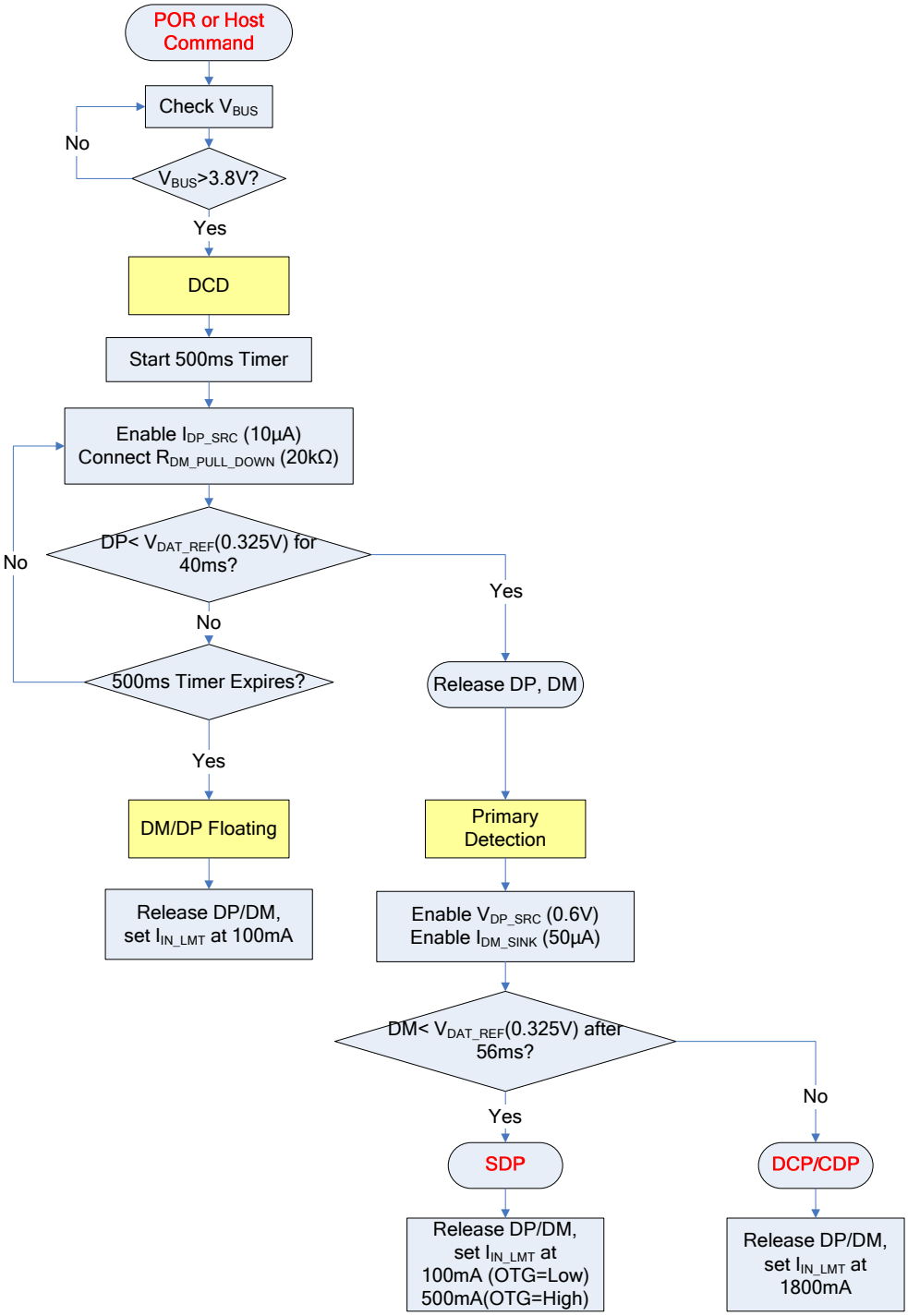

Figure 9: USB Detection Flow Chart

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DM/DP USB Detection

The USB ports in personal computers are convenient places for portable devices (PDs) to draw current for charging batteries. If the portable device is attached to a USB host of hub, then the USB specification requires the portable device to draw a limited current (100mA/500mA in USB2.0, and 150mA/ 900mA in USB3.0). When the device is attached to a charging port, it is allowed to draw more than 1.5A.

The MP2624 features input source detection compatible with the Battery Charging Specification Revision 1.2 (***BC1.2***) to program the input current limit during default mode. The user can force DP/DM detection in the host mode by writing 1 to REG07 Bit [7].

When the input source is first applied, the input current limit begins with 100mA by default. If the input source passes the input source qualification, the MP2624 starts DP/DM detection. The DP/DM detection circuit is shown in Figure 10.

The DP/DM detection has two steps:

1. Data Contact Detection (DCD)
2. Primary Detection.

DCD detection uses a current source to detect when the data pins have made contact during an attach event. The protocol for data contact detect is as follows:

- The power device (PD) detects V_{IN} asserted.
- The PD turns on DP I_{DP_SRC} and the DM pull-down resistor for 40ms.
- The PD waits for the DP line to be low.
- The PD turns off I_{DP_SRC} and the DM pull-down resistor when the DP line is detected as low or the 40ms timer is expired.

DCD allows the PD to start primary detection as soon as the data pins have made contact. Once the data contact is detected, the MP2624 will jump to the primary detection immediately. If the data contact is not detected, the MP2624 will jump automatically to the primary detection after 300ms from the beginning of the DCD.

Primary detection is used to distinguish between the USB host (or SDP) and different types of charging ports.

During primary detection, the PD turns on the V_{DP_SRC} on DP and the I_{DM_SINK} on DM. If the portable device is attached to a USB host, the DM is low.

Figure 9 shows the USB detection flow chart.

To be compatible with the USB specification and BC1.2, set the input current limit according to the values listed in Table 2.

Table 2: Input Current Limit vs. USB Type

DP/DM Detection	OTG	I_{IN_LMT}	REG08 [7:6]
Floating	X	100mA	00
SDP	LOW	100mA	10
SDP	HIGH	500mA	10
DCP	X	1.8A	01

The USB detection runs as soon as the V_{IN} is detected and is independent of the charge enable status. After the DP/DM detection is complete, the MP2624 will set the input current limit according to Table 2 and assert the USB port type in REG08 Bit [7-6]. The host is able to revise the input current limit as well according to the USB port type asserted in the REG08 Bit [7:6].

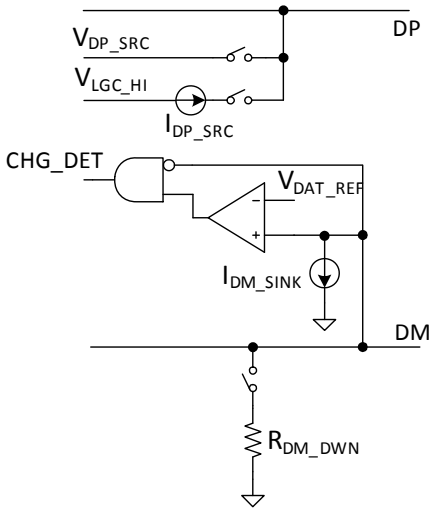

Figure 10: DP/DM Detection Circuit

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When the detection algorithm is complete, the DP and DM signal lines enter a high-Z (HZ) state with an approximate 4pF capacitive load.

Input Current Limit Setting via ILIM

For safe operation, the MP2624 has an additional hardware pin (ILIM) to adjust the maximum input current limit. It can be set by a resistor connected from ILIM to GND. The actual input current limit is the lower value between the ILIM setting and the register setting value via I²C.

Interrupt to Host (INT)

The MP2624 has an alert mechanism, which can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low state INT pulse. All of the events below trigger the INT output:

- Good input source detected
- USB detection completed
- UVLO
- Charge completed
- Any fault in REG09 (Watchdog timer fault, OTG fault, thermal fault, safety timer fault, battery OVP fault, and NTC fault)

When a fault occurs, the charger device sends out an INT signal and latches the fault state in REG09 until the host reads the fault register. Before the host reads REG09, the charger device will not send a new INT signal upon new faults except for NTC faults. The NTC fault is not latched and always reports the current thermistor conditions.

In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads the fault register status from the last INT, and the 2nd reads the current fault register status.

Safety Timer

The MP2624 provides both a pre-charge and complete charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is 1 hour when the battery voltage is lower than V_{BATT_PRE}. The complete charge safety timer starts when the battery enters constant-current charge. The constant-current charge safety timer can be programmed by I²C. The safety timer feature can be disabled via I²C. The safety timer does not operate in USB OTG mode.

The safety timer is reset at the beginning of a new charging cycle. Also, it can be reset by toggling $\overline{CE}$ or write 00 and 01 sequentially to the REG01 Bit [5:4]. The following actions restart the safety timer:

- A new charge cycle has begun.
- Toggling $\overline{CE}$ from low to high to low (charge enable)
- Write REG01 Bit [5:4] from 00 to 01 (charge enable)
- Write REG05 Bit [3] from 0 to 1 (safety timer enable)
- Write REG01 Bit [7] from 0 to 1 (software reset)

The timer can be refreshed after timer out when one of the following thing happens:

- The input power reset.
- Toggling $\overline{CE}$ from low to high to low (charge enable).
- Writing REG01 Bit[5:4] from 00 to 01 (charge enable).

MP2624 adjusts automatically or suspends the timer when a fault occurs.

The timer is suspended during the conditions below:

- The battery is discharging
- System OVP occurs
- NTC hot or cold fault

If the input current limit, input voltage regulation, or thermal regulation threshold is reached, the rest of the timer is doubled by enable the 2X timer in PPM function (REG07H Bit[6]=1). Once the PPM operation is removed, the rest of the timer returns to the original setting. This setting may cause an application issue, if the IC operates in and out of PPM frequently, the single timer period will be divided, which causes false timer out termination. The solution is to disable the 2X timer function by set REG07H Bit[6] to 0.

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USB Timer

The total charging timer in default mode from the 100mA USB source is limited by a 45 minute timer. When this timer expires, the MP2624 stops the converter and goes into high-Z mode.

Once the device enters the HIZ state in host mode, it stays in HIZ until the host writes REG00 [7] to 0. When the processor starts-up, it is recommended to first check if the charger is in HIZ mode or not.

In default mode, the charger will reset REG00 [7] back to 0 when the input source is removed. When another power source is plugged in, the charger will run detection again and update the current limit.

Host Mode and Default Mode

The MP2624 is a host-controlled device. After the power-on reset, the MP2624 starts in the watchdog timer expiration state or default mode. All the registers are in the default settings.

Any write to the MP2624 makes it transition into host mode. All the device parameters are programmable by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG01 Bit [6] before the watchdog timer expires. Once the watchdog timer expires, the MP2624 returns to default mode.

VREF LDO Output

The VREF LDO supplies the internal bias circuits as well as the high-side and low-side FET gate drive. The pull-up rail of STAT can be connected to VREF as well. The VREF LDO will be enabled once OTG is enabled. In non-OTG mode, the internal VREF LDO is enabled when the following conditions are valid:

- V_{IN} > 3.3V
- No thermal shutdown

Both the internal LDO output and V_{BATT} will be passed to VREF via a PMOS. Only when V_{IN} > V_{BATT} +250mV, the internal LDO output will be delivered to VREF.

The VREF power supply circuit is shown in Figure 11.

Figure 12 shows the host mode and default mode change flow chart.

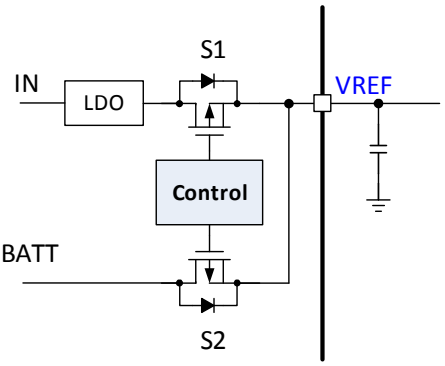

Figure 11: VREF Power Supply Circuit

Thermal Regulation and Thermal Shutdown

The MP2624 monitors continuously the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset threshold, the MP2624 starts to reduce the charge current to prevent higher power dissipation.

When the junction temperature reaches 150°C, the PWM step-down converter goes into shutdown mode.

Battery Discharge Function

If only the battery is connected and the input source is absent (but the OTG function is disabled), the battery FET is turned on completely when V_{BATT} is above the V_{BATT_UVLO} threshold. The 10mΩ battery FET minimizes the conduction loss during discharge and VREF LDO stays off. The quiescent current of the MP2624 is as low as 20μA. The low on resistance and low quiescent current help extend the running time of the battery.

There is an over-current limit designed in the MP2624 to avoid system over current when the battery is discharging. Once the discharged current exceeds this limit (I_{DSG_LMT} in EC Table) for a 20μs blanking time, the discharge FET is turned off. After a one second recovery time, the discharge FET is turned on again.

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